

Vishay Siliconix

Low Voltage, Dual DPDT in miniQFN16

DESCRIPTION

The DG2599 is a CMOS Dual DPDT (Dual Double Pole Double Throw) analog switch that operates over a wide voltage range of 1.65 V to 5 V. It is optimized for portable applications switching audio, SIM card signals, and other low power signals.

The DG2599 features low ON resistance of 2.8 W at 3 V power supply, fast switching speed, and low power consumption even when control logic signals are below V+ power supply voltage. The well matched dual DPDT switches conduct signals equally in both directions. The DG2599 is designed to guarantee break before make switching.

As a committed partner to the community and the environment, Vishay Siliconix manufactures this product with lead (Pb)-free device terminations. DG2599 are offered in a miniQFN package. The miniQFN package has a nickel palladium- gold device termination and is represented by the lead (Pb)-free "-E4" suffix. The nickel-palladium-gold device terminations meet all JEDEC[®] standards for reflow and MSL ratings.

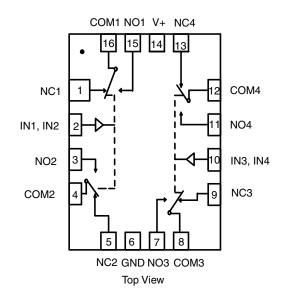
FEATURES

- Halogen-free according to IEC 61249-2-21 definition
- Low voltage operation: 1.65 V to 5.5 V
- Low on-resistance: 2.8 W at V+ = 3 V
- Power off protection on COM1 and COM2 pins
- Latch up current great than 300 mA per JESD78
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>

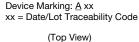
APPLICATIONS

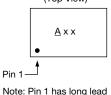
- Cellular phones
- PMPs and PDAs
- Modems and peripherals
- Computers and ebooks
- Tablet devices
- Displays and gaming
- STB

ORDERING INFORMATION					
PART NUMBER	PACKAGE				
DG2599DN-T1-GE4	miniQFN16 1.8 mm x 2.6 mm				



TRUTH TABLE (DG2599)						
LOGIC	OGIC NC1, 2, 3 AND 4 NO 1, 2, 3 AN					
0	ON	OFF				
1	OFF	ON				





ROHS COMPLIANT HALOGEN



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ABSOLUTE MAXIMUM RATINGS ($T_A = 25 \text{ °C}$, unless otherwise noted)						
PARAMETER		SYMBOL	LIMIT	UNIT		
Reference to GND	V+		-0.3 to +6	V		
Reference to GND	IN, COM, NC, NO ^a		-0.3 to (V+ + 0.3)	v		
Current (any terminal except NO, NC or		30				
Continuous current (NO, NC, or COM)		± 300	mA			
Peak current (pulsed at 1 ms, 10 % duty cycle)			± 500			
Storage temperature (D suffix)			-65 to +150			
Package solder reflow conditions ^d	miniQFN16		250			
Power dissipation (packages) ^b	miniQFN16 °		525	525 mW		

Note

a. Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings

b. All leads welded or soldered to PC board

c. Derate 6.6 mW/°C above 70 °C

d. Manual soldering with iron is not recommended for leadless components. The miniQFN-16 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper lip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection

ELECTRICAL CHARACTERISTICS ($V + = 3 V$)							
PARAMETER	TEST CONDITIONS	TEMP.	MIN.	TYP.	MAX.	UNIT	
Power Supply and Signal							
V+ supply voltage		Full	1.65	-	5.5	V	
V+ supply current	V _{IN} = 0 or V+	Full	-	0.001	2	μA	
Analog signal range		Full	0	-	V+	V	
Switch On-Resistance and Leaka	ge						
Drain-source on-resistance	V+ = 3 V, I _{NO/NC} = 100 mA, V _{COM} = 0.9 V, 2.3 V	Room	-	2.8	3.3		
Drain-source on-resistance	$v + = 3 v$, $v_{NO/NC} = 100 mA$, $v_{COM} = 0.9 v$, 2.3 v	Full	-	-	3.6	14/	
On-resistance flatness		Room	-	0.24	1.1	W	
On-resistance hatness	V+ = 3 V, $I_{NO/NC}$ = 100 mA, V_{COM} = 0 to V+	Full	-	-	1.3		
Switch off lookage ourrest		Room	-10	0.1	10	nA	
Switch off leakage current	V+ = 4.3 V, $V_{NO/NC}$ = 0.3 V/4 V, V_{COM} = 4 V / 0.3 V	Full	-100	-	100		
Channel on lookage ouwant		Room	-10	0.1	10		
Channel on-leakage current	V+ = 4.3 V, V _{NO/NC} and V _{COM} = 0.3 V / 4 V	Full	-100	-	100		
Digital Control							
Input high voltage	V+ = 4.3 V	Full	1.6	-	-	-	
Input, high voltage	V+ = 3 V		1.3	-	-	V	
	V+ = 4.3 V	Full	-	-	0.6	V	
Input, low voltage	V+ = 3 V		-	-	0.5		
Input, bias current	$V_{IN} = V+$	Full	-1	0.01	1	μA	
Dynamic Characteristics			•	•	•		
Turne and time a		Room	-	-	90		
Turn on-time	V_{COM} or $V_{NO/NC}$ = 3 V, R_L = 50 Ω , C_L = 35 pF	Full	-	-	115	1	
Turn off-time		Room	-	-	70		
	V_{COM} or $V_{NO/NC}$ = 3 V, R_L = 50 Ω , C_L = 35 pF	Full	-	-	85	- ns	
		Room	2	-	-		
Break before make time	V_{COM} or $V_{NO/NC}$ = 3 V, R_L = 50 Ω , C_L = 35 pF	Full	2	-	-		
Charge injection	$C_L = 1 \text{ nF}, R_{GEN} = 0 \Omega$	Room	-	± 10	-	рС	
Off isolation	$R_L = 50 \Omega$, $C_L = 5 pF$, $f = 1 MHz$		-	-66	-		
Crosstalk	$R_L = 50 \Omega$, $C_L = 5 pF$, f = 1 MHz, non-adjacent channels		-	-110	-	dB	
3 dB bandwith	$C_L = 5 \text{ pF}, R_L = 50 \Omega$		-	186	-	MHz	

S21-0507-Rev. D, 24-May-2021

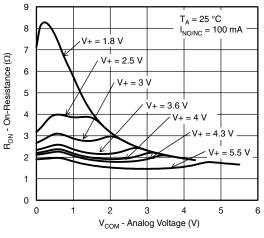
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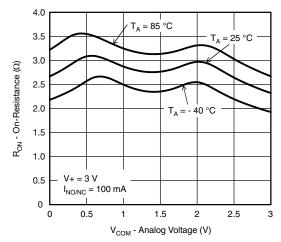
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ELECTRICAL CHARACTERISTICS (V+ = $3 V$)						
PARAMETER	TEST CONDITIONS	TEMP.	MIN.	TYP.	MAX.	UNIT
Source off capacitance	$V_{IN} = 0$ or V+, f = 1 MHz		-	9	-	pF
Channel on capacitance	$V_{IN} = 0$ or V+, f = 1 MHz		-	26	-	рг

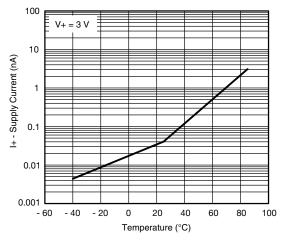
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



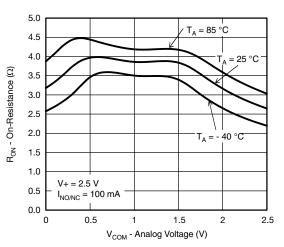
R_{ON} vs. V_{COM} and Single Supply Voltage



R_{ON} vs. Analog Voltage and Temperature



Supply Current vs. Temperature

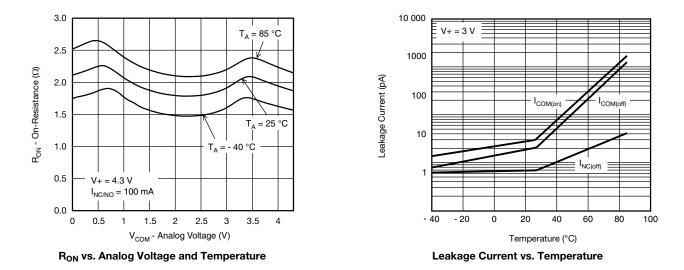


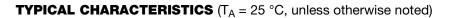
R_{ON} vs. Analog Voltage and Temperature

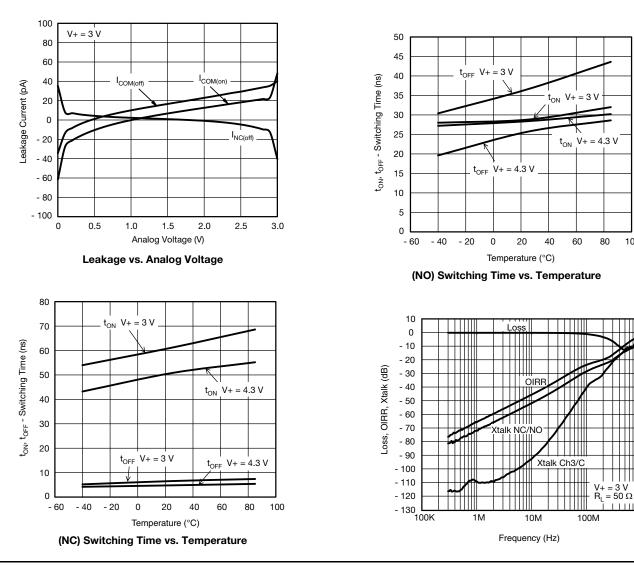
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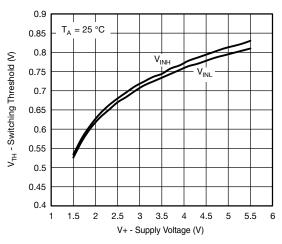
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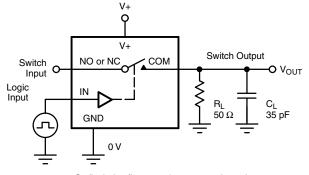


Insertion Loss, Off Isolation and Crosstalk



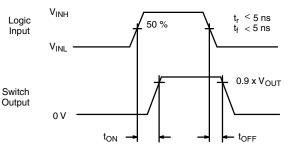
Switching Threshold vs. Supply Voltage

TEST CIRCUITS



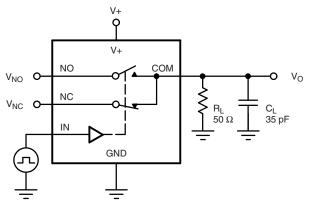
CL (includes fixture and stray capacitance)

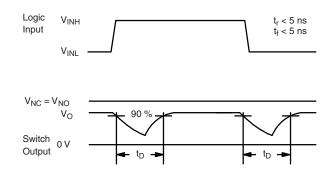
$$V_{OUT} = V_{COM} \left(\frac{R_L}{R_L + R_{ON}} \right)$$



Logic "1" = Switch On Logic input waveforms inverted for switches that have the opposite logic sense.







C_L (includes fixture and stray capacitance)

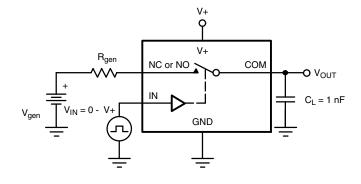
Break-Before-Make Interval

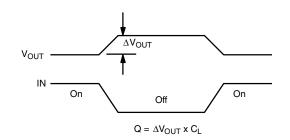
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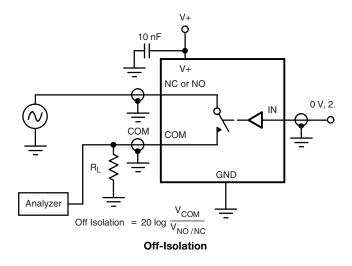
IN depends on switch configuration: input polarity determined by sense of switch.

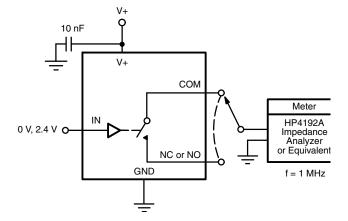
Charge Injection



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TEST CIRCUITS





Channel Off / On Capacitance

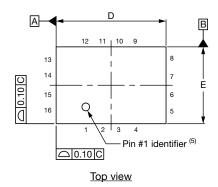
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <u>www.vishay.com/ppg?67667</u>.

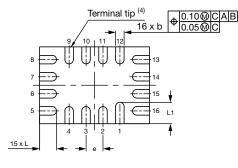
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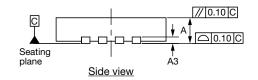
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Thin miniQFN16 Case Outline





Bottom view



DIMENSIONS	MILLIMETERS ⁽¹⁾ INCHES						
DIMENSIONS	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
А	0.50	0.55	0.60	0.020	0.022	0.024	
A1	0	-	0.05	0	-	0.002	
A3	0.15 ref.			0.006 ref.			
b	0.15	0.20	0.25	0.006	0.008	0.010	
D	2.50	2.60	2.70	0.098	0.102	0.106	
е	0.40 BSC			0.016 BSC			
E	1.70	1.80	1.90	0.067	0.071	0.075	
L	0.35	0.40	0.45	0.014	0.016	0.018	
L1	0.45	0.50	0.55	0.018	0.020	0.022	
N ⁽³⁾	16			16			
Nd ⁽³⁾		4			4		
Ne ⁽³⁾	4			4			

Notes

⁽¹⁾ Use millimeters as the primary measurement.

- ⁽²⁾ Dimensioning and tolerances conform to ASME Y14.5M. 1994.
- ⁽³⁾ N is the number of terminals. Nd and Ne is the number of terminals in each D and E site respectively.

 $^{(4)}$ Dimensions b applies to plated terminal and is measured between 0.15 mm and 0.30 mm from terminal tip.

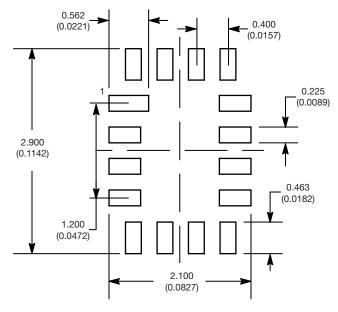
⁽⁵⁾ The pin 1 identifier must be existed on the top surface of the package by using identification mark or other feature of package body.

⁽⁶⁾ Package warpage max. 0.05 mm.

ECN: T16-0226-Rev. B, 09-May-16 DWG: 6023



RECOMMENDED MINIMUM PADS FOR MINI QFN 16L



Mounting Footprint Dimensions in mm (inch)



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