Data Sheet

CDK1307

Ultra Low Power, 20/40/65/80MSPS, 12/13-bit Analog-to-Digital Converters (ADCs)

FEATURES

- 13-bit resolution
- 20/40/65/80MSPS max sampling rate
- Ultra-Low Power Dissipation: 19/33/50/60mW
- 72.4dB SNR at 80MSPS and 8MHz F_{IN}
- Internal reference circuitry
- 1.8V core supply voltage
- 1.7 – 3.6V I/O supply voltage
- Parallel CMOS output
- 40-pin QFN package
- Pin compatible with CDK1308

APPLICATIONS

- Medical Imaging
- Portable Test Equipment
- Digital Oscilloscopes
- IF Communication

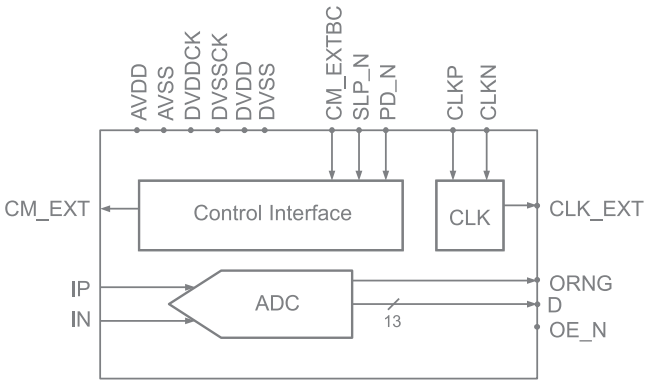
General Description

The CDK1307 is a high performance ultra low power Analog-to-Digital Converter (ADC). The ADC employs internal reference circuitry, a CMOS control interface and CMOS output data, and is based on a proprietary structure. Digital error correction is employed to ensure no missing codes in the complete full scale range.

Two idle modes with fast startup times exist. The entire chip can either be put in Standby Mode or Power Down mode. The two modes are optimized to allow the user to select the mode resulting in the smallest possible energy consumption during idle mode and startup.

The CDK1307 has a highly linear THA optimized for frequencies up to Nyquist. The differential clock interface is optimized for low jitter clock sources and supports LVDS, LVPECL, sine wave, and CMOS clock inputs.

Functional Block Diagram



CDK1307 Ultra Low Power, 20/40/65/80MSPS, 12/13-bit ADCs Rev 1B

Ordering Information

Part Number	Speed	Package	Pb-Free	RoHS Compliant	Operating Temperature Range	Packaging Method
CDK1307AILP40	20MSPS	QFN-40	Yes	Yes	-40°C to +85°C	Tray
CDK1307BILP40	40MSPS	QFN-40	Yes	Yes	-40°C to +85°C	Tray
CDK1307CILP40	65MSPS	QFN-40	Yes	Yes	-40°C to +85°C	Tray
CDK1307DILP40	80MSPS	QFN-40	Yes	Yes	-40°C to +85°C	Tray

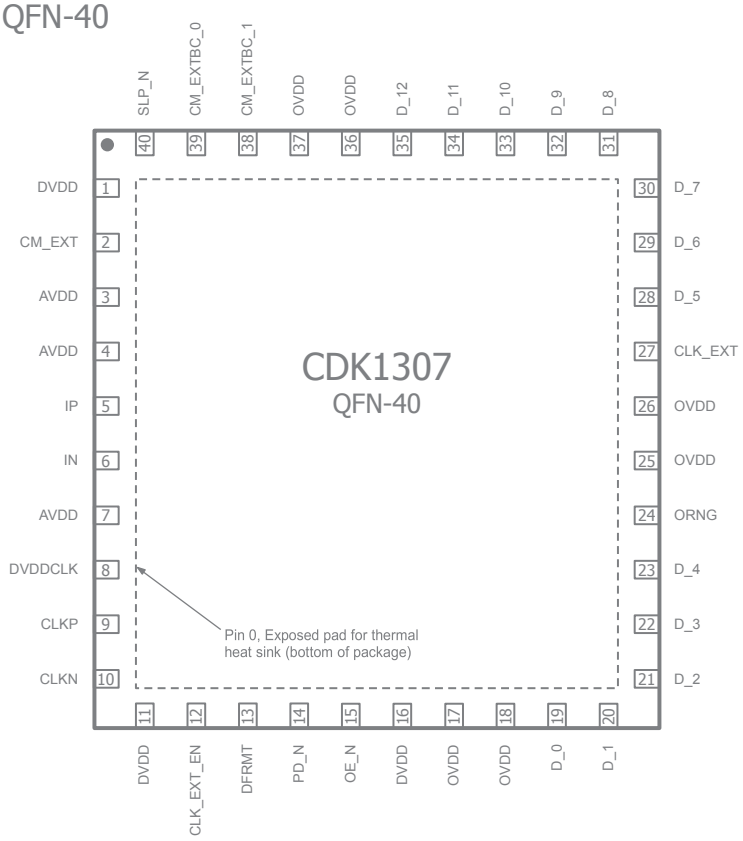
Moisture sensitivity level for all parts is MSL-2A.

Exar Corporation
48720 Kato Road, Fremont CA 94538, USA

www.exar.com
Tel. +1 510 668-7000 - Fax. +1 510 668-7001

Pin Configuration

QFN-40



Pin Assignments

Pin No.	Pin Name	Description
0	VSS	Ground connection for all power domains. Exposed pad
1, 11, 16	DVDD	Digital and I/O-ring pre driver supply voltage, 1.8V
2	CM_EXT	Common Mode voltage output
3, 4, 7	AVDD	Analog supply voltage, 1.8V
5, 6	IP, IN	Analog input (non-inverting, inverting)
8	DVDDCLK	Clock circuitry supply voltage, 1.8V
9	CLKP	Clock input, non-inverting (format: LVDS, LVPECL, CMOS/TTL, Sine Wave)
10	CLKN	Clock input, inverting. For CMOS input on CLKP, Connect CLKN to ground
12	CLK_EXT_EN	CLK_EXT signal enabled when low (zero). Tristate when high.
13	DFRMT	Data format selection. 0: Offset Binary, 1: Two's Complement
14	PD_N	Full chip Power Down mode when Low. All digital outputs reset to zero. After chip power up always apply Power Down mode before using Active Mode to reset chip.
15	OE_N	Output Enable. Tristate when high
17, 18, 25, 26, 36, 37	OVDD	I/O ring post-driver supply voltage. Voltage range 1.7 to 3.6V
19	D_0	Output Data (LSB, 13-bit output or $1V_{pp}$ full scale range)
20	D_1	Output Data (LSB, 12-bit output $2V_{pp}$ full scale range)
21	D_2	Output Data
22	D_3	Output Data

Pin Assignments *(Continued)*

Pin No.	Pin Name	Description
23	D_4	Output Data
24	ORNG	Out of Range flag. High when input signal is out of range
27	CLK_EXT	Output clock signal for data synchronization. CMOS levels
28	D_5	Output Data
29	D_6	Output Data
30	D_7	Output Data
31	D_8	Output Data
32	D_9	Output Data
33	D_10	Output Data
34	D_11	Output Data (MSB for $1V_{pp}$ full scale range, see Reference Voltages section)
35	D_12	Output Data (MSB for $2V_{pp}$ full scale range)
38, 39	CM_EXTBC_1, CM_EXTBC_0	Bias control bits for the buffer driving pin CM_EXT
		00: OFF 01: 50µA
		10: 500µA 11: 1mA
40	SLP_N	Sleep Mode when low

Absolute Maximum Ratings

The safety of the device is not guaranteed when it is operated above the "Absolute Maximum Ratings". The device should not be operated at these "absolute" limits. Adhere to the "Recommended Operating Conditions" for proper device function. The information contained in the Electrical Characteristics tables and Typical Performance plots reflect the operating conditions noted on the tables and plots.

Parameter	Min	Max	Unit
AVDD	-0.3	+2.3	V
DVDD	-0.3	+2.3	V
AVSS, DVSSCK, DVSS, OVSS	-0.3	+0.3	V
OVDD, OVSS	-0.3	+3.9	V
CLKP, CLKN	-0.3	+3.9	V
Analog inputs and outpts (IPx, INx)	-0.3	+2.3	V
Digital inputs	-0.3	+3.9	V
Digital outputs	-0.3	+3.9	V

Reliability Information

Parameter	Min	Typ	Max	Unit
Junction Temperature			TBD	°C
Storage Temperature Range	-60		+150	°C
Lead Temperature (Soldering, 10s)		J-STD-020		

ESD Protection

Product	QFN-40
Human Body Model (HBM)	2kV

Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Operating Temperature Range	-40		+85	°C

Electrical Characteristics

(AVDD = 1.8V, DVDD = 1.8V, DVDDCLK = 1.8V, OVDD = 2.5V, 20/40/65/80MSPS clock, 50% clock duty cycle, -1dBFS 8MHz input signal, 13-bit output, unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DC Accuracy						
	No Missing Codes			Guaranteed		
	Offset Error	Midscale offset		1		mV
	Gain Error	Full scale range deviation from typical	-6		6	%FS
DNL	Differential Non-Linearity	12-bit level		±0.2		LSB
INL	Integral Non-Linearity	12-bit level		±0.6		LSB
V_{CMO}	Common Mode Voltage Output			$V_{AVDD}/2$		V
Analog Input						
V_{CMI}	Input Common Mode	Analog input common mode voltage	V_{CM} -0.1		V_{CM} +0.2	V
V_{FSR}	Full Scale Range, Normal	Differential input voltage range,		2.0		V_{pp}
	Full Scale Range, Option	Differential input voltage range, 1V (see section Reference Voltages)		1.0		V_{pp}
	Input Capacitance	Differential input capacitance		2		pF
	Bandwidth	Input bandwidth, full power	500			MHz
Power Supply						
AVDD, DVDD	Core Supply Voltage	Supply voltage to all 1.8V domain pins. See Pin Configuration and Description	1.7	1.8	2.0	V
OVDD	I/O Supply Voltage	Output driver supply voltage (OVDD). Must be higher than or equal to Core Supply Voltage ($V_{OVDD} \geq V_{OCVDD}$)	1.7	2.5	3.6	V

Electrical Characteristics - CDK1307A

(AVDD = 1.8V, DVDD = 1.8V, DVDDCLK = 1.8V, OVDD = 2.5V, 20MSPS clock, 50% clock duty cycle, -1dBFS 8MHz input signal, 13-bit output, unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Performance						
SNR	Signal to Noise Ratio	F_{IN} = 2MHz		72.5		dBFS
		F_{IN} = 8MHz	71.5	72.2		dBFS
		F_{IN} ≈ FS/2		72.1		dBFS
		F_{IN} = 20MHz		71.6		dBFS
SINAD	Signal to Noise and Distortion Ratio	F_{IN} = 2MHz		72.4		dBFS
		F_{IN} = 8MHz	71	72.0		dBFS
		F_{IN} ≈ FS/2		71.7		dBFS
		F_{IN} = 20MHz		71.3		dBFS
SFDR	Spurious Free Dynamic Range	F_{IN} = 2MHz		87		dBc
		F_{IN} = 8MHz	75	85		dBc
		F_{IN} ≈ FS/2		80		dBc
		F_{IN} = 20MHz		80		dBc
HD2	Second order Harmonic Distortion	F_{IN} = 2MHz		-90		dBc
		F_{IN} = 8MHz	-85	-95		dBc
		F_{IN} ≈ FS/2		-95		dBc
		F_{IN} = 20MHz		-95		dBc
HD3	Third order Harmonic Distortion	F_{IN} = 2MHz		-87		dBc
		F_{IN} = 8MHz	-75	-85		dBc
		F_{IN} ≈ FS/2		-80		dBc
		F_{IN} = 20MHz		-80		dBc
ENOB	Effective number of Bits	F_{IN} = 2MHz		11.7		bits
		F_{IN} = 8MHz	11.5	11.7		bits
		F_{IN} ≈ FS/2		11.6		bits
		F_{IN} = 20MHz		11.6		bits
Power Supply						
AI_{DD}	Analog Supply Current			7.8		mA
DI_{DD}	Digital Supply Current	Digital core supply		1.0		mA
OI_{DD}	Output Driver Supply	2.5V output driver supply, sine wave input, F_{IN} = 1MHz, CLK_EXT enabled		1.7		mA
		2.5V output driver supply, sine wave input, F_{IN} = 1MHz, CLK_EXT disabled		1.3		mA
	Analog Power Dissipation			14.0		mW
	Digital Power Dissipation	OVDD = 2.5V, 5pF load on output bits, F_{IN} = 1MHz, CLK_EXT disabled		5.1		mW
	Total Power Dissipation	OVDD = 2.5V, 5pF load on output bits, F_{IN} = 1MHz, CLK_EXT disabled		19.1		mW
	Power Down Dissipation			9.9		µW
	Sleep Mode	Power Dissipation, Sleep mode		9.2		mW
Clock Inputs						
	Max. Conversion Rate		20			MSPS
	Min. Conversion Rate				15	MSPS

Electrical Characteristics - CDK1307B

(AVDD = 1.8V, DVDD = 1.8V, DVDDCLK = 1.8V, OVDD = 2.5V, 40MSPS clock, 50% clock duty cycle, -1dBFS 8MHz input signal, 13-bit output, unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Performance						
SNR	Signal to Noise Ratio	F_{IN} = 2MHz		72.5		dBFS
		F_{IN} = 8MHz	71.9	72.7		dBFS
		F_{IN} ≈ FS/2		72		dBFS
		F_{IN} = 30MHz		70.8		dBFS
SINAD	Signal to Noise and Distortion Ratio	F_{IN} = 2MHz		71.7		dBFS
		F_{IN} = 8MHz	71	72.1		dBFS
		F_{IN} ≈ FS/2		71.5		dBFS
		F_{IN} = 30MHz		71.2		dBFS
SFDR	Spurious Free Dynamic Range	F_{IN} = 2MHz		81		dBc
		F_{IN} = 8MHz	75	81		dBc
		F_{IN} ≈ FS/2		80		dBc
		F_{IN} = 30MHz		80		dBc
HD2	Second order Harmonic Distortion	F_{IN} = 2MHz		-90		dBc
		F_{IN} = 8MHz	-85	-95		dBc
		F_{IN} ≈ FS/2		-95		dBc
		F_{IN} = 30MHz		-90		dBc
HD3	Third order Harmonic Distortion	F_{IN} = 2MHz		-81		dBc
		F_{IN} = 8MHz		-81		dBc
		F_{IN} ≈ FS/2	-75	-80		dBc
		F_{IN} = 30MHz		-80		dBc
ENOB	Effective number of Bits	F_{IN} = 2MHz		11.6		bits
		F_{IN} = 8MHz	11.5	11.7		bits
		F_{IN} ≈ FS/2		11.6		bits
		F_{IN} = 30MHz		11.4		bits
Power Supply						
AI_{DD}	Analog Supply Current			13.4		mA
DI_{DD}	Digital Supply Current	Digital core supply		1.7		mA
OI_{DD}	Output Driver Supply	2.5V output driver supply, sine wave input, F_{IN} = 1MHz, CLK_EXT enabled		3.3		mA
		2.5V output driver supply, sine wave input, F_{IN} = 1MHz, CLK_EXT disabled		2.4		mA
	Analog Power Dissipation			24.1		mW
	Digital Power Dissipation	OVDD = 2.5V, 5pF load on output bits, F_{IN} = 1MHz, CLK_EXT disabled		9.1		mW
	Total Power Dissipation	OVDD = 2.5V, 5pF load on output bits, F_{IN} = 1MHz, CLK_EXT disabled		33.2		mW
	Power Down Dissipation			9.7		µW
	Sleep Mode	Power Dissipation, Sleep mode		14.2		mW
Clock Inputs						
	Max. Conversion Rate		40			MSPS
	Min. Conversion Rate				20	MSPS

Electrical Characteristics - CDK1307C

(AVDD = 1.8V, DVDD = 1.8V, DVDDCLK = 1.8V, OVDD = 2.5V, 65MSPS clock, 50% clock duty cycle, -1dBFS 8MHz input signal, 13-bit output, unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Performance						
SNR	Signal to Noise Ratio	F_{IN} = 8MHz	71.6	72.6		dBFS
		F_{IN} = 20MHz		71.8		dBFS
		F_{IN} ≈ FS/2		71.5		dBFS
		F_{IN} = 40MHz		70.4		dBFS
SINAD	Signal to Noise and Distortion Ratio	F_{IN} = 8MHz	70.5	71.7		dBFS
		F_{IN} = 20MHz		71.7		dBFS
		F_{IN} ≈ FS/2		71.1		dBFS
		F_{IN} = 40MHz		70		dBFS
SFDR	Spurious Free Dynamic Range	F_{IN} = 8MHz	75	81		dBc
		F_{IN} = 20MHz		84		dBc
		F_{IN} ≈ FS/2		79		dBc
		F_{IN} = 40MHz		77		dBc
HD2	Second order Harmonic Distortion	F_{IN} = 8MHz	-85	-95		dBc
		F_{IN} = 20MHz		-95		dBc
		F_{IN} ≈ FS/2		-95		dBc
		F_{IN} = 40MHz		-95		dBc
HD3	Third order Harmonic Distortion	F_{IN} = 8MHz	-75	-81		dBc
		F_{IN} = 20MHz		-84		dBc
		F_{IN} ≈ FS/2		-79		dBc
		F_{IN} = 40MHz		-79		dBc
ENOB	Effective number of Bits	F_{IN} = 8MHz	11.4	11.6		bits
		F_{IN} = 20MHz		11.6		bits
		F_{IN} ≈ FS/2		11.5		bits
		F_{IN} = 40MHz		11.3		bits
Power Supply						
AI_{DD}	Analog Supply Current			20.4		mA
DI_{DD}	Digital Supply Current	Digital core supply		2.3		mA
OI_{DD}	Output Driver Supply	2.5V output driver supply, sine wave input, F_{IN} = 1MHz, CLK_EXT enabled		5.1		mA
		2.5V output driver supply, sine wave input, F_{IN} = 1MHz, CLK_EXT disabled		3.5		mA
	Analog Power Dissipation			36.7		mW
	Digital Power Dissipation	OVDD = 2.5V, 5pF load on output bits, F_{IN} = 1MHz, CLK_EXT disabled		12.9		mW
	Total Power Dissipation	OVDD = 2.5V, 5pF load on output bits, F_{IN} = 1MHz, CLK_EXT disabled		49.6		mW
	Power Down Dissipation			9.3		µW
	Sleep Mode	Power Dissipation, Sleep mode		20.4		mW
Clock Inputs						
	Max. Conversion Rate		65			MSPS
	Min. Conversion Rate				40	MSPS

Electrical Characteristics - CDK1307D

(AVDD = 1.8V, DVDD = 1.8V, DVDDCLK = 1.8V, OVDD = 2.5V, 80MSPS clock, 50% clock duty cycle, -1dBFS 8MHz input signal, 13-bit output, unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Performance						
SNR	Signal to Noise Ratio	F_{IN} = 8MHz	70.4	72		dBFS
		F_{IN} = 20MHz		71.7		dBFS
		F_{IN} = 30MHz		71.2		dBFS
		F_{IN} ≈ FS/2		70.7		dBFS
SINAD	Signal to Noise and Distortion Ratio	F_{IN} = 8MHz	69.5	70.5		dBFS
		F_{IN} = 20MHz		70.5		dBFS
		F_{IN} = 30MHz		70.5		dBFS
		F_{IN} ≈ FS/2		70.3		dBFS
SFDR	Spurious Free Dynamic Range	F_{IN} = 8MHz	74	77		dBc
		F_{IN} = 20MHz		78		dBc
		F_{IN} = 30MHz		78		dBc
		F_{IN} ≈ FS/2		78		dBc
HD2	Second order Harmonic Distortion	F_{IN} = 8MHz	-80	-95		dBc
		F_{IN} = 20MHz		-90		dBc
		F_{IN} = 30MHz		-90		dBc
		F_{IN} ≈ FS/2		-85		dBc
HD3	Third order Harmonic Distortion	F_{IN} = 8MHz	-74	-77		dBc
		F_{IN} = 20MHz		-78		dBc
		F_{IN} = 30MHz		-78		dBc
		F_{IN} ≈ FS/2		-78		dBc
ENOB	Effective number of Bits	F_{IN} = 8MHz	11.3	11.4		bits
		F_{IN} = 20MHz		11.4		bits
		F_{IN} = 30MHz		11.4		bits
		F_{IN} ≈ FS/2		11.4		bits
Power Supply						
AI_{DD}	Analog Supply Current			24.5		mA
DI_{DD}	Digital Supply Current	Digital core supply		2.9		mA
OI_{DD}	Output Driver Supply	2.5V output driver supply, sine wave input, F_{IN} = 1MHz, CLK_EXT enabled		6.1		mA
		2.5V output driver supply, sine wave input, F_{IN} = 1MHz, CLK_EXT disabled		4.1		mA
	Analog Power Dissipation			44.1		mW
	Digital Power Dissipation	OVDD = 2.5V, 5pF load on output bits, F_{IN} = 1MHz, CLK_EXT disabled		15.5		mW
	Total Power Dissipation	OVDD = 2.5V, 5pF load on output bits, F_{IN} = 1MHz, CLK_EXT disabled		59.6		mW
	Power Down Dissipation			9.1		µW
	Sleep Mode	Power Dissipation, Sleep mode		24.1		mW
Clock Inputs						
	Max. Conversion Rate		80			MSPS
	Min. Conversion Rate				65	MSPS

Digital and Timing Electrical Characteristics

(AVDD = 1.8V, DVDD = 1.8V, DVDDCLK = 1.8V, OVDD = 2.5V, 20/40/65/80MSPS clock, 50% clock duty cycle, -1 dBFS input signal, 5pF capacitive load, unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Clock Inputs						
	Duty Cycle		20		80	% high
	Compliance		CMOS, LVDS, LVPECL, Sine Wave			
	Input Range	Differential input swing	-200		200	mV_{pp}
		Differential input swing, sine wave clock input	-800		800	mV_{pp}
	Input Common Mode Voltage	Keep voltages within ground and voltage of OV_{DD}	0.3		V_{OVDD} -0.3	V
	Input Capacitance	Differential		1.7		pF
Timing						
T_{PD}	Start Up Time from Power Down	From Power Down Mode to Active Mode References has reached 99% of final value			900	clk cycles
T_{SLP}	Start Up Time from Sleep	From Sleep Mode to Active Mode		0.5		µs
T_{OVR}	Out Of Range Recovery Time			1		clk cycles
T_{AP}	Aperture Delay			0.8		ns
ε_{RMS}	Aperture Jitter			<0.5		ps
T_{LAT}	Pipeline Delay			12		clk cycles
T_D	Output Delay	5pF load on output bits (see timing diagram)		4		ns
		10pF load on output bits (see timing diagram)			TBD	ns
T_{DC}	Output Delay Relative to CLK_EXT	See timing diagram		2		ns
Logic Inputs						
V_{IH}	High Level Input Voltage	$V_{OVDD} \geq 3.0V$	2			V
		V_{OVDD} = 1.7V – 3.0V	$0.8 \cdot V_{OVDD}$			V
V_{IL}	Low Level Input Voltage	$V_{OVDD} \geq 3.0V$	0		0.8	V
		V_{OVDD} = 1.7V – 3.0V	0		$0.2 \cdot V_{OVDD}$	V
I_{IH}	High Level Input Leakage Current		-10		10	µA
I_{IL}	Low Level Input Leakage Current		-10		10	µA
C_I	Input Capacitance			3		pF
Logic Outputs						
V_{OH}	High Level Output Voltage		$-0.1 + V_{OVDD}$			V
V_{OL}	Low Level Output Voltage				0.1	V
C_L	Max Capacitive Load	Post-driver supply voltage equal to pre-driver supply voltage $V_{OVDD} = V_{OCVDD}$			5	pF
		Post-driver supply voltage above 2.25V (1)		10		pF

Note:

(1) The outputs will be functional with higher loads. However, it is recommended to keep the load on output data bits as low as possible to keep dynamic currents and resulting switching noise at a minimum.

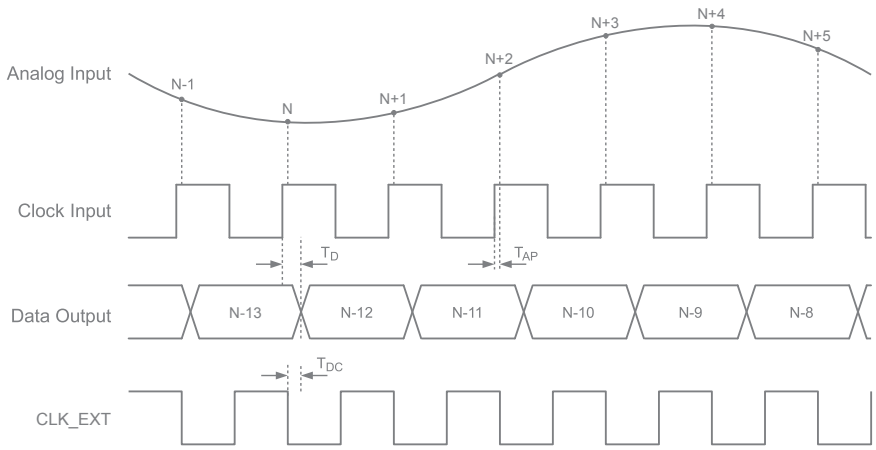


Figure 1. Timing Diagram

Recommended Usage

Analog Input

The analog inputs to the CDK1307 is a switched capacitor track-and-hold amplifier optimized for differential operation. Operation at common mode voltages at mid supply is recommended even if performance will be good for the ranges specified. The CM_EXT pin provides a voltage suitable as common mode voltage reference. The internal buffer for the CM_EXT voltage can be switched off, and driving capabilities can be changed by using the CM_EXT-BC control input.

Figure 2 shows a simplified drawing of the input network. The signal source must have sufficiently low output impedance to charge the sampling capacitors within one clock cycle. A small external resistor (e.g. 22Ω) in series with each input is recommended as it helps reducing transient currents and dampens ringing behavior. A small differential shunt capacitor at the chip side of the resistors may be used to provide dynamic charging currents and may improve performance. The resistors form a low pass filter with the capacitor, and values must therefore be determined by requirements for the application.

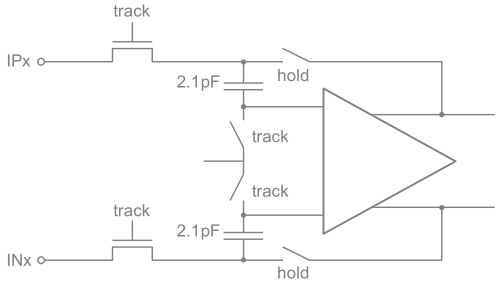


Figure 2. Input Configuration

DC-Coupling

Figure 3 shows a recommended configuration for DC-coupling. Note that the common mode input voltage must be controlled according to specified values. Preferably, the CM_EXT output should be used as a reference to set the common mode voltage.

The input amplifier could be inside a companion chip or it could be a dedicated amplifier. Several suitable single ended to differential driver amplifiers exist in the market. The system designer should make sure the specifications of the selected amplifier is adequate for the total system, and that driving capabilities comply with the CDK1307 input specifications.

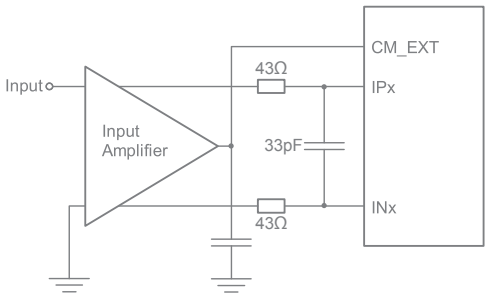


Figure 3. DC-Coupled Input

Detailed configuration and usage instructions must be found in the documentation of the selected driver, and the values given in Figure 3 must be varied according to the recommendations for the driver.

AC-Coupling

A signal transformer or series capacitors can be used to make an AC-coupled input network. Figure 4 shows

a recommended configuration using a transformer. Make sure that a transformer with sufficient linearity is selected, and that the bandwidth of the transformer is appropriate. The bandwidth should exceed the sampling rate of the ADC with at least a factor of 10. It is also important to keep phase mismatch between the differential ADC inputs small for good HD2 performance. This type of transformer coupled input is the preferred configuration for high frequency signals as most differential amplifiers do not have adequate performance at high frequencies. If the input signal is traveling a long physical distance from the signal source to the transformer (for example a long cable), kick-backs from the ADC will also travel along this distance. If these kick-backs are not terminated properly at the source side, they are reflected and will add to the input signal at the ADC input. This could reduce the ADC performance. To avoid this effect, the source must effectively terminate the ADC kick-backs, or the traveling distance should be very short. If this problem could not be avoided, the circuit in Figure 6 can be used.

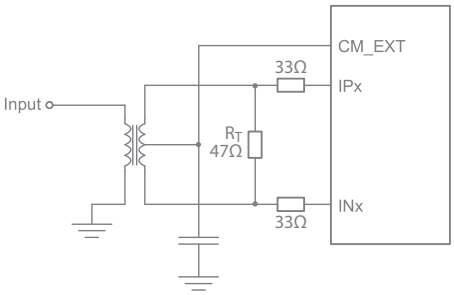


Figure 4. Transformer-Coupled Input

Figure 5 shows AC-coupling using capacitors. Resistors from the CM_EXT output, R_{CM}, should be used to bias the differential input signals to the correct voltage. The series capacitor, C_I, form the high-pass pole with these resistors, and the values must therefore be determined based on the requirement to the high-pass cut-off frequency.

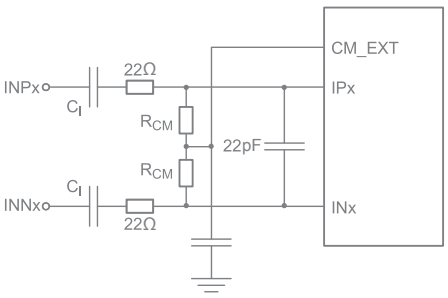


Figure 5. AC-Coupled Input

Note that startup time from Sleep Mode and Power Down Mode will be affected by this filter as the time required to charge the series capacitors is dependent on the filter cut-off frequency.

If the input signal has a long traveling distance, and the kick-backs from the ADC not are effectively terminated at the signal source, the input network of Figure 6 can be used. The configuration is designed to attenuate the kickback from the ADC and to provide an input impedance that looks as resistive as possible for frequencies below Nyquist. Values of the series inductor will however depend on board design and conversion rate. In some instances a shunt capacitor in parallel with the termination resistor (e.g. 33pF) may improve ADC performance further. This capacitor attenuate the ADC kick-back even more, and minimize the kicks traveling towards the source. However, the impedance match seen into the transformer becomes worse.

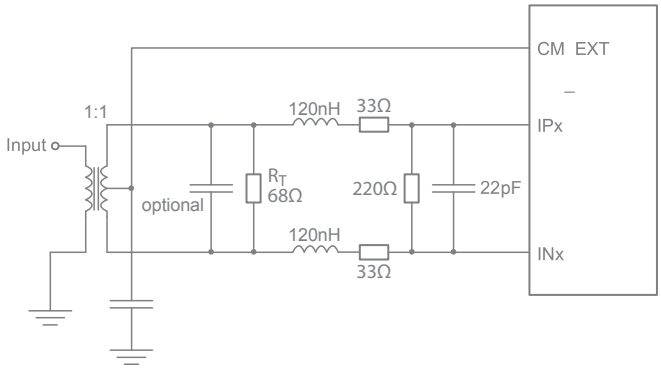


Figure 6. Alternative Input Network

Clock Input And Jitter Considerations

Typically high-speed ADCs use both clock edges to generate internal timing signals. In the CDK1307 only the rising edge of the clock is used. Hence, input clock duty cycles between 20% and 80% is acceptable.

The input clock can be supplied in a variety of formats. The clock pins are AC-coupled internally, and hence a wide common mode voltage range is accepted. Differential clock sources as LVDS, LVPECL or differential sine wave can be connected directly to the input pins. For CMOS inputs, the CLKN pin should be connected to ground, and the CMOS clock signal should be connected to CLKP. For differential sine wave clock input the amplitude must be at least $\pm 800mV_{pp}$.

The quality of the input clock is extremely important for high-speed, high-resolution ADCs. The contribution to SNR from clock jitter with a full scale signal at a given frequency is shown in the equation below:

$$SNR_{jitter} = 20 \cdot \log (2 \cdot \pi \cdot F_{IN} \cdot \varepsilon_t)$$

where F_{IN} is the signal frequency, and ε_t is the total rms jitter measured in seconds. The rms jitter is the total of all jitter sources including the clock generation circuitry, clock distribution and internal ADC circuitry.

For applications where jitter may limit the obtainable performance, it is of utmost importance to limit the clock jitter. This can be obtained by using precise and stable clock references (e.g. crystal oscillators with good jitter specifications) and make sure the clock distribution is well controlled. It might be advantageous to use analog power and ground planes to ensure low noise on the supplies to all circuitry in the clock distribution. It is of utmost importance to avoid crosstalk between the ADC output bits and the clock and between the analog input signal and the clock since such crosstalk often results in harmonic distortion.

The jitter performance is improved with reduced rise and fall times of the input clock. Hence, optimum jitter performance is obtained with LVDS or LVPECL clock with fast edges. CMOS and sine wave clock inputs will result in slightly degraded jitter performance.

If the clock is generated by other circuitry, it should be retimed with a low jitter master clock as the last operation before it is applied to the ADC clock input.

Digital Outputs

Digital output data are presented on parallel CMOS form. The voltage on the OVDD pin set the levels of the CMOS outputs. The output drivers are dimensioned to drive a wide range of loads for OVDD above 2.25V, but it is recommended to minimize the load to ensure as low transient switching currents and resulting noise as possible. In applications with a large fanout or large capacitive loads, it is recommended to add external buffers located close to the ADC chip.

The timing is described in the Timing Diagram section. Note that the load or equivalent delay on CK_EXT always should be lower than the load on data outputs to ensure sufficient timing margins.

The digital outputs can be set in tristate mode by setting the OE_N signal high.

The CDK1307 employs digital offset correction. This means that the output code will be 4096 with shorted inputs. However, small mismatches in parasitics at the input can cause this to alter slightly. The offset correction also results in possible loss of codes at the edges of the full scale range. With no offset correction, the ADC would clip in one end before the other, in practice resulting in code loss at the opposite end. With the output being centered digitally, the output will clip, and the out of range flags will be set, before max code is reached. When out of range flags are set, the code is forced to all ones for over-range and all zeros for under-range.

Data Format Selection

The output data are presented on offset binary form when DFRMT is low (connect to OV_{SS}). Setting DFRMT high (connect to OV_{DD}) results in 2's complement output format. Details are shown in Table 1 on page 14.

The data outputs can be used in three different configurations.

Normal mode:

All 13-bits are used. MSB is D_12 and LSB is D_0. This mode gives optimum performance due to reduced quantization noise.

12-bit mode:

The LSB is left unconnected such that only 12 bits are used. MSB is D_12 and LSB is D_1. This mode gives slightly reduced performance, due to increased quantization noise.

Reduced full scale range mode:

The full scale range is reduced from $2V_{pp}$ to $1V_{pp}$ which is equivalent to 6dB gain in the ADC frontend. MSB is D_11 and LSB is D_0. Note that the codes will wrap around when exceeding the full scale range, and that out of range bits should be used to clamp output data. See section Reference Voltages for details. This mode gives slightly reduced performance.

Table 1: Data Format Description for $2V_{pp}$ Full Scale Range

Differential Input Voltage (IP - IN)	Output data: D_12 : D_0 (DFRMT = 0, offset binary)	Output Data: D_12 : D_0 (DFRMT = 1, 2's complement)
1.0 V	1 1111 1111 1111	0 1111 1111 1111
+0.24mV	1 0000 0000 0000	0 0000 0000 0000
-0.24mV	0 1111 1111 1111	1 1111 1111 1111
-1.0V	0 0000 0000 0000	1 0000 0000 0000

Reference Voltages

The reference voltages are internally generated and buffered based on a bandgap voltage reference. No external decoupling is necessary, and the reference voltages are not available externally. This simplifies usage of the ADC since two extremely sensitive pins, otherwise needed, are removed from the interface.

If a lower full scale range is required the 13-bit output word provides sufficient resolution to perform digital scaling

with an equivalent impact on noise compared to adjusting the reference voltages.

A simple way to obtain $1.0V_{pp}$ input range with a 12-bit output word is shown in the Table 2 below. Note that only 2's complement output data are available in this mode and that out of range conditions must be determined based on a two bit output. The output code will wrap around when the code goes outside the full scale range. The out of range bits should be used to clamp the output data for overrange conditions.

Operational Modes

The operational modes are controlled with the PD_N and SLP_N pins. If PD_N is set low, all other control pins are overridden and the chip is set in Power Down mode. In this mode all circuitry is completely turned off and the internal clock is disabled. Hence, only leakage current contributes to the Power Down Dissipation. The startup time from this mode is longer than for other idle modes as all references need to settle to their final values before normal operation can resume.

The SLP_N bus can be used to power down each channel independently, or to set the full chip in Sleep Mode. In this mode internal clocking is disabled, but some low bandwidth circuitry is kept on to allow for a short startup time. However, Sleep Mode represents a significant reduction in supply current, and it can be used to save power even for short idle periods.

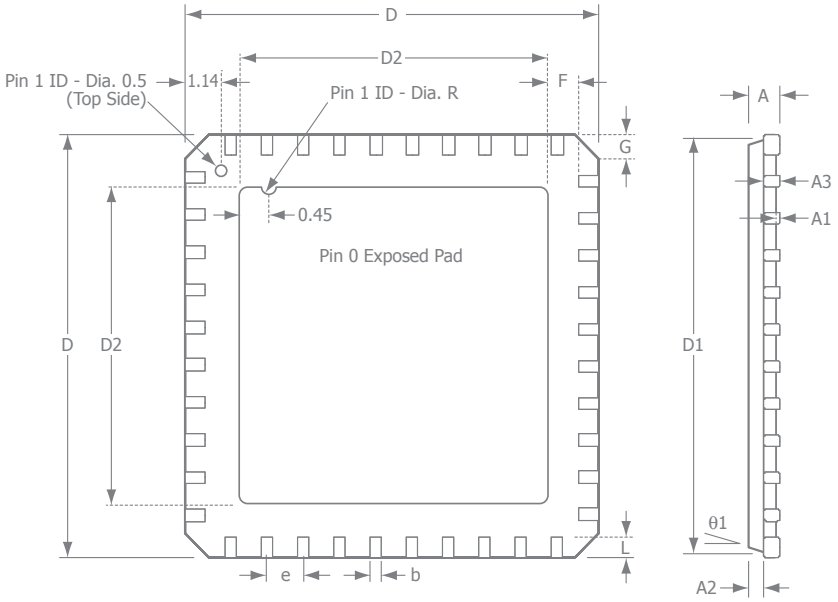
The input clock could be kept running in all idle modes. However, even lower power dissipation is possible in Power Down mode if the input clock is stopped. In this case it is important to start the input clock prior to enabling active mode.

Table 2: Data Format Description for $1V_{pp}$ Full Scale Range

Differential Input Voltage (IP - IN)	Output data: D_11: D_0 (DFRMT = 0) (2's Complement)	Out of Range (Use Logical AND Function for &)	Output Data: D_11: D_0 (DFRMT = 1) (2's Complement)	Out of Range (Use Logical AND Function for &)
> 0.5V	0111 1111 1111	D_12 = 1 & D_11 = 1	0111 1111 1111	D_12 = 0 & D_11 = 1
0.5V	0111 1111 1111		0111 1111 1111	
+0.24mV	0000 0000 0000		0000 0000 0000	
-0.24mV	1111 1111 1111		1111 1111 1111	
-0.5V	1000 0000 0000		1000 0000 0000	
< -0.5V	1000 0000 0000	D_12 = 0 & D_11 = 0	1000 0000 0000	D_12 = 1 & D_11 = 0

Mechanical Dimensions

QFN-40 Package



	Inches			Millimeters		
Symbol	Min	Typ	Max	Min	Typ	Max
A	–	–	0.035	–	–	0.9
A_1	0.001	0.0004	0.002	0.00	0.01	0.05
A_2	–	0.023	0.028	–	0.65	0.7
A_3		0.008 REF			0.2 REF	
b	0.008	0.010	0.013	0.2	0.25	0.32
D		0.236 BSC			6.00 BSC	
D_1		0.226 BSC			5.75 BSC	
D_2	0.156	0.162	0.167	3.95	4.10	4.25
L	0.012	0.016	0.020	0.3	0.4	0.5
e		0.020 BSC			0.50 BSC	
θ_1	0°	–	12°	0°	–	12°
F	0.008	–	–	0.2	–	–
G	0.0096	0.0168	0.024	0.24	0.42	0.6
R	0.004	0.008	–	0.1	0.2	–

NOTE:
Package dimensions in millimeter unless otherwise noted.

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