MP5095

Low I_Q, Dual-Channel, 2.3A Load Switch

The Future of Analog IC Technology

DESCRIPTION

The MP5095 integrates a dual-load switch to provide load protection covering a 0.5V to 5.5V voltage range. Each channel provides up to 2.3A of load protection covering a 0.5V to 5.5V voltage range with a 1.85V VCC power supply. With a small $R_{DS(ON)}$ in a tiny package, the MP5095 provides a very highly efficient and space-saving solution for notebook, tablet, or other portable device applications.

With the internal soft start function, the MP5095 can avoid inrush current during circuit start up. MP5095 also provides internal current limit, hiccup protection and thermal shutdown features. MP5095 also easily parallel both channels to double current capability.

The MP5095 is available in the small TSOT23-8 package.

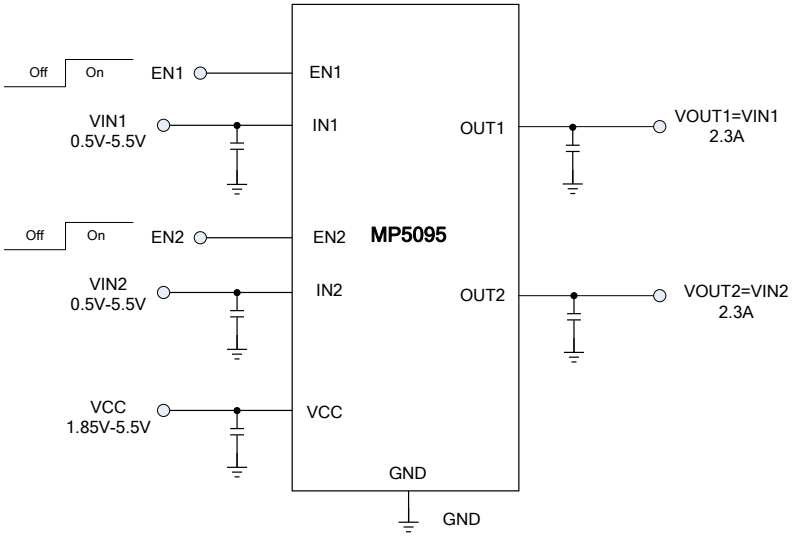
FEATURES

- Integrated 30mΩ Low $R_{DS(ON)}$ MOSFETs
- Low Quiescent Current: 40μA
- Wide V_{IN} Range from 0.5V to 5.5V
- <1μA Shutdown Current
- Output Discharge Function
  Continuous Current Capability: 2.3A
- Enable Pin (EN1, EN2)
- Short-Circuitry Response Protection
- Easily Parallel-Connect Dual Channel
- Supports Reverse Block Connection
- Thermal Protection
- Available in a TSOT23-8 Package

APPLICATIONS

- Notebook and Tablet Computers
- Portable Devices
- Solid State Drivers
- Handheld Devices

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking
MP5095GJ	TSOT23-8	*See Below*

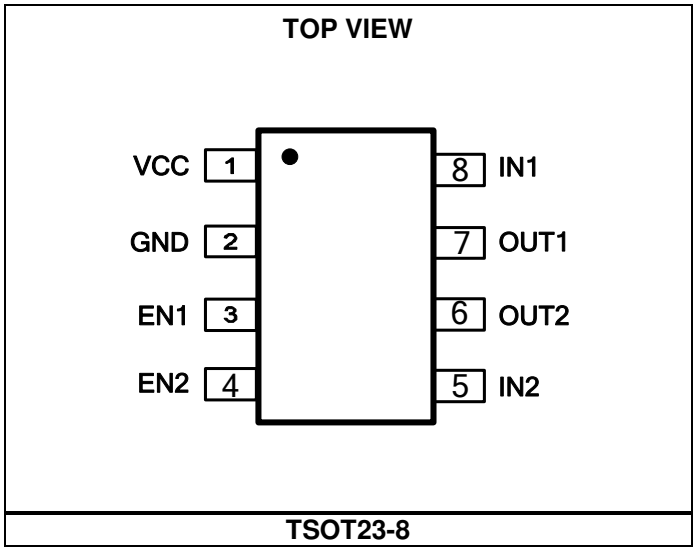
* For Tape & Reel, add suffix –Z (e.g. MP5095GJ–Z).

TOP MARKING

|AUJY

AUJ: Product code of MP5095GJ
Y: Year code

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

$V_{IN1/2}$ ..... -0.3V to +6V
VCC ..... -0.3V to +6V
$V_{OUT1/2}$ ..... -0.3V to +6V
All other pins ..... -0.3V to +6V
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Continuous power dissipation (2) (4) 2.2W

Recommended Operating Conditions (3)

Supply voltage ($V_{IN1/2}$) ..... 0.5V to 5.5V
Supply voltage (VCC) ..... 1.85V to 5.5V
Output voltage ($V_{OUT1/2}$) ..... 0.5V to 5.5V
Operating junction temp. (T_J). .. -40°C to +125°C

Thermal Resistance (2)	θ_{JA}	θ_{JC}	
EV5095-J-00A(4)	54	22	°C/W
JESD51-7(5)	100	55	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on MPS EV5095-J-00A, 2-layer PCB
5) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 3.6V, VCC = 3.6V, T_J = -40°C to +125°C, Typical value is tested at T_J = +25°C. The limit over temperature is guaranteed by characterization, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Input and Supply Voltage Range						
Input voltage	$V_{IN1/2}$		0.5		5.5	V
Supply voltage	V_{CC}		1.85		5.5	V
Supply Current (Single Channel)						
Off state leakage current	I_{OFF}	V_{IN} = 5V, EN = 0, T_J = 25°C			1	µA
VCC standby current	I_{STBY}	VCC = 3.6V, EN = 0, T_J = 25°C		0.1	1	µA
		VCC = 3.6V, enable, no load		40		
Power MOSFET						
On resistance	$R_{DSON1/2}$	VCC = 5.0V, single channel		30		mΩ
		VCC = 3.3V, single channel		35		
Thermal Shutdown and Recovery						
Shutdown temperature (5)	T_{STD}			155		°C
Hysteresis (5)	T_{HYS}			30		°C
Under-Voltage Lockout (UVLO) Protection						
VCC under-voltage lockout threshold	$V_{CC\ UVLO}$	UVLO rising threshold		1.7	1.85	V
UVLO hysteresis	$V_{UVLOHYS}$			100		mV
Soft Start (SS)						
Vo rise time	T_{ss}	Vo = 3.6V, 10% to 90%		30		µs
EN turn on time	T_{DELAY}			30		µs
Enable (ENx)						
EN rising threshold	V_{ENH}			1	1.2	V
EN hysteresis	V_{ENHYS}			200		mV
EN resistance		Between EN and GND		1		MΩ
ILIM						
Current limit (5)	I_{LIM}	VCC = 5V, T_J = 25°C	2.3	2.75	3.2	A
Hiccup on time	T_{ON}			2		ms
Hiccup off time	T_{OFF}			90		ms
Discharge Resistance (Single Channel)						
Resistance	R_{DIS}			50		Ω

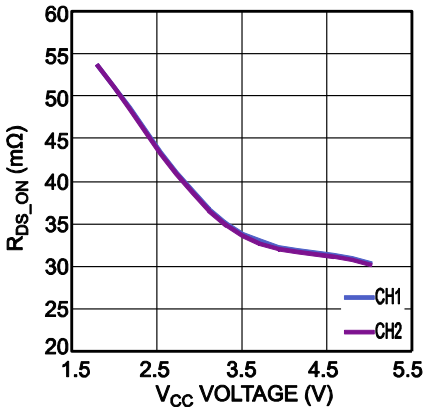
NOTE:

6) Guarantee by characterization -Not production tested.

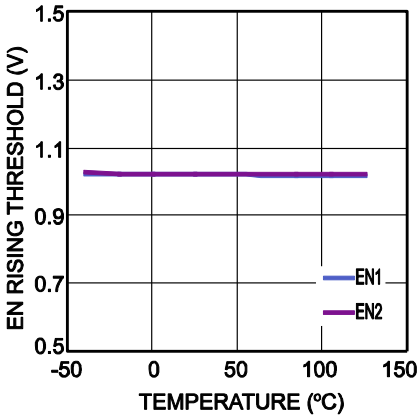
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.6V, VCC = 3.6V, T_A = 25°C, unless otherwise noted.

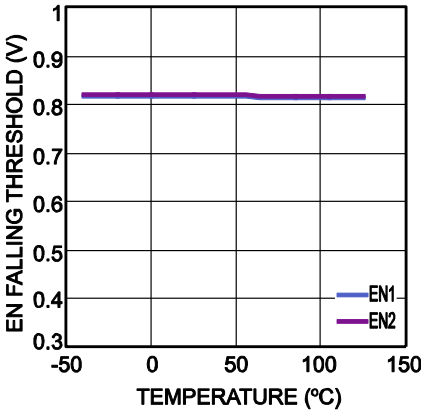
$R_{DS(ON)}$ vs. VCC



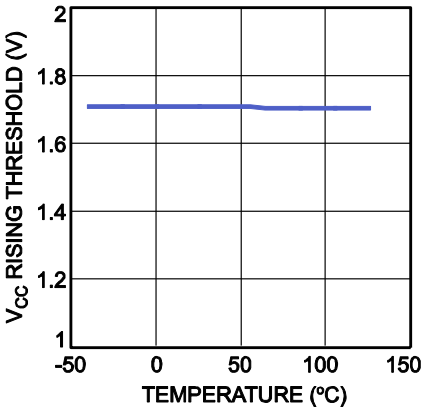
EN Rising Threshold



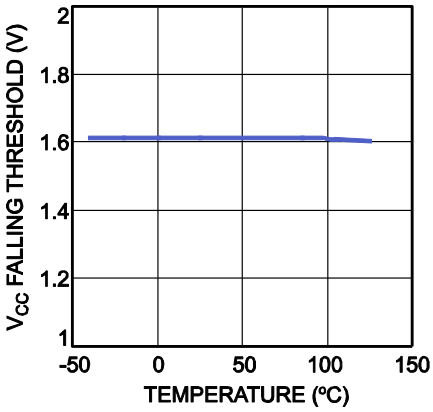
EN Falling Threshold



VCC Rising Threshold



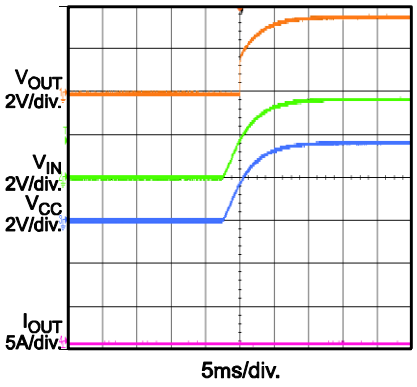
VCC Falling Threshold



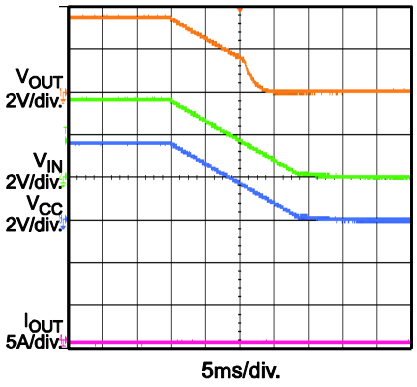
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.6V, VCC = 3.6V, T_A = 25°C, unless otherwise noted.

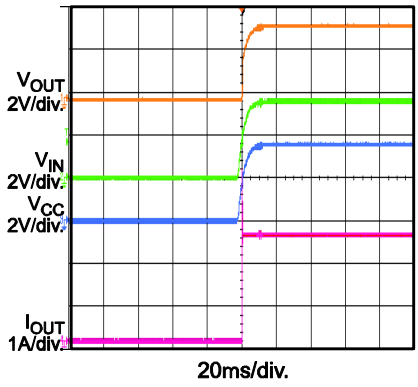
V_{IN} Start-Up
with No Load



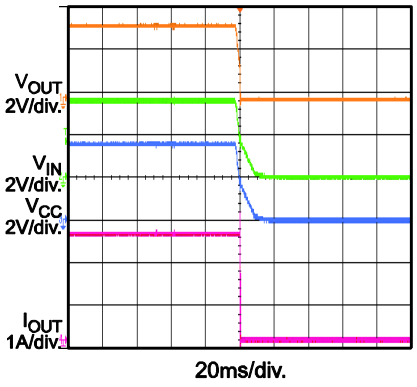
V_{IN} Shutdown
with No Load



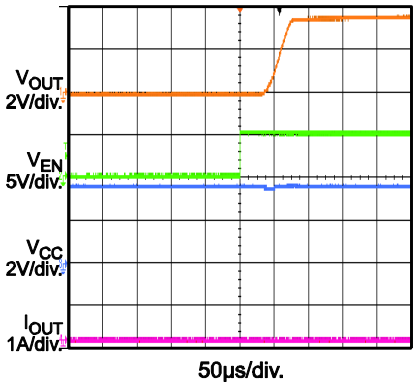
V_{IN} Start-Up
with 2.3A Load



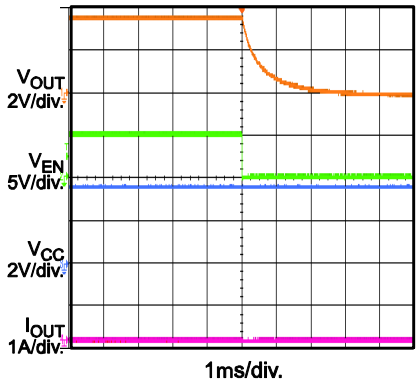
V_{IN} Shutdown
with 2.3A Load



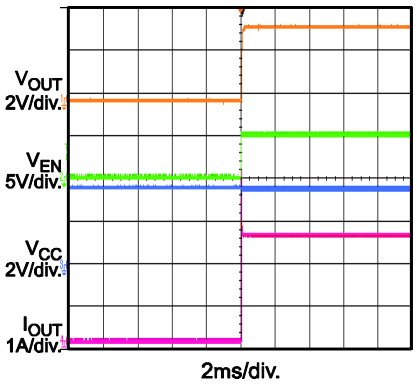
EN Start-Up
with No Load



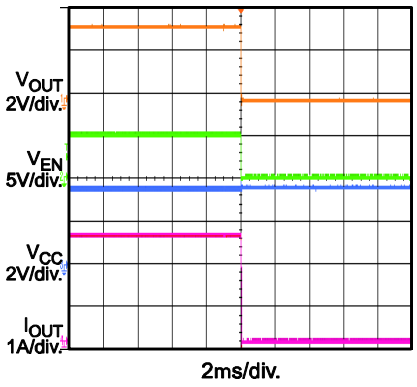
EN Shutdown
with No Load



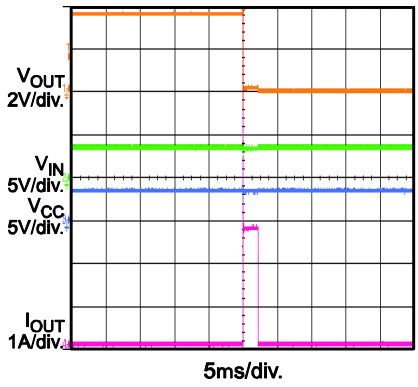
EN Start-Up
with 2.3A Load



EN Shutdown
with 2.3A Load



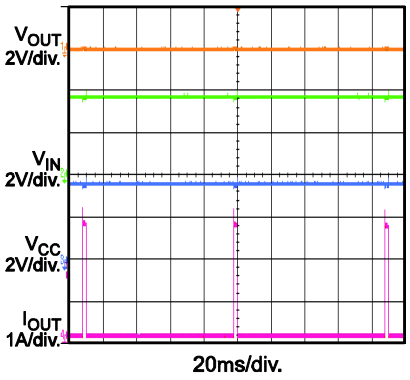
Short Enter



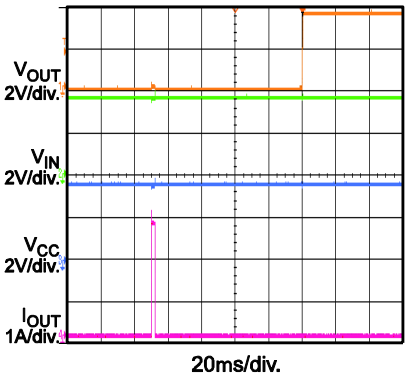
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.6V, VCC = 3.6V, T_A = 25°C, unless otherwise noted.

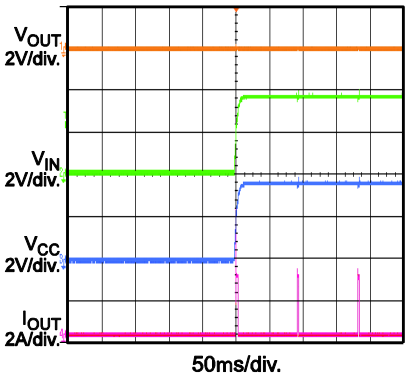
Short Steady State



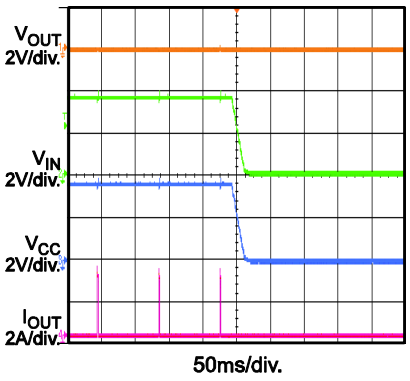
Short Recovery



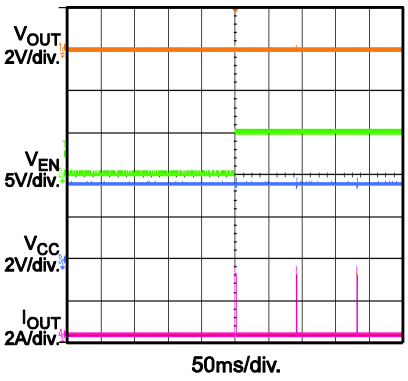
V_{IN} Start-Up with Short



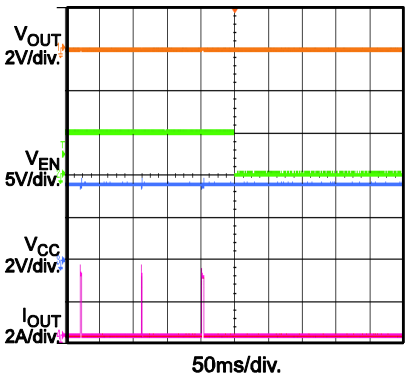
V_{IN} Shutdown with Short



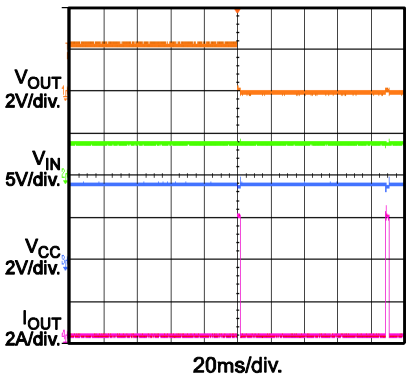
EN Start-Up with Short



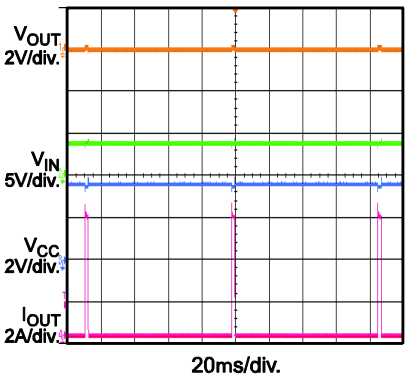
EN Shutdown with Short



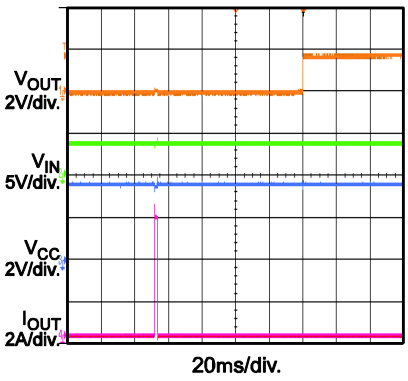
Short Enter (Parallel)



Short Steady (Parallel)



Short Recovery (Parallel)



PIN FUNCTIONS

Pin #	Name	Description
1	VCC	**Load switch supply voltage to the control circuitry.**
2	GND	**Ground.**
3	EN1	**Enable input of switch 1.** Pull EN1 below the specified threshold to shut the chip down.
4	EN2	**Enable input of switch 2.** Pull EN2 below the specified threshold to shut the chip down.
5	IN2	**Input power supply of switch 2.**
6	OUT2	**Output to the load of switch 2.**
7	OUT1	**Output to the load of switch 1.**
8	IN1	**Input power supply of switch 1.**

BLOCK DIAGRAM

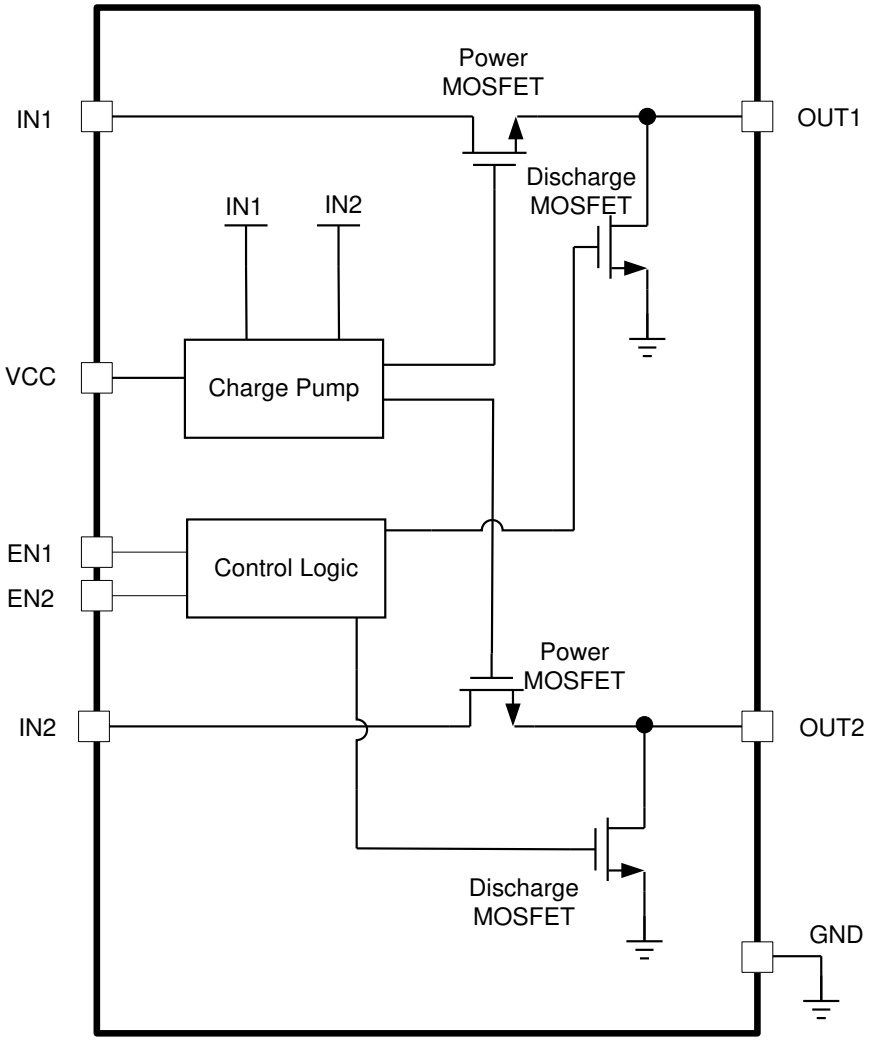


Figure 1: Functional Block Diagram

OPERATION

The MP5095 is designed to limit the inrush current to the load when a circuit card is inserted into a live backplane power source, thereby limiting the backplane's voltage drop and the slew rate of the voltage to the load. MP5095 integrates dual load switches. Each channel can provide 2.3A of current load capability. The MP5095 can also easily parallel both channels connected together to achieve a maximum 5A load.

Enable (EN1, EN2)

When the input voltage is greater than the under-voltage lockout (UVLO) threshold (typically 0.5V), and VCC is higher than 1.85V, the MP5095 can be enabled by pulling EN above 1.2V. Pull EN to ground to disable the MP5095. The recommended start-up sequence is to power up VCC and V_{IN} first. After they are ready, pull the EN voltage to high.

Short-Circuit Protection (SCP)

If the load current increases rapidly due to a short circuit, the current may exceed the current limit threshold greatly before the control loop can respond. If the current reaches an internal secondary current limit level (about 5A), a fast turn-off circuit activates to turn off the power MOSFET. This limits the peak current through the switch to limit the input voltage drop. The total short-circuit response time is about 200ns. Fast off keeps the power MOSFET off for 80µs before turning it back on.

If the current limit block starts to regulate the output current, the power loss on the power MOSFET causes the IC temperature to rise. Hiccup protection limits the current for 2ms and turns it off for another 90ms for the thermal sink. If the junction temperature rises high enough during the hiccup on time, thermal shutdown is triggered. After thermal shutdown, the output is disabled until the over-temperature fault is removed. The over-temperature threshold is 155°C, and the hysteresis is 30°C.

Output Discharge

The MP5095 has an output discharge function. The output discharge resistor is active when EN or VCC is low. This function can discharge Vo by pulling down the resistance when the IC is disabled and the load is very light.

APPLICATION INFORMATION

Selecting the VCC Capacitor

VCC is an internal load switch supply voltage to the control circuitry. Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 1µF capacitor is sufficient.

Selecting the Input and Output Capacitor

The input capacitor is very important for protecting the part from input voltage spikes when a dead short or V_{IN} hot-plug occurs. 0805 ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 10µF 0805 input capacitor and a 1µF 0603 output capacitor are sufficient for each channel. For high input voltage applications, an input capacitor 22µF or greater for each channel is highly recommended.

Reverse Current Block Usage

The dual-channel load switch can be combined to a single-channel load switch with a reverse current block function (see Figure 2). IN1 is the input port, and IN2 is the output port. When EN1 = EN2 = high, the internal MOSFET is on. When EN1 = EN2 = low, the internal MOSFET is off, and the body diode blocks the reverse current.

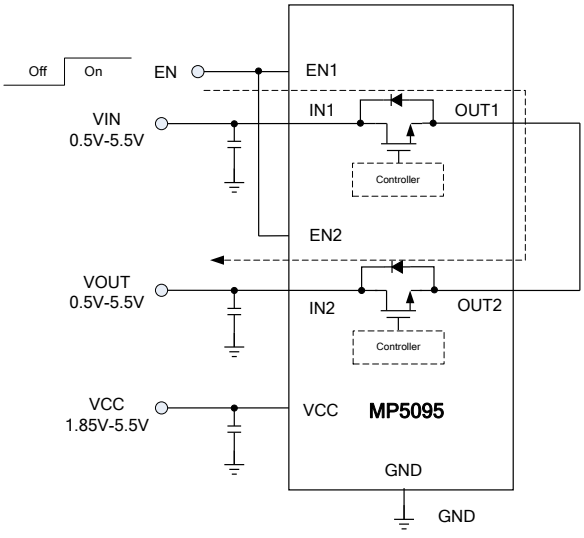


Figure 2: Reverse Current Block Usage

Parallel Channels Usage

The MP5095 can be parallel-connected to achieve a 4.6A single-load switch (see Figure 3). In this parallel connection, IN1 is connected to IN2 externally, and OUT1 is connected to OUT2 externally.

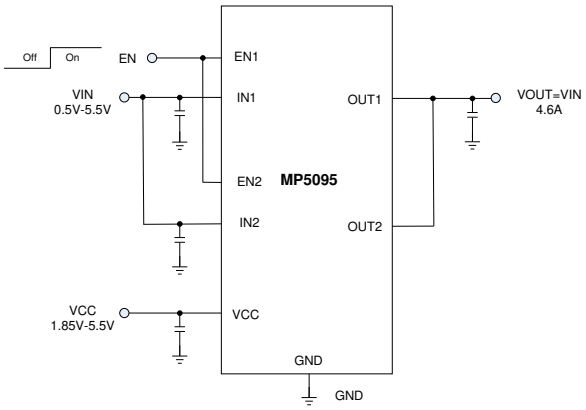
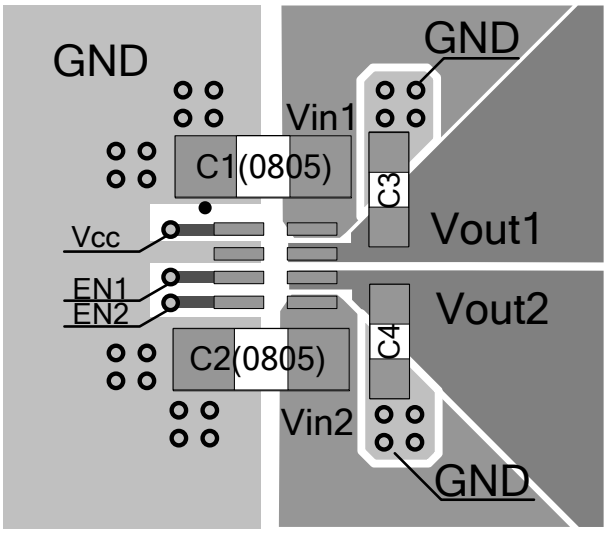


Figure 3: Parallel Channels Usage

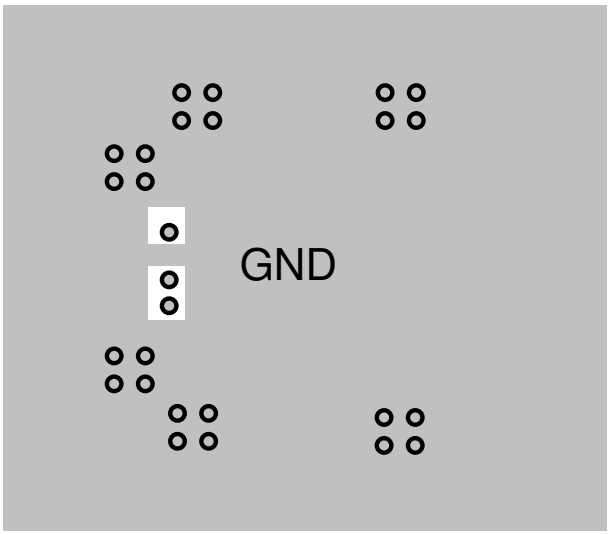
PCB **Layout Guidelines**

Efficient PCB layout is critical for stable operation. For best results, refer to Figure 4 and follow the guidelines below.

1. Place the caps close to the pins.
2. Place enough vias around the IC to achieve better thermal performance.



Top Layer



Bottom Layer

Figure 4: Recommended Layout

TYPICAL APPLICATION CIRCUIT

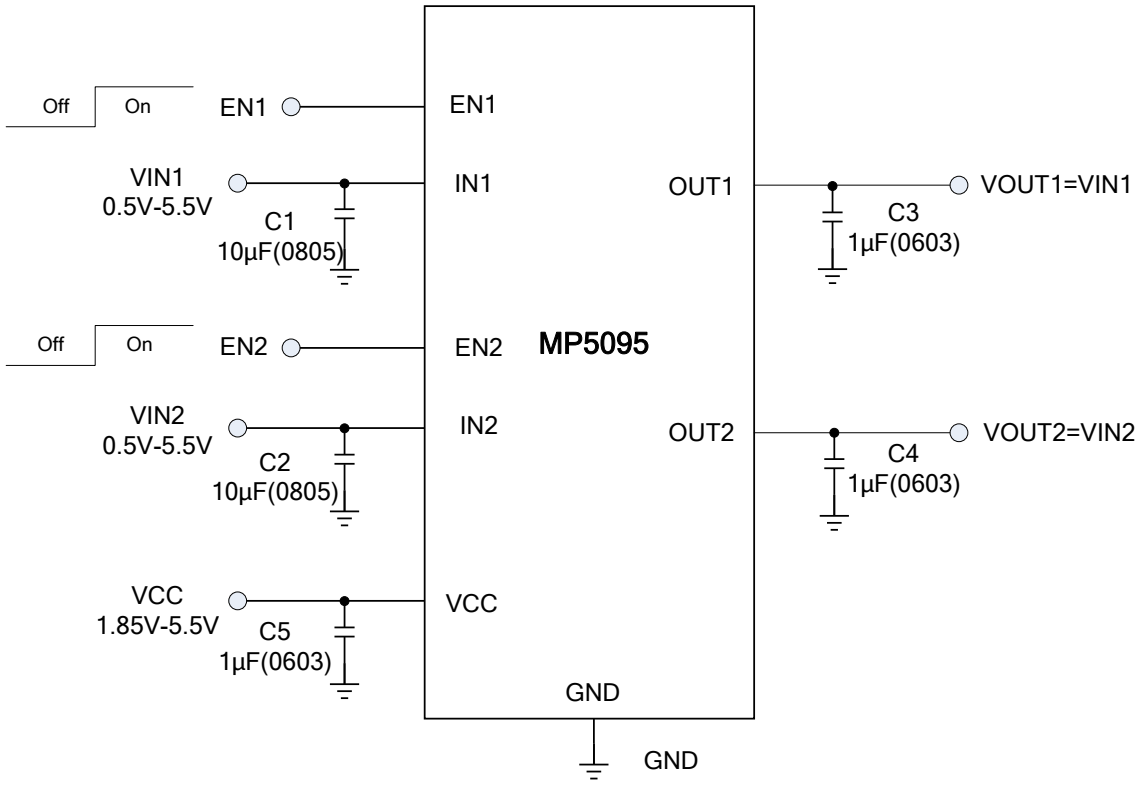
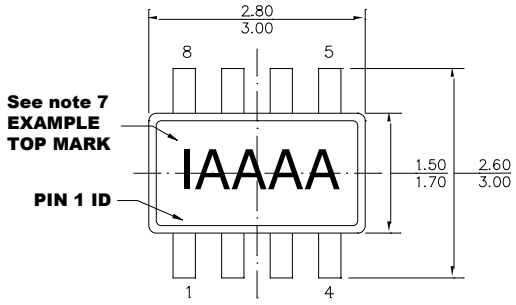


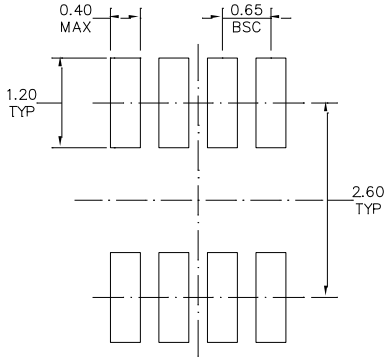
Figure 5: Typical Application Schematic

PACKAGE INFORMATION

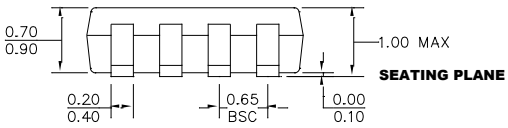
TSOT23-8



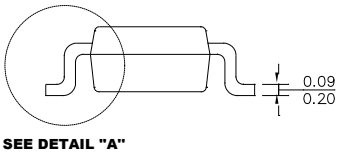
TOP VIEW



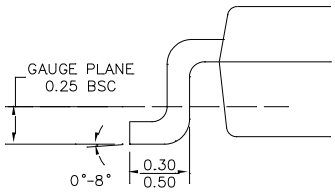
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-193, VARIATION BA.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)