Qorivva 32-bit MCUs

Qorivva MPC567xK Family

Automotive safety and chassis control applications

Overview

The MPC5675K is a Qorivva 32-bit embedded MCU designed for automotive safety and chassis applications such as advanced driver assistance systems (ADAS) with radar, CMOS imaging, LIDAR and ultrasonic sensing functionality. The MPC567xK MCU is part of the SafeAssure program, which is designed to help system manufacturers more easily achieve compliance with functional safety standards. Part of the MPC5500/5600 family, the MPC5675K contains the Book E compliant core built on Power Architecture® technology with variable length encoding (VLE). This core complies with the Power Architecture embedded category, and is 100 percent user mode compatible with the original PowerPC user instruction set architecture. It offers system performance up to four times that of its MPC5561 predecessor, while bringing you the reliability and familiarity of proven Power Architecture technology.

All devices in this family are built around a dual-core safety platform with an innovative safety concept targeting systems with ISO 26262, ASIL-D safety integrity levels. In order to minimize additional software and module level features to reach this target, on-chip redundancy is offered for the critical components of the MCU (CPU core, DMA controller, interrupt controller, crossbar bus system, memory protection unit, flash memory and RAM controllers, peripheral bus bridge, system timers and watchdog timer). Lock step redundancy checking units are implemented at each output of this sphere of replication (SoR).

A comprehensive suite of hardware and software development tools is available to help simplify and speed system design. Development support is available from leading tool vendors, providing compilers, debuggers and simulation development environments.

Features

The Qorivva MPC567xK features a dual-core 180 MHz Qorivva MCU, with up to 2 MB flash and 512 KB SRAM, plus a feature set optimized for ADAS and chassis control applications.

The ADAS market is growing fast. As historically premium applications such as RADAR and camera-based assistance systems proliferate into the mid range, there is a need to reduce system cost.

MPC567xK has a decoupled parallel mode where the two e200 cores may be separated in order to run parallel processing tasks. Together with up to 512 KB SRAM and 2 MB flash, the MPC567xK provides enough data handling headroom to manage these applications. Additional peripherals such as quad ADC, DDR, PDI and FEC help at the system level.

Additionally, there is a trend towards safety assessment for ADAS systems. The safety architecture of the Qorivva MPC567xK assists with assessment and a reduction of common faults.

Development Tools

Compilers

- Freescale CodeWarrior IDE (freescale.com/CodeWarrior)
- Green Hills Software
- Wind River Diab

Debuggers

- P&E Micro
- Lauterbach
- Green Hills Software

Runtime Software

- Flash and FEE drivers
- Software core self test
- AUTOSAR MCU

Abstraction Layer

- AUTOSAR OS

Specifications

Core

- Up to 180 MHz Power Architecture ISA dual e200z7 core
- 16 KB D cache and 16 KB I cache
- Safety enhanced cores + SPE2 + VLE + MMU
- Dual parallel or lock step configuration + HW/SW monitoring

Memory

- Up to 2 MB flash with ECC
- 4 x 16 KB EEPROM flash with ECC
- Up to 512 KB SRAM with ECC
- Dual crossbar with MPUs

I/O

- 4 x FlexCAN (32 message buffers each)
- 1 x FlexRay (64 msg. buffers)
- 1 x Fast Ethernet controller
- 4 x LINFlex (SCI)
- 3 x I^2C
- 3 x DSPI
- 3 x FlexPWM (3 x 12 channels)
- 3 x eTimer (3 x 6 channels)
- Quad ADC (11 channels each, 12-bit)
- 2 x CTU
- External bus interface (slave only)
- Parallel digital interface
- MDDR interface

SafeAssure Program: Functional Safety. Simplified

Freescale's SafeAssure functional safety program is designed to help system manufacturers more easily achieve system compliance with functional safety standards: International Standards Organization (ISO) 26262 and 61508. The program highlights Freescale solutions—hardware and software—that are optimally designed to support functional safety implementations and come with a rich set of enablement collateral.

For more information, visit **freescale.com/SafeAssure.**

Features		MPC5673K	MPC5674K	MPC5675K
CPU	Type	2×e200z7d (SoR) in lock-step or decoupled operation		
	Architecture	Harvard		
	Execution speed	0–150 MHz (+2% FM)	0–180 MHz (+2% FM)	0–180 MHz (+2% FM)
	Nominal platform frequency (in 1:1, 1:2, and 1:3 modes)	0–75 MHz (+2% FM)	0–90 MHz (+2% FM)	0–90 MHz (+2% FM)
	MMU	64 entries (SoR)		
	Instruction set PPC	Yes		
	Instruction set VLE	Yes		
	Instruction cache	16 KB, 4-way with EDC (SoR)		
	Data cache	16 KB, 4-way with EDC (SoR)		
	MPU	Yes (SoR)		
Buses	Core bus	32-bit address, 64-bit data		
	Internal periphery bus	32-bit address, 32-bit data		
XBAR	Master x slave ports	Yes (SoR)		
Memory	Static RAM	256 KB (ECC)	384 KB (ECC)	512 KB (ECC)
	Code flash memory	1 MB	1.5 MB	2 MB
	Data flash memory	64 KB2		
Modules	Analog-to-digital converter	257 pin pkg: 4 x 12-bit (22 external channels), 473 pin pkg: 4 x 12-bit (up to 34 external channels)		
	CRC unit	Two (three contexts each)		
	Cross triggering unit	Two modules		
	Deserial serial peripheral interface	Two modules (three chip selects)	Three modules (three chip selects)	
	Digital I/Os	≥16		
	DRAM controller	No	Yes	
	Enhanced direct memory access	Two modules, 32 channels each		
	eTimer	Three modules, six channels each		
	External bus interface	One module, 16-bit data + address or 32-bit data with address bus muxed		
	Fast ethernet controller	One module		
	Fault collection and control unit	One module		
	FlexCAN	Four modules (32 message buffers each)		
	FlexPWM	Three modules (each 4 x 3 channels)		
	FlexRay	Optional		
	I^2C	Two modules	Three modules	
	Interrupt controller	Yes (SoR)		
	LINFlex	Three modules	Four modules	
	Parallel data interface	One module		
	Periodic interrupt timer	One module, four channels		
	Software watchdog timer	Yes (SoR)		
	System timer module	Yes (SoR)		
	Temperature sensor	One module		
	Wakeup unit	Yes		
	Crossbar switch	Three modules, two are user-configurable		
Clocking	Clock monitor unit	Three modules		
	Clock output	Two modules		
	Frequency-modulated phase-locked loop	Two modules (system and auxiliary)		
	IRCOSC—16 MHz	One		
	XOSC 4 MHz–40 MHz	One		
Supply	Power management unit	Yes		
	1.2V low-voltage detector (LVD12)	One		
	1.2V high-voltage detector (HVD12)	One		
	2.7V low-voltage detector (LVD27)	Four		
Debug	Nexus	Class 3+ (for cores and SRAM ports)		
Packages	MAPBGA	257 pins, 473 pins		
Temperature	Ambient	See the TA recommended operating condition in the device data sheet		

For more information, visit freescale.com/Qorivva

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