

Qorivva 32-bit MCUs

Qorivva MPC567xK Family

Power



Overview

The MPC5675K is a Qorivva 32-bit embedded MCU designed for automotive safety and chassis applications such as advanced driver assistance systems (ADAS) with radar, CMOS imaging, LIDAR and ultrasonic sensing functionality. The MPC567xK MCU is part of the SafeAssure program, which is designed to help system manufacturers more easily achieve compliance with functional safety standards. Part of the MPC5500/5600 family, the MPC5675K contains the Book E compliant core built on Power Architecture® technology with variable length encoding (VLE). This core complies with the Power Architecture embedded category, and is 100 percent user mode compatible with the original PowerPC user instruction set architecture. It offers system performance up to four times that of its MPC5561 predecessor, while bringing you the reliability and familiarity of proven Power Architecture technology.

All devices in this family are built around a dual-core safety platform with an innovative safety concept targeting systems with ISO 26262, ASIL-D safety integrity levels. In order to minimize additional software and module level features to reach this target,

Automotive safety and chassis control applications

on-chip redundancy is offered for the critical components of the MCU (CPU core, DMA controller, interrupt controller, crossbar bus system, memory protection unit, flash memory and RAM controllers, peripheral bus bridge, system timers and watchdog timer). Lock step redundancy checking units are implemented at each output of this sphere of replication (SoR).

A comprehensive suite of hardware and software development tools is available to help simplify and speed system design. Development support is available from leading tool vendors, providing compilers, debuggers and simulation development environments.

Features

The Qorivva MPC567xK features a dual-core 180 MHz Qorivva MCU, with up to 2 MB flash and 512 KB SRAM, plus a feature set optimized for ADAS and chassis control applications.

The ADAS market is growing fast. As historically premium applications such as RADAR and camera-based assistance systems proliferate into the mid range, there is a need to reduce system cost.

MPC567xK has a decoupled parallel mode where the two e200 cores may be separated in order to run parallel processing tasks. Together

with up to 512 KB SRAM and 2 MB flash, the MPC567xK provides enough data handling headroom to manage these applications.

Additional peripherals such as quad ADC, DDR, PDI and FEC help at the system level.

Additionally, there is a trend towards safety assessment for ADAS systems. The safety architecture of the Qorivva MPC567xK assists with assessment and a reduction of common faults.

Development Tools

Compilers

- Freescale CodeWarrior IDE (freescale.com/CodeWarrior)
- o Green Hills Software
- Wind River Diab

Debuggers

- P&E Micro
- Lauterbach
- o Green Hills Software

Runtime Software

- o Flash and FEE drivers
- o Software core self test
- AUTOSAR MCU

Abstraction Layer

• AUTOSAR OS





Specifications

Core

- Up to 180 MHz Power Architecture ISA dual e200z7 core
- 16 KB D cache and 16 KB I cache
- Safety enhanced cores + SPE2 + VLE + MMU
- Dual parallel or lock step configuration
 + HW/SW monitoring

Memory

- Up to 2 MB flash with ECC
- 4 x 16 KB EEPROM flash with ECC
- Up to 512 KB SRAM with ECC
- · Dual crossbar with MPUs

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- 4 x FlexCAN (32 message buffers each)
- 1 x FlexRay (64 msg. buffers)
- 1 x Fast Ethernet controller
- 4 x LINFlex (SCI)
- 3 x I²C
- 3 x DSPI
- 3 x FlexPWM (3 x 12 channels)
- 3 x eTimer (3 x 6 channels)
- Quad ADC (11 channels each, 12-bit)
- 2 x CTU
- External bus interface (slave only)
- Parallel digital interface
- MDDR interface

SafeAssure Program: Functional Safety. Simplified

Freescale's SafeAssure functional safety program is designed to help system manufacturers more easily achieve system compliance with functional safety standards: International Standards Organization (ISO) 26262 and 61508. The program highlights Freescale solutions—hardware and software—that are optimally designed to support functional safety implementations and come with a rich set of enablement collateral.

For more information, visit freescale.com/SafeAssure.

Nominal platform frequency (in 1:1, 1:2, and 1:3 modes) Nominal platform frequency (in 1:1, 1:2, in 2:2 modes) Nominal platform frequency (in 1:1, 1:2, in 2:2 modes) Nominal platform frequency (in 1:1, 1:2, in 2:2 modes) Nominal platform frequency (in 1:1, 1:2, in 2:2 modes) Nominal platform frequency (in 1:1, 1:2, in 2:2 modes) Nominal platform frequency (in 1:1, 1:2, in 2:2 modes) Nominal platform fr		Features	MPC5673K	MPC5674K	MPC5675K	
Execution speed		Туре	2×e200z7d (SoF	R) in lock-step or decoup	led operation	
Nominal platform frequency (in 1:1, 1:2, and 1:3 modes) Nominal platform frequency (in 1:1, 1:2, and 1:3 modes) Nominal platform frequency (in 1:1, 1:2, and 1:3 modes) Nominal platform frequency (in 1:1, 1:2, and 1:3 modes) Nominal platform frequency (in 1:1, 1:2, and 1:3 modes) Nominal platform frequency (in 1:1, 1:2, and 1:3 modes) Nominal platform frequency (in 1:1, 1:2, and 1:3 modes) Nominal platform frequency (in 1:1, 1:2, and 1:3 modes) Nominal platform frequency (in 1:1, 1:2, and 1:3 modes) Nominal platform frequency Nominal platf	СРИ	Architecture	Harvard			
Modules		Execution speed	0–150 MHz (+2% FM)	0–180 MHz (+2% FM)	0–180 MHz (+2% FM)	
Instruction set PPC			0–75 MHz (+2% FM)	0–90 MHz (+2% FM)	0–90 MHz (+2% FM)	
Instruction set VLE		MMU	64 entries (SoR)			
Instruction cache		Instruction set PPC	Yes			
Data cache		Instruction set VLE	Yes			
MPU		Instruction cache	16 KB, 4-way with EDC (SoR)			
Core bus 32-bit address, 64-bit data		Data cache	16 KB, 4-way with EDC (SoR)			
Internal periphery bus 32-bit address, 32-bit data		MPU	Yes (SoR)			
Internal periphery bus 32-bit address, 32-bit data	Buses	Core bus				
Static RAM	4000	Internal periphery bus	32-bit address, 32-bit data			
Memory Code flash memory 1 MB	BAR	Master x slave ports				
Data flash memory Analog-to-digital converter Analog-to-digital converter CRC unit CRC unit Deserial serial peripheral interface Digital I/Os DRAM controller External bus interface Fast ethernet controller Fault collection and control unit FlexRay PC Interrupt controller LINFlex Parallel data interface Clock ing Clock ing Clock ing Clock ing Clock ing Clock ing Analog-to-digital converter Analog-to-digital converter 257 pin pkg: 4 x 12-bit (up to 34 external channels), 473 pin 4 x 12-bit (up to 34 external channels), 473 pin 4 x 12-bit (up to 34 external channels), 473 pin 4 x 12-bit (up to 34 external channels), 473 pin 4 x 12-bit (up to 34 external channels), 473 pin 4 x 12-bit (up to 34 external channels) Two modules (three chip sel chip s	Memory	Static RAM	256 KB (ECC)	384 KB (ECC)	512 KB (ECC)	
Analog-to-digital converter CRC unit CRC unit Two (three contexts each) Two modules Deserial serial peripheral interface Digital I/Os DRAM controller Enhanced direct memory access eTimer Three modules, 32 channels each External bus interface Fast ethernet controller Fault collection and control unit FlexCAN FlexPWM FlexRay PiexRay Periodic interrupt timer Software watchdog timer Cross triggering unit Two modules (12 external channels), 473 pin 4 x 12-bit (22 external channels) Two (three contexts each) Two modules (three chip sel three chip sel three chip sel three chip sel three modules, 12 channels each Three modules, 32 channels each One module, 16-bit data + address or 32-bit data waddress bus muxed One module Fault collection and control unit FlexCAN Four modules (32 message buffers each) FlexPWM Three modules (32 message buffers each) FlexRay Optional FiexPWM Three modules (32 message buffers each) FlexRay Optional FiexCAN Four modules (32 message buffers each) FlexRay Optional FiexCAN Four modules (32 message buffers each) FlexRay Optional FiexCAN Four modules (32 message buffers each) FlexRay Optional FiexCAN Four modules (32 message buffers each) FlexRay Optional FiexCAN Four modules (32 message buffers each) FlexRay Optional FiexCAN Four modules (32 message buffers each) FlexRay Optional FlexCAN Four modules (32 message buffers each) FlexRay Optional FlexCAN Four modules (system and unxiliary) Three modules, four channels One module Preiodic interrupt timer One module, four channels One module Clock onlitor unit Three modules (tyree chipselects) Three modules (system and auxiliary) Frequency-modulated phase-locked loop Frequency-modulated phase-locke			1 MB		2 MB	
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Cross triggering unit		Analog-to-digital converter	257 pin pkg: 4 x 12-bit (22 external channels), 473 pin pkg: 4 x 12-bit (up to 34 external channels)			
Deserial serial peripheral interface Deserial serial peripheral interface Digital I/Os DRAM controller Enhanced direct memory access Fimer Three modules, 32 channels each eTimer Three modules, six channels each External bus interface Fast ethernet controller Fault collection and control unit FlexCAN FlexPWM FlexRay Deservation FlexRay Deservation Interrupt controller Parallel data interface Parallel data interface Periodic interrupt timer Software watchdog timer System timer module Wakeup unit Clock monitor unit Clock monitor unit Two modules (three chip sel chip selects) Two modules, 32 channels each One module, 16-bit data + address or 32-bit data w address bus muxed One module FlexCAN Four modules (32 message buffers each) Three modules (32 message buffers each) FlexPWM Three modules (32 message buffers each) Three modules (92 message buffers each) Three modules (92 message buffers each) Three modules Pone modules Clock monitor unit Three modules (92 message buffers each) Three modules (92 message buf		CRC unit	Two (three contexts each)			
Deserial serial peripheral interface Chip selects Digital I/Os ≥16		Cross triggering unit		Two modules	odules	
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Enhanced direct memory access eTimer Three modules, six channels each External bus interface Fast ethernet controller Four module Fault collection and control unit FlexCAN Four modules (32 message buffers each) FlexRay Optional FlexRay Optional Interrupt controller Parallel data interface One modules Software watchdog timer Software watchdog timer Wakeup unit Crossbar switch Clock ing Frequency-modulated phase-locked loop IRCOSC -16 MHz Vow-voltage detector (LVD12) Pone modules, ix channels and charter and charter and control unit One modules, six channels and charter and c		Digital I/Os		≥16		
## Part		DRAM controller	No	Yes		
External bus interface Cone module, 16-bit data + address or 32-bit data w address bus muxed		Enhanced direct memory access	Two	Two modules, 32 channels each		
Modules Fast ethernet controller Fault collection and control unit FlexCAN Four modules (32 message buffers each) FlexPWM Three modules (each 4 x 3 channels) FlexRay Optional I*C Two modules Interrupt controller Four modules Interrupt controller Interrupt controller Four modules Parallel data interface One module Periodic interrupt timer One module, four channels Software watchdog timer Yes (SoR) System timer module Yes (SoR) Temperature sensor One module Wakeup unit Crossbar switch Three modules, two are user-configurable Clock monitor unit Three modules Clock output Two modules Frequency-modulated phase-locked loop Two modules (system and auxiliary) IRCOSC—16 MHz XOSC 4 MHz—40 MHz Power management unit Yes 1.2V low-voltage detector (LVD12) One		eTimer	Three modules, six channels each			
Fault collection and control unit FiexCAN FiexPWM FlexRay PiexRay Parallel data interface Periodic interrupt timer Software watchdog timer Wakeup unit Crossbar switch Clocking Foult collection and control unit Flex CAN Four modules (32 message buffers each) Three modules (each 4 x 3 channels) Poptional Piex CAN Three modules Three modules Three modules Four modules Four modules Pone module, four channels Yes (SoR) System timer module Yes (SoR) Temperature sensor One module Clock monitor unit Three modules, two are user-configurable Clock output Two modules Frequency-modulated phase-locked loop Frequency-modulated phase-locked loop IRCOSC – 16 MHz XOSC 4 MHz–40 MHz Power management unit Yes 1.2V low-voltage detector (LVD12) One		External bus interface	One module, 16-bit data + address or 32-bit data with address bus muxed			
FiexCAN FiexPWM FiexRay FiexRay FiexRay Four modules (32 message buffers each) FiexRay FiexRay FiexRay FiexRay FiexRay Fiex modules Four modules Fo		Fast ethernet controller	One module			
FlexCAN Four modules (32 message buffers each) FlexPWM Three modules (each 4 x 3 channels) FlexRay Optional **Percontroller		Fault collection and control unit	One module			
FlexRay P2C Two modules Three modules Interrupt controller Yes (SoR) LINFlex Three modules Four modules Parallel data interface One module Periodic interrupt timer One module, four channels Software watchdog timer Yes (SoR) System timer module Yes (SoR) Temperature sensor One module Wakeup unit Yes Crossbar switch Three modules, two are user-configurable Clock monitor unit Three modules Clock output Two modules Clock output Two modules Frequency-modulated phase-locked loop Two modules (system and auxiliary) IRCOSC - 16 MHz One XOSC 4 MHz-40 MHz One Power management unit Yes 1.2V low-voltage detector (LVD12) One		FlexCAN	Four modules (32 message buffers each)			
P2C		FlexPWM	Three modules (each 4 x 3 channels)			
Interrupt controller		•		Optional		
LINFlex		I ² C	Two modules	l .	odules	
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Periodic interrupt timer			Three modules			
Software watchdog timer Yes (SoR)						
System timer module Yes (SoR)		·				
Temperature sensor		•				
Wakeup unit Yes		•				
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IRCOSC = 16 MHz						
XOSC 4 MHz—40 MHz Power management unit 1.2V low-voltage detector (LVD12) One						
Power management unit Yes 1.2V low-voltage detector (LVD12) One						
1.2V low-voltage detector (LVD12) One						
		<u> </u>				
Supply	Supply		One			
2.7V low-voltage detector (LVD27) Four		0 0 , ,				
	ebug		Class 3+ (for cores and SRAM ports)			
	_		257 pins, 473 pins			
	-		See the TA recommended operating condition in the device data			



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