PM5326 ARROW 2x192
SONET/SDH Transport Framer/Aggregator for OC-48 and OC-192

Released Product Brief

FEATURES

- Dual SONET/SDH framer/aggregator for use in channelized STS-192/STM- 64 and STS-48/STM-16 applications.
- 20 Gbit/s aggregate capacity. Each of the two framers within the device can be independently configured to support:
  - One STS-192/STS-192c/STM-64/STM-64c stream.
  - Four STS-48/STS-48c/STM-16/STM-16c streams.
- Supports two STS-192/STM-64 streams via two standard OIF SFI-4 interfaces (duplex 16-bit 622 MHz LVDS) for direct connection to SERDES and CRU/CSU devices.
- Supports up to eight STS-48/STM-16 via SFI-4 interfaces operating in nibble mode.
- Provides two sets of working, protect, and APS interfaces for connection across system backplanes. Each interface consists of four ESSI (Extended SONET Serial Interface) RASIO 3G links, operating at 2.488 Gbit/s.
- Supports channelized (down to STS-1), concatenated, and arbitrarily concatenated (STS-3cxN) traffic. Changes in traffic configurations are automatically detected.
- Terminates (or monitors) SONET/SDH Section, Line, and Path overhead and provides STS-1 granularity frame alignment and pointer processing.
- Detects and inserts transport and path BIP-8 errors (B1, B2, B3). Detects signal degrade (SD) and signal fail (SF) threshold crossing alarms for B2 and B3.

- Provides overhead passthrough for entire TOH, and re-mapping for B1, B2, M0/M1, and J0 bytes.
- Provides dedicated pins to extract and reinsert the entire transport overhead.
- Provides dedicated pins to extract section and line DCC.
- Supports Automatic Protection Switching:
  - K1/K2 byte filtering and BER monitoring.
  - Direct line card APS connections via system side APS ports.
- Supports centralized control of SONET/SDH processing by providing in-band status messaging (Transport, Path, and Equipment Status) on the ESSI ports.
- Provides independent STS-1 Memory Switching Units (MSU) for combined time-slot interchange (TSI) and muxing functions in transmit and receive directions.
- Provides independent STS-1 Memory Switching Units (MSU) at the DROP APS port for grooming traffic to support line card pairing or local traffic termination.
- Can be configured in line to line mode (SFI-4 to SFI-4) while independently adding/dropping traffic to/from working and protect system interfaces:
  - Supports STS-192/STM-64 or STS-48/STM-16 passthrough, or aggregation of 4xSTS-48/STM-16 via SONET multiplexing or byte interleaving.
- Provides line loopback from the line side receive streams to the transmit streams and supports diagnostic loopback on the system side interface.

Block Diagram
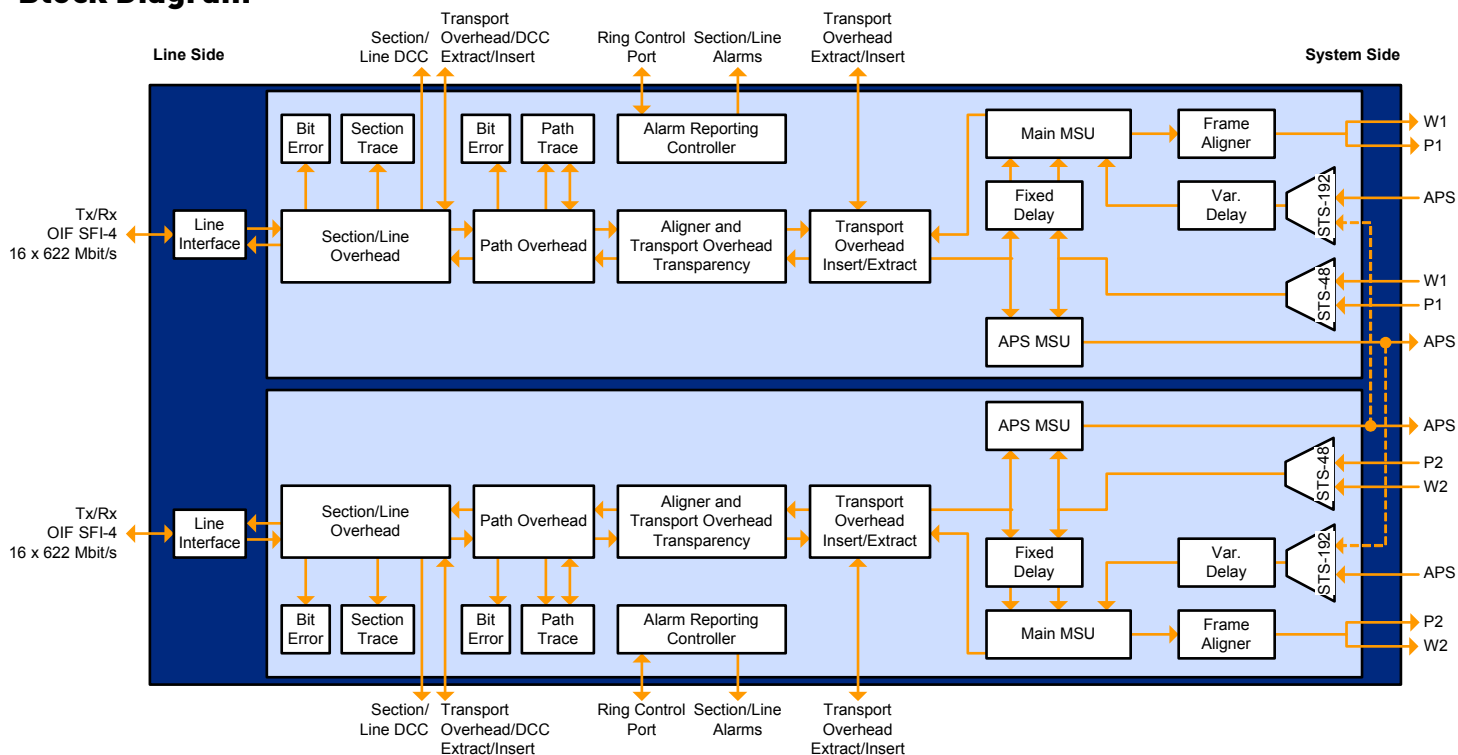
GENERAL

- General purpose 16-bit microprocessor interface for configuration, control, and status monitoring.
- Low power 1.2 V core with 2.5/3.3 V I/O.
- Standard 5-signal IEEE 1149.1 JTAG test port for boundary scan board test purposes.
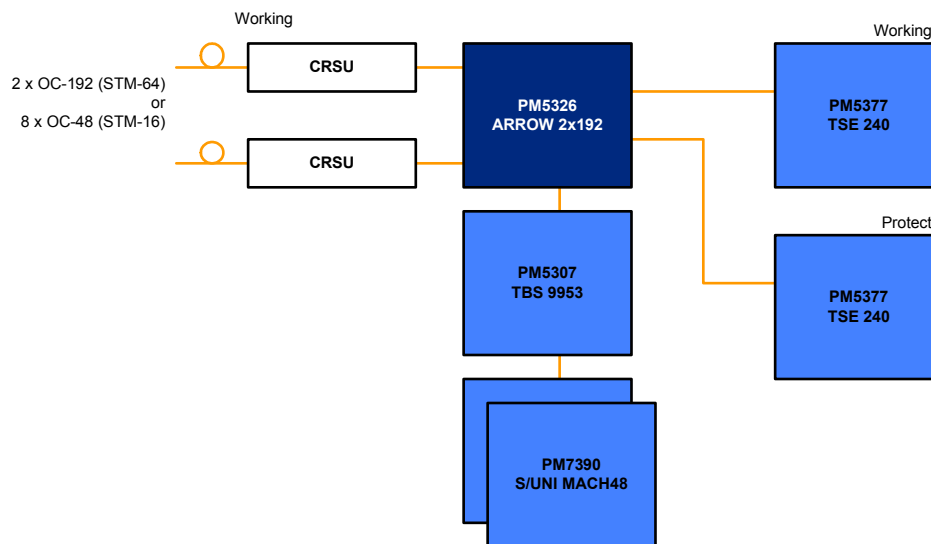- 1292-pin FCBGA package.

APPLICATIONS

- Multi Service Provisioning Platforms (MSPP).
- Sub Wavelength Cross Connects.
- Add/Drop Multiplexers.
- DWDM Platforms.
- Channelized Routers and Multi Service Switches.

Typical Applications

Cross-Connect
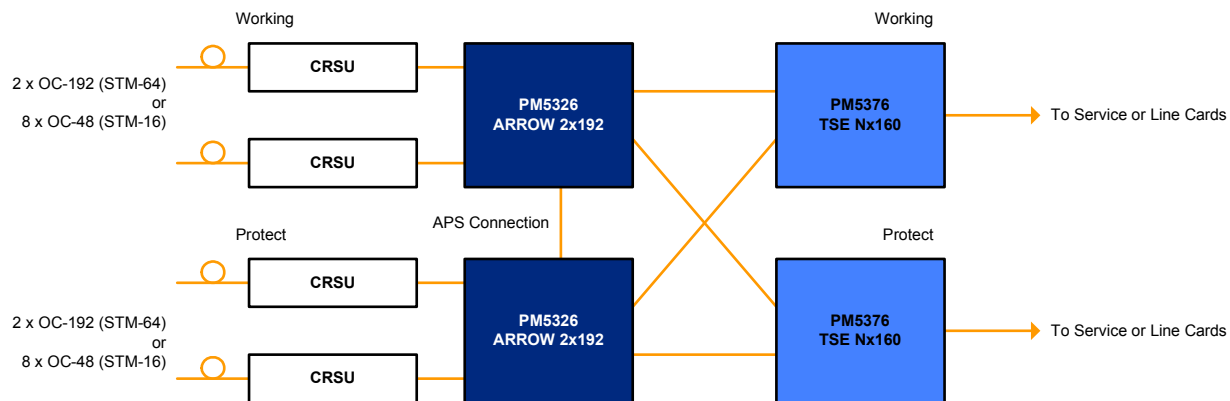
20G Line Card with Local Layer 2 Processing

Further Resources

Technical Documentation

www.pmcs.com/resources/downloads_support.html

About PMC

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