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Team Nexperia

BUK9C07-65BIT

N-channel TrenchPLUS logic level FET

Rev. 03 — 15 July 2010 **Product data sheet**

1. Product profile

1.1 General description

N-channel enhancement mode field-effect power transistor in SOT427. Device is manufactured using NXP High-Performance TrenchPLUS technology, featuring very low on-state resistance, integrated current sensing transistor and over temperature protection diodes.

1.2 Features and benefits

- AEC-Q101 compliant
- Low conduction losses due to low on-state resistance

1.3 Applications

- Lamp switching
- Motor drive systems
- Power distribution
- Solenoid drivers

1.4 Quick reference data

Table 1. Quick reference data

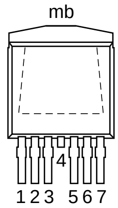
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
R_{DSon}	drain-source on-state resistance	V_{GS} = 5 V; I_D = 25 A; T_j = 25 °C; see Figure 12; see Figure 13	-	6	7	mΩ
I_D/I_{sense}	ratio of drain current to sense current	T_j = 25 °C; V_{GS} = 5 V; see Figure 14	10861	12068	13275	A/A
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C	65	-	-	V

2. Pinning information

Table 2. Pinning information

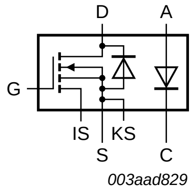
Pin	Symbol	Description
1	G	gate
2	IS	current sense
3	A	anode
4	D	drain
5	K	cathode
6	KS	Kelvin source
7	S	source
mb	D	mb

Simplified outline



SOT427 (D2PAK)

Graphic symbol



3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9C07-65BIT	D2PAK	plastic single-ended surface-mounted package (D2PAK); 7 leads (one lead cropped)	SOT427

4. Limiting values

Table 4. Limiting values

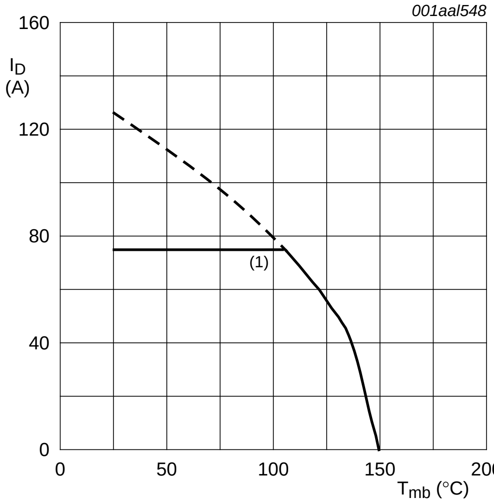
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 150 °C		-	65	V
V_{DGR}	drain-gate voltage	R_{GS} = 20 kΩ; 25 °C ≤ T_j ≤ 150 °C		-	65	V
V_{GS}	gate-source voltage			-15	15	V
I_D	drain current	V_{GS} = 5 V; T_{mb} = 25 °C; see Figure 1	[1]	-	75	A
		V_{GS} = 5 V; T_{mb} = 100 °C; see Figure 1	[1]	-	75	A
I_{DM}	peak drain current	T_{mb} = 25 °C; single pulse; t_p ≤ 10 µs; see Figure 4		-	550	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; see Figure 2		-	245	W
T_{stg}	storage temperature			-55	150	°C
T_j	junction temperature			-55	150	°C
$V_{isol(FET-TSD)}$	FET to temperature sense diode isolation voltage			-	100	V
Source-drain diode						
I_S	source current	T_{mb} = 25 °C	[1]	-	75	A
I_{SM}	peak source current	single pulse; t_p ≤ 10 µs; T_{mb} = 25 °C		-	550	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 75 A; V_{sup} = 65 V; V_{GS} = 5 V; $T_{j(init)}$ = 25 °C; unclamped; see Figure 3	[2][3]	-	0.605	J
Electrostatic discharge						
V_{ESD}	electrostatic discharge voltage	HBM; C = 100 pF; R = 1.5 kΩ; all pins		-	0.15	kV
		HBM; C = 100 pF; R = 1.5 kΩ; pin 4 to pin 7		-	4	kV

[1] Current is limited by package.

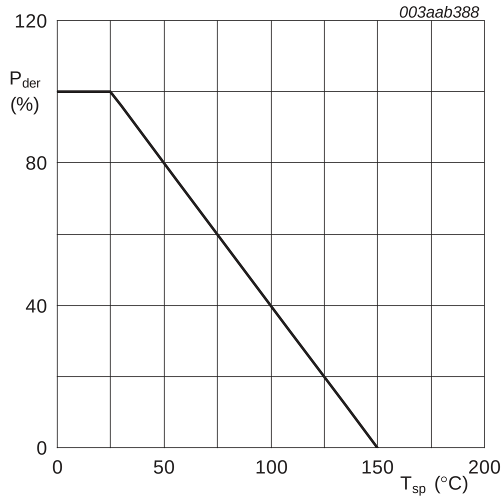
[2] Single-pulse avalanche rating limited by maximum junction temperature of 150 °C.

[3] Refer to application note AN10273 for further information.



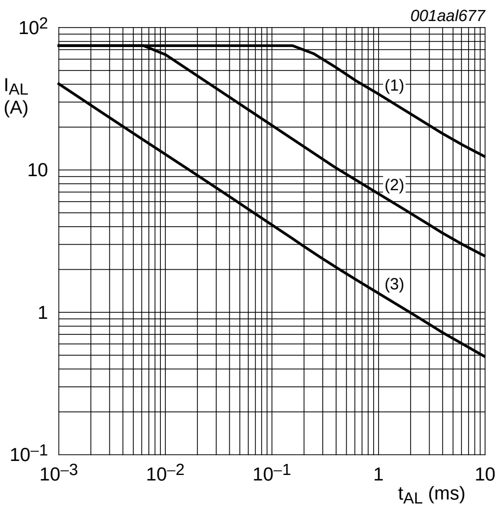
$$V_{GS} \geq 5V$$

Fig 1. Continuous drain current as a function of solder point temperature.



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig 2. Normalized total power dissipation as a function of solder point temperature

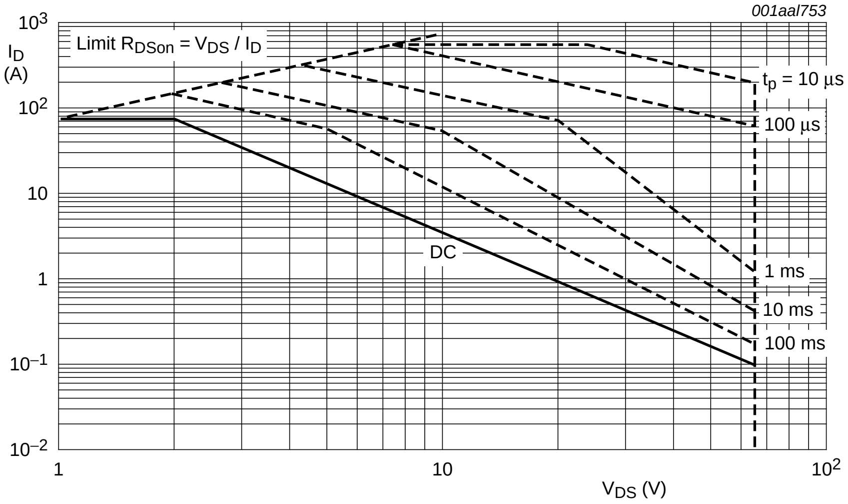


(1) Single-pulse; $T_j = 25\,°C$.

(2) Single-pulse; $T_j = 150\,°C$.

(3) Repetitive.

Fig 3. Single-Pulse and repetitive avalanche rating; avalanche current as a function of avalanche time.



$T_{mb} = 25\,°C; I_{DM}$ is single pulse

Fig 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 5	-	-	0.51	K/W

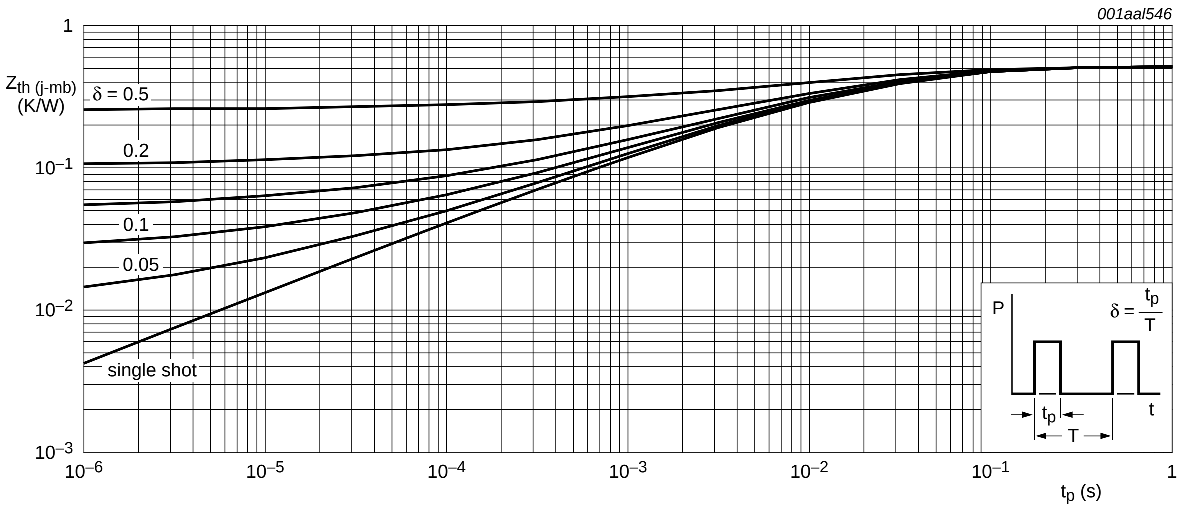


Fig 5. Transient thermal impedance from junction to mounting base as a function of pulse duration.

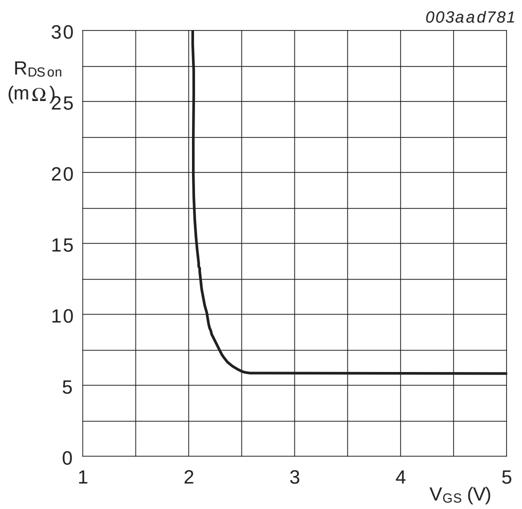
6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C	65	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C	59	-	-	V
V_{GSth}	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C; see Figure 10; see Figure 11	1	1.5	2	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 150 °C; see Figure 10; see Figure 11	0.5	-	-	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55 °C; see Figure 10; see Figure 11	-	-	2.3	V
I_{DSS}	drain leakage current	V_{DS} = 52 V; V_{GS} = 0 V; T_j = 25 °C	-	0.02	3	µA
		V_{DS} = 52 V; V_{GS} = 0 V; T_j = 150 °C	-	-	125	µA
I_{GSS}	gate leakage current	V_{DS} = 0 V; V_{GS} = 15 V; T_j = 25 °C	-	2	300	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 25 A; T_j = 25 °C; see Figure 12; see Figure 13	-	-	7.6	mΩ
		V_{GS} = 5 V; I_D = 25 A; T_j = 25 °C; see Figure 12; see Figure 13	-	6	7	mΩ
		V_{GS} = 5 V; I_D = 25 A; T_j = 150 °C; see Figure 12; see Figure 13	-	-	13.5	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; see Figure 12; see Figure 13	-	-	6.5	mΩ
I_D/I_{sense}	ratio of drain current to sense current	V_{GS} = 5 V; T_j = 25 °C; see Figure 14	10861	12068	13275	A/A
$S_{F(TSD)}$	temperature sense diode temperature coefficient	I_F = 250 µA; 25 °C ≤ T_j ≤ 150 °C; see Figure 15	-5.4	-5.7	-6	mV/K
$V_{F(TSD)}$	temperature sense diode forward voltage	I_F = 250 µA; T_j = 25 °C; see Figure 15	2.855	2.9	2.945	V
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 52 V; V_{GS} = 5 V; see Figure 16	-	102.8	-	nC
Q_{GS}	gate-source charge		-	16.4	-	nC
Q_{GD}	gate-drain charge		-	36.4	-	nC
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz; T_j = 25 °C; see Figure 17	-	7127	-	pF
C_{oss}	output capacitance		-	900	-	pF
C_{rss}	reverse transfer capacitance		-	354	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 30 V; R_L = 1.2 Ω; V_{GS} = 5 V; $R_{G(ext)}$ = 10 Ω	-	59	-	ns
t_r	rise time		-	180	-	ns
$t_{d(off)}$	turn-off delay time		-	328	-	ns
t_f	fall time		-	173	-	ns
L_D	internal drain inductance	from pin to center of die	-	0.9	-	nH
L_S	internal source inductance	from source lead to source bonding pad	-	2	-	nH

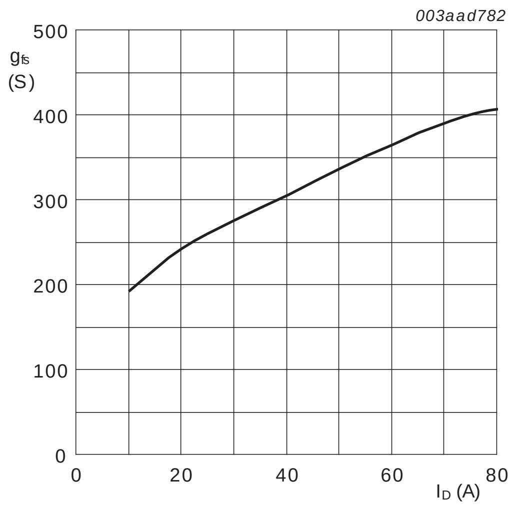
Table 6. Characteristics *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C; see Figure 18	-	0.85	1.2	V
t_{rr}	reverse recovery time	I_S = 10 A; dI_S/dt = -100 A/µs; V_{GS} = -10 V; V_{DS} = 30 V	-	60.1	-	ns
Q_r	recovered charge		-	0.161	-	nC



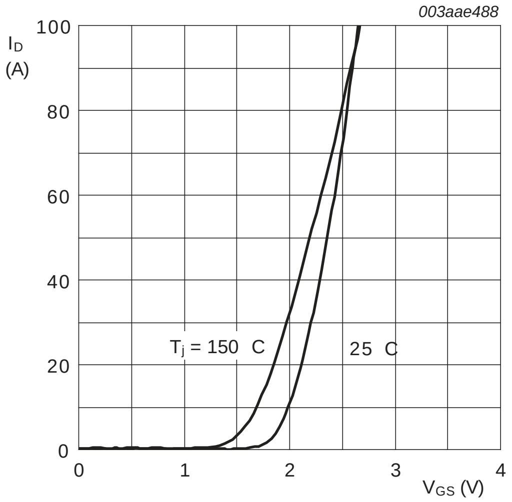
$T_j = 25°C; I_D = 25A$

Fig 6. Drain-source on-state resistance as a function of gate-source voltage



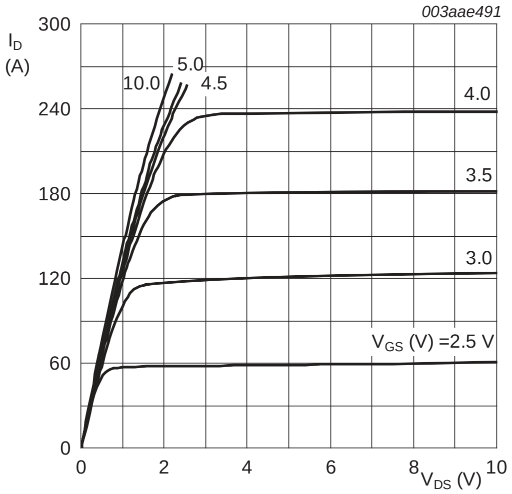
$T_j = 25°C; V_{DS} = 25V$

Fig 7. Forward transconductance as a function of drain current; typical values



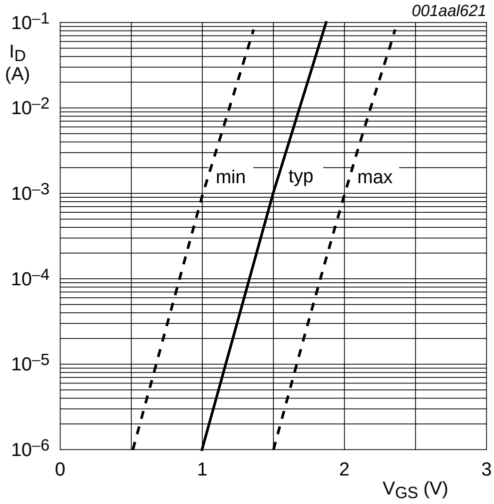
$V_{DS} = 25V$

Fig 8. Transfer characteristics; drain current as a function of gate-source voltage



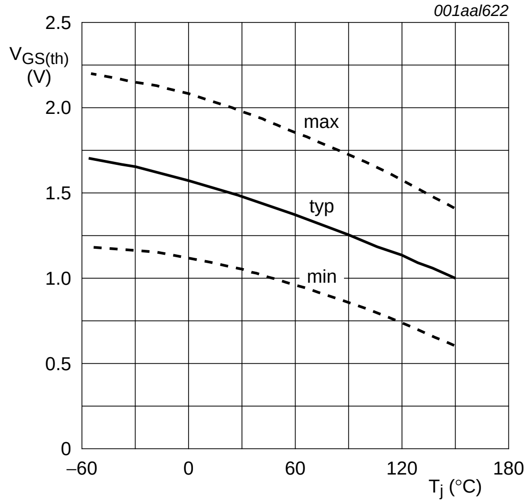
$T_j = 25°C; t_p = 300µs$

Fig 9. Output characteristics: drain current as a function of drain-source voltage; typical values.



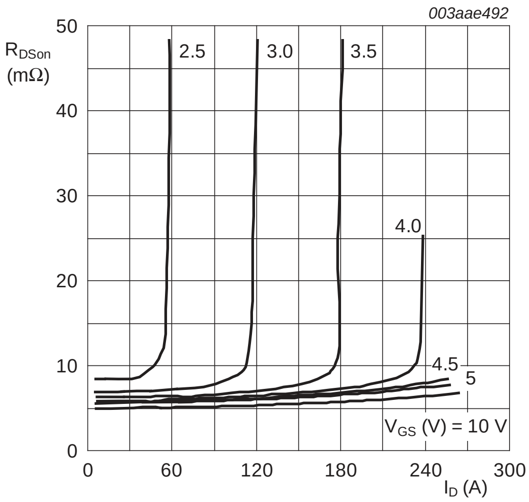
$T_j = 25\,°C; V_{DS} = V_{GS}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



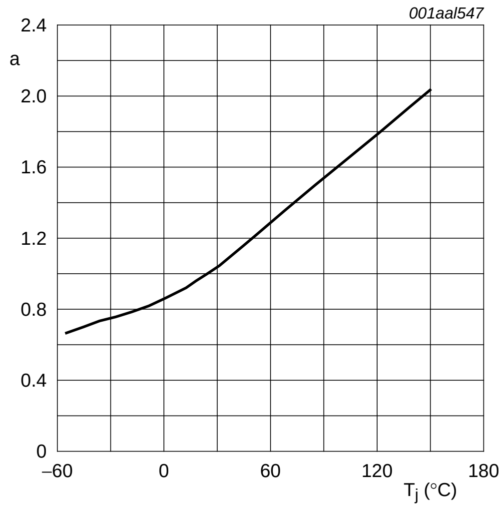
$I_D = 1mA; V_{DS} = V_{GS}$

Fig 11. Gate-source threshold voltage as a function of junction temperature.



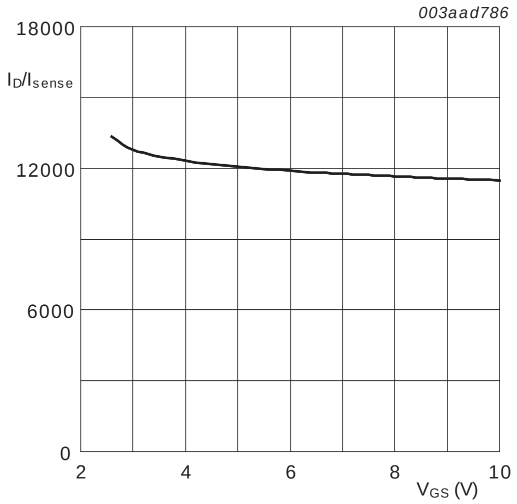
$T_j = 25\,°C; t_p = 300\mu s$

Fig 12. Drain-source on-state resistance as a function of drain current



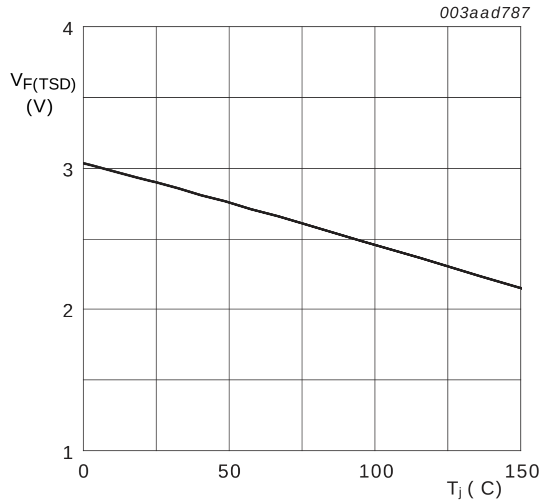
$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig 13. Normalized Drain-Source on-state resistance factor as a function of junction temperature.



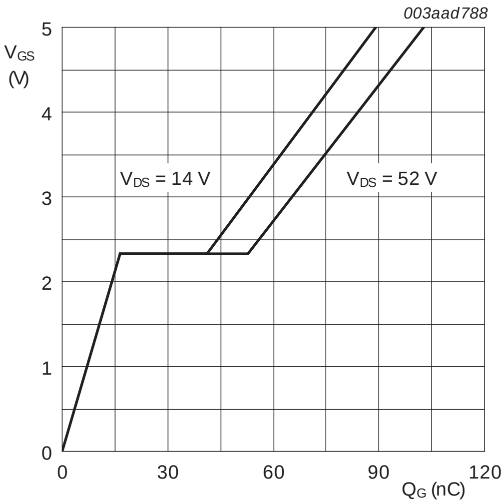
$T_j = 25\,°C; I_D = 5A$

Fig 14. Ratio of drain current to sense current as a function of gate-source voltage



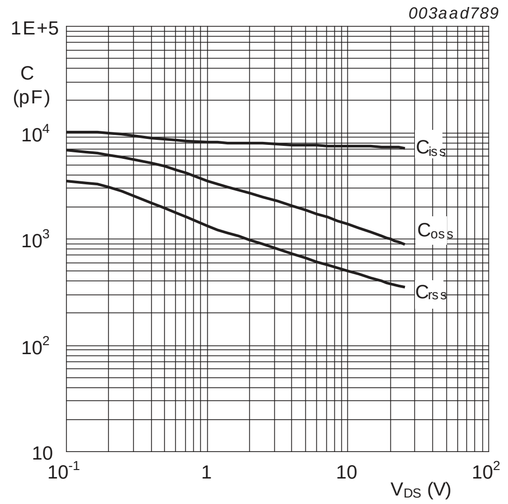
$I_F = 250\mu A$

Fig 15. Temperature sense diode forward voltage as a function of junction temperature



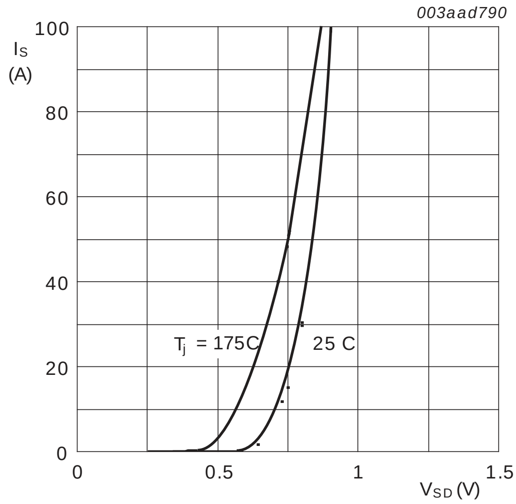
$T_j = 25\,°C; I_D = 25A$

Fig 16. Gate-source voltage as a function of turn-on gate charge



$V_{GS} = 0V; f = 1MHz$

Fig 17. Input, output and reverse transfer capacitances as a function of drain-source voltage

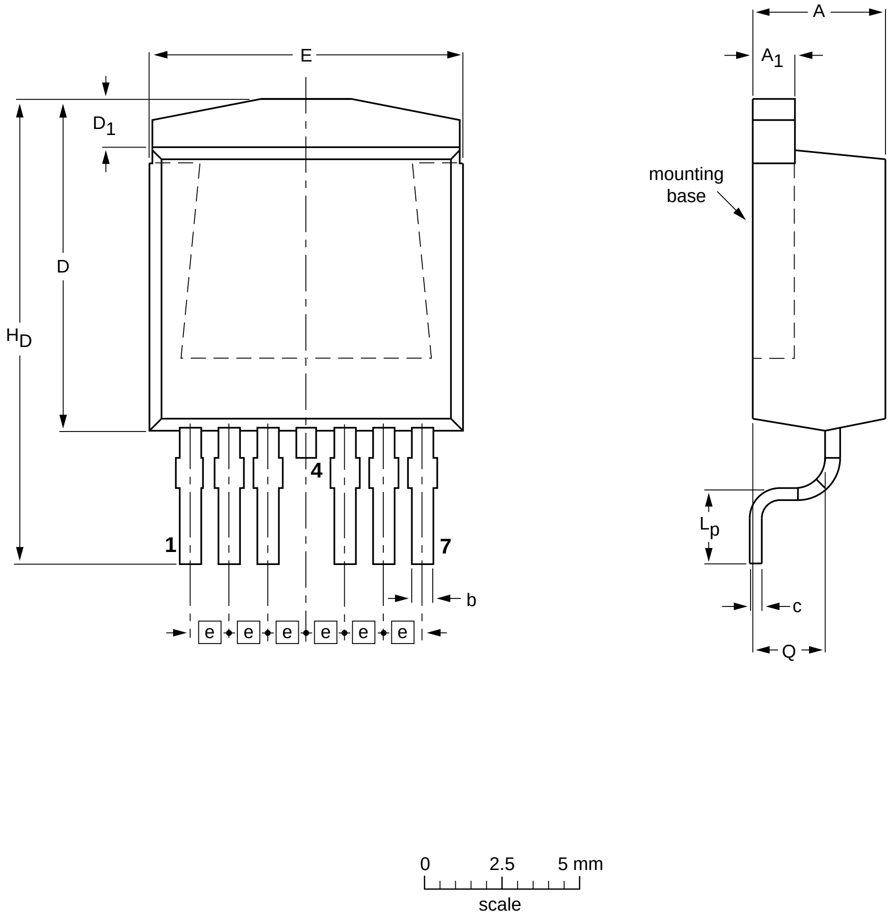


$V_{GS} = 0\,V$

Fig 18. Source (diode forward) current as a function of source-drain (diode forward) voltage

7. Package outline

Plastic single-ended surface-mounted package (D2PAK); 7 leads (one lead cropped) **SOT427**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	c	D max.	D_1	E	e	L_p	H_D	Q
mm	4.50 4.10	1.40 1.27	0.85 0.60	0.64 0.46	11	1.60 1.20	10.30 9.70	1.27	2.90 2.10	15.80 14.80	2.60 2.20

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT427						~~05-03-09~~ 06-03-16

Fig 19. Package outline SOT427 (D2PAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK9C07-65BIT v.3	20100715	Product data sheet	-	BUK9C07-65BIT v.2
Modifications:	• Various changes to content.			
BUK9C07-65BIT v.2	20100617	Product data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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11. Contents

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Date of release: 15 July 2010
Document identifier: BUK9C07-65BIT