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November 2014

FAN54020
USB-Compliant 1.5 A Single-Cell Li-Ion Switching Charger with DBP and OTG Boost

Features

- Fully Integrated, High-Efficiency Charger for Single-Cell Li-Ion and Li-Polymer Battery Packs
- Faster Charging / Less Dissipation than Linear Charger
- Charge Voltage Accuracy:
  - ±0.5% at 25°C
  - ±1% from -30°C to 125°C
- ±10% Charge Current Regulation Accuracy
- 28 V Absolute Maximum Input Voltage
- 1.5 A Maximum Charge Current
- Support for Dead Battery Provision (DBP) of USB Battery Charging Specification 1.2
- Programmable through I^2C Interface with Fast Mode (400 kHz) Compatibility
  - Input Current
  - Fast-Charge / Termination Current
  - Charger (Float) Voltage
- Safety Timer with Reset Control
- Dynamic Input Voltage Control Automatically Reduces Charging Current with Weak Input Sources
- Low Reverse Leakage Prevents Battery Drain to V_{BUS}
- Small Footprint 1µH External Inductor
- 3.3 V Regulated Output from V_{BUS} for Auxiliary Circuits
- 5 V, 500 mA Boost Mode for USB OTG for 3.0 to 4.5 V Battery Input
- Attachment Detect Protocol (ADP) Support per On-The-Go and Embedded Host Supplement to the USB Rev. 2.0 Specification

Applications

- Cell Phones, Smart Phones
- Tablet, Portable Media Players
- Gaming Device, Digital Cameras

Description

The FAN54020 combines a highly integrated switch-mode charger, to minimize single-cell Li-Ion charging time from a USB power source, and a boost regulator to power a USB peripheral from the battery.

The charging parameters and operating modes are programmable through an I2C interface. The charger and boost regulator switch at 3 MHz and utilize the same external components to minimize size.

The FAN54020 supports battery charging in three modes: pre-charge, constant current fast charger, and constant voltage float charge.

To ensure USB compliance and minimize charging time, the input current limit can be changed via I2C by the host processor. Charge termination is determined by a programmable minimum current level. A safety timer with reset control provides a safety back-up for the I2C host. Charge status is reported to the host using the I2C port.

The FAN54020 automatically restarts the charge cycle when the battery falls below an internal threshold. Charge current is reduced when die temperature reaches a programmable level, preventing damage.

The FAN54020 can operate as a boost regulator on command from the system. The boost regulator includes a soft-start that limits inrush current from the battery.

The FAN54020 includes Dead Battery Provision (DBP) from the BC1.2 specification, including a 30 minute timer.

The FAN54020 is available in a 25-bump, 0.4 mm pitch, Wafer-Level Chip-Scale Package (WLCSP).

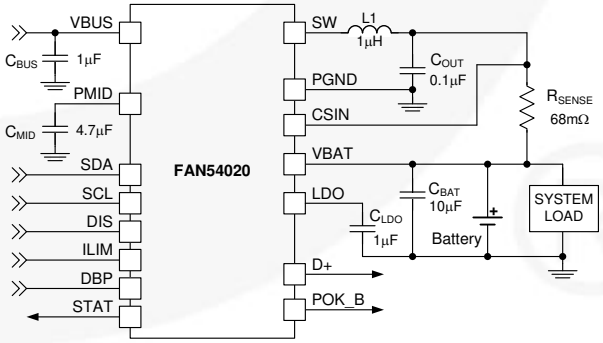

Figure 1. Typical Application

Ordering Information

Part Number	PN R0[4:3]	Temperature Range	Package	Packing Method
FAN54020UCX	01	-40 to 85°C	25-Bump, Wafer-Level Chip-Scale (WLCSP), 0.4 mm Pitch	Tape and Reel

Block Diagram

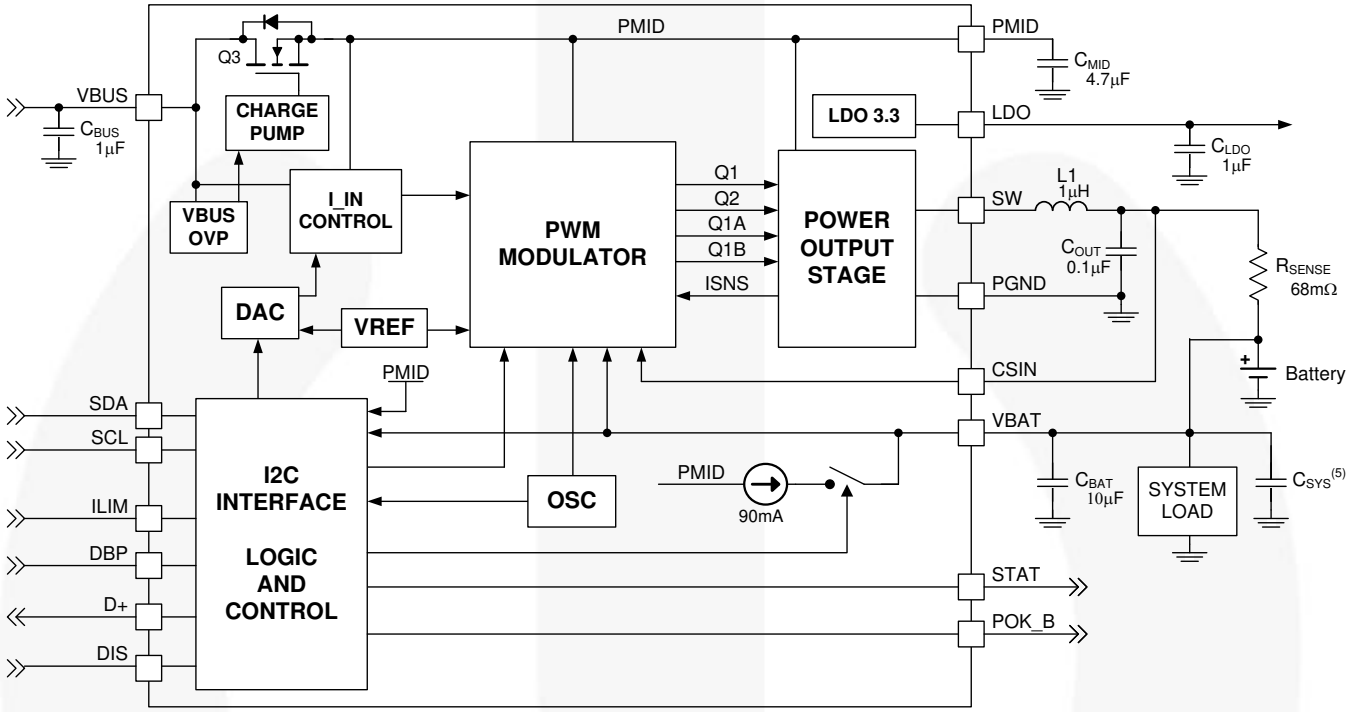

Figure 2. IC and System Block Diagram

Table 1. Recommended External Components

Component	Description	Vendor	Parameter	Min.	Typ.(1)	Unit
L1	Charge Currents to 1 A: 1 µH, 30%, 1.3 A, 2016	Murata: LQM2MPN1R0NG0L	L	0.5	1.0	µH
			DCR		85	mΩ
	Charge Currents above 1 A: 1 µH, 20%, 1.6 A, 2520	Murata: LQM2HPN1R0MG0	L	0.5	1.0	µH
			DCR		55	mΩ
C_{BUS}	1.0 µF, 10%, 16 V, X5R, 0603	Murata GRM188R61E105K TDK:C1608X5R1E105K	C	0.5	1.0	µF
C_{BAT}	10 µF, 20%, 6.3 V, X5R, 0603	Murata: GRM188R60J106M TDK: C1608X5R0J106M	C	3.7	10.0	µF
C_{MID}	4.7 µF, 10%, 10 V, X5R, 0603	Murata: GRM188R61A475K TDK: C1608X5R1A475K	C	2.0	4.7	µF
C_{LDO}	1.0 µF, 10%, 6.3 V, X5R, 0402	Murata GRM155R60J105M	C	0.35	1.00	µF
C_{OUT}	0.1 µF, 10%, 6.3 V, X5R, 0201	Murata GRM033R60J104K	C	0.07	0.10	µF
R_{SENSE}	68 mΩ, 1%, 0603, $I_{CHG} \leq$ 900 mA		R		68	mΩ

Note:
1. Does not reflect effects of bias, tolerance, and temperature.

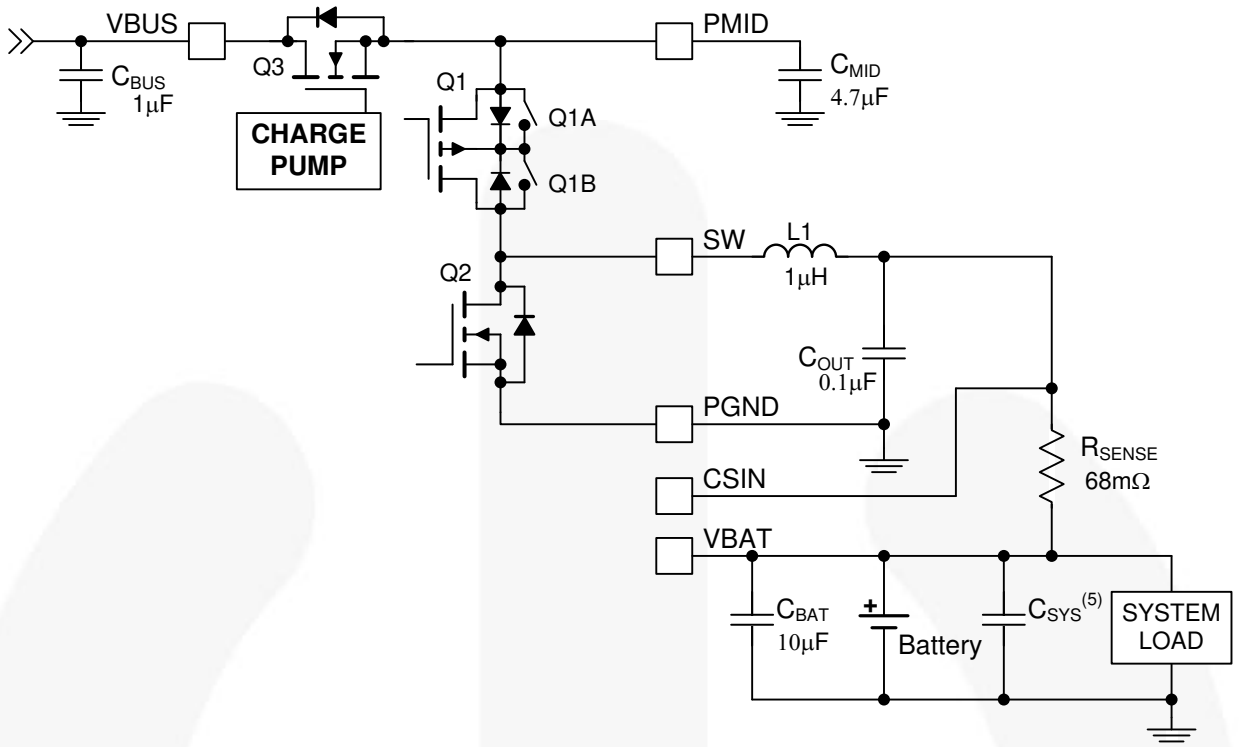

Figure 3. Power Output Stage

Pin Configuration

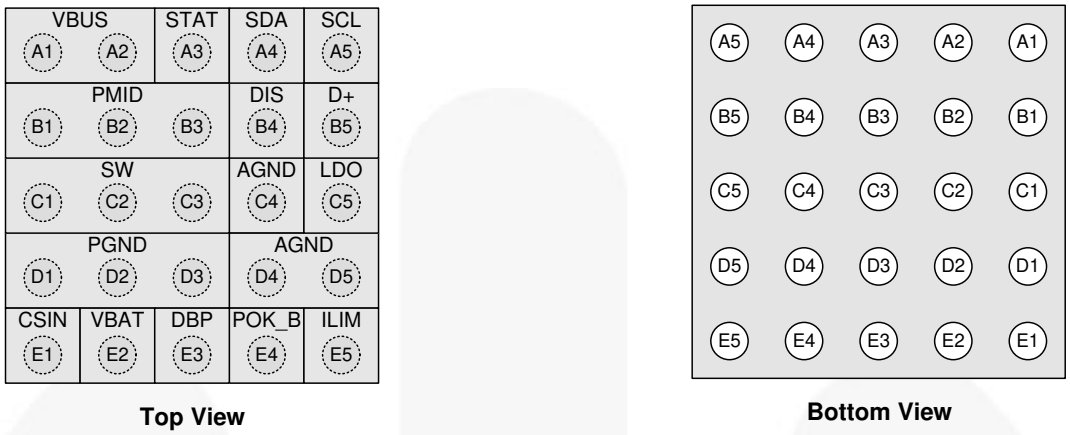

Figure 4. WLCSP-25 Pin Assignments

Pin Definitions

Pin #	Name	Description
A1, A2	VBUS	Charger Input Voltage. Bypass with a 1 μF capacitor to PGND.
A3	STAT	Status/Interrupt. Open-drain output indicating charge status. The IC pulls this pin LOW when charge is in process. It is high impedance when charging is done or the charger is disabled. It is also used as a system interrupt. 128 μs pulse, then high impedance indicates to the system that a fault has occurred.
A4	SDA	I^2C Interface Serial Data.
A5	SCL	I^2C Interface Serial Clock.
B1-B3	PMID	Power Input Voltage. Power input to the charger regulator, bypass point for the input current sense, and high-voltage input switch. Bypass with a minimum of 4.7 μF, 6.3 V capacitor to PGND.
B4	DIS	Disable. When pulled HIGH, the charger is disabled. Internal pull-down resistor.
B5	D+	Connect to the USB connector D+ pin. Charger IC sources 0.6 V on this pin whenever the IC is charging and the DBP pin is LOW. In all other conditions, the pin is tri-stated.
C1-C3	SW	Switching Node. Connect to the output inductor.
C4, D4, D5	AGND	Analog Ground. All analog signals are referenced to this pin. This pin can be tied to PGND under the IC.
C5	LDO	3.3 V LDO. 3.3 V regulator output.
D1-D3	PGND	Power Ground. Power return for gate drive and power transistors.
E1	CSIN	Current-Sense Input. Connect to the sense resistor in series with the battery. The IC uses this node to sense current into the battery. Bypass this pin with a 0.1 μF capacitor to PGND.
E2	VBAT	Battery Voltage. Connect to the positive (+) terminal of the battery pack. Bypass with a 10 μF capacitor to PGND if the battery is separated from other system bypass capacitance by long traces.
E3	DBP	Dead Battery Provision Disable. Pull HIGH to disable charger D+ output. Internal pull–down resistor.
E4	POK_B	V_{BUS} Power OK Monitor. Open-drain output that is internally pulled LOW when VBUS is greater than the V_{BUS} validation threshold and lower than V_{BUS} OVP. It is high impedance when outside this range.
E5	ILIM	Input Current Limit. This pin sets the input current limit for t_{30MIN} charging. Internal pull-down resistor.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{BUS}	VBUS Voltage		-2[2]	28	V
V_I	PMID, SW Voltage		-0.3	6.5	V
V_O	Voltage on Other Pins		-0.3	[3]	V
$\frac{dV_{BUS}}{dt}$	Maximum V_{BUS} Slope above 5.5 V when Boost or Charger are Active			4	V/µs
ESD	Electrostatic Discharge Protection Level	Human Body Model per JESD22-A114 (All Pins)	1500		V
		Charged Device Model per JESD22-C101 (All Pins)	500		
		IEC 61000-4-2 System (VBUS and D+ Pin)	8000		
T_J	Junction Temperature		-40	+150	°C
T_{STG}	Storage Temperature		-65	+150	°C
T_L	Lead Soldering Temperature, 10 Seconds			+260	°C

Notes:

2. 5 s maximum pulse, non-repetitive, for V_{BUS} slew rates faster than -5 V/ms, resulting in -0.7 V>V_{BUS}>-2.0 V, applies only for an open battery condition.
3. Lesser of 6.5 V or V_{BAT} + 0.3 V.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter		Min.	Max.	Unit
V_{BUS}	Supply Voltage		[4]	7.5	V
$V_{BAT(MAX)}$	Maximum Battery Voltage when Boost enabled			4.5	V
$-\frac{dV_{BUS}}{dt}$	Negative V_{BUS} Slew Rate during VBUS Short Circuit, $C_{MID} \leq 4.7\ \mu F$	$T_A \leq 60°C$		4	V/µs
		$T_A \geq 60°C$		2	
T_A	Ambient Temperature		-30	+85	°C
T_J	Junction Temperature (*see Thermal Regulation Loop section*)		-30	+120	°C

Note:

4. Greater of V_{BAT} or 4 V.

Thermal Properties

Junction-to-ambient thermal resistance is a function of application and board layout. This data is measured with four-layer 2s2p boards in accordance to JEDEC standard JESD51. Special attention must be paid not to exceed junction temperature $T_{J(max)}$ at a given ambient temperature T_A. *For measured data, see Table 3.*

Symbol	Parameter	Typical	Unit
θ_{JA}	Junction-to-Ambient Thermal Resistance	60	°C/W
θ_{JB}	Junction-to-PCB Thermal Resistance	20	°C/W

Electrical Specifications

Unless otherwise specified: circuit of Figure 2, recommended operating temperature range for T_J and T_A, V_{BUS} = 5.0 V, DIS = 0, (Charger Mode operation); SCL, SDA = 0 or 1.8 V; typical values are for T_J = 25°C.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
Power Supplies							
$V_{IN(MIN)1}$	V_{BUS} Input Voltage Rising	To Initiate and Pass V_{BUS} Validation		4.30	4.40	4.50	V
$V_{IN(MIN)2}$	Minimum V_{BUS}	While Charging		3.60	3.70	3.80	V
V_{BUS_REF}	V_{BUS} Reg. Loop Threshold	V_{BUS_REF} = 01 (Reg2 [3:2])		4.22	4.32	4.42	V
		Other V_{BUS_REF} Codes (Reg2 [3:2])		-3		+3	%
t_{VBUS_VALID}	V_{BUS} Validation Time				32		ms
I_{VBUS}	V_{BUS} Current	$V_{BUS} > V_{BUS\_REF}$, PWM Switching			22		mA
		$V_{BUS} > V_{BUS\_REF}$; $V_{BAT} > V_{OREG}$ I_{BUS} Setting = 100 mA			2.0		
		0°C < T_J < 85°C, HZ_MODE = 1, I_{REG} = 0 A			188	250	µA
I_{BAT}	Battery Discharge Current in Sleep Mode	0°C < T_J < 85°C, V_{BAT} = 4.2 V, V_{BUS}=Open, SDA = SCL = DIS = ILIM = DBP = 0 V, STAT = POK_B = Float			1.7	5.0	µA
I_{BUSLKG}	V_{BAT} to V_{BUS} Leakage Current	0°C < T_J < 85°C, V_{BAT}=4.2 V, V_{BUS}=0 V, SDA = SCL = DIS = ILIM = DBP = 0 V, STAT = POK_B = Float			0.01	1.00	µA
Charger Voltage Regulation							
V_{OREG}	Charge Voltage Range			3.38		4.44	V
	Charge Voltage Accuracy	V_{OREG} = 4.2 V, I_{BUSLIM}=No Limit	T_J = 25°C	-0.5		+0.5	%
			Temp. Range	-1.0		+1.0	
		3.38 V < V_{OREG} < 4.44 V	T_J = 25°C	-1.0		+1.0	
			Temp. Range	-1.5		+1.5	
	VBAT Overshoot[6]	*See Figure 5*			10	15	mV
Fast Charging Current Regulation							
I_{OCHRG}	Output Charge Current Range	$V_{BAT} < V_{OREG}$, R_{SENSE} = 68 mΩ		350		1500	mA
	Charge Current Accuracy	Measured as V Across R_{SENSE} [$V_{CSIN} - V_{BAT}$]	$I_{OCHARGE}$ Setting > 500 mA_{MAX}	-10	-5	0	%
			$I_{OCHARGE}$ Setting ≤ 500 mA_{MAX}	-15	-7	0	

V_{BAT} Overshoot Test

In Figure 5, $I_{OCHARGE}$ = 1.5 A (1100), V_{OREG} = 4.2 V. I_{LOAD} t_R = t_F = 1 µs. Charge current prior to load transient = $\frac{20mV}{200m\Omega} = 100mA$. Overshoot is measured as the peak voltage above V_{BAT} level prior to the load transient application.

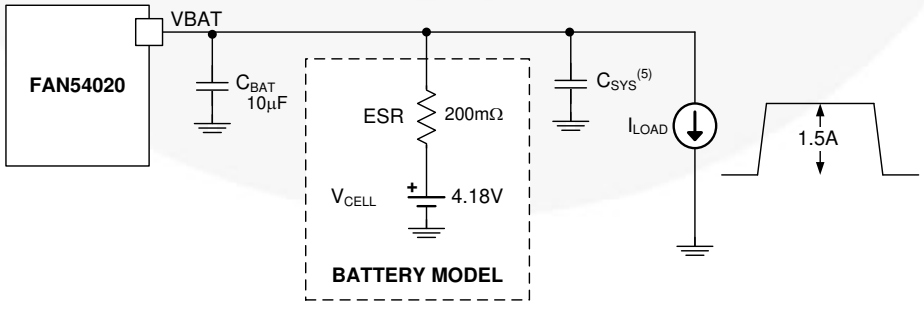

Figure 5. V_{BAT} Overshoot Test Conditions

Electrical Specifications

Unless otherwise specified: circuit of Figure 2, recommended operating temperature range for T_J and T_A, V_{BUS} = 5.0 V, DIS = 0, (Charger Mode operation); SCL, SDA = 0 or 1.8 V; typical values are for T_J = 25°C.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Charge Termination Detection						
$I_{(TERM)}$	Termination Current Range	$V_{BAT} > V_{OREG} – V_{RCH}$, $V_{BUS} > V_{BUS\_REF}$ R_{SENSE}=68 mΩ	50		425	mA
	Termination Current Accuracy	[$V_{CSIN} – V_{BAT}$] from 3 mV to 10.2 mV	-25		+25	%
		[$V_{CSIN} – V_{BAT}$] from 10.2 mV to 20.4 mV	-10		+10	
		[$V_{CSIN} – V_{BAT}$] > 20.4 mV	-5		+5	
	Termination Current Deglitch Time	2 mV Overdrive		32		ms
Input Current Limit						
I_{BUSLIM}	Input Current Limit Threshold Includes I_{LDO}	I_{BUS} Set to 100 mA	87	93	100	mA
		I_{BUS} Set to 500 mA	450	475	500	
Logic Levels: DIS, SDA, SCL, ILIM, DBP						
V_{IH}	High-Level Input Voltage		1.05			V
V_{IL}	Low-Level Input Voltage				0.4	V
I_{IN}	Input Bias Current	Input Tied to GND or VBUS		0.01	1.00	μA
R_{PD}	ILIM, DBP, DIS Pull-Down Resistance		0.65	1.00	1.40	MΩ
3.3 V Linear Regulator						
V_{LDO}	3.3 V Regulator Output	I_{LDO} from 0 to 40 mA	3.20	3.30	3.47	V
I_{LDO_IN}	LDO Quiescent Current	V_{BAT} = 3.6 V		125		μA
$V_{LDO\_IN(MIN)}$	LDO Drop-Out Voltage	I_{LDO} = 40 mA, V_{BUS} = 0 V, $V_{LDO\_IN} = V_{BAT}$		270	330	mV
$t_{3.3}$	Regulator Startup Time	$V_{BUS}>V_{IN(MIN)1}$, DBP=0 or LDO_OFF (Reg2[4]) =1		4.5	5.0	ms
Battery Recharge Threshold						
V_{RCH}	Recharge Threshold[6]	Below V_{OREG}		120		mV
	Deglitch Time	V_{BAT} Falling below V_{RCH} Threshold		132		ms
D+ Output						
V_{DBP_SRC}	Voltage on D+	DBP = 0, I_{LOAD} on D+ from 0 to 250 μA	0.51	0.64	0.69	V
I_{DBP_OFF}	Leakage Current	DBP = 1, V_{D+} from 0 to 5 V	-1		+1	μA
STAT and POK_B Output						
$V_{STAT(OL)}$	STAT and POK_B Output Low	I_{STAT} = 10 mA			0.4	V
$I_{STAT(OH)}$	STAT and POK_B High Leakage Current	V_{STAT} = 5 V			1	μA
Power Switches *(see Figure 3)*						
$R_{DS(ON)}$	Q3 On Resistance (VBUS to PMID)	$I_{IN(LIMIT)}$ > 500 mA		160	220	mΩ
	Q1 On Resistance (PMID to SW)			110	160	
	Q2 On Resistance (SW to GND)			110	170	

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Electrical Specifications (Continued)

Unless otherwise specified: circuit of Figure 2, recommended operating temperature range for T_J and T_A, V_{BUS} = 5.0 V, DIS = 0, (Charger Mode operation); SCL, SDA = 0 or 1.8 V; typical values are for T_J = 25°C.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Charger PWM Modulator						
f_{SW}	Oscillator Frequency		2.7	3.0	3.3	MHz
D_{MAX}	Maximum Duty Cycle				100	%
D_{MIN}	Minimum Duty Cycle			0		%
I_{SYNC}	Synchronous to Non-Synchronous Current Cut-Off Threshold	Low-Side MOSFET (Q2) Cycle-by-Cycle Current Limit		180		mA
VBUS Load Resistance						
R_{VBUS}	VBUS to PGND Resistance	Normal Operation		1500		Ω
		During V_{BUS} Validation		100		
Protection and Timers						
$VBUS_{OVP}$	V_{BUS} OVP Accuracy	V_{BUS} Rising	-5		+5	%
	Hysteresis	V_{BUS} Falling		140		mV
V_{SHORT}	Battery Short-Circuit Threshold	V_{BAT} Rising	2.15	2.24	2.36	V
	Hysteresis	V_{BAT} Falling		160		mV
$V_{IBUS(DIS)}$	V_{BUS} Voltage above which the I_{BUS} Limit is Disabled	V_{BUS} Rising	5.80	6.00	6.25	V
		V_{BUS} Falling	5.50	5.75		
I_{SHORT}	Linear Charging Current	$V_{BAT} < V_{SHORT}$	80	90	100	mA
$I_{LIMPK(CHG)}$	Q1 Cycle-by-Cycle I_{PEAK} Limit	Charge or PTM Mode	3.3	3.8		A
$T_{SHUTDWN}$	Thermal Shutdown Threshold(6)	T_J Rising		145		°C
	Re-Enable Threshold(6)	T_J Falling		T_{CF}		°C
T_{CF}	Thermal Regulation Accuracy(6)	Relative to T_{CF} Setting	-10		+10	°C
t_{32S}	32-Second Timer	Charger Enabled, Boost Disabled	20.5	24.3	28.0	s
		Charger Disabled, Boost Enabled	17.0	24.3	31.6	s
t_{30MIN}	30-Minute Timer		30	38	45	Min
t_{osc}	Internal Oscillator Tolerance	Charge or ADP Probe	-10		10	%
		Boost and ADP_Detect Modes	-30		30	
Production Test Mode						
$I_{BAT(PTM)}$	Production Test Output Current(6)	20% Duty with Max. Period 10 ms, V_{BUS} = 5.5 V, $V_{OREG} \leq$ 4.2 V	2.3			A
ADP Circuit *(see Figure 49)*						
I_{SRC}	ADP Probe Source Current	$V_{BUS} \geq V_{700}$	1.20	1.40	1.60	mA
I_{SINK}	ADP Probe Sink Current	$V_{BUS} \geq V_{100}$, ADP_SNS = 0	1.15	1.55	1.95	mA
V_{100}	Lower ADP Comparator Threshold	ADP_SNS = 0	75	100	125	mV
V_{700}	700 mV ADP Threshold		650	700	750	mV
dV_{ADP}	$V_{700} – V_{100}$		570	600	630	mV
V_{SENSE}	ADP Sense Threshold, ADP_SNS = 1	V_{BUS} Rising	390	450	510	mV
		V_{BUS} Falling	230	290	350	
		Hysteresis	100	150		
$I_{REFRESH}$	Battery Current during Refresh			60		μA
$t_{REFRESH}$	RDVBUS Set to STAT Pulse				1	ms

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Electrical Specifications (Continued)

Unless otherwise specified: circuit of Figure 2, recommended operating temperature range for T_J and T_A, V_{BUS} = 5.0 V, DIS = 0, (Charger Mode operation); SCL, SDA = 0 or 1.8 V; typical values are for T_J = 25°C.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Boost Mode Operation						
V_{BOOST}	Boost Output Voltage at VBUS	2.5 V < V_{BAT} < 4.5 V, I_{LOAD} from 0 to 200 mA	4.80	5.07	5.17	V
		3.0 V < V_{BAT} < 4.5 V, I_{LOAD} from 0 to 500 mA	4.77	5.07	5.17	
$I_{BAT(BOOST)}$	Boost Mode Quiescent Current	PFM Mode, V_{BAT}=3.6 V, I_{OUT} = 0, LDO On with No Load		300	450	μA
$t_{REG(BST)}$	Boost Startup Time[6]	To within 2% of V_{BOOST} Final Value, I_{LOAD} < 200 mA, C_{BUS} ≤ 15 μF		0.5	2.0	ms
$I_{LIMPK(BST)}$	Q2 Peak Current Limit		1350	1550	1950	mA
$UVLO_{BST}$	Minimum Battery Voltage for Boost Operation	While Boost Active		2.32		V
		To Start Boost Regulator		2.48	2.70	

Notes:

5. C_{BAT} is placed as close to the charger IC as possible. An additional 30 μF of distributed system capacitance (C_{SYS}) is parallel with CBAT, but is located further from the IC.
6. Guaranteed by design; not tested in production.

I²C Timing Specifications

Guaranteed by design.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{SCL}	SCL Clock Frequency	Standard Mode			100	kHz
		Fast Mode			400	
		High-Speed Mode, $C_B \leq 100$ pF			3400	
		High-Speed Mode, $C_B \leq 400$ pF			1700	
t_{BUF}	Bus-Free Time between STOP and START Conditions	Standard Mode		4.7		µs
		Fast Mode		1.3		
$t_{HD;STA}$	START or Repeated START Hold Time	Standard Mode		4		µs
		Fast Mode		600		ns
		High-Speed Mode		160		
t_{LOW}	SCL LOW Period	Standard Mode		4.7		µs
		Fast Mode		1.3		
		High-Speed Mode, $C_B \leq 100$ pF		160		ns
		High-Speed Mode, $C_B \leq 400$ pF		320		
t_{HIGH}	SCL HIGH Period	Standard Mode		4		µs
		Fast Mode		600		ns
		High-Speed Mode, $C_B \leq 100$ pF		60		
		High-Speed Mode, $C_B \leq 400$ pF		120		
$t_{SU;STA}$	Repeated START Setup Time	Standard Mode		4.7		µs
		Fast Mode		600		ns
		High-Speed Mode		160		
$t_{SU;DAT}$	Data Setup Time	Standard Mode		250		ns
		Fast Mode		100		
		High-Speed Mode		10		
$t_{HD;DAT}$	Data Hold Time	Standard Mode	0		3.45	µs
		Fast Mode	0		900	ns
		High-Speed Mode, $C_B \leq 100$ pF	0		70	
		High-Speed Mode, $C_B \leq 400$ pF	0		150	
t_{RCL}	SCL Rise Time	Standard Mode	$20+0.1C_B$		1000	ns
		Fast Mode	$20+0.1C_B$		300	
		High-Speed Mode, $C_B \leq 100$ pF		10	80	
		High-Speed Mode, $C_B \leq 400$ pF		20	160	
t_{FCL}	SCL Fall Time	Standard Mode	$20+0.1C_B$		300	ns
		Fast Mode	$20+0.1C_B$		300	
		High-Speed Mode, $C_B \leq 100$ pF		10	40	
		High-Speed Mode, $C_B \leq 400$ pF		20	80	
t_{RDA} t_{RCL1}	SDA Rise Time Rise Time of SCL after a Repeated START Condition and after ACK Bit	Standard Mode	$20+0.1C_B$		1000	ns
		Fast Mode	$20+0.1C_B$		300	
		High-Speed Mode, $C_B \leq 100$ pF		10	80	
		High-Speed Mode, $C_B \leq 400$ pF		20	160	

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I²C Timing Specifications

Guaranteed by design.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{FDA}	SDA Fall Time	Standard Mode		$20+0.1C_B$	300	ns
		Fast Mode		$20+0.1C_B$	300	
		High-Speed Mode, $C_B \leq 100$ pF		10	80	
		High-Speed Mode, $C_B \leq 400$ pF		20	160	
$t_{SU;STO}$	Stop Condition Setup Time	Standard Mode		4		µs
		Fast Mode		600		ns
		High-Speed Mode		160		
C_B	Capacitive Load for SDA, SCL				400	pF

Timing Diagrams

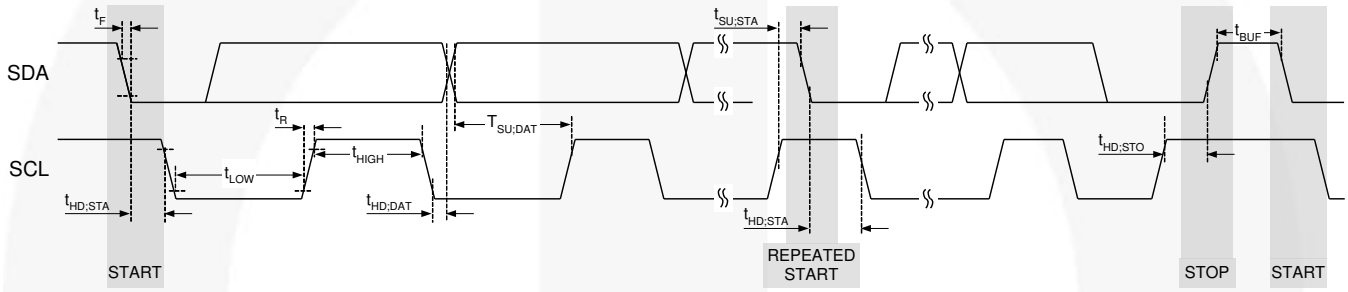


Figure 6. I²C Interface Timing for Fast and Slow Modes

Charge Mode Typical Performance Characteristics

Unless otherwise specified, using circuit of Figure 2, V_{OREG}=4.24 V, V_{BUS}=5.0 V, DIS=0, SCL=SDA=1.8 V, LDO no load, and T_A=25°C.

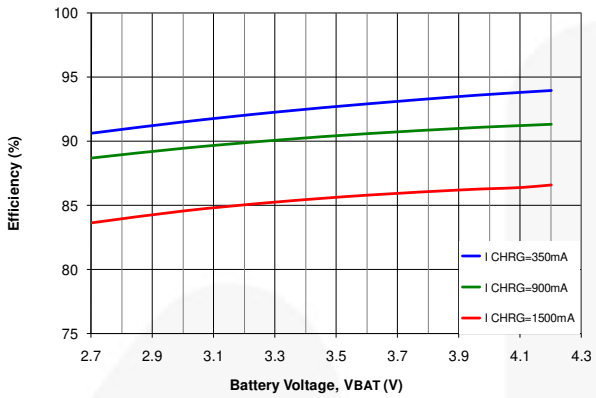


Figure 7. Efficiency vs. Battery Voltage Over-I_{CHRG} Range

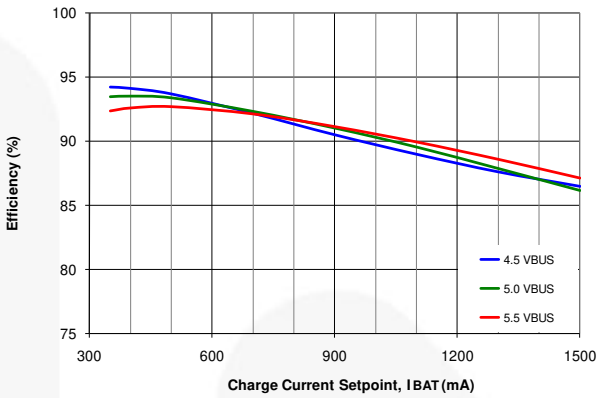


Figure 8. Efficiency vs. I_{CHRG} Over-V_{BUS} Range

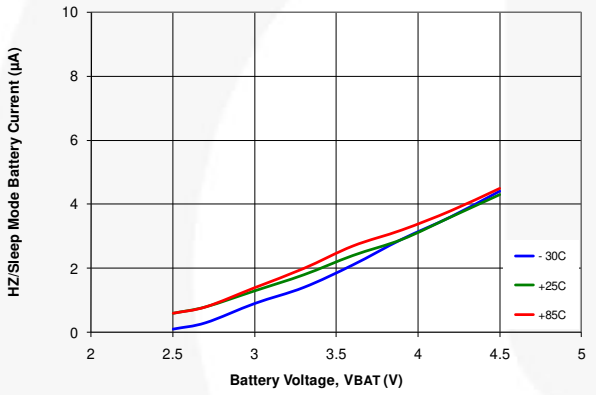


Figure 9. HZ/Sleep Mode Battery Discharge Current, SDA=SCL=1.8 V, DIS=DBP=0

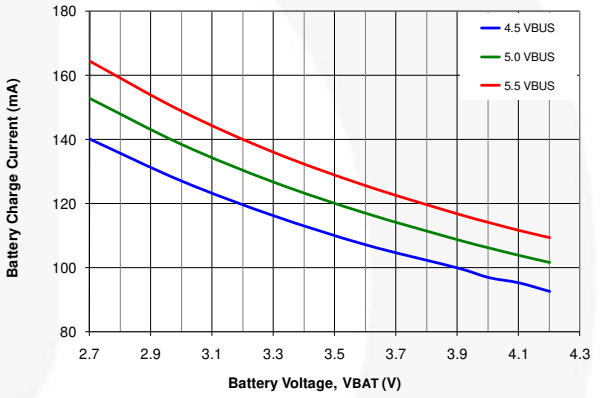


Figure 10. Charge Current vs. Battery Voltage, I_{BUSLIM}=100 mA

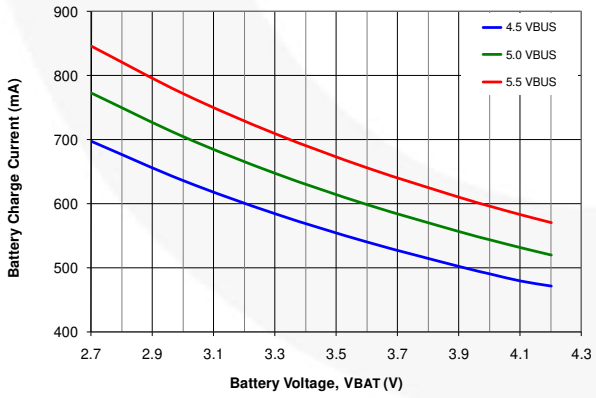


Figure 11. Charge Current vs. Battery Voltage, I_{BUSLIM}=500 mA

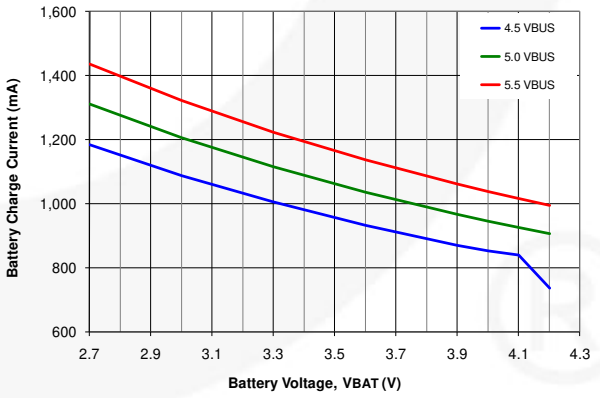


Figure 12. Charge Current vs. Battery Voltage, I_{BUSLIM}=900 mA

Charge Mode Typical Performance Characteristics

Unless otherwise specified, using circuit of Figure 2, V_{OREG}=4.24 V, V_{BUS}=5.0 V, DIS=0, SCL=SDA=1.8 V, LDO no load, and T_A=25°C.

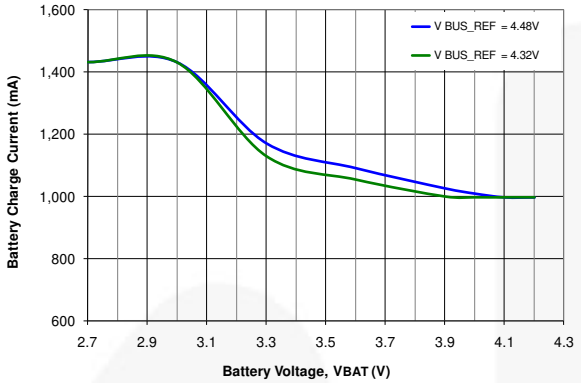


Figure 13. Charge Current vs. Battery Voltage, 5.2 V_{BUS}, 1 A Source Limited

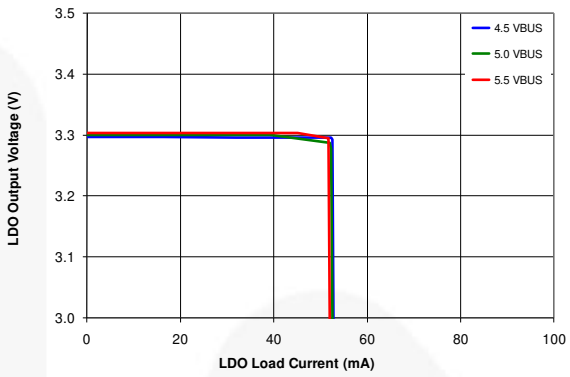


Figure 14. LDO Regulation vs. Load Over-V_{BUS} Range, 4.2 V_{BAT}

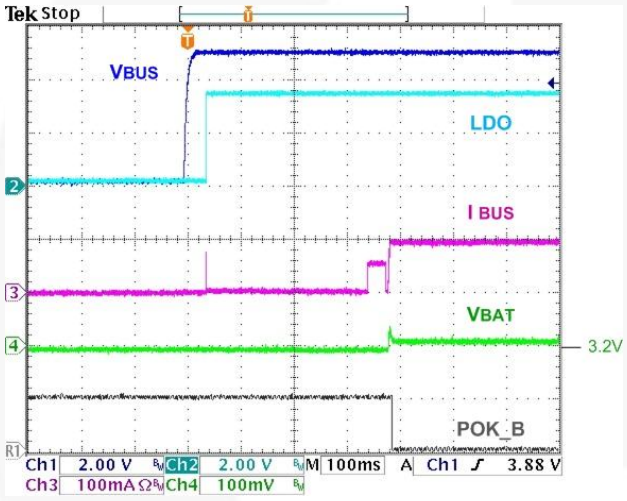


Figure 15. Charger Startup at V_{BUS} Plug-In, 3.2 V_{BAT}, ILIM=DBP=0, 1 kΩ LDO Load

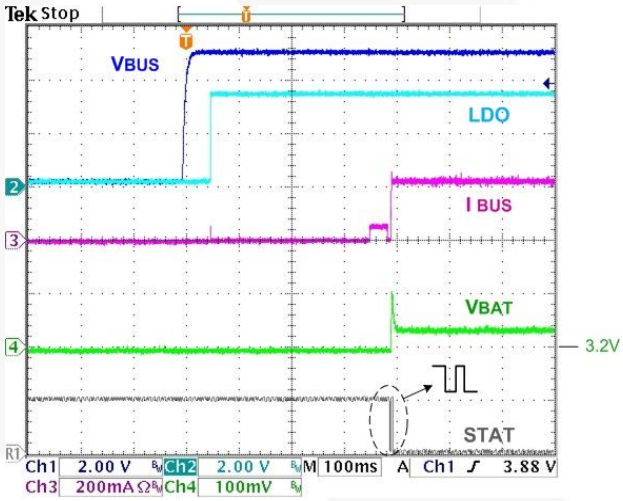


Figure 16. Charger Startup at V_{BUS} Plug-In, 3.2 V_{BAT}, ILIM=1, DBP=0, 1 kΩ LDO Load

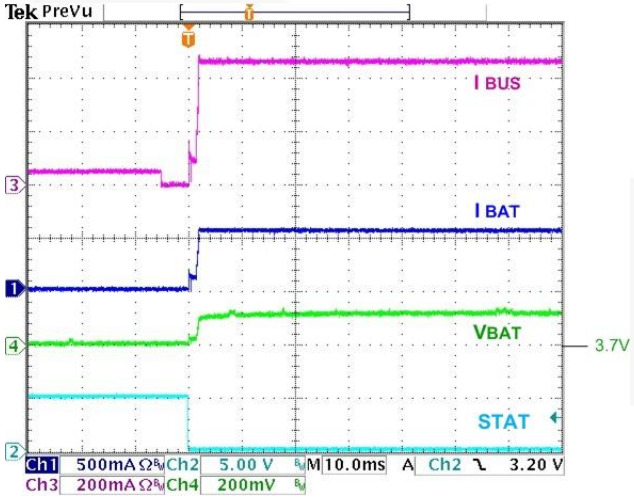


Figure 17. Charger Startup at HZ Bit Reset, 3.7 V_{BAT}, ILIM=DBP=1, 1 kΩ LDO Load, I_{CHRG}=1.0 A

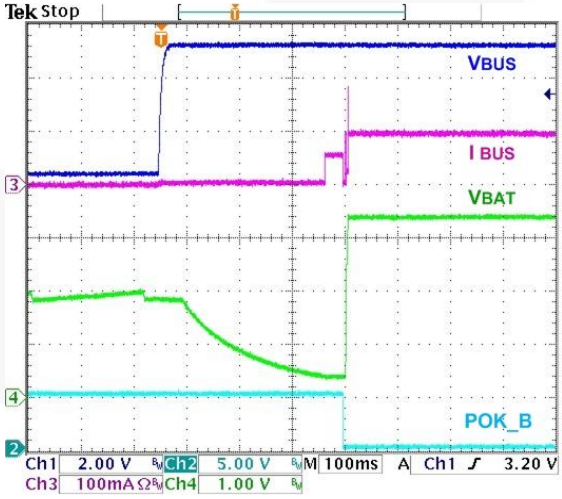


Figure 18. Charger Startup at V_{BUS} Plug-In, Dead Battery, ILIM=DBP=0, 1 kΩ LDO Load

Charge Mode Typical Performance Characteristics

Unless otherwise specified, using circuit of Figure 2, V_{OREG}=4.24 V, V_{BUS}=5.0 V, DIS=0, SCL=SDA=1.8 V, LDO no load, and T_A=25°C.

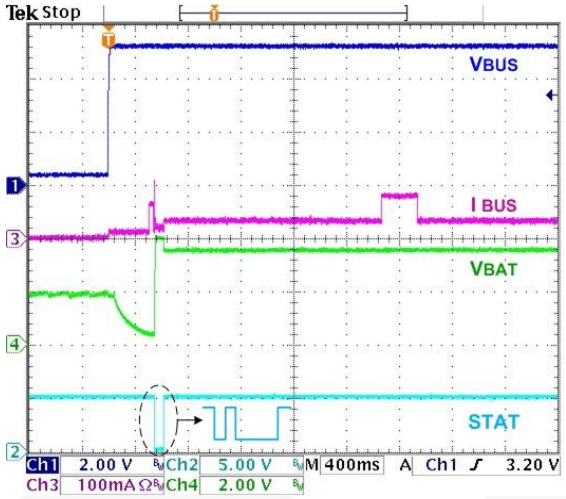


Figure 19. Charger Startup at V_{BUS} Plug-In, No Battery, ILIM=DBP=0, 300 Ω LDO Load

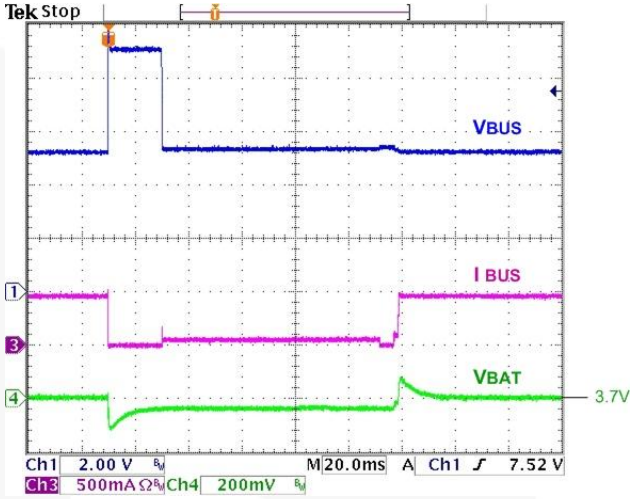


Figure 20. V_{BUS} OVP Response while Charging, 5-9-5 V_{BUS}, 3.7 V_{BAT},I_{BUSLIM}=500 mA, I_{CHRG}=1.0 A

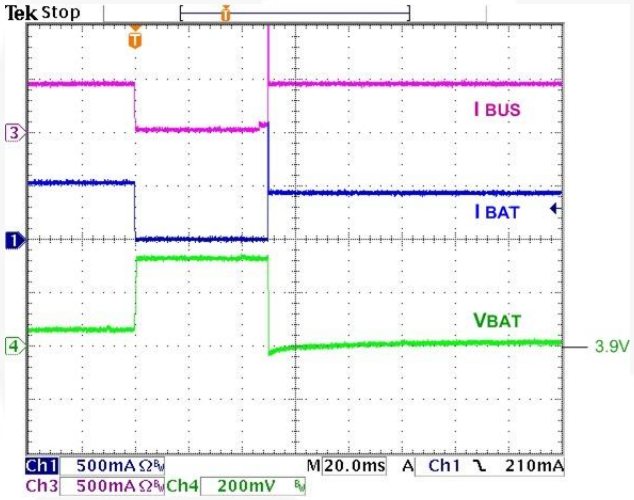


Figure 21. Battery Removal/Insertion while Charging, TE_DIS=1, 3.7 V_{BAT}, 1 kΩ LDO Load, I_{BUSLIM}=500 mA, I_{CHRG}=1.0 A

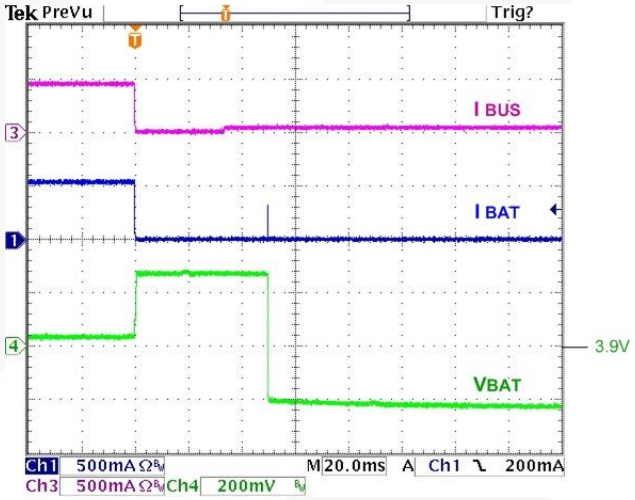


Figure 22. Battery Removal/Insertion while Charging, TE_DIS=0, 3.7 V_{BAT}, 1 kΩ LDO Load, I_{BUSLIM}=500 mA, I_{CHRG}=1.0 A

Charge Mode Typical Performance Characteristics

Unless otherwise specified, using circuit of Figure 2, V_{OREG}=4.24 V, V_{BUS}=5.0 V, DIS=0, SCL=SDA=1.8 V, LDO no load, and T_A=25°C.

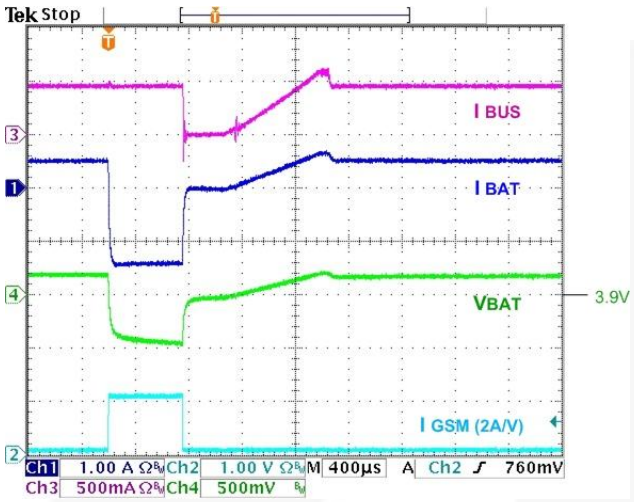


Figure 23. GSM Pulse (2 A Step, t_R/t_F=5 µs) Response, 3.9 V_{BAT}, 1 kΩ LDO Load, I_{BUSLIM}=500 mA, I_{CHRG}=1.0 A

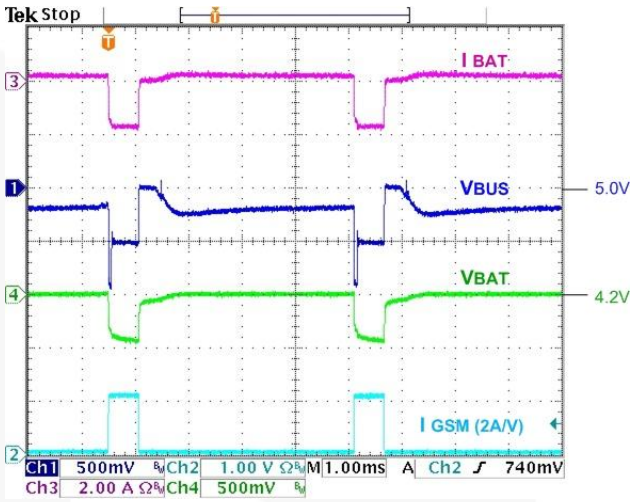


Figure 24. GSM Pulse (2 A Step, t_R/t_F=5 µs) Response, 3.9 V_{BAT}, 1 kΩ LDO Load, I_{BUSLIM}=No Limit, I_{CHRG}=1.0 A, 500 mA V_{BUS} Source Limited

Boost Mode Typical Characteristics

Unless otherwise specified, using circuit of Figure 2 V_{BAT}=3.6 V, DIS=0, SCL=SDA=1.8 V, LDO no load, T_A=25°C.

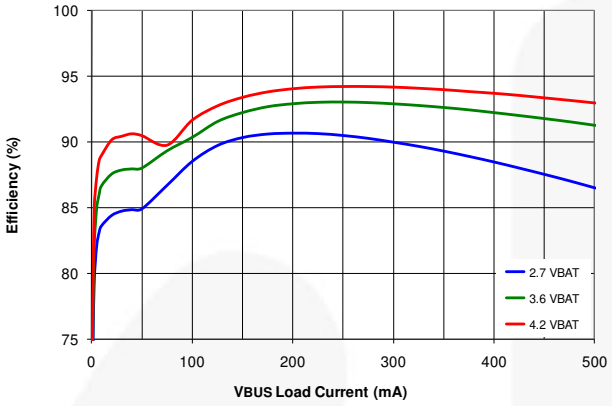


Figure 25. Efficiency vs. Load Current Over-Input Voltage (V_{BAT}) Range

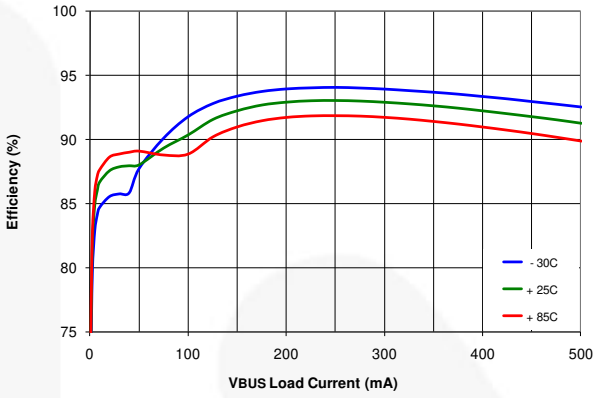


Figure 26. Efficiency vs. Load Current Over-Temperature Range, 3.6 V_{BAT}

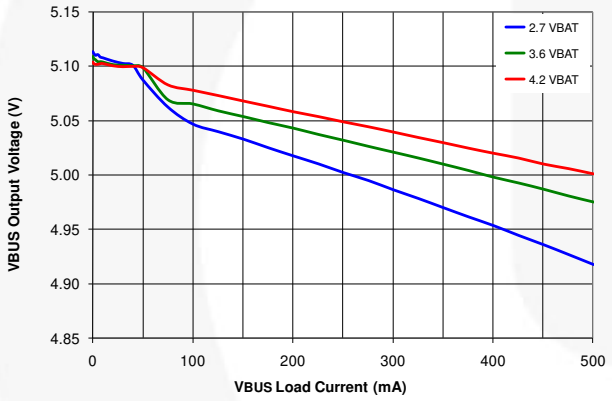


Figure 27. Output Regulation vs. Load Current Over- Input Voltage (V_{BAT}) Range

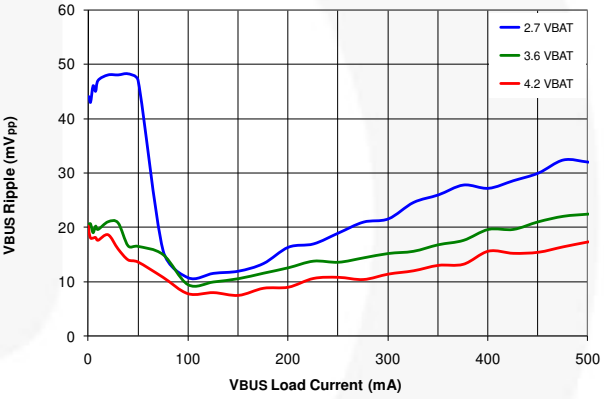


Figure 28. Output Ripple vs. Load Current Over-Input Voltage (V_{BAT}) Range

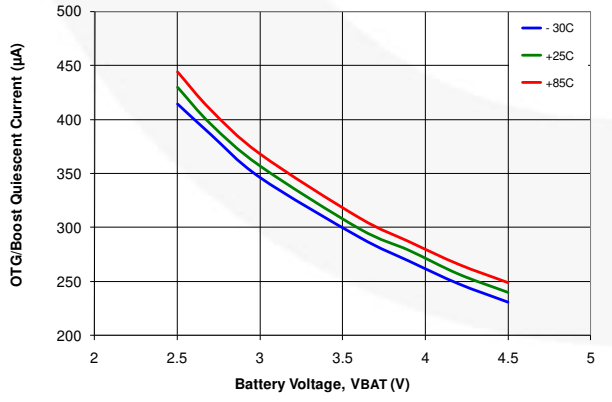


Figure 29. OTG / Boost Quiescent Current vs. Input Voltage (V_{BAT}) Over-Temperature

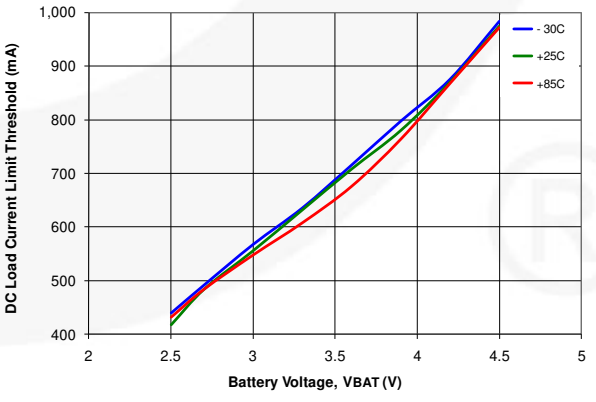


Figure 30. OTG / Boost DC Load Current Limit Threshold vs. Input Voltage (V_{BAT}) Over-Temperature

Boost Mode Typical Characteristics

Unless otherwise specified, using circuit of Figure 2 V_{BAT}=3.6 V, DIS=0, SCL=SDA=1.8 V, LDO no load, T_A=25°C.

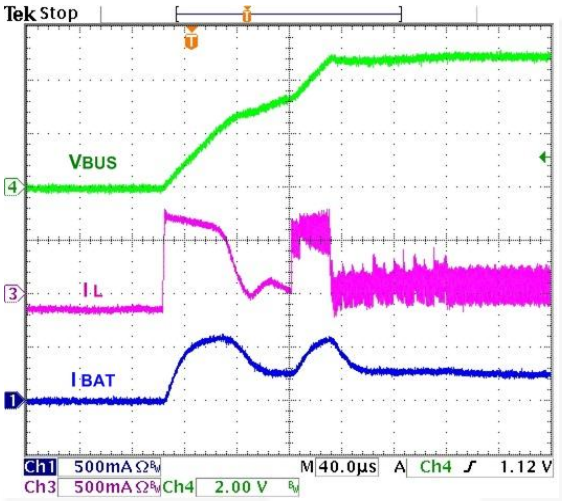


Figure 31. Startup, 50 Ω Load, Additional 10 µF on V_{BUS}

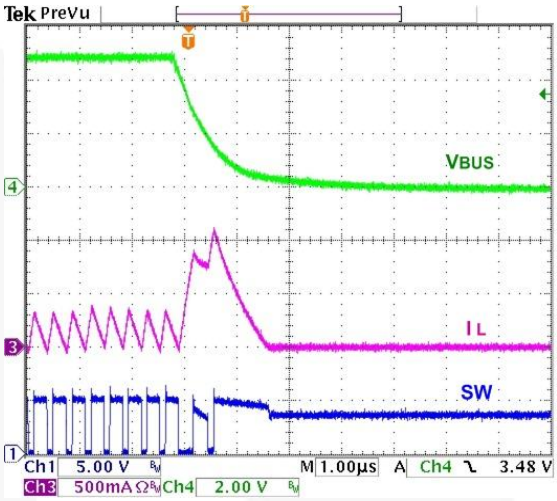


Figure 32. V_{BUS} Output Fault Response

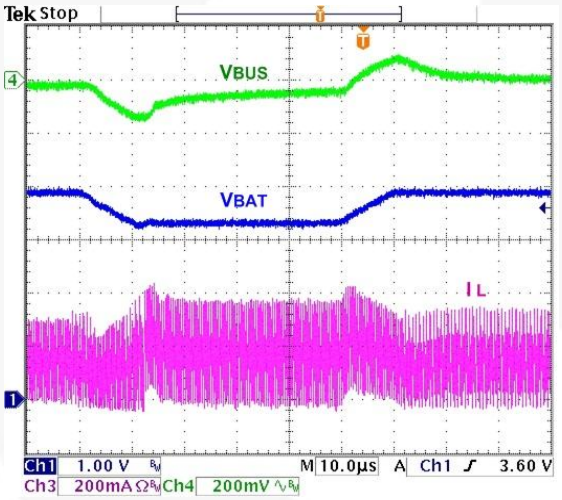


Figure 33. Line Transient Response, 50 Ω Load, 3.9-3.3-3.9 V_{BAT}, t_R/t_F=10 µs

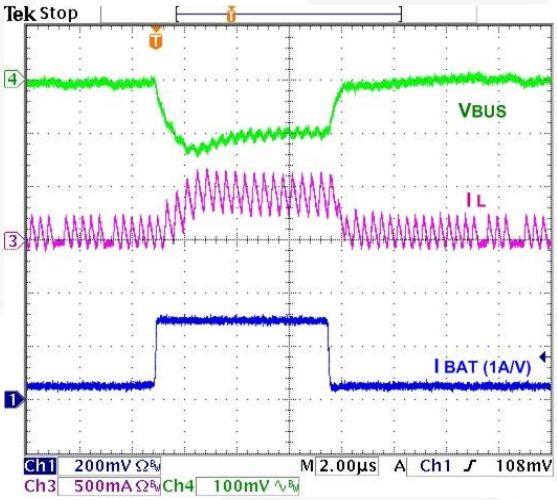


Figure 34. Load Transient Response, 50-300-50 mA, t_R/t_F=100 ns

Operation and Applications Description

The FAN54020 is a USB-compliant single-cell Li-Ion switching charger with support for dead battery provision (DBP) within the BC1.2 specification, including a 30-minute timer that cannot exceed 45 minutes. The maximum charge current is rated at 1.5 A. The FAN54020 is designed to be stable with space-saving ceramic capacitors.

Charging Stages

Figure 35 shows the different stages of Li+ charging when a charger is connected to the USB pins and a battery is present and discharged below 2.25 V. Generally, the prequalification (called “PRE-CHARGE” in Figure 35) stage is when the battery voltage is below 2.25 V when an I_{SHORT} current of 90 mA charges the battery to V_{SHORT} voltage of 2.25 V. Then Fast Charge starts if a battery is detected and the current is increased considerably to a programmable $I_{OCHARGE}$ level (“CURRENT REGULATION” in the figure). The battery voltage climbs quickly based on the drop caused by the current across the load elements of the battery. Then the voltage climbs linearly until the constant voltage stage is reached at the programmable voltage of V_{OREG}. The current is monitored during this stage (“VOLTAGE REGULATION” in the figure) and, when it reaches the end of current I_{TERM}, charging stops.

Figure 36 shows the charge stages using a switching charger when the input power of the charging source is limited by the IC. During current regulation, as V_{BAT} rises, charge current decreases because input power is limited.

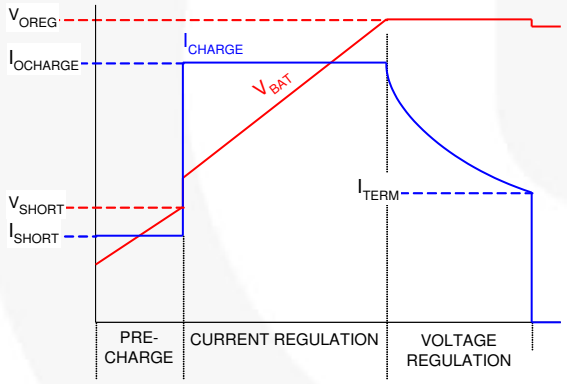


Figure 35. Typical Charging Profile

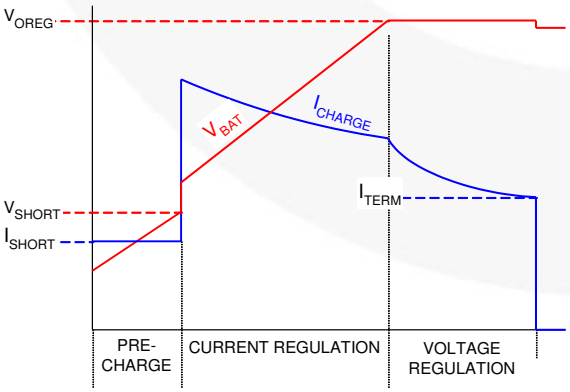


Figure 36. Charge Curve, I_{INLIM} Limits I_{CHARGE}

VBUS_CON

The VBUS_CON bit is set after V_{BUS} rises above V_{BAT} and V_{INMIN1} (4.4 V)[7].

As soon as V_{BUS} falls below either $V_{IN(MIN)2}$ (3.7 V) or V_{BAT}, the IC turns off the charger and applies 50 mA to VBUS for 66 ms. If V_{BUS} is below V_{BAT} or 3.7 V at the end of this period, VBUS_CON is reset.

The STAT pin pulses whenever the VBUS_CON bit changes from HIGH to LOW. For VBUS_CON LOW to HIGH, the STAT pulse occurs per timing in Figure 37 or Figure 38, depending on whether or not charge or HZ state is entered after VBUS is connected.

Note:

7. If V_{BUS} is above V_{INMIN2} (3.7 V), but below V_{INMIN1} (4.4 V); VBUS_CON is set for 132 ms. POK_B also pulses LOW for 132 ms.

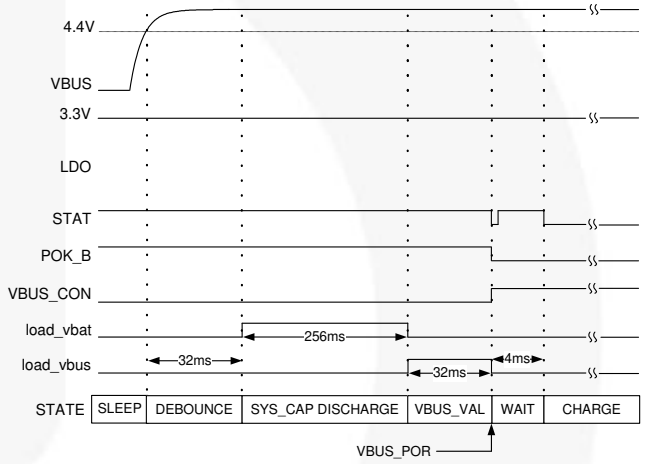


Figure 37. VBUS Plug-in Timing: Battery Present, DBP=1, DIS = 0, HZ_MODE = 0

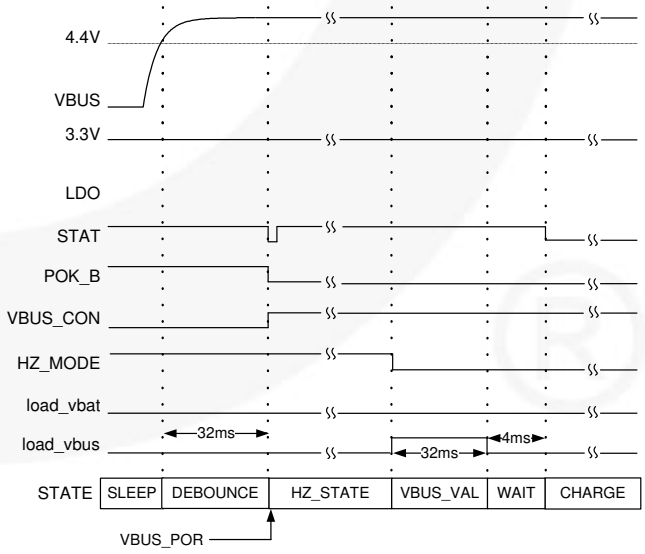


Figure 38. VBUS Plug-in Timing from HZ_MODE: Battery Present, DBP = 1

VBUS POR and DBP *(see Figure 37)*

When the IC detects that V_{BUS} has risen above $V_{IN(MIN)1}$ (4.4 V), Q3's charge pump turns on. If V_{BUS} remains above this threshold for 16 ms, the IC then applies a 1 mA load to VBAT for 256 ms to ensure that, if the battery was removed or its discharge protection switch is open, the system capacitors across VBAT will be discharged below the V_{SHORT} threshold.

V_{BUS} validation is then performed to ensure a valid charging source. Validation occurs with a 50 mA load on VBUS. To pass validation, V_{BUS} must remain above $V_{IN(MIN)1}$ and below V_{BUSOVP} for t_{VBUS_VALID} (32 ms) before the IC initiates charging. If V_{BUS} fails validation; the load is removed, the VALIDATION FAIL bit is set, and validation is attempted every two seconds.

Once V_{BUS} is validated; VBUS_CON (Reg7[7]) is set, POK_B pulls low, and the STAT pin pulses to indicate to the system that VBUS is connected. This point is considered to be VBUS_POR.

If V_{BUS} fails validation, the POK_B pin and bit (Reg7[6]) are raised and the STAT pin pulsed to indicate a V_{BUS} fault. V_{BUS} validation is subsequently re-tried every two seconds. Setting HZ_MODE or DIS prevents periodic re-validation. V_{BUS} validation is also performed prior to entering CHARGE state from any state where the charger is off.

At VBUS POR, the IC operates in accordance with its I^2C register settings as long as the DBP pin is HIGH. If the DBP pin is LOW, the IC sets all registers to their default values and the I_{BUS} current is controlled by the ILIM pin, with $IBUS_{(MAX)}$ = 100 mA when ILIM is LOW and $IBUS_{(MAX)}$ = 500 mA when ILIM is HIGH. Once DBP returns HIGH, D+ is tri-stated and charge parameters may be programmed by the host. $IBUS_{(MAX)}$ remains controlled by the state of the ILIM pin until the first I^2C write occurs; at which time, $IBUS_{(MAX)}$ is controlled by the I_{BUS} register bits (Reg5). The first I^2C write after DBP rises stops the t_{30MIN} timer and starts the 32-second timer (t_{32S}).

BC1.2 and USB 2.0 allow a portable device (defined as a device with a battery) with a dead battery to take a maximum of 100 mA from the USB VBUS line for a maximum of 45 minutes as long as the portable device forces the D+ line to 0.6 V typical.

If the DBP pin is LOW at VBUS POR or transitions from HIGH to LOW when VBUS is valid, the FAN54020:

1. Resets its registers to default values;
2. Starts the t_{30MIN} timer;
3. Charges with its input current limit set by the state of the ILIM pin as described above; and
4. Sources 0.6 V to the D+ pin.

Both ILIM and DBP are internally pulled down and there is typically nothing to force them HIGH at this point due to the processor/system not being awake. When t_{30MIN} expires, the FAN54020 removes the 0.6 V from D+ and stops charging. The D+ pin is also tri-stated when DBP is HIGH.

After a t_{30MIN} timer expiration, charging may only be restarted after a new VBUS POR.

LDO

The FAN54020 contains a 3.3 V LDO available to provide power to the USB PHY. By default, the LDO is enabled and biased from VBAT when DBP is HIGH and $V_{BUS} < V_{BAT}$. When $V_{BUS} > V_{BAT}$, the LDO is biased from VBUS. If DBP is LOW, the LDO is only biased from VBUS and off when $V_{BUS} < V_{IN(MIN)1}$. When the LDO_OFF bit (Reg02[4]) is raised, the LDO is biased from VBUS and off when $V_{BUS} < V_{IN(MIN)1}$.

Pre-Charging Stage

A typical battery has a protection circuit within the battery pack to prevent further discharge if its cell voltage falls below 2.25 V. This causes V_{BAT} to decay quickly to ground since all that is holding V_{BAT} up is the external decoupling capacitors. Another way V_{BAT} can get so low is if VBAT is shorted to ground accidentally. Both are very rare in a typical system because a dead battery is typically above 3 V and only goes below 3 V via leakage over a long period of time.

When $V_{BUS} > V_{BAT}$, the IC takes its power from VBUS while monitoring VBAT to determine the optimal charging profile.

If V_{BAT} is below 2.25 V, a charging current of 90 mA is used to trickle charge the battery. If it is not a short circuit, V_{BAT} should recover very quickly above 2.25 V since it is only charging decoupling capacitors. If there is a short circuit, the timer continues up to 30 minutes and expires, shutting down the charger. This limits the short-circuit current of 90 mA to be drawn only for 30 minutes. The only way to recover from this fault is to remove the short circuit. If the short circuit is not removed, detaching and re-attaching the charger restarts the dead battery provision timer for another 30 minutes before shutting off again.

Battery Absent / Present Response

The FAN54020 detects if the battery is absent if V_{BAT} is below 2.25 V at the start of charging. To accomplish this, the IC raises V_{OREG} to 4.0 V for up to 128 ms after V_{BAT} is above 2.25 V. After 64 ms, V_{BAT} is compared to 3.7 V. If V_{BAT} rises above 3.7 V at any time in that 64 ms period, the battery is assumed to be absent *(see Figure 39)*.

If battery absence is detected; all registers are reset, the NOBAT bit is set, an interrupt generated, and V_{OREG} reverts to its default value of 3.54 V. The charger continues to provide power to the system with STAT HIGH in DBP Mode until otherwise instructed through I^2C commands. This allows the host processor an opportunity to detect charger type and negotiate with the USB host for higher current.

The IC continues to provide current, provided that:

1. A timer (T_{30MIN} or T_{32S}) is running; and
2. HZ_MODE = 0 and DIS = 0.

The current drawn from VBUS is determined by the state of the ILIM pin and the $I_{OCHARGE}$ settings.

Once the initial battery absence test is performed, the only other battery absent test performed occurs if ITERM_DIS = 0 and the charge current drops below the ITERM setting.

Constant Current / Constant Voltage Charging

In this stage, V_{BAT} is above the pre-qualification voltage of 2.25 V, but below V_{OREG}. At a certain V_{BAT} level, the system begins a low-level software boot sequence and uses the USB PHY to determine if a Dedicated Charging Port (DCP), Charging Downstream Port (CDP), or a typical PC host (a Standard Downstream Port (SDP)) is connected. The result of the interrogation determines how much current the FAN54020 can draw and remain USB compliant.

For SDP and CDP, enumeration is required. After enumeration, the system can raise the ILIM pin to increase charge current to 500 mA or the host can use the I^2C bus to program the charge current via the $I_{OCHARGE}$ bits in IBAT (REG3[7:4]).

After DBP transitions from LOW to HIGH, writing to any register through I^2C stops and resets the t_{30MIN} timer, which in turn enables the 32-second timer (t_{32S}). As long as t_{32S} is enabled, charge current is controlled by I^2C register settings.

If the t_{32S} timer subsequently expires, charging stops and the IC enters IDLE state *(see Figure 42)*. To continue charging when t_{32S} is enabled, the host must reset the t_{32S} timer by periodically setting the TMR_RST bit (Reg0A[7]). Once the IDLE state is entered; charging can resume only after VBUS is disconnected and reconnected, the DBP pin is lowered, or a new I^2C write starts the t_{32S} timer.

The constant voltage, V_{OREG}, threshold is also expected to be set based on battery type and battery temperature, which should be monitored by the processor via separate controls. Thermal regulation within the FAN54020 may have little correlation to the battery temperature since the heat dissipation of the PCB that the FAN54020 is soldered to may be completely different from the heat dissipation within the battery pack.

Charge Termination and Recharge

When V_{BAT} reaches V_{OREG} (Reg4[5:0]), the current charging the battery is reduced, limited by the battery's ESR and its internal cell voltage. Charging continues until the $I_{BAT} < I_{TERM}$ (set by Reg3[3:0] bits) threshold is crossed. If ITERM_DIS = 0, charging stops (charge termination), and t_{32S} stops.

After charge termination, a small load is placed across VBAT for 132 ms. The battery is presumed absent if V_{BAT} stays below V_{RCH} (140 mV below V_{OREG}) for the next 132 ms. The NOBAT bit is then set and the NOBAT Fault state is entered *(see Figure 46)*. The charger restarts after two seconds and:

1. If $V_{BAT} < V_{SHORT}$, a battery absent/present test described in Figure 39 is performed;

OR

2. If $V_{BAT} > V_{SHORT}$, PWM charging resumes.

The NOBAT bit is reset only if one of the battery absent / present tests is performed with battery presence detected or after a VBUS POR with the battery present.

If V_{BAT} falls to 140 mV below V_{OREG}, the Fast Charge charging cycle starts again, if VRCH_DIS = 0. A recharge condition debounce time of 132 ms is used to prevent transient battery load currents (such as GSM current pulses) from triggering recharge unnecessarily.

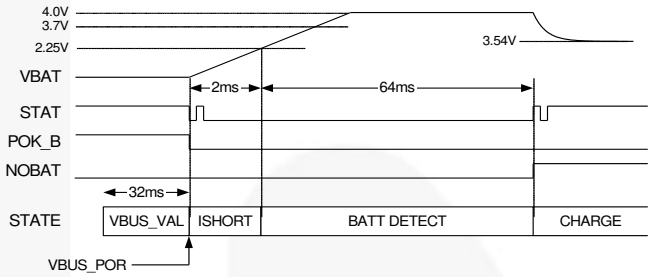


Figure 39. Battery Absent After VBUS POR

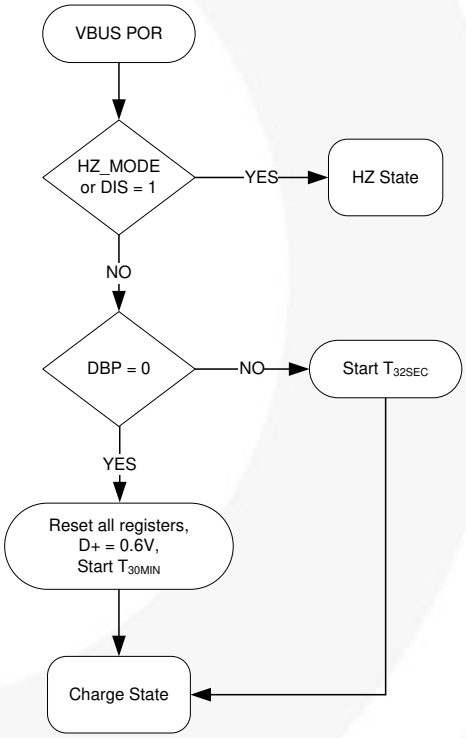


Figure 40. VBUS_POR Flow Chart

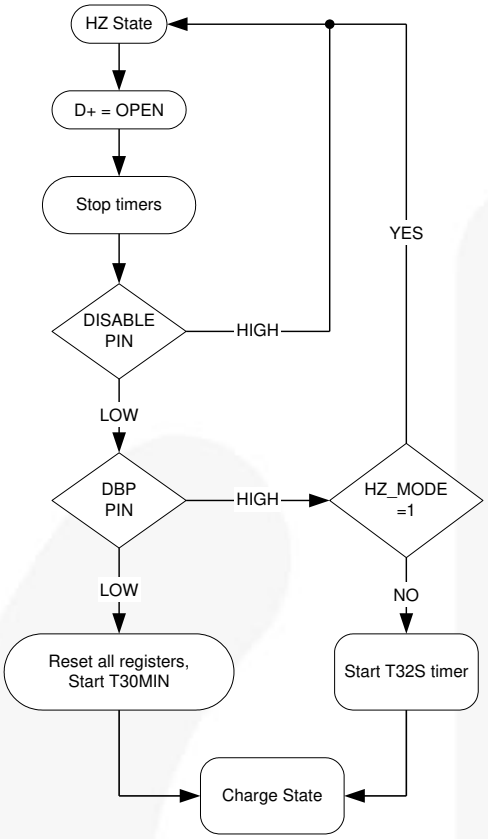


Figure 41. HZ State Flow Chart

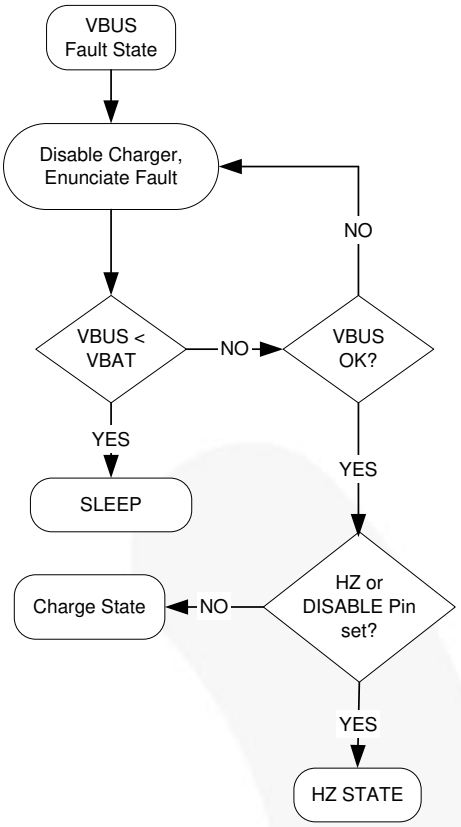


Figure 43. VBUS Fault State Flow Chart

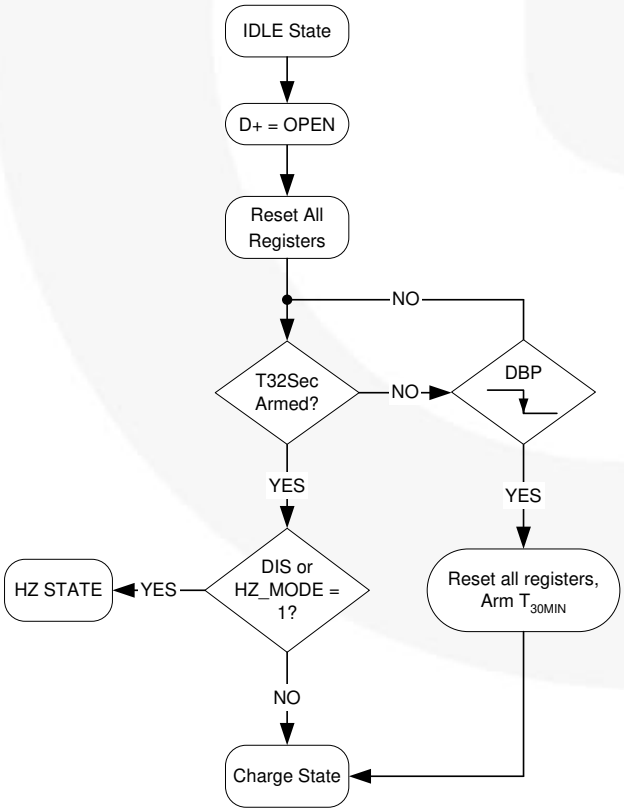


Figure 42. IDLE State Flow Chart

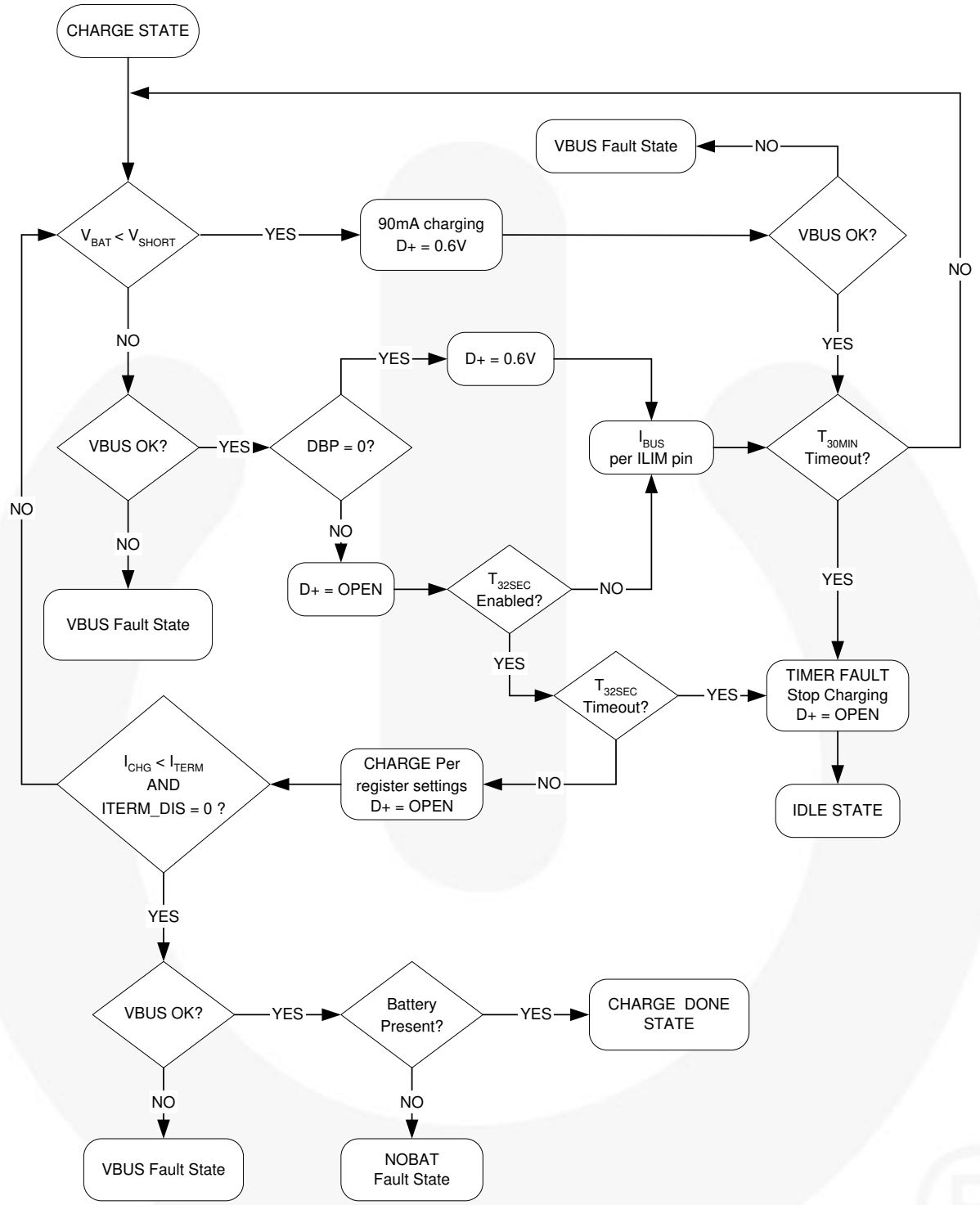


Figure 44. Charge State Flow Chart

Note:

8. If HZ_MODE is set, or DIS = 1, Charge State exits to HZ State.

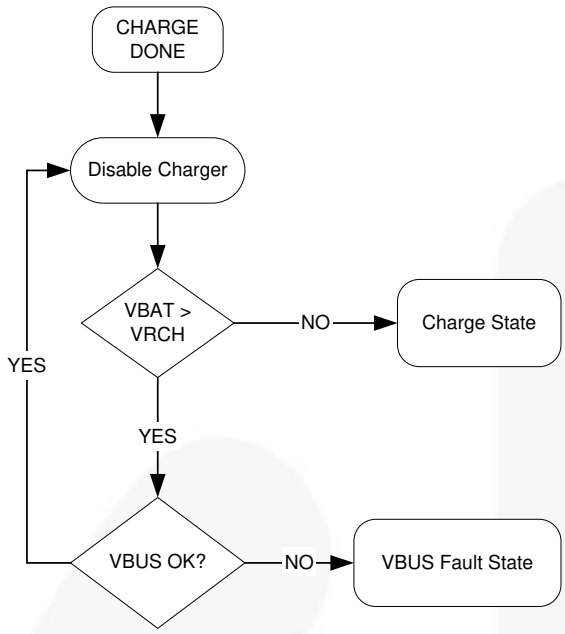


Figure 45. Charge Done State Flow Chart

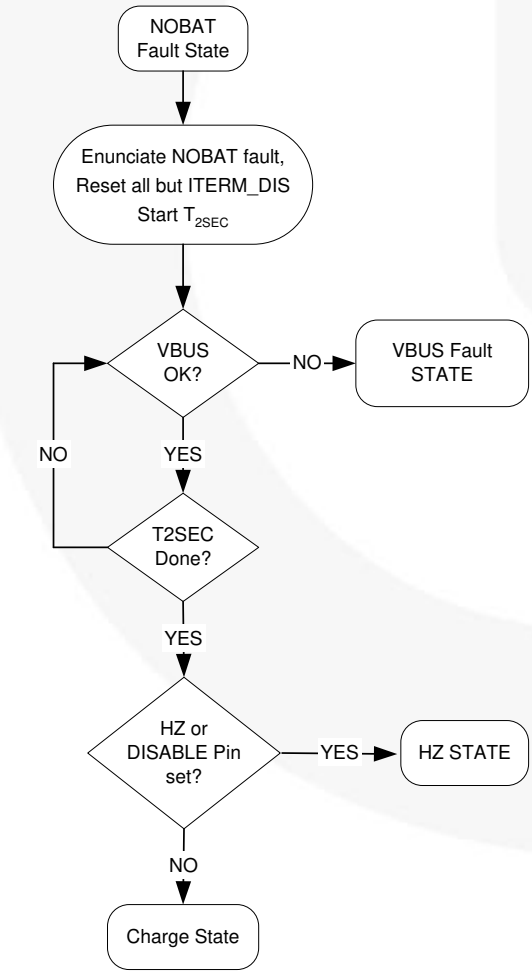


Figure 46. NOBAT Fault State Flow Chart

Production Test Mode

Production Test Mode (PTM) provides power for the system from the USB port.

PTM is enabled when the PTM_EN bit is HIGH and the battery is absent (NOBAT = 1). Only the OREG loop is active and V_{OREG} must be programmed by the user. The 32second timer (T_{32S}) is stooped during PTM.

During PTM, high-current pulses (load currents greater than 1.5 A) must be limited to 20% duty cycle with a minimum period of 10 ms. A 50 mA minimum DC load is required.

STAT Pin and Interrupts

The STAT pin is used to indicate charging status, as well as to signal the host processor of a change in the status of the IC or system. The STAT pin emits a 125 μs low-going pulse whenever an unmasked interrupt event occurs (*see Reg6 – Reg7*). The static state of the STAT pin is determined by whether the IC is charging a battery:

Table 2. STAT Pin Static State

CHARGER	NOBAT Bit	STAT Pin
ON	0	0
OFF	X	1
X	1	1

Any interrupt pulse that occurs while STAT was statically LOW is preceded by a 125 μs STAT HIGH pulse, as shown in Figure 47.

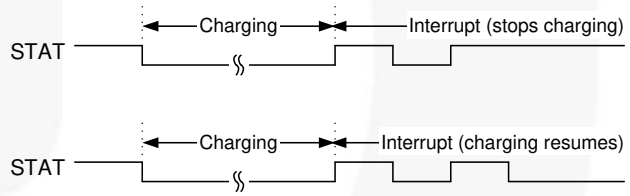


Figure 47. STAT Interrupt Pulse Behavior

If the condition causing the interrupt also causes the charger to stop charging (for example, a Timer fault (TC_TO)), STAT remains HIGH after the 125 μs low-going pulse. If charging continues after the interrupt (as with TREG_FLAG interrupt), STAT goes HIGH for 125 μs after the 125 μs low-going pulse, then returns LOW.

When bits in the INTERRUPT or STATUS register are set, if the corresponding MASK bit is reset, the INTERRUPT bit (Reg1[0]) is set before the falling edge of STAT, which enunciates the interrupt. The INTERRUPT bit is cleared when the host reads Reg1. For an interrupt to be enunciated by the STAT pin, the following conditions must ALL be true:

1. An interrupt condition occurs, which sets an interrupt bit in INTERRUPT or STATUS registers; and
2. The corresponding mask bit = 0; and
3. The INTERRUPT bit (Reg1[0]) = 0.

If additional interrupt conditions occur before the host clears the INTERRUPT bit by reading Reg1, the STAT pin does not pulse.

OVP and VBUS_IN Regulation

The FAN54020 contains programmable over-voltage protection (OVP) on VBUS, ranging from 6.5 V to 8.0 V, as specified in the V_{BUSOVP} bits (Reg1[2:1), with the default setting of 7 V. If OVP is detected, the FAN54020 suspends charging functionality if charging is active when OVP is detected. The FAN54020 interrupts the host when the OVP event occurs and sets the OVP_FLAG bit.

Charging resumes when V_{BUS} returns below the OVP threshold. While charging is suspended, the t_{30MIN} or t_{32S} timer continues and D+ remains at 0.6 V if DBP is LOW.

When V_{BUS} rises above $V_{IBUS(DIS)}$ (6.0 V typical), the IBUS loop is disabled and remains disabled for the next one second. If V_{BUS} falls below $V_{IBUS(DIS)}$ (5.75 V), the IBUS loop is re-enabled. This allows Q3 to be used as a linear regulator to protect PMID from going above about 6 V, while still allowing the charger to operate up to its OVP threshold. When Q3 is used as a linear regulator, it can no longer be used as a sense element for IBUS.

V_{BUS} is typically 5 V ±10%, depending on the charging current. If the FAN54020 is programmed to a higher current than the charger can support, a VBUS regulation loop ensures that the "weak" source does not create a situation where VBUS collapses due to loading. The FAN54020 attempts to lower the charger current and maintain VBUS to the value set in the VBUS_REF bits (Reg2[3:2]). The VBUS regulation loop is enabled by default and has a default value of 4.3 V.

Charging is stopped if V_{BUS} falls below $V_{IN(MIN)1}$ (3.7 V typical) or V_{BAT}, typically indicating that VBUS has been disconnected. Charging remains stopped until V_{BUS} rises above $V_{IN(MIN)1}$ (4.4 V typical) and stays above this threshold.

Thermal Regulation Loop

If the IC junction temperature reaches T_{CF} (Reg5[7:6]), the charger reduces its output current to 300 mA to prevent overheating and the TREG_FLAG bit is set. If the temperature increases beyond $T_{SHUTDWN}$; charging is suspended and the TSD_FLAG is set. While charging is suspended, the t_{30MIN} or t_{32S} timer continues to run and D+ remains at 0.6 V if DBP is LOW. Charging resumes at programmed current after the die cools below T_{CF}. This algorithm allows for the fastest recovery from a thermal regulation event, while still averaging a current that keeps the temperature below T_{CF}.

In both cases, removal of the over-temperature conditions is indicated via the OT_RECOV bit. Temperature is continuously monitored whenever the charger is enabled.

Additional θ_{JA} data points, measured using the FAN54020 evaluation board, are given in Table 3 (measured with T_A=25°C). As power dissipation increases, the effective θ_{JA} decreases due to the larger difference between the die temperature and its ambient.

Table 3. FAN54020 Evaluation Board Θ_{JA}

Power (W)	θ_{JA}
0.504	54°C/W
0.844	50°C/W
1.506	46°C/W

Safety Registers

The SAFETY register (Reg0Fh) prevents the values in V_{OREG} (Reg4[5:0]) and $I_{OCHARGE}$ (Reg3 [7:4]) from exceeding the SAFETY register values of V_{SAFE} (Reg0Fh[3:0]) and I_{SAFE} (Reg0Fh[7:4]).

After DBP pin is set HIGH, the SAFETY register may only be written before any other register is written. After writing to any other register, the SAFETY register is locked until DBP is set LOW. When DBP pin transitions from LOW to HIGH, the default value of the Safety register is loaded.

V_{SAFE} and I_{SAFE} establish values that limit the maximum values of OREG and ICHG. If the host attempts to write a value higher than V_{SAFE} or I_{SAFE} to V_{OREG} or $I_{OCHARGE}$, respectively; the V_{SAFE} and I_{SAFE} value appears as the V_{OREG} and $I_{OCHARGE}$ register values, respectively.

Boost Mode

Boost Mode can be enabled by the BOOST_EN bit (Reg2[6]). To remain in BOOST Mode, the TMR_RST bit must be periodically reset to prevent the t_{32S} timer from overflowing. To remain in Boost Mode, the TMR_RST must be set by the host before the t_{32S} timer times out. If t_{32S} times out in Boost Mode; the IC resets the BOOST_EN bit and pulses the STAT pin.

Boost PWM Control

The IC uses a minimum on-time and computed minimum off-time to regulate V_{BUS}. The regulator achieves excellent transient response by employing current-mode modulation. This technique causes the regulator to exhibit a load line. During PWM Mode, the output voltage drops slightly as the input current rises. With a constant V_{BAT}, this appears as a constant output resistance.

The "droop" caused by the output resistance when a load is applied allows the regulator to respond smoothly to load transients with no undershoot from the load line. This can be seen in Figure 48.

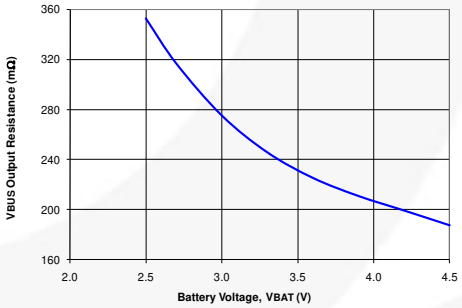


Figure 48. Output Resistance (R_{OUT})

V_{BUS} as a function of I_{LOAD} can be computed when the regulator is in PWM Mode (continuous conduction) as:

$$V_{OUT} = 5.07 - R_{OUT} \bullet I_{LOAD}$$

At V_{BAT}=3.6 V and I_{LOAD}=500 mA, V_{BUS} would drop to:

$$V_{OUT} = 5.07 - 0.225 \bullet 0.5 = 4.979V$$

At V_{BAT}=2.7 V and I_{LOAD}=200 mA, V_{BUS} would drop to:

$$V_{OUT} = 5.07 - 0.317 \bullet 0.2 = 5.007V$$

PFM Mode

If V_{BUS} > $VREF_{BOOST}$ (nominally 5.07 V) when the minimum off-time has ended, the regulator enters PFM Mode. Boost pulses are inhibited until V_{BUS} < $VREF_{BOOST}$. The minimum on-time is increased to enable the output to pump up sufficiently with each PFM boost pulse. Therefore, the regulator behaves like a constant on-time regulator, with the bottom of its output voltage ripple at 5.07 V in PFM Mode.

Table 4. Boost PWM Operating States

Mode	Description	Invoked When
LIN	Linear Startup	V_{BAT} > V_{BUS}
SS	Boost Soft-Start	V_{BUS} < V_{BST}
BST	Boost Mode	V_{BAT} > $UVLO_{BST}$ + SS Completed

Shutdown State

When the boost regulator is shut down, current flow is prevented from V_{BAT} to V_{BUS} and from V_{BUS} to V_{BAT}.

LIN State

When the boost is enabled, if V_{BAT} > $UVLO_{BST}$, the regulator first attempts to bring PMID within 400 mV of V_{BAT} using an internal 580 mA current source from VBAT (LIN State). If PMID has not achieved V_{BAT} – 400 mV after 512 μs, a FAULT state is initiated.

SS State

When PMID > V_{BAT} – 400 mV, the boost regulator begins switching with a peak current limit of about 50% of its normal current limit. The output slews up until V_{BUS} is within 5% of its set point; at which time, the regulation loop is closed and the current limit is set to 100%.

If the output fails to achieve 95% of its set point (V_{BST}) within 128 μs, the current limit is increased to 100%. If the output fails to achieve 95% of its set point after this second 384 μs period, a Fault state is initiated.

BST State

This is the normal operating mode of the regulator. The regulator uses a minimum t_{OFF}-minimum t_{ON} modulation scheme. The minimum t_{OFF} is proportional to $\frac{V_{IN}}{V_{OUT}}$, which keeps the regulator's switching frequency reasonably constant in CCM. $T_{ON(MIN)}$ is proportional to V_{BAT} and is a higher value if the inductor current reaches zero before $t_{OFF(MIN)}$ in the prior cycle.

To ensure the V_{BUS} does not pump significantly above the regulation point, the boost switch remains off as long as V_{FB} > $VREF_{BOOST}$.

Boost Faults

If a boost fault occurs:

1. The STAT pin pulses (if the fault's mask bit is reset) with the corresponding interrupt bit set *(see Table 25)*.
2. BOOST_EN bit is reset.
3. The power stage is in High-Impedance Mode.

Boost Mode can only be re-enabled through I^2C commands since BOOST_EN is reset on boost faults.

Attach Detection Protocol (ADP) Support

The FAN54020 supports Attach Detection Protocol (ADP) as described in *USB_OTG_and_EH_2-0-version_1_1*, which can be downloaded from: *www.usb.org/developers/onthego/*.

ADP support requires a mechanism for measuring the capacitance on VBUS. A change in VBUS capacitance signifies that a device requiring OTG power may have been connected to VBUS. The FAN54020 supports ADP by providing current sources, comparators, and a counter *(see Figure 49)*, enabling the host processor to periodically initiate an ADP probe sequence, as described below:

When the OTG boost turns off, the IC turns on a 50 mA (I_{DIS}) current sink and waits until V_{BUS} < 0.10 V. Once V_{BUS} crosses 0.1 V, the current sink is disabled and a VBUSLOW interrupt is generated. At this point, the IC is in Sleep State with all bias circuits turned off to minimize power drawn on the battery.

The host can also periodically monitor the status of VBUS by writing a 1 to the RDVBUS bit. This causes the IC to turn on its analog circuitry with power supplied from VBAT. The IC issues a STAT pulse after it has refreshed VBUS_100, VBUS_700, and VBUS_CMP to reflect the current condition of VBUS, then powers down. The reference for VBUS_CMP in this state is 3.9 V. After these bits are refreshed, (1 ms maximum) the IC returns to Sleep State.

If V_{BUS} fails to reach 0.1 V within 132 ms, the IBUS load is turned off and a STAT pulse occurs. The system can determine that VBUS failed to discharge below 0.1 V because the VBUS_100 bit is HIGH.

ADP Probe

Host begins an ADP probe by setting ADP_PRB bit, which will both turn on a 1.4 mA current and start the ADP_CNT counter, when VBUS rises above 0.1 V.

If V_{BUS} > 0.1 V (V_{100}) when the host sets ADP_PRB, the 1.55 mA current sink is enabled (IBUSSINK = 1) to first discharge VBUS to 0.1 V before enabling the current source and ADP_CNT counter. If V_{BUS} fails to reach 0.1 V within 32 ms; an ADP_PRBERR interrupt is generated, ADP_PRB is reset, and the VBUS_100 bit is set.

When V_{BUS} reaches 0.7 V (V_{700}), the current source (IBUS_SRC) is turned off, with the count stored in the ADP_CNT register, and an ADP_PRB interrupt is generated. The counter counts in 40 μs increments, so the capacitance on the bus is calculated as shown in Table 5.

Table 5. ADP_CNT Equation

ADP_RATE	C_{BUS}
0	$1.4mA \bullet \frac{ADP\_CNT \bullet 40\mu s}{0.6V}$
1	$1.4mA \bullet \frac{ADP\_CNT \bullet 80\mu s}{0.6V}$

For example, for ADP_RATE = 0 (default), ADP_CNT = 50 when the VBUS capacitance is 4.7 μF. Each increment of ADP_CNT represents a capacitance of 93 nF.

CADP_THR(MIN) = 200 nF is therefore represented by an difference of 2 between ADP_CNT readings.

If ADP_CNT reaches 255 while ADP_PRB = 1, it indicates the attached capacitance exceeds 24 μF, so an ADP_PRBERR interrupt is generated and ADP_PRB is reset.

Once the PRBDONE interrupt occurs, the IC turns on the current sink by setting the IBUSSINK bit, until either V_{BUS} crosses 0.1 V (VBUS_100 bit = 0) or 32 ms elapses. If 32 ms elapses; an ADP_PRBERR interrupt is generated, IBUSSINK is reset, and the IC returns to full Sleep State with VBUS_100 bit remaining HIGH.

ADP_CNT retains its value (either the value when VBUS_700 rose or 255) until it is read by the host or ADP_PRB is again set.

To cancel or exit the ADP probe sequence, write ADP_PRB=0.

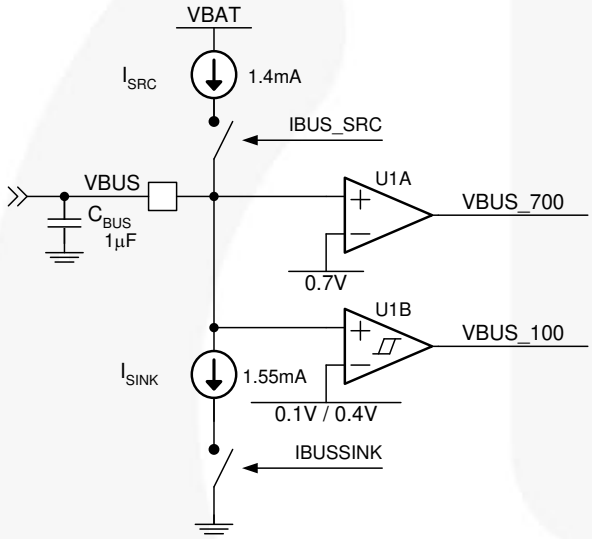


Figure 49. ADP Hardware

ADP Sense

The USB specification requires that a device determine whether an attached device is performing an ADP Probe before activating its own ADP probe. To perform an ADP Sense, the host sets the ADP_SNS bit. This causes the threshold of U1B in Figure 49 to be set to 400 mV and then captures the state of U1B's output. If U1B's output subsequently changes state, an ADP_SNSI interrupt is generated and the ADP_SNS bit is reset, which indicates that a connected device may have performed an ADP Probe.

If U1B's output remains in the same state it was in when ADP_SNS was set, that indicates that no other device was conducting an ADP Probe. The host can then reset the ADP_SNS bit to terminate ADP Sense.

If V_{BUS} becomes greater than V_{BAT} during either ADP Probe, ADP Sense, or RDVBUS operations; the operation is aborted and the IC starts the VBUS plug-in sequences shown in Figure 37 or Figure 38.

To exit the ADP sense sequence, write ADP_SNS bit to 0.

IC State Decode

The STATE register (Reg31) is provided for diagnostic purposes.

Table 6. STATE Register Decode

Value	STATE
00	Initialization – Sleep state
01	Wait for POK and 30 clocks
02	Wait for temperature ok
03	V_{BUS} debounce
04	V_{BUS} debounce
05	V_{BAT} discharge
06	V_{BUS} POR
07	V_{BUS} validation V_{BUS} load
08	Charge Mode SEL
09	Linear charging
0A	PWM charging
0B	V_{BUS} detect
0C	V_{BAT} detect wait
0D	Battery absent / battery full detect
0E	Battery absent
0F	Battery full
10	Post charge
11	High-Z State
12	Idle State
13	VBUS disconnect
14	VBUS disconnect
15	No battery
16	No battery
17	No battery
18	Over-temperature wait
19	Wait OVP
1A	Fault
1B	Fault 0
1C	Fault 1
1D	Fault 2

Value	STATE
20	Production Test Mode
21	Production Test Mode
22	Production Test Mode
28	ADP 30 clocks, TOK
29	ADP sense 4 zeros
2A	ADP sense 100 mV
2B	ADP sense 700 mV
2C	ADP Sense State
30	Boost power up
31	Boost strong bat
32	Boost linear done
33	Boost PWM soft-start
34	Top off
35	Run
36	Boost down
37	Boost down

I²C Interface

The FAN54020 serial interface is compatible with Standard, Fast, Fast-Plus, and High-Speed Mode I²C Bus® specifications. The FAN54020 SCL line is an input and the SDA line is a bi-directional open-drain output; it can only pull down the bus when active. The SDA line only pulls LOW during data reads and when signaling ACK. All data is shifted in MSB (bit 7) first.

Slave Address

Table 7. I²C Slave Address Byte

7	6	5	4	3	2	1	0
1	1	0	1	0	1	1	R/$\overline{W}$

In hex notation, the slave address assumes a 0 LSB. The hex slave address is D6H. Other slave addresses can be accommodated upon request; contact a Fairchild Semiconductor representative.

Bus Timing

As shown in Figure 50, data is normally transferred when SCL is LOW. Data is clocked in on the rising edge of SCL. Typically, data transitions shortly at or after the falling edge of SCL to allow ample time for the data to set up before the next SCL rising edge.

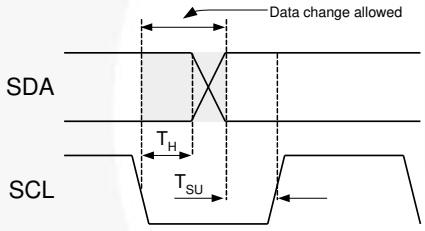


Figure 50. Data Transfer Timing

Each bus transaction begins and ends with SDA and SCL HIGH. A transaction begins with a START condition, which is defined as SDA transitioning from 1 to 0 with SCL HIGH, as shown in Figure 51.

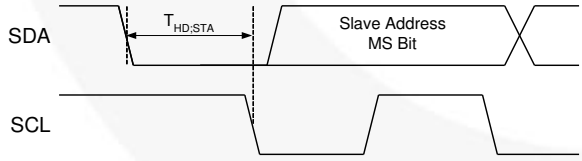


Figure 51. Start Bit

A transaction ends with a STOP condition, which is defined as SDA transitioning from 0 to 1 with SCL HIGH, as shown in Figure 52.

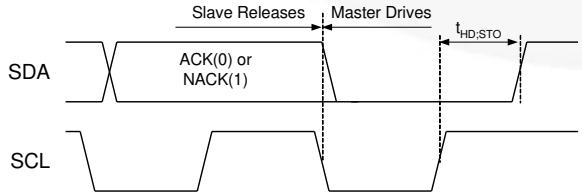


Figure 52. Stop Bit

During a read from the FAN54020 (Figure 55), the master issues a Repeated Start after sending the register address and before resending the slave address. The Repeated Start is a 1-to-0 transition on SDA while SCL is HIGH, as shown in Figure 53.

High-Speed (HS) Mode

The protocols for High-Speed (HS), Low-Speed (LS), and Fast-Speed (FS) Modes are identical except the bus speed for HS Mode is 3.4 MHz. HS Mode is entered when the bus master sends the HS master code 00001XXX after a Start condition. The master code is sent in Fast or Fast-Plus Mode (less than 1 MHz clock); slaves do not ACK this transmission.

The master then generates a Repeated Start condition (Figure 53) that causes all slaves on the bus to switch to HS Mode. The master then sends I²C packets, as described above, using the HS Mode clock rate and timing.

The bus remains in HS Mode until a stop bit (Figure 52) is sent by the master. While in HS Mode, packets are separated by Repeated Start conditions (Figure 53).

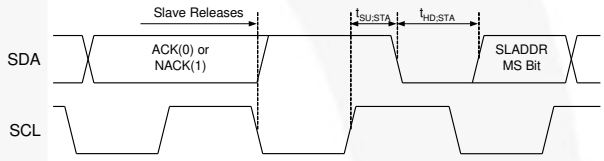


Figure 53. Repeated Start Timing

Read and Write Transactions

Figure 54 – Figure 57 outline the sequences for data read and write. Bus control is signified by the shading of the packet, defined as Master Drives Bus and Slave Drives Bus. All addresses and data are MSB first.

Table 8. Bit Definitions for Figure 54 – Figure 57

Symbol	Definition
S	START, *see Figure 51*
A	ACK. The slave drives SDA to 0 to acknowledge the preceding packet.
$\overline{A}$	NACK. The slave sends a 1 to NACK the preceding packet.
R	Repeated START, *see Figure 53*
P	STOP, *see Figure 52*

Multi-Byte (Sequential) Read and Write Transactions

Sequential Write (Figure 56)
The slave address, Reg Addr address, and the first data byte are transmitted to the FAN54020 in the same way as in a byte write (Figure 54). However, instead of generating a Stop condition, the master transmits additional bytes written to consecutive sequential registers after the falling edge of the eighth bit. After the last byte is written and its ACK bit received, the master issues a STOP bit. The IC contains an 8-bit counter that increments the address pointer after each byte is written.

Sequential Read (Figure 57)
Sequential reads are initiated in the same way as a single-byte read (Figure 55), except that once the slave transmits the first data byte, the master issues an acknowledge instead of a STOP condition. This directs the slave's I^2C logic to transmit the next sequentially addressed 8-bit word. The FAN54020 contains an 8-bit counter that increments the address pointer after each byte is read, which allows the entire memory contents to be read in one I^2C transaction.

Figure 54. Single-Byte Write Transaction

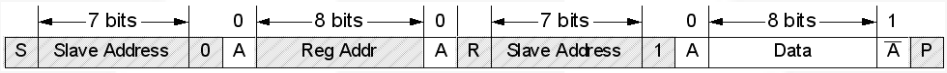


Figure 55. Single-Byte Read Transaction

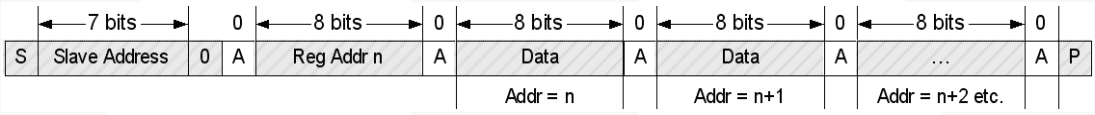


Figure 56. Multi-Byte (Sequential) Write Transaction

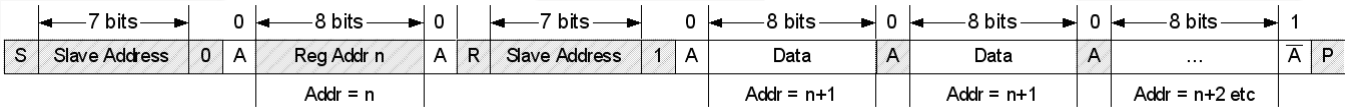


Figure 57. Multi-Byte (Sequential) Read Transaction

Register Descriptions

Table 9. I²C Register Address

Register		Address Bits							
Name	**REG#**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
IC_INFO	0	0	0	0	0	0	0	0	0
CHARGE_CTRL1	1	0	0	0	0	0	0	0	1
CHARGE_CTRL2	2	0	0	0	0	0	0	1	0
IBAT	3	0	0	0	0	0	0	1	1
VOREG	4	0	0	0	0	0	1	0	0
IBUS	5	0	0	0	0	0	1	0	1
INT	6	0	0	0	0	0	1	1	0
STATUS	7	0	0	0	0	0	1	1	1
INT_MASK	8	0	0	0	0	1	0	0	0
ST_MASK	9	0	0	0	0	1	0	0	1
TMR_RST	0AH (10)	0	0	0	0	1	0	1	0
SAFETY	0FH (15)	0	0	0	0	1	1	1	1
MONITOR	10H (16)	0	0	0	1	0	0	0	0
STATE	1FH (31)	0	0	0	1	1	1	1	1
ADP_CTRL	20H (32)	0	0	1	0	0	0	0	0
ADP_CNT	21H (33)	0	0	1	0	0	0	0	1
TMR_CTRL	22H (34)	0	0	1	0	0	0	1	0

Register Bit Definitions

Default values are in **bold** text. Blue text indicates that operations performed on these bits map to the same physical register bits, regardless of which slave address is used.

Table 10. Reg Addr: 0

IC_INFO			**Reg Addr: 0**	**Default = 100X XXXX**
Bit	**Name**	**Type**	**Description**	
7:5	VENDOR	R	**100:** Identifies Fairchild as the supplier	
4:3	PN	R	Part number bits, *see the Ordering Info on page 2*	
2:0	REV	R	IC Revision. Revision is 1.X, where X is the decimal of these 3 bits.	

Table 11. Reg Addr: 1

CHARGE_CTRL1			Reg Addr: 1	Default = 000x 0010
Bit	**Name**	**Type**	**Description**	
7	RESET	W	Setting this bit to 1 resets all registers and operation to default values. This bit returns 0 when read.	
6	HZ_MODE	R/W	**0: Charging is enabled**. 1: Charging is disabled.	
5	Reserved	R	This bit returns 0 when read.	
4	VBUS_LOOP	R	0: VBUS regulation loop is active ($V_{BUS} = V_{BUS\_REF}$). 1: $V_{BUS} > V_{BUS\_REF}$ when in charge state.	
3	Reserved	R	This bit returns 0 when read.	
2:1	V_{BUSOVP}	R/W	When V_{BUS} is at or above this threshold, a V_{BUS} OVP fault is enunciated and the charger is disabled until the fault clears. **Table 12. V_{BUSOVP} Threshold**	
0	INTERRUPT	R	**0: No interrupt has occurred**. This bit is reset when this register is read. 1: Interrupt has occurred.	

[2:1]	V_{BUSOVP} Threshold
00	6.5
01	**7.0**
10	7.5
11	8.0

Table 13. Reg Addr: 2

CHARGE_CTRL2			Reg Addr: 2	Default = 0000 0111 (07H)
Bit	**Name**	**Type**	**Description**	
7	PTM_EN	R/W	**0: Normal operation** 1: Production Test Mode is enabled if NOBAT (Reg5[0]) = 1. *See Production Test Mode description.*	
6	BOOST_EN	R/W	**0: OTG boost regulator is disabled**. 1: OTG boost regulator is enabled.	
5	BOOST_UP	R	**0: Boost output is either disabled or out of regulation**. 1: Boost regulator is enabled and in regulation (not in a fault condition).	
4	LDO_OFF	R/W	**0: 3.3 V LDO is ON and biased from VBAT when**: **($V_{BUS} < V_{BAT}$ and the DBP pin is HIGH)** 1: 3.3 V LDO is OFF when $V_{BUS} < V_{IN(MIN)1}$	
3:2	VBUS_REF	R/W	Sets the V_{BUS_REF} threshold. **Table 14. V_{BUS_REF} Threshold**	
1	VRCH_DIS	R/W	0: Charging re-starts if $V_{BAT} < V_{OREG}$-V_{RCH}. **1: Charging does not re-start automatically if VBAT drops**.	
0	ITERM_DIS	R/W	0: Charging terminates at the programmed ITERM level. **1: Charging does not terminate at the programmed ITERM level**.	

DEC	BIN	V_{BUS_REF}
0	00	4.24
1	**01**	**4.32**
2	10	4.40
3	11	4.48

Table 15. Reg Addr: 3

IBAT	Reg Addr: 3	Default = 0000 0010 (02H)

Bit	Name	Type	Description
7:4	$I_{OCHARGE}$	R/W	**Table 16. $I_{OCHARGE}$ Settings; Current for R_{SENSE} = 68 mΩ**
3:0	ITERM	R/W	**Table 17. I_{TERM} Settings; Current for R_{SENSE} = 68 mΩ**

Table 16. $I_{OCHARGE}$ Settings; Current for R_{SENSE} = 68 mΩ

DEC	BIN	HEX	V_{RSENSE} (mV)		$I_{OCHARGE}$ (mA)	
			Typ	Max	Typ	Max
0	**0000**	**00**	**22.13**	**23.80**	**326**	**350**
1	0001	**01**	25.30	27.20	372	400
2	0010	02	31.62	34.00	465	500
3	0011	03	38.76	40.80	570	600
4	0100	04	45.22	47.60	665	700
5	0101	05	51.68	54.40	760	800
6	0110	06	58.14	61.20	855	900
7	0111	07	64.60	68.00	950	1,000
8	1000	08	71.06	74.80	1,045	1,100
9	1001	09	77.52	81.60	1,140	1,200
10	1010	0A	83.98	88.40	1,235	1,300
11	1011	0B	90.44	95.20	1,330	1,400
12	1100	0C	96.90	102.00	1,425	1,500
13	1101	0D	96.90	102.00	1,425	1,500
14	1110	0E	96.90	102.00	1,425	1,500
15	1111	0F	96.90	102.00	1,425	1,500

Table 17. I_{TERM} Settings; Current for R_{SENSE} = 68 mΩ

BIN	HEX	V_{RSENSE} (mV)	I_{TERM} (mA)
0000	00	3.4	50
0001	01	5.1	75
0010	**02**	**6.8**	**100**
0011	03	8.5	125
0100	04	10.2	150
0101	05	11.9	175
0110	06	13.6	200
0111	07	15.3	225
1000	08	17.0	250
1001	09	18.7	275
1010	0A	20.4	300
1011	0B	22.1	325
1100	0C	23.8	350
1101	0D	25.5	375
1110	0E	27.2	400
1111	0F	28.9	425

Table 18. Reg Addr: 4

OREG	Reg Addr: 4		Default = 0000 1000 (08H)
Bit	**Name**	**Type**	**Description**
7:6	Reserved	R	These bits return 0 when read.
5:0	V_{OREG}	R/W	**Table 19. OREG Settings**

DEC	BIN	HEX	V_{OREG} (V)	Dec	Binary	Hex	V_{OREG} (V)
0	000000	00	3.38	32	100000	20	4.02
1	000001	01	3.40	33	100001	21	4.04
2	000010	02	3.42	34	100010	22	4.06
3	000011	03	3.44	35	100011	23	4.08
4	000100	04	3.46	36	100100	24	4.10
5	000101	05	3.48	37	100101	25	4.12
6	000110	06	3.50	38	100110	26	4.14
7	000111	07	3.52	39	100111	27	4.16
8	**001000**	**08**	**3.54**	40	101000	28	4.18
9	001001	09	3.56	41	101001	29	4.20
10	001010	0A	3.58	42	101010	2A	4.22
11	001011	0B	3.60	43	101011	2B	4.24
12	001100	0C	3.62	44	101100	2C	4.26
13	001101	0D	3.64	45	101101	2D	4.28
14	001110	0E	3.66	46	101110	2E	4.30
15	001111	0F	3.68	47	101111	2F	4.32
16	010000	10	3.70	48	110000	30	4.34
17	010001	11	3.72	49	110001	31	4.36
18	010010	12	3.74	50	110010	32	4.38
19	010011	13	3.76	51	110011	33	4.40
20	010100	14	3.78	52	110100	34	4.42
21	010101	15	3.80	53	110101	35	4.44
22	010110	16	3.82	54	110110	36	4.44
23	010111	17	3.84	55	110111	37	4.44
24	011000	18	3.86	56	111000	38	4.44
25	011001	19	3.88	57	111001	39	4.44
26	011010	1A	3.90	58	111010	3A	4.44
27	011011	1B	3.92	59	111011	3B	4.44
28	011100	1C	3.94	60	111100	3C	4.44
29	011101	1D	3.96	61	111101	3D	4.44
30	011110	1E	3.98	62	111110	3E	4.44
31	011111	1F	4.00	63	111111	3F	4.44

Table 20. Reg Addr: 5

IBUS	Reg Addr: 5		Default = 1000 0000 (80H)
Bit	**Name**	**Type**	**Description**
7:6	T_{CF}	R/W	Temperature threshold at which the current is reduced to allow the device to cool. *See Thermal Regulation Loop*. **Table 21. Temperature Threshold Settings** **DEC** / **BIN** / **T_{CF}** 0 / 00 / 70 1 / 01 / 85 **2 / 10 / 100** 3 / 11 / 120
5:2	Reserved	R	These bits return 0 when read.
1:0	I_{BUS}	R/W	**Table 22. IBUS Settings** **DEC** / **BIN** / **I_{BUS} Limit (Max.)** **0 / 00 / 100 mA** 1 / 01 / 500 mA 2 / 10 / 900 mA 3 / 11 / No Limit

Table 23. Reg Addr: 6

INTERRUPT	Reg Addr: 6		Default = 0000 0000 (00H)
Bit	**Name**	**Type**	**Description**
7:0	INT	R	A 1 in a given bit position indicates that a specific fault has occurred as described in the table below. Items in blue are transient conditions, whose bits are cleared when this register is read. The other interrupts herein are not cleared unless the underlying condition has been removed. **Table 24. Charger Interrupt Conditions** **Bit # / FLAG / Interrupt** 7 / TSD_FLAG / Thermal shutdown (TJ > 145°C). 6 / OVP_FLAG / VBUS OVP (OVP shutdown). 5 / TREG_FLAG / Charger thermal regulation is active. 4 / TC_TO / T32Sec timer has timed out. 3 / DBP_TO / Dead-Battery (DBP) timer (T30) has timed out. 2 / OT_RECOV / Die temperature has fallen below 120°C. 1 / OVP_RECOV / VBUS OVP recovery has occurred. 0 / NOBAT / Battery absence detected either at VBUS POR or after charger termination. **Table 25. Boost Mode Interrupt Conditions** **Bit # / FLAG / Interrupt** 7 / TSD_FLAG / Thermal Shutdown (TJ > T_{CF}°C) 6 / OVP_FLAG / V_{BUS} OVP (Over-Voltage shutdown) 5 / BOOSTOV / Boost output is out of regulation due to sustained current limit. 4 / TC_TO / t_{32S} timer has timed out. 3 / BAT_UV / Battery voltage below 2.7 V. 2 / NA / 1 / NA / 0 / N/A / This bit is always 0 in Boost Mode.

Table 26. Reg Addr: 7

STATUS		Reg Addr: 7	Default = 0100 0000 (40H)
Bit	**Name**	**Type**	**Description**
7:5	VBUS_STAT	R	An interrupt is generated when there is a state change in the bit, provided the corresponding bit in the VBUS_MASK = 0. Items in blue are transient conditions, whose bits are cleared when this register is read. The other interrupts are not cleared unless the underlying condition has been removed. **Table 27. Interrupt Conditions** **Bit # / FLAG / Interrupt generated** 7 / VBUS_CON / 1 when VBUS is connected, 0 when VBUS is disconnected. 6 / POK_B / State of the POK_B pin. 5 / VALIDATION FAIL / 1 indicates V_{BUS} validation is attempted and failed. After a failure, V_{BUS} validation is attempted every two seconds.
4	Reserved	R	This bit returns 0 when read.
3:0	ADP_STAT	R	An interrupt is generated when there is a state change in the bit, provided the corresponding bit in the ADP_MASK = 0. Reading this register will reset these bits. **Table 28. ADP Interrupt Conditions** **Bit # / FLAG / Interrupt Generated** 3 / PRBDONE / When VBUS reaches 700 mV (VBUS_700 ↑) when IBUS_SRC = 1. 2 / ADP_PRBERR / If V_{BUS} fails to reach its threshold before a timer times out. This can occur if: 1. ADP_PRB was set with V_{BUS} > 100 mV and V_{BUS} failed to fall within 32 ms while being discharged with 1.55 mA. 2. V_{BUS} failed to reach 700 mV within 255 counts of ADP_CNT (16 ms) while IBUS_SRC was on. 3. VBUS was above 0.1 V 132 ms after boost disabled. 1 / VBUSLOW / V_{BUS} crossed 0.1 V within 132 ms after boost disabled. 0 / ADP_SNSI / VBUS_100 changed state from the state it had at the rising edge ADP_SNS (R20[5]). When this bit rises, the ADP_SNS bit is reset.

Table 29. Reg Addr: 8

INT_MASK		Reg Addr: 8	Default = 0000 0000 (00H)
Bit	**Name**	**Type**	**Description**
7:0	INT_MASK	R/W	A 1 in a bit masks the interrupt corresponding to that bit position in the INTERRUPT register (Reg 6). When the interrupt is masked, the STAT pin does not pulse when the masked event occurs, but the event is still flagged in the INTERRUPT register.

Table 30. Reg Addr: 9

ST_MASK		Reg Addr: 9	Default = 0000 0000 (00H)
Bit	**Name**	**Type**	**Description**
7:0	ST_MASK	R/W	A 1 in a bit masks the interrupt corresponding to that bit position in the STATUS register (Reg07). When the interrupt is masked, the STAT pin does not pulse when the masked event occurs, but the event is still flagged in the STATUS register.

Table 31. Reg Addr: 0AH (10)

TMR_RST		Reg Addr: 0AH (10)	Default = 0000 0X00
Bit	**Name**	**Type**	**Description**
7	TMR_RST	W	Setting this bit to 1 resets the t_{32s} timer, allowing the IC to continue charging under control of the I^2C host. This bit returns 0 when read.
6	Reserved	R	This bit returns 0 when read.
5	DBP_LEVEL	R	Monitors level of DBP pin: 0: DBP pin is LOW. 1: DBP pin is HIGH.
4	ILIM_LEVEL	R	Monitors level of ILIM pin. 0: ILIM pin is LOW. 1: ILIM pin is HIGH.
3	Reserved	R	Return 0 or 1 when read.
2:0	Reserved	R	These bits return 0 when read.

Table 32. Reg Addr: 0FH (15)

SAFETY		Reg Addr: 0FH (15)	Default = 0111 0000 (70H)
Bit	**Name**	**Type**	**Description**
7:4	I_{SAFE}	R/W	Any attempt to write a value to $I_{OCHARGE}$ (Reg3[7:4]) higher than the contents of I_{SAFE} sets $I_{OCHARGE} = I_{SAFE}$.

Table 33. I_{SAFE} Settings

DEC	BIN	HEX	I_{SAFE}
0	0000	00	350
1	0001	01	400
2	0010	02	500
3	0011	03	600
4	0100	04	700
5	0101	05	800
6	0110	06	900
7	**0111**	**07**	**1000**
8	1000	08	1100
9	1001	09	1200
10	1010	0A	1300
11	1011	0B	1400
12	1100	0C	1500
13	1101	0D	1500
14	1110	0E	1500
15	1111	0F	1500

SAFETY		Reg Addr: 0FH (15)	Default = 0111 0000 (70H)
Bit	**Name**	**Type**	**Description**
3:0	V_{SAFE}	R/W	Any attempt to write a value to V_{OREG} (Reg4[5:0]) higher than the contents of V_{SAFE} sets $V_{OREG} = V_{SAFE}$.

Table 34. V_{SAFE} Settings

DEC	BIN	HEX	V_{SAFE}
0	**0000**	**00**	**4.20**
1	0001	01	4.22
2	0010	02	4.24
3	0011	03	4.26
4	0100	04	4.28
5	0101	05	4.30
6	0110	06	4.32
7	0111	07	4.34
8	1000	08	4.36
9	1001	09	4.38
10	1010	0A	4.40
11	1011	0B	4.42
12	1100	0C	4.44
13	1101	0D	4.44
14	1110	0E	4.44
15	1111	0F	4.44

Table 35. Reg Addr: 10H (16)

MONITOR		Reg Addr: 10H (16)	
Bit	**Name**	**Type**	**Description**
7	ITERM_CMP	R	0: $I_{BAT} < I_{TERM}$ reference. 1: $I_{BAT} > I_{TERM}$ reference.
6	VBUS_VBAT	R	0: $V_{BUS} < V_{BAT}$. 1: $V_{BUS} > V_{BAT}$.
5	VSHORT	R	0: $V_{BAT} > V_{SHORT}$ or IC is not charging. 1: $V_{BAT} < V_{SHORT}$ and IC is charging.
4	DIS_LEVEL	R	0: DIS pin is LOW. 1: DIS pin is HIGH.
3	INACTIVE	R	0: Charger is either logically disabled or is actively charging (switcher is active). 1: Charger is enabled, but is not delivering power because $V_{BAT} > V_{OREG}$.
2	IBUS	R	0: IBUS loop is limiting the charge current. 1: IBUS loop is not limiting the charge current.
1	ICHG	R	0: ICHG loop is limiting the charge current. 1: ICHG loop is not limiting the charge current.
0	CV	R	0: Charger is not in CV Mode. Charger is off or another loop (VBUS, IBUS, or ICHG) is limiting charge current. 1: Charger is on and in Constant Voltage (CV) Mode.

Table 36. Reg Addr: 1FH (31)

STATE			Reg Addr: 1FH (31)
Bit	**Name**	**Type**	**Description**
7:0	STATE	R	Charger state machine value. *See Table 6.*

Table 37. Reg Addr: 20H (32)

ADP_CTRL			Reg Addr: 20H (32) Default = 0000 00XX
Bit	**Name**	**Type**	**Description**
7	IBUSSINK	R	0: VBUS current sink is off. 1: VBUS current sink is on.
6	ADP_PRB	R/W	**0: ADP probe sequence not activated.** 1: ADP probe sequence active. This bit is reset once ADP probe is completed.
5	ADP_SNS	R/W	**0: VBUS_100 comparator threshold = 100 mV and ADP Sense interrupt is disabled.** 1: VBUS_100 comparator threshold is set to 400 mV and ADP Sense interrupt is enabled.
4	ADP_RATE	R/W	**0: ADP_CNT increment = 40 μs**. 1: ADP_CNT increment = 80 μs.
3	RDVBUS	W	Writing a 1 to this bit temporarily (about 1 ms) brings the IC out of Sleep State to refresh all VBUS comparator bits in this register. An interrupt is issued when the IC returns to Sleep State.
2	VBUS_CMP	R	0: V_{BUS} < $VBUS\_CMP_{REF}$. 1: V_{BUS} > $VBUS\_CMP_{REF}$. **Table 38. V_{BUS} Comparator Reference** STATE | VBUS < VBAT | CHARGING | VALIDATION $VBUS\_CMP_{REF}$ | 3.9 | 3.7 | 4.4
1	VBUS_700	R	0: V_{BUS} < 700 mV. 1: V_{BUS} > 700 mV.
0	VBUS_100	R	0: V_{BUS} < 100 mV. 1: V_{BUS} > 100 mV.

Table 39. Reg Addr: 21H (33)

ADP_CNT			Reg Addr: 21H (33) Default = 0000 0000
Bit	**Name**	**Type**	**Description**
7:0	ADP_CNT	R	Counter that increments every 40 μs (default or 80 μs if ADP_RATE=1) after V_{BUS} crosses 100 mV with IBUS_SRC on. When VBUS_700 ↑ or when ADP_CNT reaches 255, ADP_CNT stops incrementing, which generates an PRBDONE or ADP_PRBERR, respectively. ADP_CNT is reset after being read by the host or when ADP_PRB is set.

Table 40. Reg Addr: 22H (34)

TMR_CTRL			Reg Addr: 22H (34)	Default = 0000 0000 (00H)
Bit	**Name**	**Type**	**Description**	
7	T135	R	0: Die temperature is below 135°C. 1: Die temperature is above 135°C.	
6	TCFCOMP	R	0: Die temperature is below T_{CF} *(see Table 21)*. 1: Die temperature is above T_{CF} (*see Table 21)*.	
5	EN_CHG	R	0: PWM charger is disabled. 1: PWM charger is enabled.	
4	EN_LDO	R	0: LDO is off. 1: LDO is on.	
3	NBAT	R	0: A no-battery test was not completed. 1: A no-battery test was completed.	These bits are reset if VBUS is disconnected.
2	T30M	R	0: T30M timer has not expired. 1: T30M timer has expired.	
1	DIS_30M	R/W	**0: T30M timer is enabled**. 1: T30M timer is disabled (never expires).	
0	WD_DIS	R/W	**0: T32Sec timer enabled**. 1: T32Sec timer disabled (never expires).	

PCB Layout Recommendations

Bypass capacitors should be placed as close to the IC as possible. In particular, the total loop length for CMID should be minimized to reduce overshoot and ringing on the SW, PMID, and VBUS pins. All power and ground pins must be routed to their bypass capacitors using top copper if possible. Copper area connecting to the IC should be maximized to improve thermal performance.

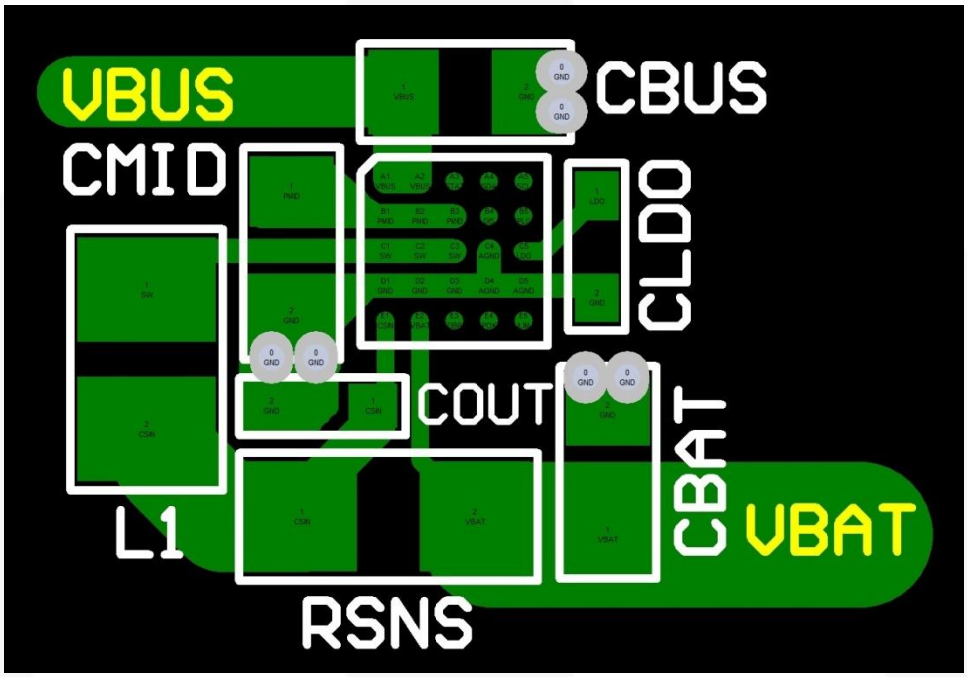
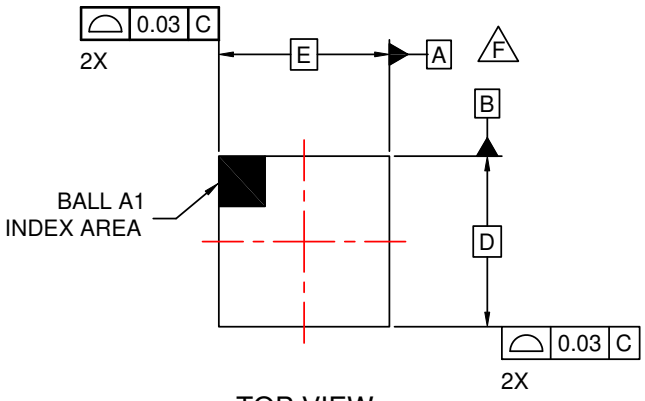


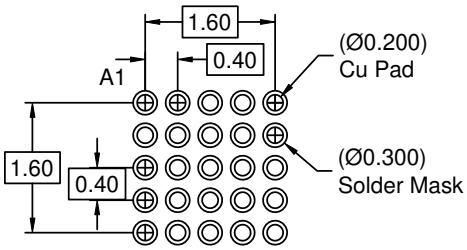
Figure 58. PCB Layout Recommendation

Product-Specific Dimensions

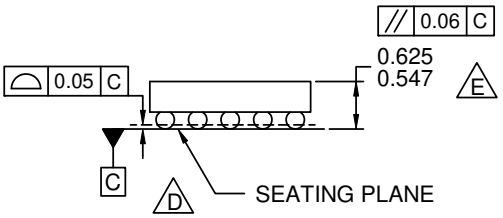
D	E	X	Y
2.050 ±0.030 mm	2.050 ±0.030 mm	0.200 mm	0.200 mm



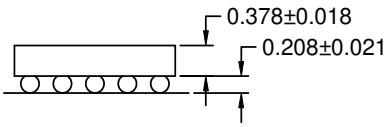
TOP VIEW

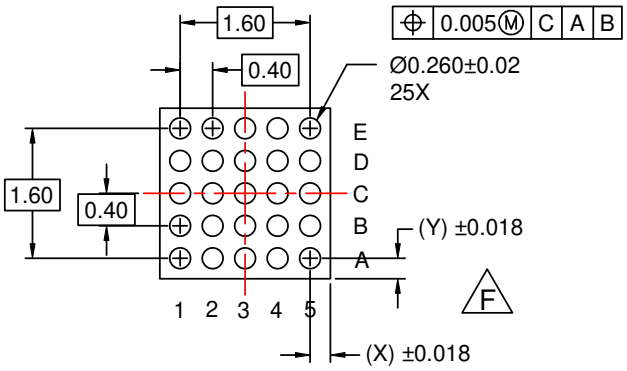


RECOMMENDED LAND PATTERN
(NSMD PAD TYPE)



SIDE VIEWS





BOTTOM VIEW

NOTES:

A. NO JEDEC REGISTRATION APPLIES.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCE PER ASMEY14.5M, 1994.

D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.

E. PACKAGE NOMINAL HEIGHT IS 586 MICRONS ±39 MICRONS (547-625 MICRONS).

F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.

G. DRAWING FILENAME: MKT-UC025AArev3.

FAIRCHILD™

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