# Smart Octal Low-Side Switch

| | | | |
|---|---|---|---|
| Supply voltage | $V_S$ | 4.5 – 5.5 | V |
| Drain source clamping voltage | $V_{DS(AZ)max}$ | 55 | V |
| On resistance | $R_{ON}$ | 0.75 | Ω |
| Output current(all outp.ON equal) | $I_{D(NOM)}$ | 500 | mA |
| (individually) | | 1 | A |

## Features

## Product Summary

- Short Circuit Protection
- Overtemperature Protection
- Overvoltage Protection
- 16 bit Serial Data Input and Diagnostic Output (2 bit/ch. acc. SPI protocol)
- Direct Parallel Control of Four Channels for PWM Applications
- Parallel Inputs High or Low Active Programmable
- General Fault Flag
- Low Quiescent Current
- Compatible with 3,3 V Micro Controllers
- **E**lecto**s**tatic **D**ischarge (ESD) Protection
- Green Product (RoHS compliant)
- AEC Qualified

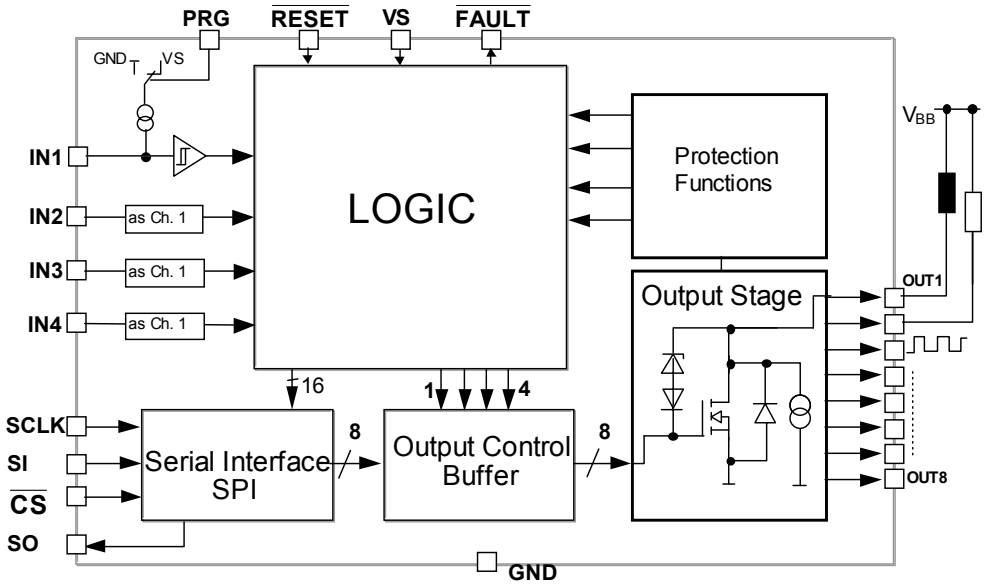
**PG-DSO 36**

## Application

- µC Compatible Power Switch for 12 V and 24V Applications
- Switch for Automotive and Industrial Systems
- Solenoids, Relays and Resistive Loads
- Robotic Controls

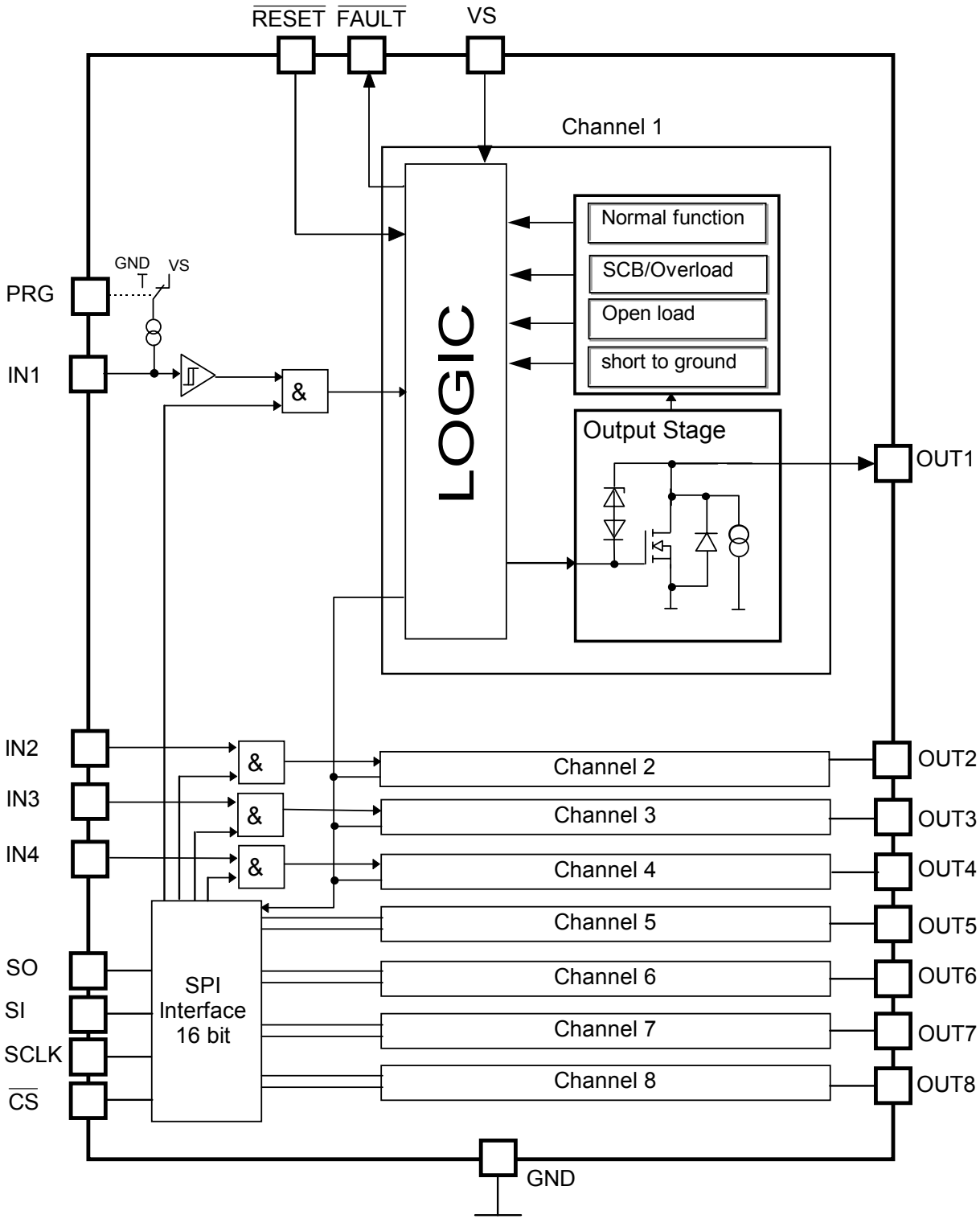
## General description

Octal Low-Side Switch in Smart Power Technology (SPT) with a **S**erial **P**eripheral **I**nterface (SPI) and eight open drain DMOS output stages. The TLE 6230 GP is protected by embedded protection functions and designed for automotive and industrial applications. The output stages are controlled via an SPI Interface. Additionally four channels can be controlled direct in parallel for PWM applications. Therefore the TLE 6230 GP is particularly suitable for engine management and powertrain systems.



## Block Diagram

### Detailed Block Diagram

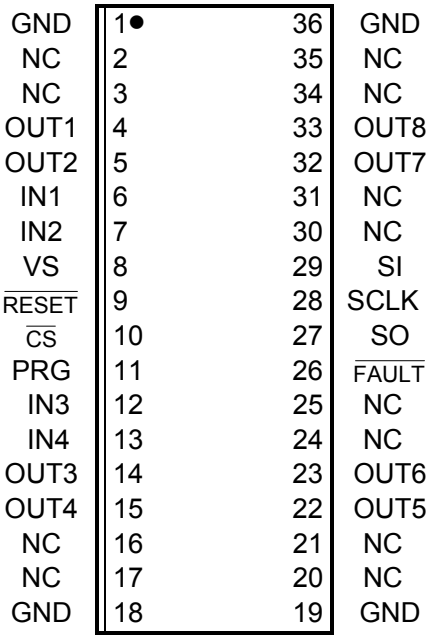


## Pin Description

| Pin | Symbol | Function |
|---|---|---|
| 1 | GND | Ground |
| 2 | NC | not connected |
| 3 | NC | not connected |
| 4 | OUT1 | Power Output Channel 1 |
| 5 | OUT2 | Power Output Channel 2 |
| 6 | IN1 | Input Channel 1 |
| 7 | IN2 | Input Channel 2 |
| 8 | VS | Supply Voltage |
| 9 | $\overline{\text{RESET}}$ | Reset |
| 10 | $\overline{\text{CS}}$ | Chip Select |
| 11 | PRG | Program (inputs high or low-active) |
| 12 | IN3 | Input Channel 3 |
| 13 | IN4 | Input Channel 4 |
| 14 | OUT3 | Power Output Channel 3 |
| 15 | OUT4 | Power Output Channel 4 |
| 16 | NC | not connected |
| 17 | NC | not connected |
| 18 | GND | Ground |
| 19 | GND | Ground |
| 20 | NC | not connected |
| 21 | NC | not connected |
| 22 | OUT5 | Power Output Channel 5 |
| 23 | OUT6 | Power Output Channel 6 |
| 24 | NC | not connected |
| 25 | NC | not connected |
| 26 | $\overline{\text{FAULT}}$ | General Fault Flag |
| 27 | SO | Serial Data Output |
| 28 | SCLK | Serial Clock |
| 29 | SI | Serial Data Input |
| 30 | NC | not connected |
| 31 | NC | not connected |
| 32 | OUT7 | Power Output Channel 7 |
| 33 | OUT8 | Power Output Channel 8 |
| 34 | NC | not connected |
| 35 | NC | not connected |
| 36 | GND | Ground |

Heat Slug internally connected to ground pins

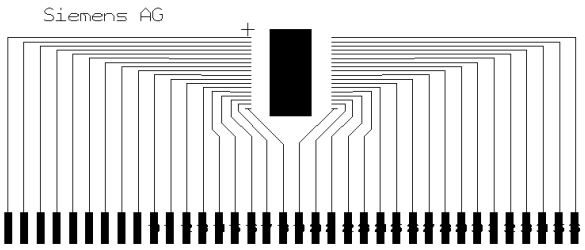
## Pin Configuration (Top view)



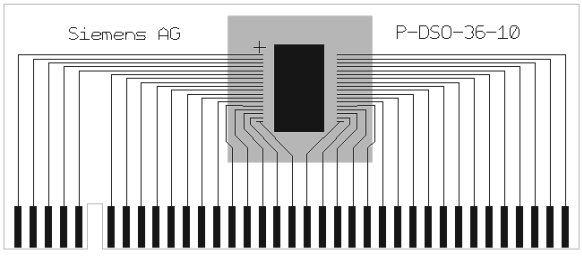

Power SO 36

## Maximum Ratings for $T_j$ = – 40°C to 150°C

| Parameter | Symbol | Values | Unit |
|---|---|---|---|
| Supply Voltage | $V_S$ | -0.3 ... + 7 | V |
| Continuous Drain Source Voltage (OUT1...OUT8) | $V_{DS}$ | 40 | V |
| Input Voltage, All Inputs and Data Lines | $V_{IN}$ | - 0.3 ... + 7 | V |
| Load Dump Protection $V_{Load\ Dump}$ = $U_P$+$U_S$; $U_P$=13.5 V<br>With Automotive Relay Load $R_L$ = 70 Ω<br>$R_I$[1)]=2 Ω; $t_d$=400ms; IN = low or high<br>With $R_L$= 24 Ω; $R_I$=2 Ω; $t_d$=400ms; IN = high or low | $V_{Load\ Dump}$[2)] | <br>80<br><br>52 | V |
| Operating Temperature Range<br>Storage Temperature Range | $T_j$<br>$T_{stg}$ | - 40 ... + 150<br>- 55 ... + 150 | °C |
| Output Current per Channel (see el. characteristics) | $I_{D(lim)}$ | $I_{D(lim)\ min}$ | A |
| Output Current per Channel @ $T_A$ = 25°C<br>(All 8 Channels ON; Mounted on PCB )[3)] | $I_D$ | 500 | mA |
| Output Clamping Energy (single pulse)<br>$I_D$ = 0.5 A | $E_{AS}$ | 50 | mJ |
| Power Dissipation (mounted on PCB) @ $T_A$ = 25°C | $P_{tot}$ | 3.3 | W |
| **E**lectro**s**tatic **D**ischarge **V**oltage (Human Body Model)<br>according to MIL STD 883D, method 3015.7 and EOS/ESD assn. standard S5.1 – 1993<br>Output 1-8 Pins<br>All other Pins | <br><br><br>$V_{ESD}$<br>$V_{ESD}$ | <br><br><br>2000<br>2000 | <br><br><br>V<br>V |
| DIN Humidity Category, DIN 40 040 | | E | |
| IEC Climatic Category, DIN IEC 68-1 | | 40/150/56 | |
| Thermal Resistance<br>junction - case<br>junction - ambient @ min. footprint<br>junction - ambient @ 6 cm² cooling area with heat pipes | <br>$R_{thJC}$<br>$R_{thJA}$<br> | <br>5<br>50<br>38 | <br>K/W<br><br> |




Minimum footprint




PCB with heat pipes,
backside 6 cm² cooling area

1) $R_I$=internal resistance of the load dump test pulse generator LD200
2) $V_{LoadDump}$ is setup without DUT connected to the generator per ISO 7637-1 and DIN 40 839.
3) Output current rating so long as maximum junction temperature is not exceeded. At $T_A$ = 125 °C the output current has to be calculated using $R_{thJA}$ according mounting conditions.

## Electrical Characteristics

| Parameter and Conditions<br>$V_S$ = 4.5 to 5.5 V ; $T_j$ = - 40 °C to + 150 °C ; Reset = H<br>(unless otherwise specified) | | Symbol | Values | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| **1. Power Supply, Reset** | | | | | | |
| Supply Voltage[4] | | $V_S$ | 4.5 | -- | 5.5 | V |
| Supply Current (outputs ON)[5] | | $I_{S(ON)}$ | -- | 1 | 2 | mA |
| Supply Current (outputs OFF) [5] | | $I_{S(OFF)}$ | -- | 1 | 2 | mA |
| Minimum Reset Duration | | $t_{Reset,min}$ | 10 | -- | -- | µs |
| **2. Power Outputs** | | | | | | |
| ON Resistance $V_S$ = 5 V; $I_D$ = 500 mA | $T_J$ = 25°C<br>$T_J$ = 150°C | $R_{DS(ON)}$ | --<br>-- | 0.8<br>-- | 1<br>1.7 | Ω |
| Output Clamping Voltage | Output OFF | $V_{DS(AZ)}$ | 40 | -- | 55 | V |
| Current Limit | | $I_{D(lim)}$ | 1 | 1.5 | 2 | A |
| Output Leakage Current | $V_{Reset}$ = L<br>$V_{bb}$=12V | $I_{D(lkg)}$ | -- | -- | 5 | µA |
| Turn-On Time | $I_D$ = 0.5 A, resistive load | $t_{ON}$ | -- | 8 | 12 | µs |
| Turn-Off Time | $I_D$ = 0.5 A, resistive load | $t_{OFF}$ | -- | 6 | 10 | µs |
| **3. Digital Inputs** | | | | | | |
| Input Low Voltage | | $V_{INL}$ | - 0.3 | -- | 1.0 | V |
| Input High Voltage | | $V_{INH}$ | 2.0 | -- | -- | V |
| Input Voltage Hysteresis | | $V_{INHys}$ | 50 | 100 | 200 | mV |
| Input Pull Down/Up Current (IN1 ... IN4) | | $I_{IN(1..4)}$ | 20 | 50 | 100 | µA |
| PRG, Reset Pull Up Current | | $I_{IN(PRG,Res)}$ | 20 | 50 | 100 | µA |
| Input Pull Down Current (SI, SCLK) | | $I_{IN(SI,SCLK)}$ | 10 | 20 | 50 | µA |
| Input Pull Up Current ( $\overline{CS}$ ) | | $I_{IN(CS)}$ | 10 | 20 | 50 | µA |
| **4. Digital Outputs (SO, $\overline{FAULT}$ )** | | | | | | |
| SO High State Output Voltage | $I_{SOH}$ = 2 mA | $V_{SOH}$ | $V_S$ - 0.4 | -- | -- | V |
| SO Low State Output Voltage | $I_{SOL}$ = 2.5 mA | $V_{SOL}$ | -- | -- | 0.4 | V |
| Output Tri-state Leakage Current | $\overline{CS}$ = H, 0 ≤ $V_{SO}$ ≤ $V_S$ | $I_{SOlkg}$ | -10 | 0 | 10 | µA |
| FAULT Output Low Voltage | $I_{FAULT}$ = 1.6 mA | $V_{FAULTL}$ | -- | -- | 0.4 | V |

[4] For $V_S$ < 4.5V the power stages are switched according the input signals and data bits or are definitely switched off. This undervoltage reset gets active at $V_S$ = 3V (typ. value) and is guaranteed by design.
[5] For Reset = H.

## Electrical Characteristics cont.

| Parameter and Conditions<br>$V_S$ = 4.5 to 5.5 V ; $T_j$ = - 40 °C to + 150 °C ; Reset = H (unless otherwise specified) | Symbol | Values min | Values typ | Values max | Unit |
|---|---|---|---|---|---|
| **5. Diagnostic Functions** | | | | | |
| Open Load Detection Voltage | $V_{DS(OL)}$ | $V_S$ -2.5 | $V_S$ -2 | $V_S$ -1.3 | V |
| Output Pull Down Current | $I_{PD(OL)}$ | 50 | 90 | 150 | µA |
| Fault Delay Time | $t_{d(fault)}$ | 50 | 100 | 200 | µs |
| Short to Ground Detection Voltage | $V_{DS(SHG)}$ | $V_S$ –3.3 | $V_S$ -2.9 | $V_S$ -2.5 | V |
| Short to Ground Detection Current | $I_{SHG}$ | -50 | -100 | -150 | µA |
| Current Limitation; Overload Threshold Current | $I_{D(lim)\ 1...8}$ | 1 | 1.5 | 2 | A |
| Overtemperature Shutdown Threshold[6] | $T_{th(sd)}$ | 170 | -- | 200 | °C |
| Hysteresis[6] | $T_{hys}$ | -- | 10 | -- | K |
| **6. SPI-Timing** | | | | | |
| Serial Clock Frequency (depending on SO load) | $f_{SCK}$ | DC | -- | 5 | MHz |
| Serial Clock Period (1/fclk) | $t_{p(SCK)}$ | 200 | -- | -- | ns |
| Serial Clock High Time | $t_{SCKH}$ | 50 | -- | -- | ns |
| Serial Clock Low Time | $t_{SCKL}$ | 50 | -- | -- | ns |
| Enable Lead Time (falling edge of $\overline{CS}$ to rising edge of CLK) | $t_{lead}$ | 250 | -- | -- | ns |
| Enable Lag Time (falling edge of CLK to rising edge of $\overline{CS}$) | $t_{lag}$ | 250 | --- | -- | ns |
| Data Setup Time (required time SI to falling of CLK) | $t_{SU}$ | 20 | -- | -- | ns |
| Data Hold Time (falling edge of CLK to SI) | $t_H$ | 20 | -- | -- | ns |
| Disable Time @ $C_L$ = 50 pF[6] | $t_{DIS}$ | -- | -- | 150 | ns |
| Transfer Delay Time[7] ($\overline{CS}$ high time between two accesses) | $t_{dt}$ | 200 | -- | -- | ns |
| Data Valid Time $C_L$ = 50 pF[6] | $t_{valid}$ | -- | 110 | 160 | ns |
| $C_L$ = 100 pF[6] | | -- | 120 | 170 | |
| $C_L$ = 220 pF[6] | | -- | 150 | 200 | |

[6] This parameter will not be tested but guaranteed by design

[7] This time is necessary between two write accesses. To get the correct diagnostic information, the transfer delay time has to be extended to the maximum fault delay time $t_{d(fault)max}$ = 200µs.

# Functional Description

The TLE 6230 GP is an octal-low-side power switch which provides a serial peripheral interface (SPI) to control the 8 power DMOS switches, as well as diagnostic feedback. The power transistors are protected against short to $V_{BB}$, overload, overtemperature and against overvoltage by an active zener clamp.
The diagnostic logic recognizes a fault condition which can be read out via the serial diagnostic output (SO).

# Circuit Description

### Output Stage Control

Each output is independently controlled by an output latch and a common reset line, which disables all eight outputs. Serial data input (SI) is read on the falling edge of the serial clock. A logic high input data bit turns the respective output channel ON, a logic low data bit turns it OFF. $\overline{CS}$ must be low whilst shifting all the serial data into the device. A low-to-high transition of $\overline{CS}$ transfers the serial data input bits to the output buffer.

**Special conditions for Channel 1 to 4:**
In addition to the serial control of the outputs it is possible to control channel 1 to channel 4 directly in parallel for PWM applications. These inputs are high or low active (programmable via PRG pin) and ANDed with the SPI control bit.

The table shows the AND-operation of the parallel input pin (here active high) and the corresponding SPI bit. For an application where the parallel input is always "ON", it is possible to switch the channel OFF via the SPI bit, e.g. for diagnosis in OFF-state.

| IN 1 - 4 | SPI-Bit 0 - 3 | OUT 1 - 4 |
|---|---|---|
| 0 | 0 | OFF |
| 0 | 1 | OFF |
| 1 | 0 | OFF |
| 1 | 1 | ON |

⇒ **SPI Priority for OFF-state**

Operation with parallel inputs: Set SPI bits to logic high.
Operation via SPI: Connect parallel inputs to logic high (if programmed to active high).

**PRG** - Program pin. PRG = High ($V_S$): Parallel inputs Channel 1 to 4 are high active
PRG = Low (GND): Parallel inputs Channel 1 to 4 are low active.
If the parallel input pins are not connected (independent of high or low activity) it is guaranteed that the channels 1 to 4 are switched OFF.
PRG pin itself is internally pulled up when it is not connected.

**Power Transistor Protection Functions[8)]**

Each of the eight output stages has its own zener clamp, which causes a voltage limitation at the power transistor when solenoid loads are switched off. The outputs are provided with a current limitation set to a minimum of 1 A. The continuous current for each channel is 500 mA (all channels ON).
Each output is protected by embedded protection functions. In the event of an overload or short to supply, the current is internally limited and the corresponding bit combination is set (early warning). If this operation leads to an overtemperature condition, a second protection level (about 170 °C) will change the output into a low duty cycle PWM (selective thermal shut-down with restart) to prevent critical chip temperatures.

## SPI Signal Description

**$\overline{\text{CS}}$** - Chip Select. The system microcontroller selects the TLE 6230 GP by means of the $\overline{\text{CS}}$ pin. Whenever the pin is in a logic low state, data can be transferred from the µC and vice versa.

**$\overline{\text{CS}}$ High to Low transition:**
- diagnostic status information is transferred from the power outputs into the shift register.
- serial input data can be clocked in from then on
- SO changes from high impedance state to logic high or low state corresponding to the SO bits

**$\overline{\text{CS}}$ Low to High transition:**
- transfer of SI bits from shift register into output buffers
- reset of diagnosis register

To avoid any false clocking the serial clock input pin SCLK should be logic low state during high to low transition of $\overline{\text{CS}}$. When $\overline{\text{CS}}$ is in a logic high state, any signals at the SCLK and SI pins are ignored and SO is forced into a high impedance state.

**SCLK** - Serial Clock. The system clock pin clocks the internal shift register of the TLE 6230 GP. The serial input (SI) accepts data into the input shift register on the falling edge of SCLK while the serial output (SO) shifts diagnostic information out of the shift register on the rising edge of serial clock. It is essential that the SCLK pin is in a logic low state whenever chip select $\overline{\text{CS}}$ makes any transition. The number of clock pulses will be counted during a chip select cycle. The received data will only be accepted, if exactly 16 clock pulses were counted during $\overline{\text{CS}}$ is active.

**SI** - Serial Input. Serial data bits are shifted in at this pin, the most significant bit first. SI information is read in on the falling edge of SCLK. Input data is latched in the shift register and then transferred to the control buffer of the output stages.
The input data consists of two bytes - a "control byte" followed by a "data byte". The control byte contains the information as to whether the data byte will be accepted or ignored (see diagnostics section). The data byte contains the input information for the eight channels. A logic

[8)] The integrated protection functions prevent an IC destruction under fault conditions and may not be used in normal operation or permanently

high level at this pin (within the data byte) will switch on the power switch, provided that the corresponding parallel input is also switched on (AND-operation for channel 1 to 4).
**SO** - Serial Output. Diagnostic data bits are shifted out serially at this pin, the most significant bit first. SO is in a high impedance state until the $\overline{CS}$ pin goes to a logic low state. New diagnostic data will appear at the SO pin following the rising edge of SCLK.

**$\overline{RESET}$** - Reset pin. If the reset pin is in a logic low state, it clears the SPI shift register and switches all outputs OFF. An internal pull-up structure is provided on chip.

## Diagnostics

**$\overline{FAULT}$** - Fault pin. There is a general fault pin (open drain) which shows a high to low transition as soon as an error occurs for any one of the eight channels. This fault indication can be used to generate a µC interrupt. Therefore a 'diagnosis' interrupt routine need only be called after this fault indication. This saves processor time compared to a cyclic reading of the SO information.

As soon as a fault occurs, the fault information is latched into the diagnosis register. A new error will over-write the old error report. Serial data out pin (SO) is in a high impedance state when $\overline{CS}$ is high. If $\overline{CS}$ receives a LOW signal, all diagnosis bits can be shifted out serially. The rising edge of $\overline{CS}$ will reset all error registers.

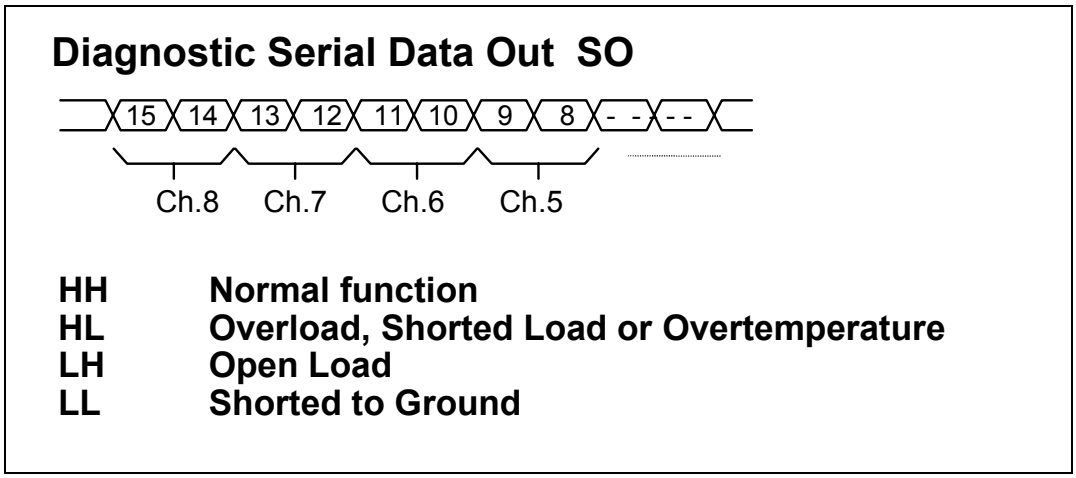



**Figure 1: Two bits per channel diagnostic feedback**
There are two diagnostic bits per channel configured as shown in Figure 1.

**Normal function:** The bit combination **HH** indicates that there is no fault condition, i.e. normal function.
**Overload, Short Circuit to Battery (SCB) or Overtemperature: HL** is set when the current limitation gets active, i.e. there is a overload, short to supply or overtemperature condition.
**Open load:** An open load condition is detected when the drain voltage decreases below 3 V (typ.). **LH** bit combination is set.
**Short Circuit to GND:** If a drain to ground short circuit exists and the drain to ground current exceeds 100 µA, short to ground is detected and the **LL** bit combination is set.

A definite distinction between open load and short to ground is guaranteed by design.

The standard way of obtaining diagnostic information is as follows:
Clock in serial information into SI pin and wait approximately 150 µs to allow the outputs tosettle. Clock in the identical serial information once again - during this process the data coming out at SO contains the bit combinations representing the diagnosis conditions as described in figure 1.

By means of the control byte it is possible either to:

a) control the eight outputs according to the data byte, as well as being able to read the diagnostic information

or b) purely get diagnostic information without changing the state of the outputs.

a) Serial Control of Outputs

**HHHHHHHH** (Control Byte) **LHLHHLLL** (Data Byte) : Serial input information

Control byte is set to FFhex: Data byte will be accepted. The outputs will be switched ON or OFF according to the information of the data byte and the parallel inputs (Channel 1 to 4 because of AND operation).
All other control words except the one for 'Diagnosis Only = 00hex' will also be accepted as a valid control word and the data will be accepted.
Example: HLLHLHLH DDDDDDDD: Outputs will switch according to the data bits.

b) Diagnosis Only

**LLLLLLLL** (Control Byte) **XXXXXXXX** (Data Byte) : Serial input information

Control byte is set to 00hex: Data byte will be ignored. Diagnostic information can be read out at any time with no change of the switching conditions. Only 00hex means 'Diagnosis Only'.

## Timing Diagrams

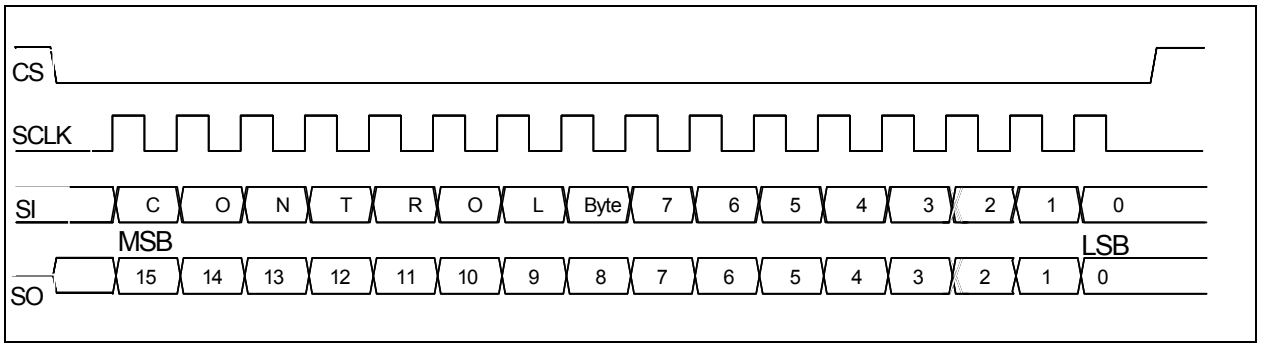



**Figure 2: Serial Interface**

**Figure 3: Input Timing Diagram**

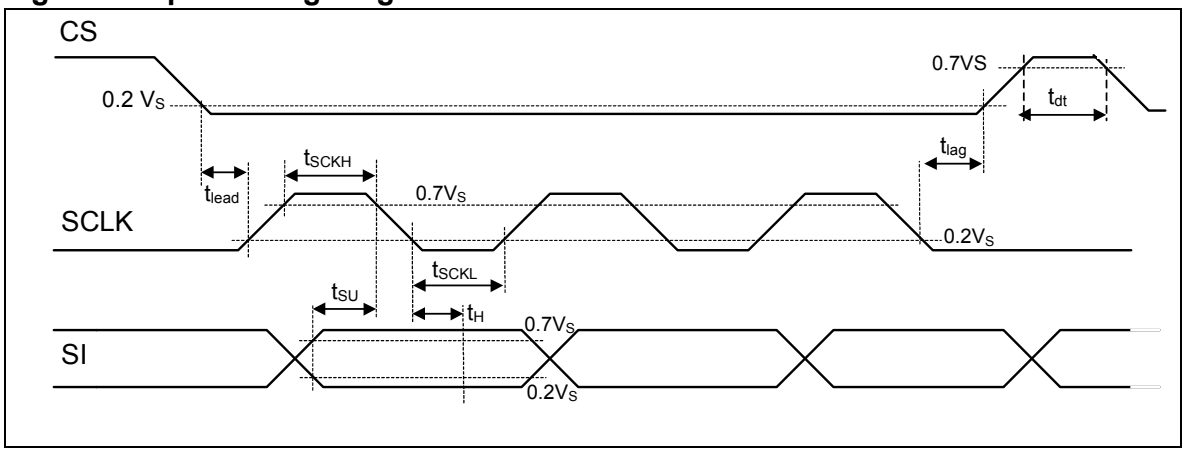
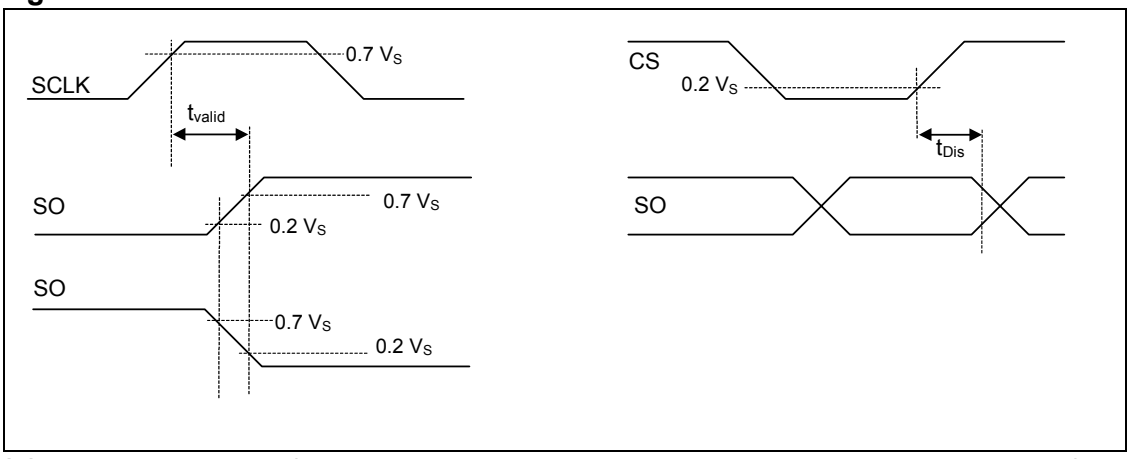



**Figure 4:**




**SO Valid Time Waveforms** **Enable and Disable Time Waveforms**

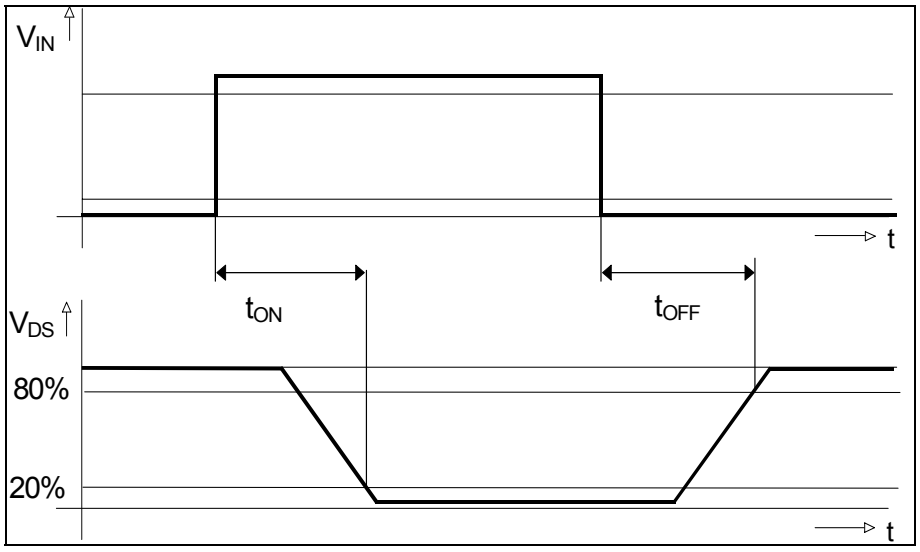
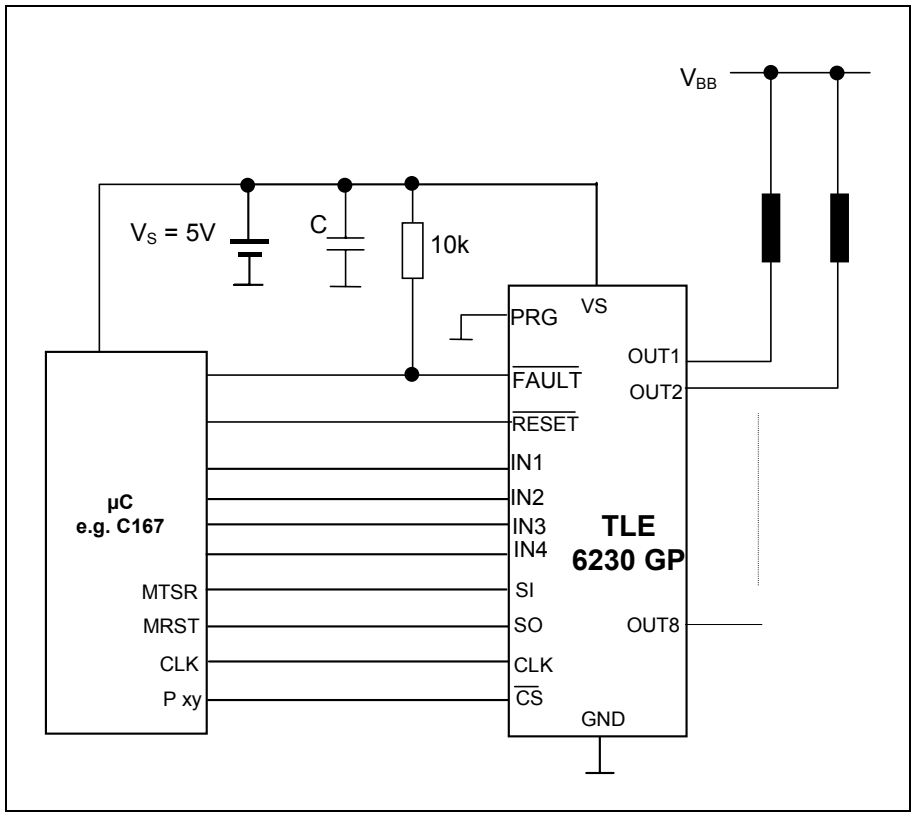



**Figure 5: Power Outputs**
Timing is valid for resistive load with parallel and serial control.
Rising edge of chip select initiates the switching

## Application Circuits



# Typical electrical Characteristics

## Drain-Source on-resistance

$R_{DS(ON)} = f(T_j)$ ; $V_s = 5V$

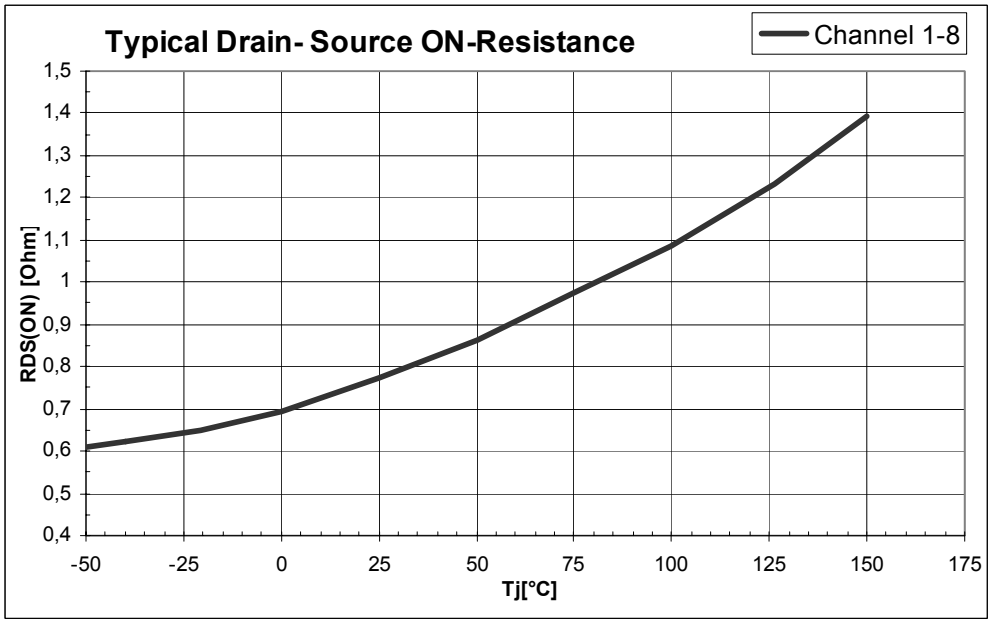



**Figure 6 :** Typical ON Resistance versus Junction-Temperature
Channel 1-8

## Output Clamping Voltage

$V_{DS(AZ)} = f(T_j)$ ; $V_s = 5V$

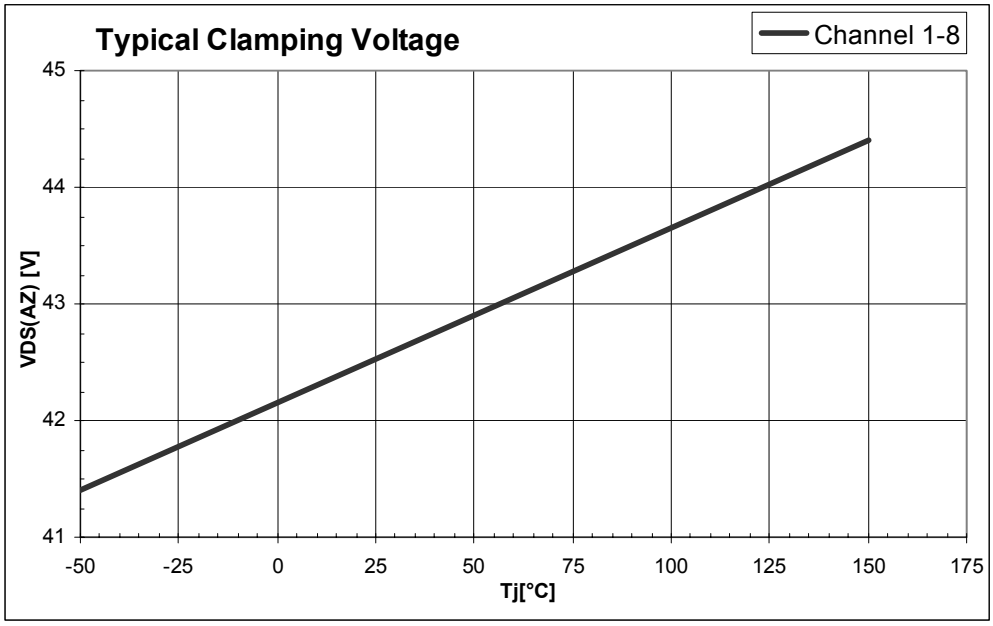



**Figure 7 :** Typical Clamp Voltage versus Junction-Temperature
Channel 1-8

## Maximum single clamp Energy

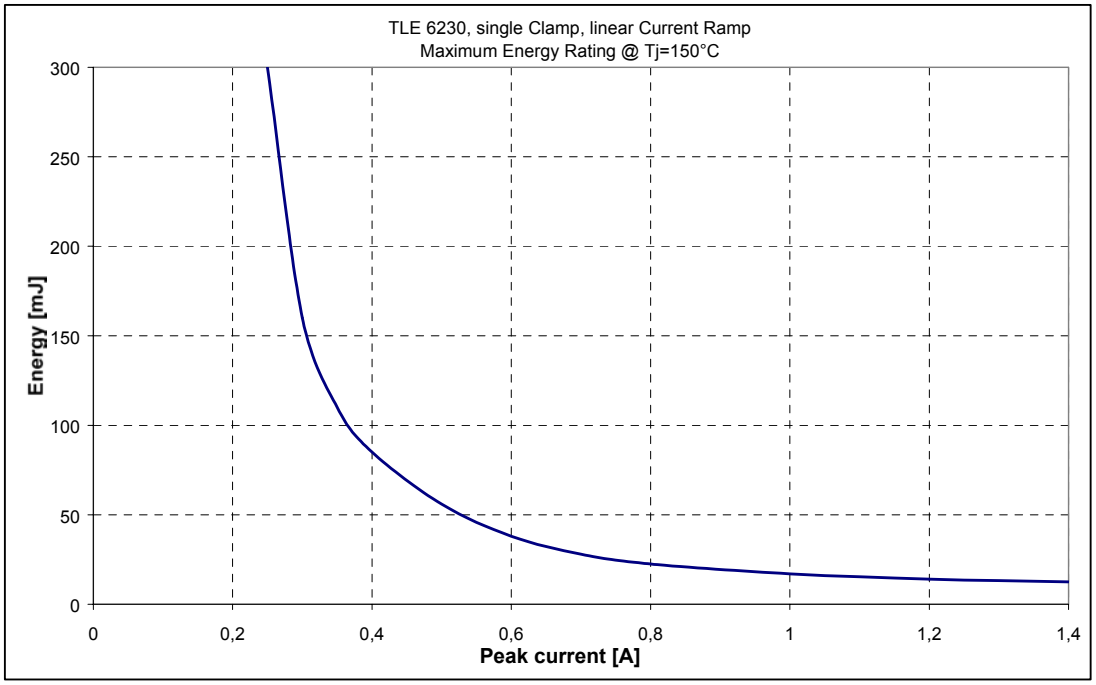
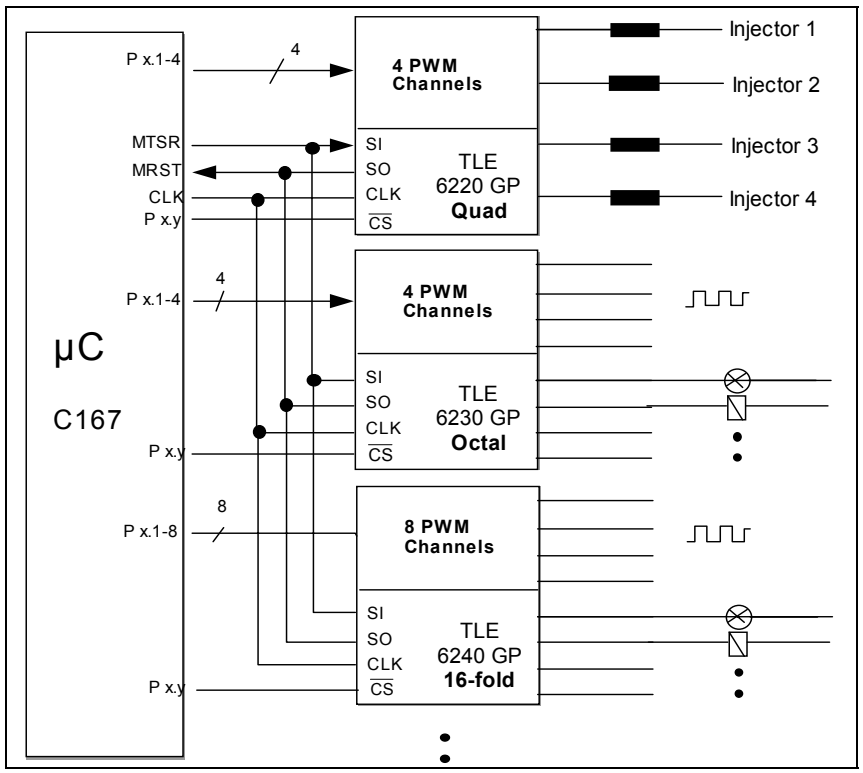



**Figure 8 :** Maximum Clamp Energy (single event) versus Peak Current Channel 1-8

## Parallel SPI Configuration




### Engine Management Application

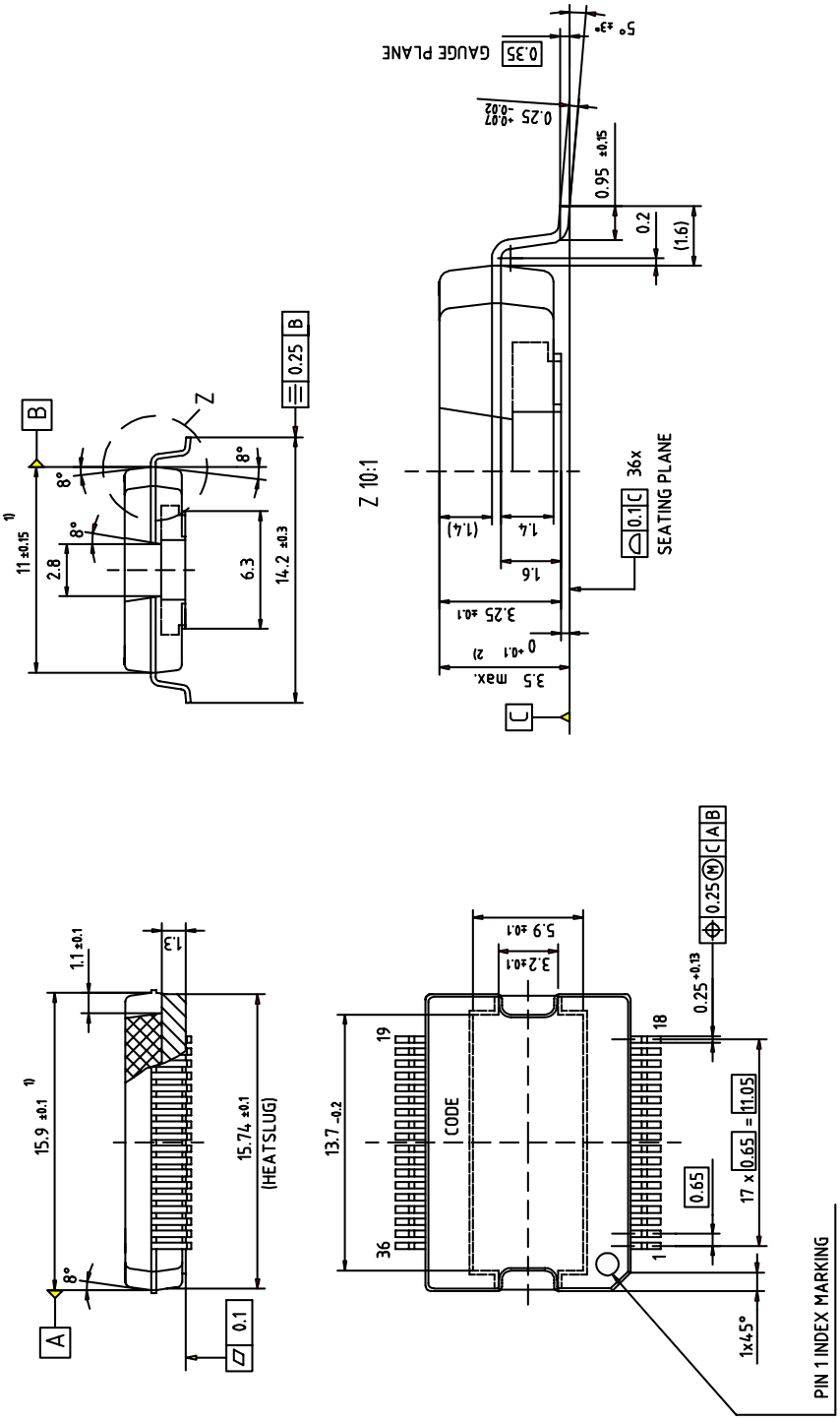
TLE 6230 GP in combination with TLE 6240 GP (16-fold switch) for relays and general purpose loads and TLE 6220 GP (quad switch) to drive the injector valves. This arrangement covers the numerous loads to be driven in a modern Engine Management/Powertrain system. From 28 channels in sum 16 can be controlled direct in parallel for PWM applications.

# Package and Ordering Code

**(all dimensions in mm)**

**PG-DSO 36**

TLE 6230 GP



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