Sine-wave Driving, High Voltage 3-phase Motor Driver with Built-in Hall Amplifiers

SIM2602M

Data Sheet

Description

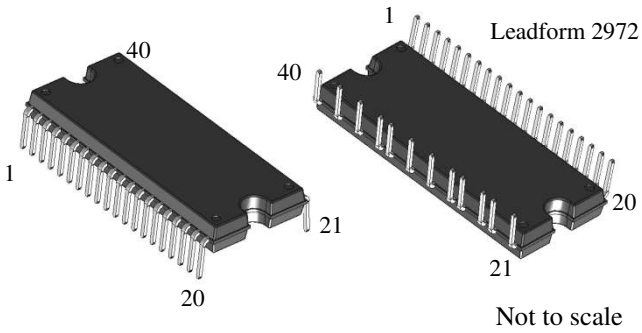
The SIM2602M is high voltage 3-phase motor driver driven by a sinusoidal control, which can support Hall element and Hall IC inputs, thus offering high-efficient yet low-noise motor control. Supplied in a highly heat-dissipating DIP package, where a controller, a gate driver, the output transistors of three phases, and bootstrap diodes are highly integrated, the SIM2602M requires only a few external components for building a motor driver. This also allows a motor driver to be highly reliable in performance and design-friendly with its compactness. These products can optimally control the inverter systems of low- to medium-capacity motors that require universal input standards.

Features

- Pb-free (RoHS Compliant)
- Isolation Voltage: 1500 V (for 1 min)
  UL-recognized Component (File No.: E118037)
- Low Noise, High Efficiency
  (Sinusoidal Current Waveform)
- Reduced Number of Parts Achieved by Built-in Bootstrap Diodes
- Hall Element and Hall IC Inputs
- Application-specific Optimal Settings with External Signals:
  - Motor Speed
  - Phase Adavance Angle
  - Motor Direction
  - User-settable Motor Lock Detection (Enabled or Disabled)
- 5 V Reference Voltage Output
  (Used for Driving Hall Elements etc.)
- Fault Signal Output at Protection Activation (FO Pin)
- Protections Include:
  - VREG Pin Undervoltage Lockout (UVLO_REG)
  - Undervoltage Lockout for Power Supplies
    VBx Pin (UVLO_VB)
    VCC Pin (UVLO_VCC)
  - Overcurrent Limit (OCL)
  - Overcurrent Protection (OCP)
  - Thermal Shutdown (TSD)
  - Motor Lock Protection (MLP)
  - Reverse Rotation Detection
  - Hall Signal Abnormality Detection

Package

DIP40
Mold Dimensions: 36.0 mm × 14.8 mm × 4.0 mm



Not to scale

Specifications

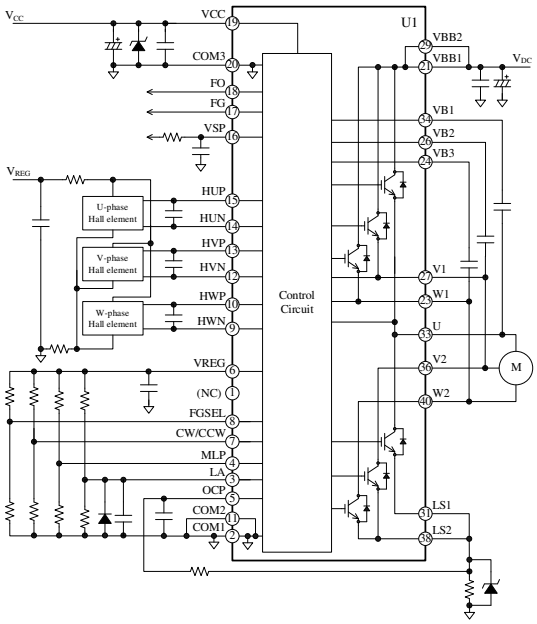
- Breakdown Voltage: 600 V
- I_O: 5.0 A
- Output Transistor: IGBT + FRD

Applications

For motor drives such as:

- Fan Motor and Pump Motor for Washer and Dryer
- Fan Motor for Air Conditioner
- Fan Motor for Air Purifier and Electric Fan

Typical Application



Contents

1. Absolute Maximum Ratings

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−).

Unless specifically noted, T_A = 25 °C, COM1 = COM2 = COM3 = COM.

Parameter	Symbol	Conditions	Rating	Unit
Main Supply Voltage (DC)	V_{DC}	VBBx–LSx	450	V
Main Supply Voltage (Surge)	$V_{DC(SURGE)}$	VBBx–LSx	500	V
IGBT Breakdown Voltage	V_{CES}	I_C = 1 mA	600	V
Logic Supply Voltage	V_{CC}	VCC–COM	20	V
	V_{BS}	VB1–U, VB2–V1, VB3–W1	20	V
Output Current (DC)(1)	I_O	T_C = 25 °C, T_J < 150 °C	5.0	A
Output Current (Pulse)	I_{OP}	T_C = 25 °C, pulse width ≤ 100 µs	7.5	A
VREG Pin Output Voltage	V_{REG}		5.5	V
VREG Pin Current	I_{REG}		30	mA
Input Voltage 1 (HUP, HUN, HVP, HVN, HWP, HWN)	$V_{IN(1)}$		−0.5 to V_{REG}	V
Input Voltage 2 (LA, MLP, OCP, CW/CCW, FGSEL)	$V_{IN(2)}$		−0.5 to V_{REG}	V
Input Voltage 3 (VSP)	$V_{IN(3)}$		−0.5 to 10	V
Output Voltage (FG, FO)	V_O		−0.5～V_{REG}	V
LSx Pin Voltage (DC)	$V_{LS(DC)}$	LSx–COM	−0.7 to 7	V
LSx Pin Voltage (Surge)	$V_{LS(SURGE)}$	LSx–COM	−4 to 7	V
Operating Case Temperature(2)	$T_{C(OP)}$		−30 to 100	°C
Junction Temperature(3)	T_J		150	°C
Storage Temperature	T_{STG}		−40 to 150	°C

(1) Should be derated depending on an actual case temperature. See Section 14.4.
(2) Refers to a case temperature measured during IC operation.
(3) Refers to the junction temperature of each chip built in the IC, including the control stage, gate drive stage, and output transistors.

2. Recommended Operating Conditions

Unless specifically noted, COM1 = COM2 = COM3 = COM.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Main Supply Voltage	V_{DC}	VBBx–LSx	—	300	400	V
Logic Supply Voltage	V_{CC}	VCC–COM	13.5	—	16.5	V
	V_{BS}	VB1–U, VB2–V, VB3–W1	13.5	—	16.5	V
Input Voltage 1 (HUP, HUN, HVP, HVN, HWP, HWN)	$V_{IN(1)}$		0	—	5.0	V
Input Voltage 2 (MLP, CW/CCW, FGSEL)	$V_{IN(2)}$		0	—	5.0	
Input Voltage 3 (VSP)	$V_{IN(3)}$		0	—	5.4	V
FO Pin Noise Filter Capacitor	C_{FO}		0.001	—	0.01	µF
Bootstrap Capacitor	C_B		1	—	—	µF
Shunt Resistor*	R_S	$I_{OP} \leq 7.5$ A	88	—	—	mΩ
RC Filter Resistor	R_O		—	—	100	Ω
RC Filter Capacitor	C_O		100	—	2200	pF
Operating Case Temperature	$T_{C(OP)}$		—	—	100	°C

* Should be a low-inductance resistor.

3. Electrical Characteristics

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−).

Unless specifically noted, T_A = 25 °C, V_{CC} = 15 V, COM1 = COM2 = COM3 = COM.

3.1 Characteristics of Control Parts

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power Supply Operation						
Low-side Logic Operation Start Voltage	$V_{CC(ON)}$	VCC–COM	10.5	11.5	12.5	V
Low-side Logic Operation Stop Voltage	$V_{CC(OFF)}$		10.0	11.0	12.0	V
High-side Logic Operation Start Voltage	$V_{BS(ON)}$	VB1–U, VB2–V1, VB3–W1	9.5	10.5	11.5	V
High-side Logic Operation Stop Voltage	$V_{BS(OFF)}$		9.0	10.0	11.0	V
Logic Supply Current	I_{CC}	V_{SP} = 5.4 V, I_{REG} = 0 A	—	5.5	—	mA
	I_{BS}	V_{Bx} = 15 V, V_{SP} = 5.4 V; VBx pin current in 1-phase operation	40	140	350	µA
VREG Pin Output Voltage	V_{REG}	I_{REG} = 0 mA to 30 mA	4.5	5.0	5.5	V
Input Signal(1)						
Input Threshold Voltage (MLP, FGSEL, CW/CCW)	V_{TH}		2.25	2.50	2.75	V
High Level Input Current 1 (LA, MLP, CW/CCW, FGSEL, VSP)	I_{IH1}	V_{IN} = V_{REG}	—	25	100	µA
Low Level Input Current 1 (LA, MLP, CW/CCW, FGSEL, VSP)	I_{IL1}	V_{INL} = 0 V	—	—	2	µA
High Level Input Current 2 (OCP)	I_{IH2}	V_{IN} = V_{REG}	−5	—	5	µA
Low Level Input Current 2 (OCP)	I_{IL2}	V_{INL} = 0 V	—	23	90	µA
High Level Input Current 3 (HUP, HUN, HVP, HVN, HWP, HWN)	I_{IH3}	V_{IN} = V_{REG}	−5	—	5	µA
Low Level Input Current 3 (HUP, HUN, HVP, HVN, HWP, HWN)	I_{IL3}	V_{INL} = 0 V	−5	—	5	µA
High Level Output Voltage (FG, FO)	V_{OH}		4.5	—	5.5	V
Low Level Output Voltage (FG, FO)	V_{OL}		—	—	0.5	V

(1) Guaranteed by design.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
PWM Control						
PWM Carrier Frequency(2)	f_C		16	17	18	kHz
Internal Oscillator Frequency(2)	f_{OSC}		4.10	4.32	4.54	MHz
Dead Time(2)	t_D		—	1.2	—	µs
Control IC Output Pulse Duty Cycle (Low-side) (2)	D	V_{SP} = 1.5 V; with bootstrap capacitors being charged	—	6.3	—	%
Control IC Output Pulse Duty Cycle (High-side) (2)	D	V_{SP} = 2.0 V	—	0	3	%
		V_{SP} = 3.7 V	47	50	53	%
		V_{SP} = 5.0 V (driven by trapezoidal control)	85.0	—	88.9	%
		V_{SP} = 5.4 V (driven by sinusoidal control)	93.7	—	100	%
Protection						
OCL Threshold Voltage	V_{LIM}		0.25	0.30	0.35	V
OCL Blanking Time	$t_{BK(OCL)}$		—	2.3	4.5	µs
OCP Threshold Voltage	V_{TRIP}		0.54	0.60	0.66	V
OCP Blanking Time	$t_{BK(OCP)}$		—	0.8	1.7	µs
OCP Hold Time	t_P		—	15	—	ms
MLP Detection Time	t_{LD}		—	5	—	s
MLP Hold Time	t_{LH}		—	64	—	s
TSD Operating Temperature(3)	T_{DH}	I_{REG} = 0 mA; without heatsink	—	130	—	°C
TSD Hysteresis Temperature(3)	$T_{D(HYS)}$		—	30	—	°C
VREG Pin Undervoltage Lockout Operating Voltage(2)	V_{UVRL}		3.24	3.60	3.96	V
VREG Pin Undervoltage Lockout Releasing Voltage(2)	V_{UVRH}		3.60	4.00	4.40	V

(2) Refers to an internal signal; guaranteed by design.
(3) Refers to the junction temperature of the gate drive stage.

3.2 Bootstrap Diode Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Bootstrap Diode Leakage Current	I_{LBD}	V_R = 600 V	—	—	100	µA
Bootstrap Diode Forward Voltage	V_{FB}	I_{FB} = 10 mA; voltage drop in R_{BOOT} included	—	3.0	—	V

3.3 Transistor Characteristics

Figure 3-1 provides the definitions of switching characteristics described in this and the following sections. Internal signals, HINx and LINx, are defined as V_{IN} (see Section 6).

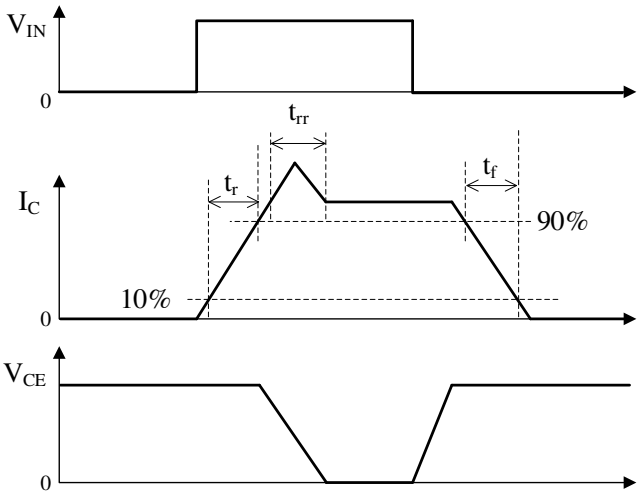


Figure 3-1. Switching Characteristics Definitions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Collector-to-Emitter Leakage Current	I_{CES}	V_{CE} = 600 V, V_{IN} = 0 V	—	—	1	mA
Collector-to-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 5.0 A, V_{IN} = 5 V	—	1.75	2.2	V
Diode Forward Voltage	V_F	I_F = 5.0 A, V_{IN} = 0 V	—	2.0	2.4	V
High-side Switching						
Source-to-Drain Diode Reverse Recovery Time*	t_{rr}	V_{DC} = 300 V, I_C = 5.0 A, V_{IN} = 0→5 V or 5→0 V, T_J = 25 °C, inductive load	—	100	—	ns
Rise Time*	t_r		—	110	—	ns
Fall Time*	t_f		—	210	—	ns
Low-side Switching						
Source-to-Drain Diode Reverse Recovery Time*	t_{rr}	V_{DC} = 300 V, I_C = 5.0 A, V_{IN} = 0→5 V or 5→0 V, T_J = 25 °C, inductive load	—	100	—	ns
Rise Time*	t_r		—	110	—	ns
Fall Time*	t_f		—	210	—	ns

* Guaranteed by design.

3.4 Thermal Resistance Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Junction-to-Case Thermal Resistance[1]	$R_{(J-C)Q}$[2]	All IGBTs operating	—	—	3.6	°C/W
	$R_{(J-C)F}$[3]	All freewheeling diodes operating	—	—	4.2	°C/W
Junction-to-Ambient Thermal Resistance	$R_{(J-A)Q}$	All IGBTs operating	—	—	25	°C/W
	$R_{(J-A)F}$	All freewheeling diodes operating	—	—	29	°C/W

[1] Refers to a case temperature at the measurement point described in Figure 3-2.
[2] Refers to steady-state thermal resistance between the junction of the built-in transistors and the case. For transient thermal characteristics, see Section 14.1.
[3] Refers to steady-state thermal resistance between the junction of the built-in freewheeling diodes and the case.

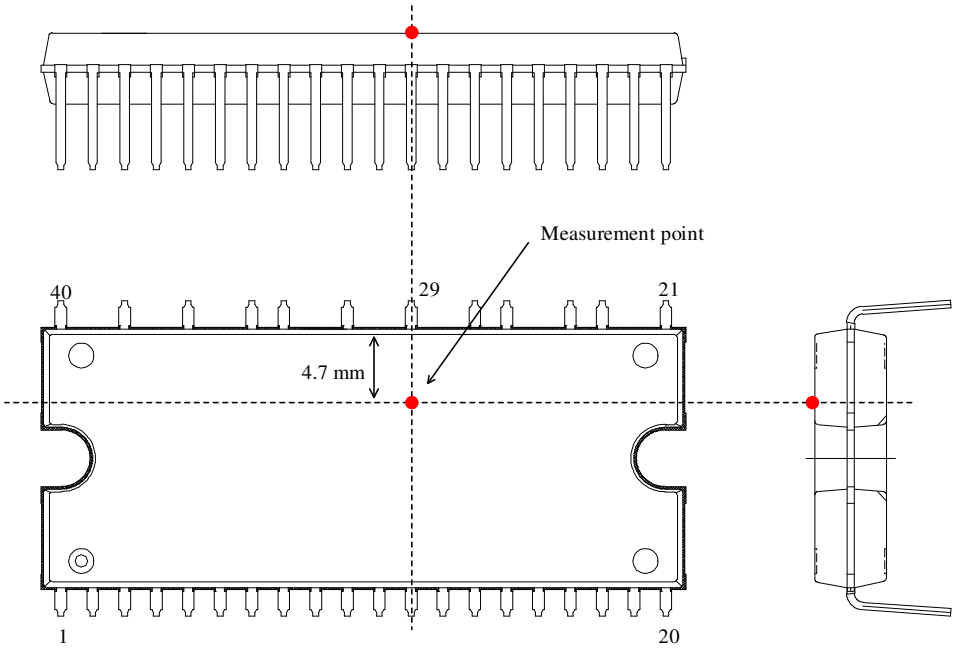


Figure 3-2. Case Temperature Measurement Point

4. Mechanical Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Unit	Remarks
Heatsink Mounting Screw Torque	*	0.294	—	0.441	N·m	
Flatness of Heatsink Attachment Area	See Figure 4-1.	0	—	100	μm	
Package Weight		—	5.2	—	g	

* Requires using a metric screw of M2.5 and a plain washer of 6.0 mm (φ). For more on screw tightening, see Section 12.3.

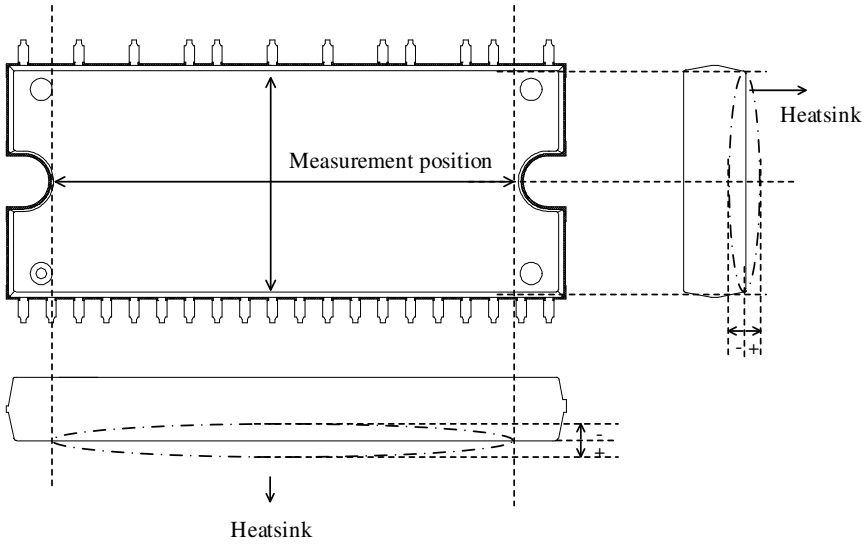


Figure 4-1. Flatness Measurement Position

5. Insulation Distance

Parameter	Conditions	Min.	Typ.	Max.	Unit	Remarks
Clearance	Between heatsink* and leads. See Figure 5-1.	1.5	—	2.1	mm	
Creepage		1.7	—	—	mm	

* Refers to when a heatsink to be mounted is flat. If your application requires a clearance exceeding the maximum distance given above, use an alternative (e.g., a convex heatsink) that will meet the target requirement.

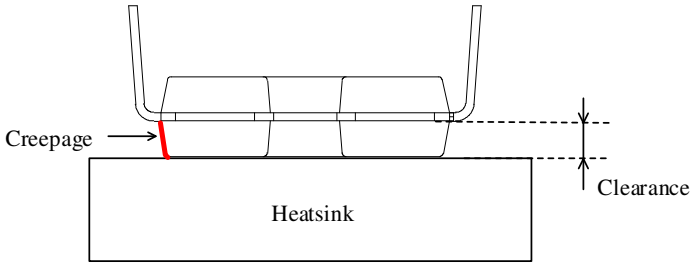


Figure 5-1. Insulation Distance Definitions

6. Block Diagrams

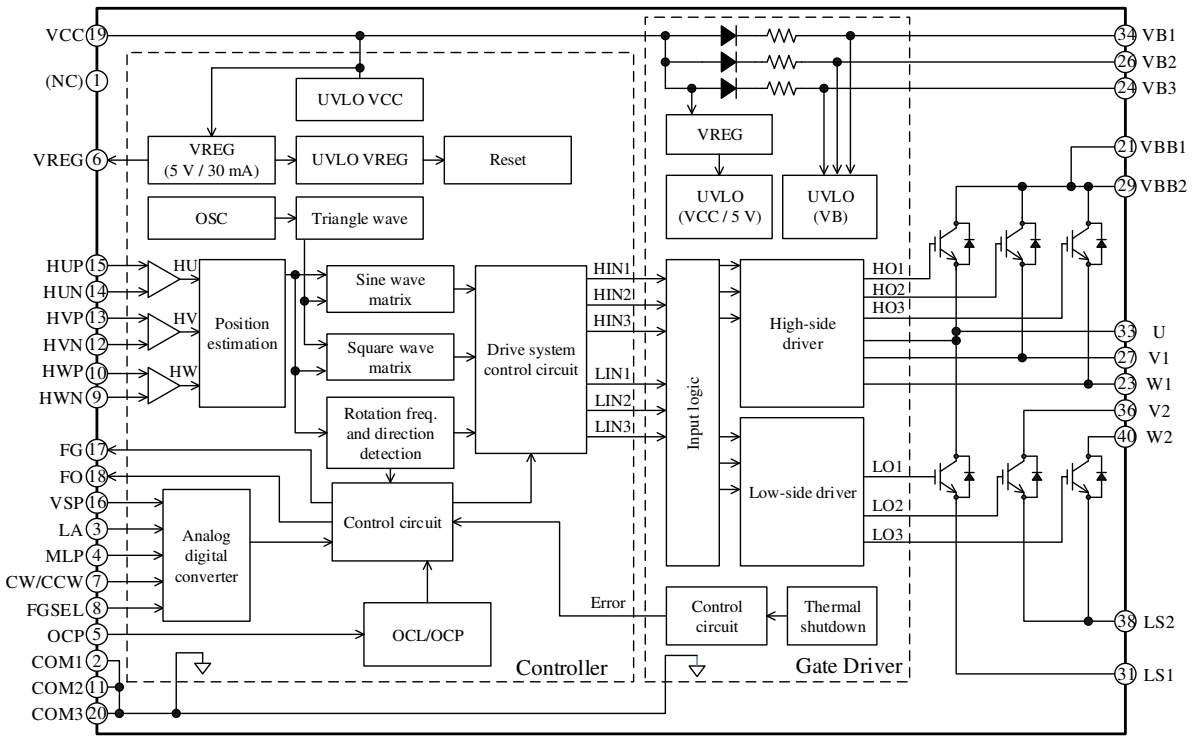
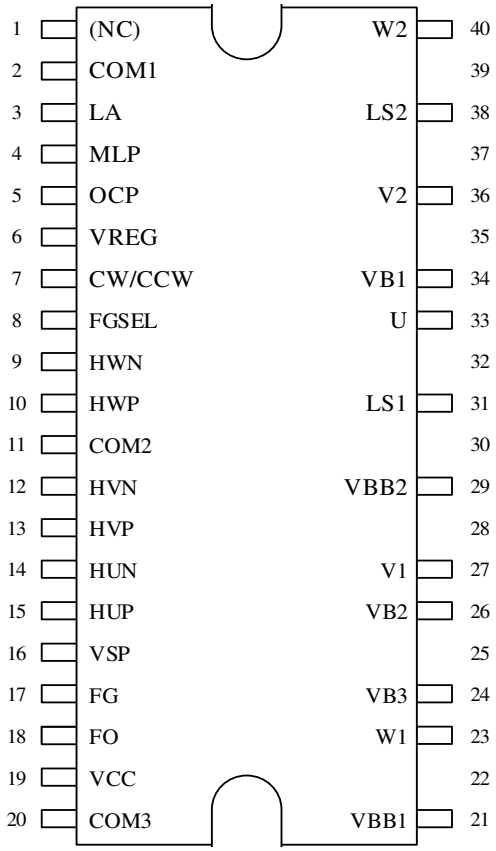


Figure 6-1. Block Diagram

7. Pin Configuration Definitions

Top View



Pin Number	Pin Name	Description
1	NC	(No connection)
2	COM1	Logic ground
3	LA	Input for phase advance angle setting signal
4	MLP	Setting pin to enable or disable the motor lock protection
5	OCP	Input for overcurrent detection signal
6	VREG	Internal regulator output
7	CW/CCW	Input for motor direction setting signal
8	FGSEL	Input for FG pin setting signal
9	HWN	W-phase Hall element negative signal input (−)
10	HWP	W-phase Hall element positive signal input (+)
11	COM2	Logic ground
12	HVN	V-phase Hall element negative signal input (−)
13	HVP	V-phase Hall element positive signal input (+)
14	HUN	U-phase Hall element negative signal input (−)
15	HUP	U-phase Hall element positive signal input (+)
16	VSP	Input for motor speed control signal
17	FG	Rotation pulse signal output
18	FO	Fault signal output
19	VCC	Input for logic supply voltage
20	COM3	Logic ground
21	VBB1	Positive DC bus supply voltage (+)
22	—	Pin removed
23	W1	W-phase output (connected to W2 externally)
24	VB3	W-phase high-side floating supply voltage input
25	—	Pin removed
26	VB2	V-phase high-side floating supply voltage input
27	V1	V-phase output (connected to V2 externally)
28	—	Pin removed
29	VBB2	Positive DC bus supply voltage (+)
30	—	Pin removed
31	LS1	U-phase low-side IGBT emitter (connected to L2 externally)
32	—	Pin removed
33	U	U-phase output
34	VB1	U-phase high-side floating supply voltage input
35	—	Pin removed
36	V2	V-phase output (connected to V1 externally)
37	—	Pin removed
38	LS2	V-/W- phases low-side IGBT emitter (connected to L1 externally)
39	—	Pin removed
40	W2	W-phase output (connected to W1 externally)

8. Typical Applications

Figure 8-1 is a typical application which uses signals input from the Hall elements; Figure 8-2 is a typical application which uses signals input from Hall ICs.

CR filters and Zener diodes should be added to your application as needed. This is to protect each pin against surge voltages causing malfunctions, and to avoid the IC being used under the conditions exceeding the absolute maximum ratings where critical damage is inevitable. Then, check all the pins thoroughly under actual operating conditions to ensure that your application works flawlessly.

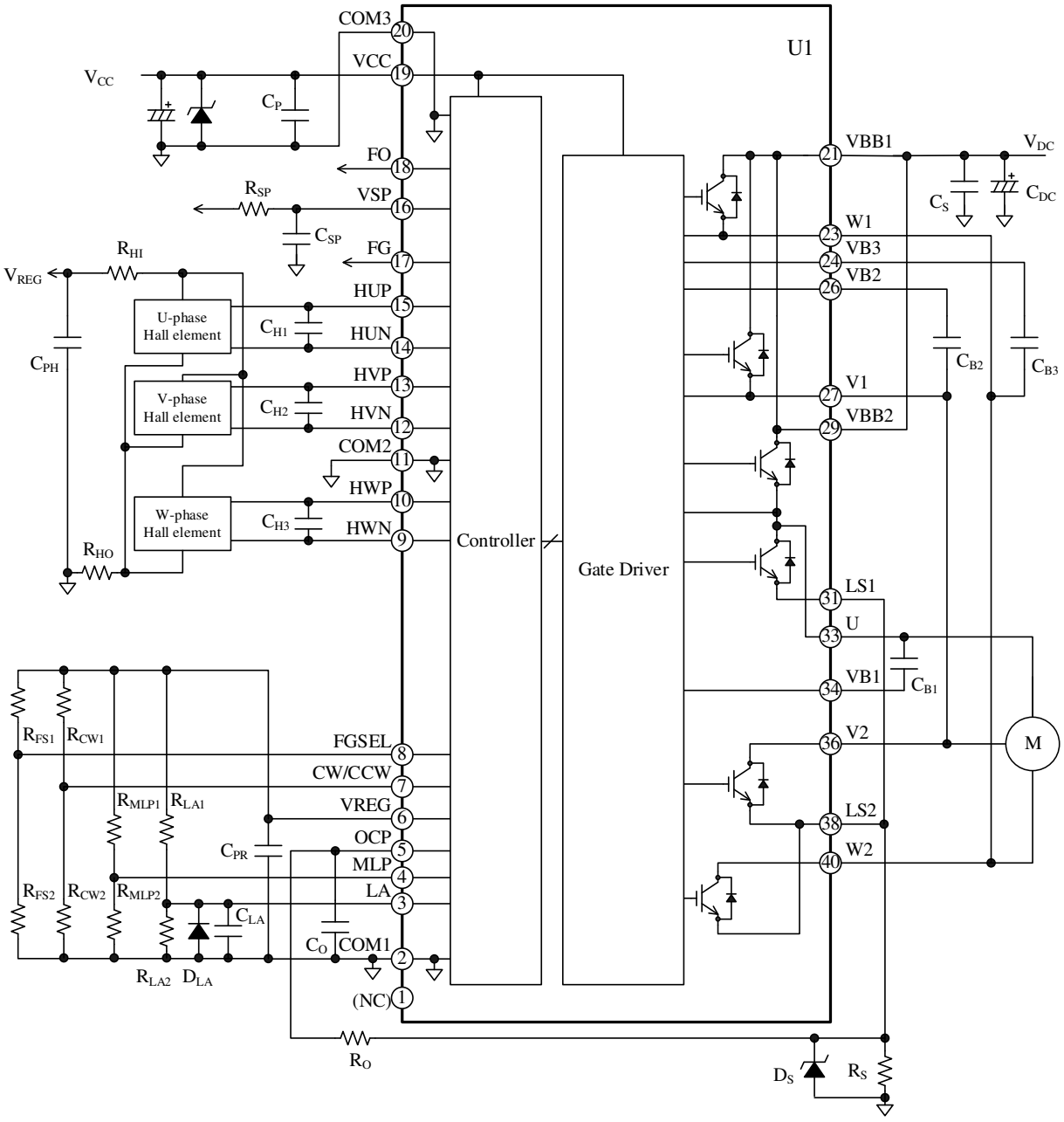


Figure 8-1. Application Using Signals Input from Hall Elements

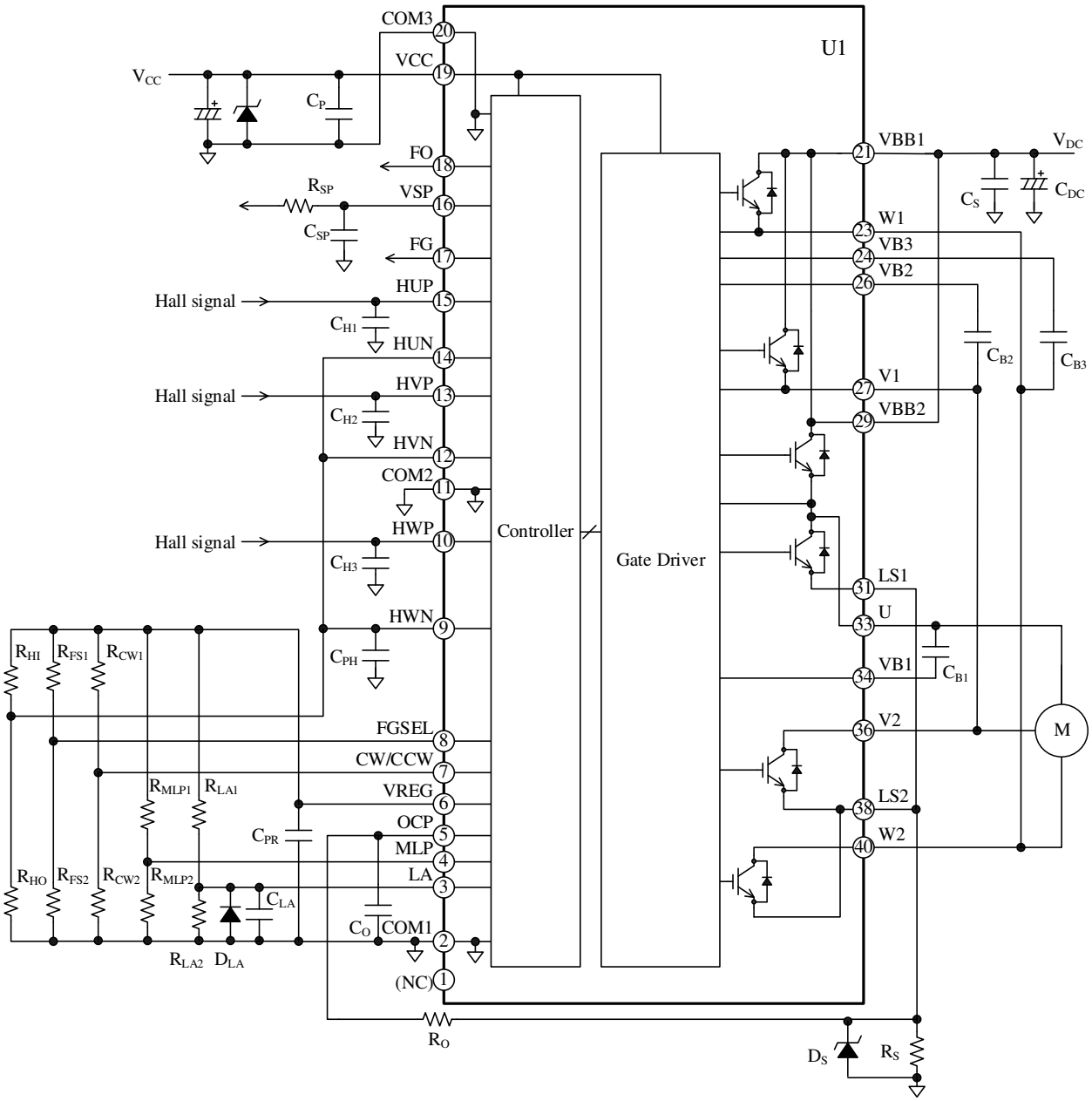
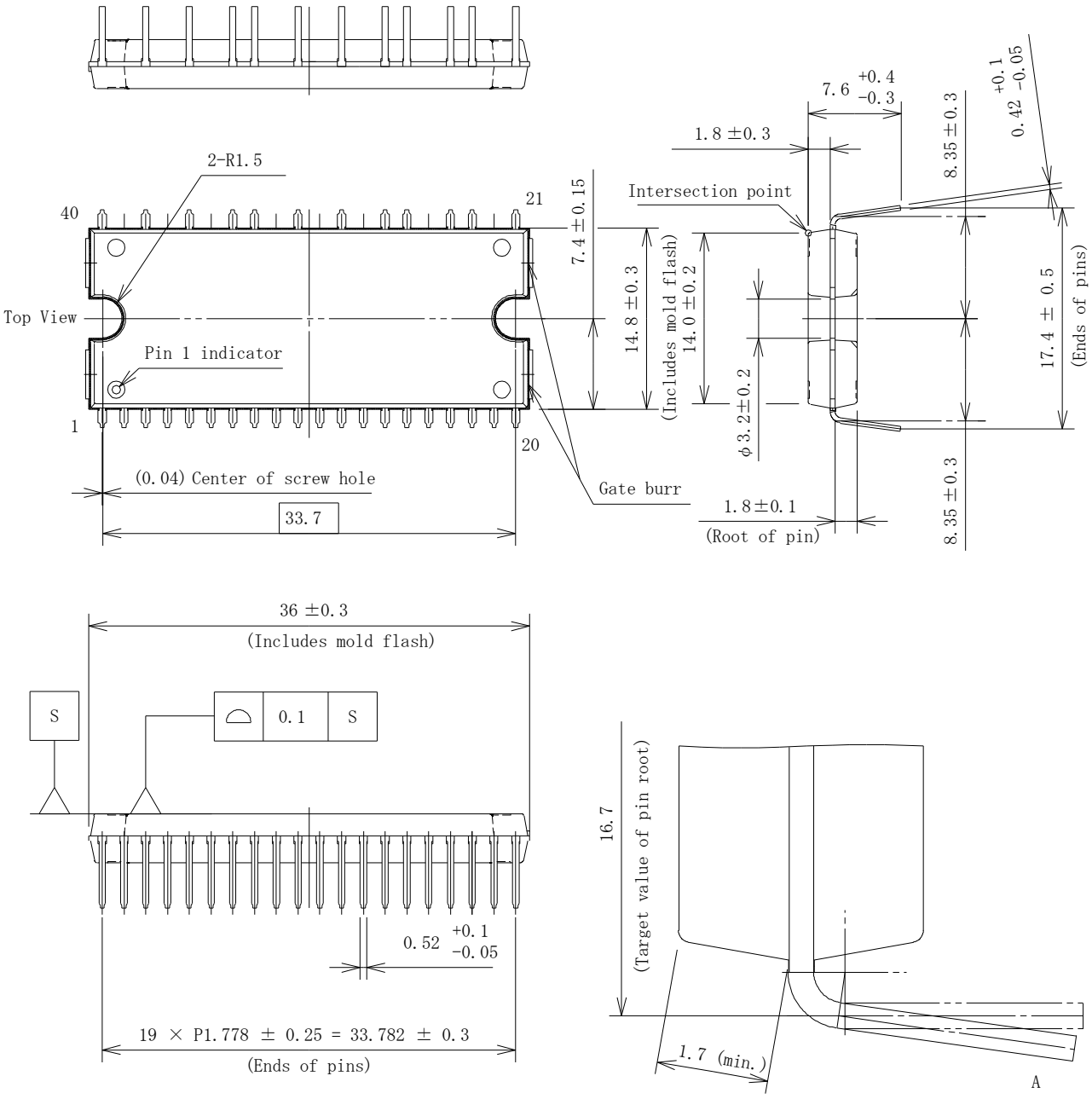


Figure 8-2. Application Using Signals Input from Hall ICs

9. Physical Dimensions

● **DIP40 Package**

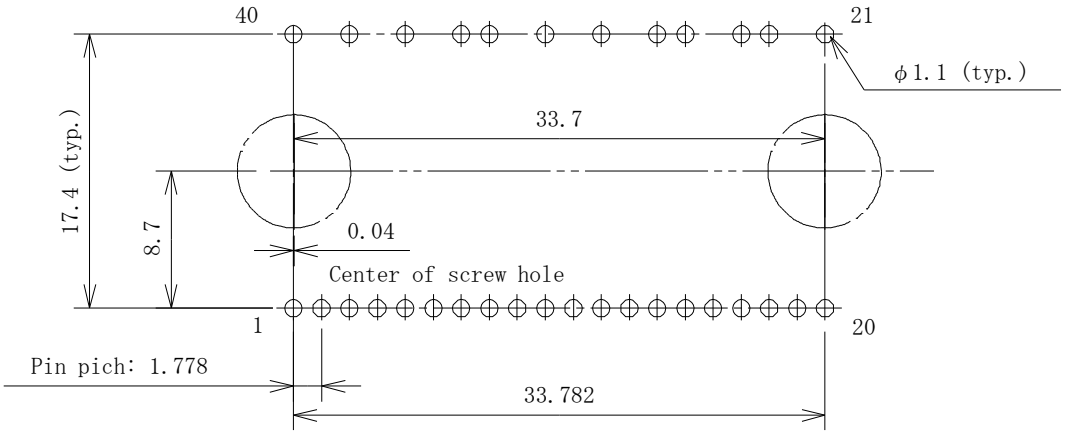


NOTES:

- Dimensions in millimeters
- Pb-free (RoHS compliant)
- "A" represents a pin illustrated for reference only, not the actual state of a bend.
- Maximum gate burr height is 0.3 mm.

● **Land Pattern Example**

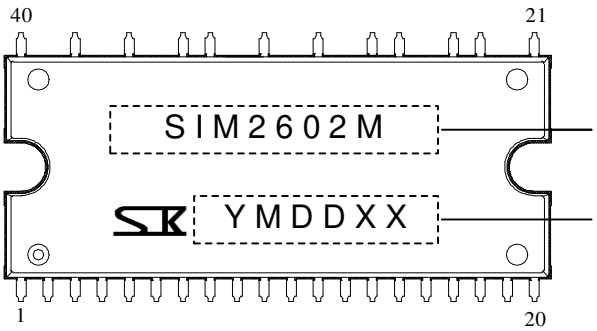
● **Reference Through Hole Size and Layout**



Unit: mm

10. Marking Diagram

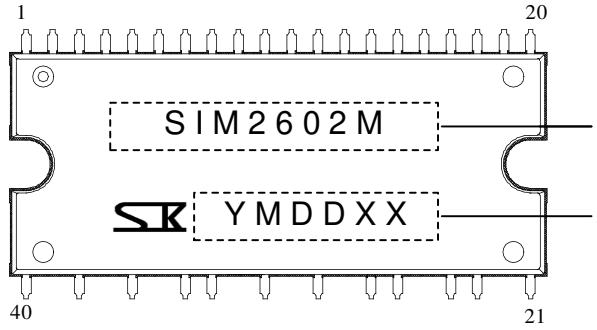
● **Front-side Marking**



Part Number

Lot Number:
Y is the last digit of the year of manufacture (0 to 9)
M is the month of the year (1 to 9, O, N, or D)
DD is the day of the month (01 to 31)
XX is the control number

● **Back-side Marking**



Part Number

Lot Number:
Y is the last digit of the year of manufacture (0 to 9)
M is the month of the year (1 to 9, O, N, or D)
DD is the day of the month (01 to 31)
XX is the control number

11. Functional Descriptions

Unless specifically noted, this section uses the following definitions:

- For concise descriptions, this section employs notation systems that denote the electrical characteristics symbols listed in Section 3 and the electronic symbol names of the typical applications in Section 8. All the characteristic values given in this section are typical values, unless they are specified as minimum or maximum.
- For pin and peripheral component descriptions, this section employs a notation system that denotes a pin name or an electronic symbol name with the arbitrary letter "x", representing the certain numbers and letters (1 to 3 and U to W). Thus, "the VBx pin" is used when referring to any or all of the VB1, VB2, and VB3 pins.

11.1 Pin Descriptions

11.1.1 COM1, COM2, and COM3

These are the logic ground pins for the built-in control ICs and are internally connected. Varying electric potential of the logic ground can be a cause of improper operations. Therefore, connect the logic ground as close and short as possible to a shunt resistor, R_S, at a single-point ground (or star ground) which is separated from the power ground (see Figure 11-1).

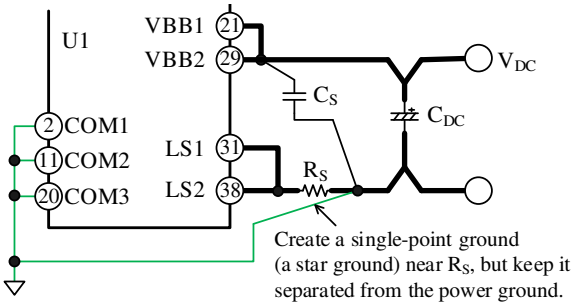


Figure 11-1. Connections to Logic Ground

11.1.2 LA

The IC features the phase advance function. The angle of phase advance is determined by an analog voltage applied to the LA pin. Section 11.5 gives detailed explanations on the LA pin settings and the phase advance function.

11.1.3 MLP

The IC determines to enable or disable the motor lock protection based on the setting of this pin. Table 11-1 provides the logic level definitions for the MLP pin. The IC detects which logic level the MLP pin has been set during a startup period (i.e., when the VCC pin voltage is rising). Figure 11-2 shows an internal circuit diagram of the MLP pin. To set the MLP pin to logic low, connect the pin to the GND pin. To set the MLP pin to logic high, connect the pin to the VREG pin. Section 11.7.5 explains more details on the motor lock protection.

Table 11-1. Logic Levels Defined for MLP Pin

MLP Pin	MLP Setting Status
L	Enabled
H	Disabled

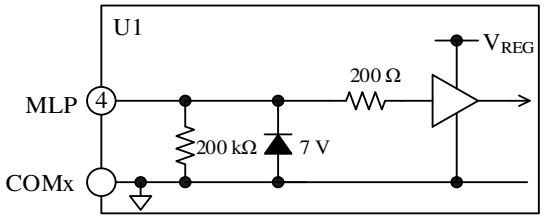


Figure 11-2. Internal Circuit Diagram of MLP Pin

11.1.4 OCP

This pin serves as the input of the overcurrent protection (OCP) which monitors the currents flowing through the output transistors. The IC determines which of the overcurrent limit (OCL) and overcurrent protection (OCP) functions to activate according to the level of a voltage applied to the OCP pin. Section 11.7.3 provides further information about the OCP circuit configuration and its mechanism.

11.1.5 VREG

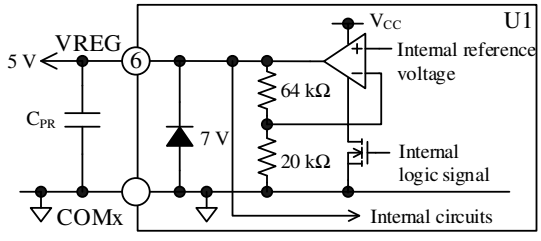


Figure 11-3. Internal Circuit Diagram of VREG Pin

This is the 5.0 V regulator output pin, which can be used for the power supply of the external Hall elements. A maximum output current of the VREG pin is 30 mA. To stabilize the VREG pin output, connect a capacitor, C_{PR}, of about 0.1 µF to the pin. The VREG pin also has

the undervoltage lockout. For more details on this function, see Section 11.7.1.

11.1.6 CW/CCW

This is the setting pin which determines the direction of motor rotation. Table 11-2 lists the logic level definitions for the CW/CCW pin and the corresponding motor directions. And Figure 11-4 shows an internal circuit diagram of the CW/CCW pin. To set the CW/CCW pin to logic low, connect the pin to the GND pin. To set the CW/CCW pin to logic high, connect the pin to the VREG pin. The IC detects which logic level the CW/CCW pin has been set during a startup period (i.e., a period during which the VCC pin voltage is rising).

Table 11-2. Logic Levels Defined for CW/CCW Pin

CW/CCW Pin	Motor Direction
L	Forward (CW)
H	Reverse (CCW)

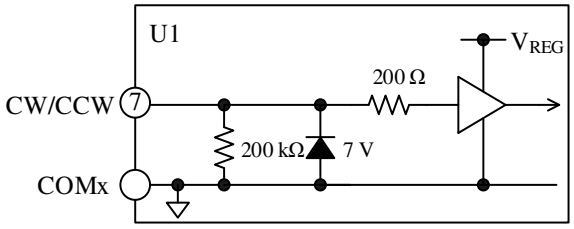


Figure 11-4. Internal Circuit Diagram of CW/CCW Pin

11.1.7 FGSEL

The FGSEL pin determines the cycle of a rotation pulse signal the FG pin outputs. Table 11-3 provides the relation between the FGSEL pin logic level and the number of pulses of a rotation pulse signal per 360° electrical angle. Figure 11-5 shows an internal circuit diagram of the FGSEL pin. To set the FGSEL pin to logic low, connect the pin to the GND pin. To set the FGSEL pin to logic high, connect the pin to the VREG pin. The IC detects which logic level the FGSEL pin has been set during a startup period (i.e., when the VCC pin voltage is rising).

Table 11-3. Number of Pulses of Rotation Pulse Signal

FGSEL Pin	Number of Signal Pulses
L	3 pulses per 360° electrical angle
H	1 pulse per 360° electrical angle

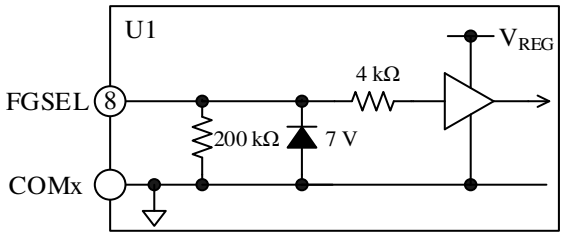


Figure 11-5. Internal Circuit Diagram of FGSEL Pin

11.1.8 HUP, HVP, and HWN; HUN, HVN, and HWP

These are the input pins for Hall element signals. The HxP pin is connected to the positive node of a Hall element, whereas the HxN pin is connected to the negative node of a Hall element. As Figure 11-6 illustrates, connect a noise filter capacitor, C_{Hx}, with a capacitance of about 0.1 µF, between the HxP and HxN pins. C_{Hx} must be placed near the IC with a minimal length of traces. The IC incorporates the protection circuit that detects abnormal signals from the external Hall elements (see Section 11.7.7).

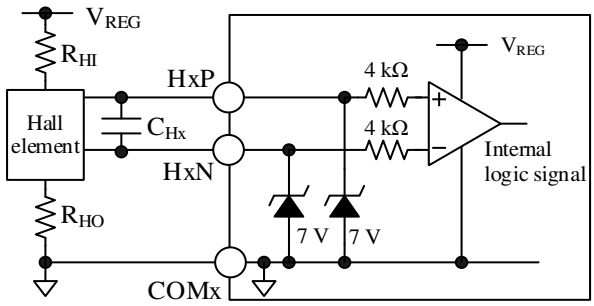


Figure 11-6. Internal Circuit Diagram of HxP and HxN Pins

11.1.9 VSP

The IC controls the speed of motor rotation with an analog voltage applied to the VSP pin. For more details on the motor speed control, see Section 11.4.

11.1.10 FG

The FG pin outputs a rotation pulse signal that is generated based on a position sensing signal. A rotation pulse signal is inverted at each edge of the Hall element signal assigned to the U-, V-, and W-phases. As shown in Figure 11-7, the FG pin is internally pulled down to the COMx pin.

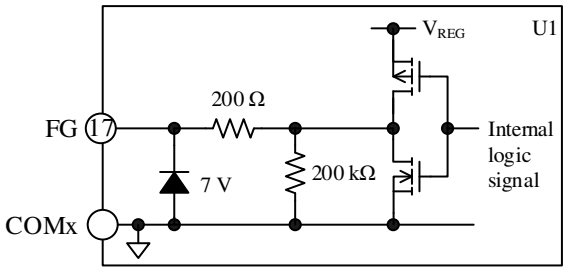


Figure 11-7. Internal Circuit Diagram of FG Pin

11.1.11 FO

The FO pin operates as the fault signal output. For more details on this function, see Section 11.6. Figure 11-8 shows an internal circuit diagram of the FO pin. The FO pin can also be directly connected to the input pin of the external microcontroller. For avoiding repeated OCP activations, the external microcontroller must shut off any input signals to the IC within an OCP hold time, t_P = 15 ms, after a fault signal output. (For more details, see Section 11.7.3)

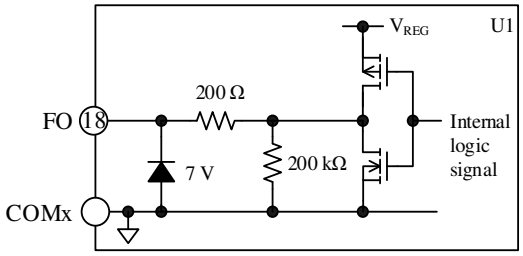


Figure 11-8. Internal Circuit Diagram of FO Pin

11.1.12 VCC

This is the logic supply pin for the built-in control ICs. The VCC pin has the undervoltage lockout for power supply (see Section 11.7.2.2). To prevent malfunction induced by supply ripples or other factors, put a 0.01 µF to 0.1 µF ceramic capacitor, C_P, near these pins. To prevent damage caused by surge voltages, put an 18 V to 20 V Zener diode, DZ, between the VCC and COMx pins. Voltages to be applied between the VCC and COMx pins should be regulated within the recommended operational range of V_{CC}, given in Section 2.

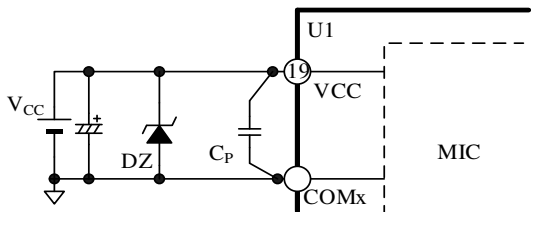


Figure 11-9. VCC Pin and Its Peripheral Circuit

11.1.13 VBB1 and VBB2

These are the input pins for the main supply voltage, i.e., the positive DC bus. All of the high-side collectors are connected to these pins. Voltages between the VBBx and COMx pins should be set within the recommended range of the main supply voltage, V_{DC}, given in Section 2.

To suppress surge voltages, put a 0.01 µF to 0.1 µF bypass capacitor, C_S, near the VBBx pin and an electrolytic capacitor, C_{DC}, with a minimal length of PCB traces to the VBBx pin.

11.1.14 VB1, VB2, and VB3

The VB1, VB2, and VB3 pins are connected to bootstrap capacitors, C_{Bx}, for the high-side floating supply. For proper startup, turn on the low-side transistors first, then fully charge the bootstrap capacitors, C_{Bx}. Section 11.2 describes the startup sequences of the IC in detail; Section 11.3 explains the procedures to charge the bootstrap capacitors.

C_{Bx} ,with a capacitance of about 1 µF, must be placed near the IC, and connected between the VBx and output (U, V1, W1) pins with a minimal length of trances. The VBx pin also has the undervoltage lockout for power supply. For more details on this function, see Section 11.7.2.1.

11.1.15 U, V1, V2, W1, and W2

These pins are the outputs of the three phases, and serve as the connection terminals to the 3-phase motor. The V1 and W1 pins must be connected to the V2 and W2 pins on a PCB, respectively. The U, V, and W1 pins are the grounds for the VB1, VB2, and VB3 pins. The U, V1, and W1 pins are connected to the negative nodes of bootstrap capacitors, C_{Bx}. Since high voltages are applied to these output pins (U, V1, V2, W1, W2), it is required to take measures for insulating as follows:

- Keep enough distance between the output pins and low-voltage traces.
- Coat the output pins with insulating resin.

11.1.16 LS1 and LS2

The LS1 pin is connected to the low-side emitter of the U-phase; the LS2 pin is connected to the low-side emitters of the V- and W-phases. The LSx pin should be connected to an external shunt resistor, R_S, on a PCB. When connecting the shunt resistor, use the resistor with low inductance (required), and place it as near as possible to the IC with a minimum length of traces to the LSx and COMx pins. Otherwise, malfunction may occur because a longer circuit trace increases its inductance and thus increases its susceptibility to improper

operations. In applications where long PCB traces are required, add a fast recovery diode, D_{RS}, between the LSx and COMx pins in order to prevent the IC from malfunctioning.

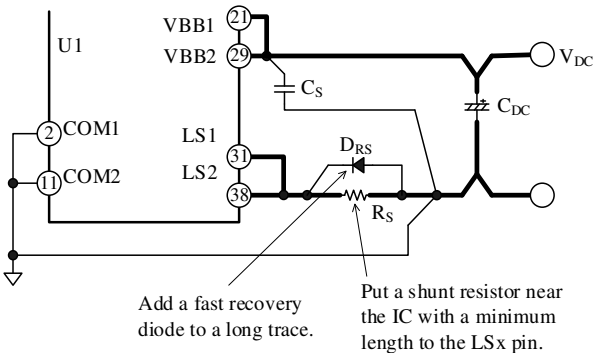


Figure 11-10. Connections to LSx Pin

11.2 Startup Operation

When the VCC pin voltage reaches $V_{CC(ON)}$ = 11.5 V, the IC starts operating. As the startup sequence starts, the IC detects and reflects the logic states of the following pins to the motor control settings: the MLP, CW/CCW, and FGSEL pins. The IC then waits for the VSP pin voltage to reach a certain level at which output duty cycles are controllable. At startup, the IC operates according to the VSP pin voltage levels as follows:

- **V_{SP} < 1.0 V:**
  All the output signals are off.
- **1.0 V ≤ V_{SP} < 2.1 V:**
  The IC starts charging bootstrap capacitors. For more details, see Section 11.3.
- **2.1 V ≤ V_{SP} ≤ 5.4 V:**
  The IC controls its output duty cycles according to the VSP pin voltage levels. While the frequency of a position sensing signal, Hx, is less than 1.0 Hz at startup, the motor is driven by a trapezoidal control. When Hx increases to 1.0 Hz or more (i.e., the condition in which a position sensing signal is detected at every rotation of 60° in electrical degrees), the IC generates a sine-wave signal and drives the motor by a sinusoidal control.

Table 11-4 and Table 11-5 are truth tables for the motor driven by the trapezoidal control in a forward or reverse rotation. Moreover, the timing charts shown later represent the operational waveforms in the following motor operations: the motor in a forward rotation (no phase advance; Figure 11-15), the motor in a forward rotation (phase advance by 15°; Figure 11-16), and the motor in a reverse rotation (Figure 11-17). The following symbols used in Figure 11-15 to Figure 11-17 represent the signals generated inside the IC: S_U, S_V, S_W, S_X, S_Y, S_Z. Then the IC detects a state in which the motor rotates inversely to the preset direction, the motor driving system is immediately switched to the trapezoidal control before a rotation of 60° electrical angle completes. For detailed descriptions on the reverse rotation detection, see Section 11.7.6.

The following are the important considerations for appropriate power startup and shutdown sequences.

- To turn on the IC, be sure to increase the VSP pin voltage last. To turn off the IC, be sure to decrease the VSP pin voltage first.
- When you have enabled the motor lock protection (MLP = L), be sure to apply a voltage to the VBBx pin at the timing described below. At startup, apply a voltage to the VCC pin and the VREG pin voltage, V_{REG}, increases. Then, apply a main supply voltage to the VBBx pin within the period from V_{REG} increase to an MLP detection time, t_{LD}. When a position sensing signal stays unchanged even after a lapse of t_{LD}, the IC determines this condition as a motor lockup state and activates the motor lock protection (see Section 11.7.5).

The IC can also operate in test mode. In test mode, the high-side transistors in the trapezoidal control are driven at duty cycle = 100%, the TSD circuit is disabled, and the phase advance angle is fixed at 0°. To start IC operations in test mode, turn on the IC after applying a voltage of ≥8.1 V on the VSP pin, and a voltage of 2.75 V (typ.) on the CW/CCW pin.

11.3 Charging of Bootstrap Capacitors

It is required to fully charge bootstrap capacitors, C_{Bx}, at startup. The charging sequence depends on the VSP pin voltage, V_{SP}. When 1.0 V ≤ V_{SP} ≤ 2.1 V at startup, the IC turns on the low-side transistors at every PWM cycle in order to charge C_{Bx}. When V_{SP} ≥ 2.1 V, the IC controls the motor speed according to the VSP pin voltage levels (see Section 11.4). However, note that the IC does not charge C_{Bx} even when 1.0 V ≤ V_{SP} ≤ 2.1 V along with the motor rotating inversely to the preset direction, or the motor coasting at a frequency of ≥1.0 Hz. If a sudden rise in the VSP pin voltage up to 2.1 V or more occurs at startup, the IC starts the motor speed control after charging C_{Bx} for a period of 9 ms ± 5%.

11.4 Motor Speed Control

The IC controls the speed of motor rotation with an analog voltage applied to the VSP pin. When 2.1 V ≤ V_{SP} ≤ 5.4 V, the IC controls its output duty cycles depending on the VSP pin voltage levels. For the IC operation when V_{SP} < 2.1 V (i.e., the startup sequence), see Section 11.2.

A duty cycle of an output signal is determined according to a digital signal that is generated by the built-in 7-bit AD converter from the VSP pin input voltage. The higher the VSP pin voltage increases, the higher the duty cycle becomes, thus causing the motor to rotate faster. Figure 11-11 depicts how a duty cycle varies according to the VSP pin voltage, V_{SP}. While V_{SP} maintains at 5.4 V or more, the IC controls its output signals at duty cycle = 100%.

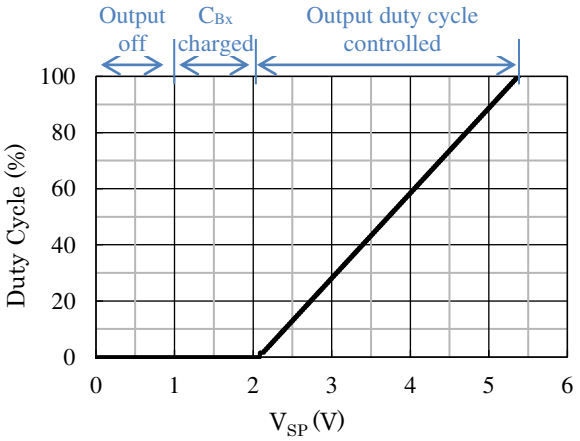


Figure 11-11. VSP Pin Voltage vs. Duty Cycle

Figure 11-12 is an internal circuit diagram describing the VSP pin and its peripheral circuit. A voltage to be applied on the VSP pin, V_{SPP}, must be set to <10 V, i.e., below the rated VSP pin input voltage. R_{SP} should have a resistance of about 100 Ω; C_{SP} should have a capacitance of about 0.1 µF.

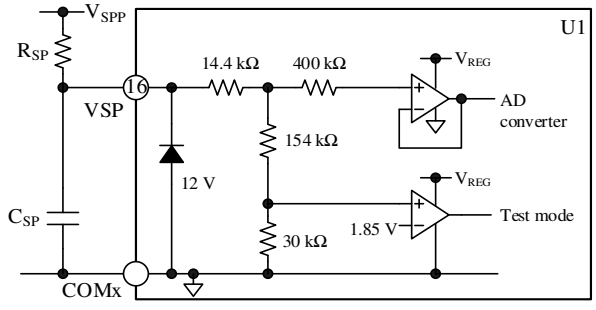


Figure 11-12. Internal Circuit Diagram of VSP Pin and Its Peripheral Circuit

11.5 Phase Advance Function

The IC features the phase advance function. The angle of phase advance is determined by an analog voltage applied to the LA pin. As shown in Figure 11-13, the VREG pin voltage divided by two resistors, R_{LA1} and R_{LA2}, is applied to the LA pin. Figure 11-14 plots how a phase advance angle changes over the LA pin voltage. When the phase advance function is enabled, each phase shifts ±0.9375° every 4 cycles of a Hall signal to the preset angle.

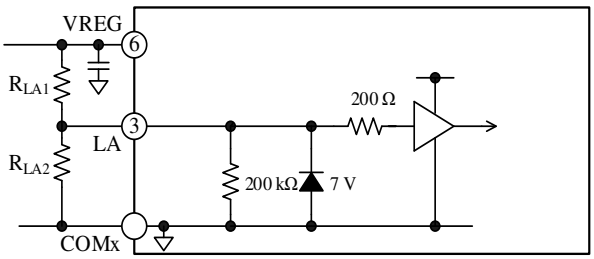


Figure 11-13. Internal Circuit Diagram of LA Pin

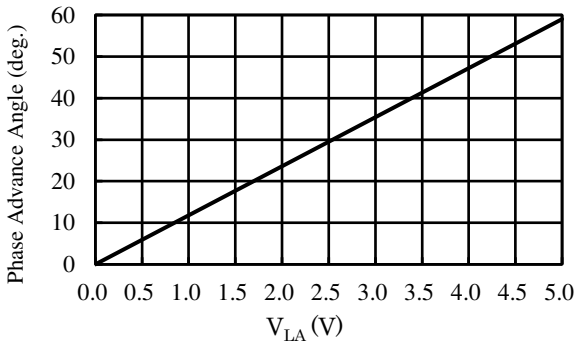


Figure 11-14. LA Pin Voltage vs. Phase Advance Angle

Table 11-4. Truth Table for Trapezoidal Control (Forward)

Position Sensing Signal			U-phase		V-phase		W-phase	
HU	HV	HW	High-side Transistor	Low-side Transistor	High-side Transistor	Low-side Transistor	High-side Transistor	Low-side Transistor
H	L	H	OFF	ON	ON	OFF	OFF	OFF
H	L	L	OFF	ON	OFF	OFF	ON	OFF
H	H	L	OFF	OFF	OFF	ON	ON	OFF
L	H	L	ON	OFF	OFF	ON	OFF	OFF
L	H	H	ON	OFF	OFF	OFF	OFF	ON
L	L	H	OFF	OFF	ON	OFF	OFF	ON
L	L	L	OFF	OFF	OFF	OFF	OFF	OFF
H	H	H	OFF	OFF	OFF	OFF	OFF	OFF

Table 11-5. Truth Table for Trapezoidal Control (Reverse)

Position Sensing Signal			U-phase		V-phase		W-phase	
HU	HV	HW	High-side Transistor	Low-side Transistor	High-side Transistor	Low-side Transistor	High-side Transistor	Low-side Transistor
L	H	L	OFF	ON	ON	OFF	OFF	OFF
L	H	H	OFF	ON	OFF	OFF	ON	OFF
L	L	H	OFF	OFF	OFF	ON	ON	OFF
H	L	H	ON	OFF	OFF	ON	OFF	OFF
H	L	L	ON	OFF	OFF	OFF	OFF	ON
H	H	L	OFF	OFF	ON	OFF	OFF	ON
H	H	H	OFF	OFF	OFF	OFF	OFF	OFF
L	L	L	OFF	OFF	OFF	OFF	OFF	OFF

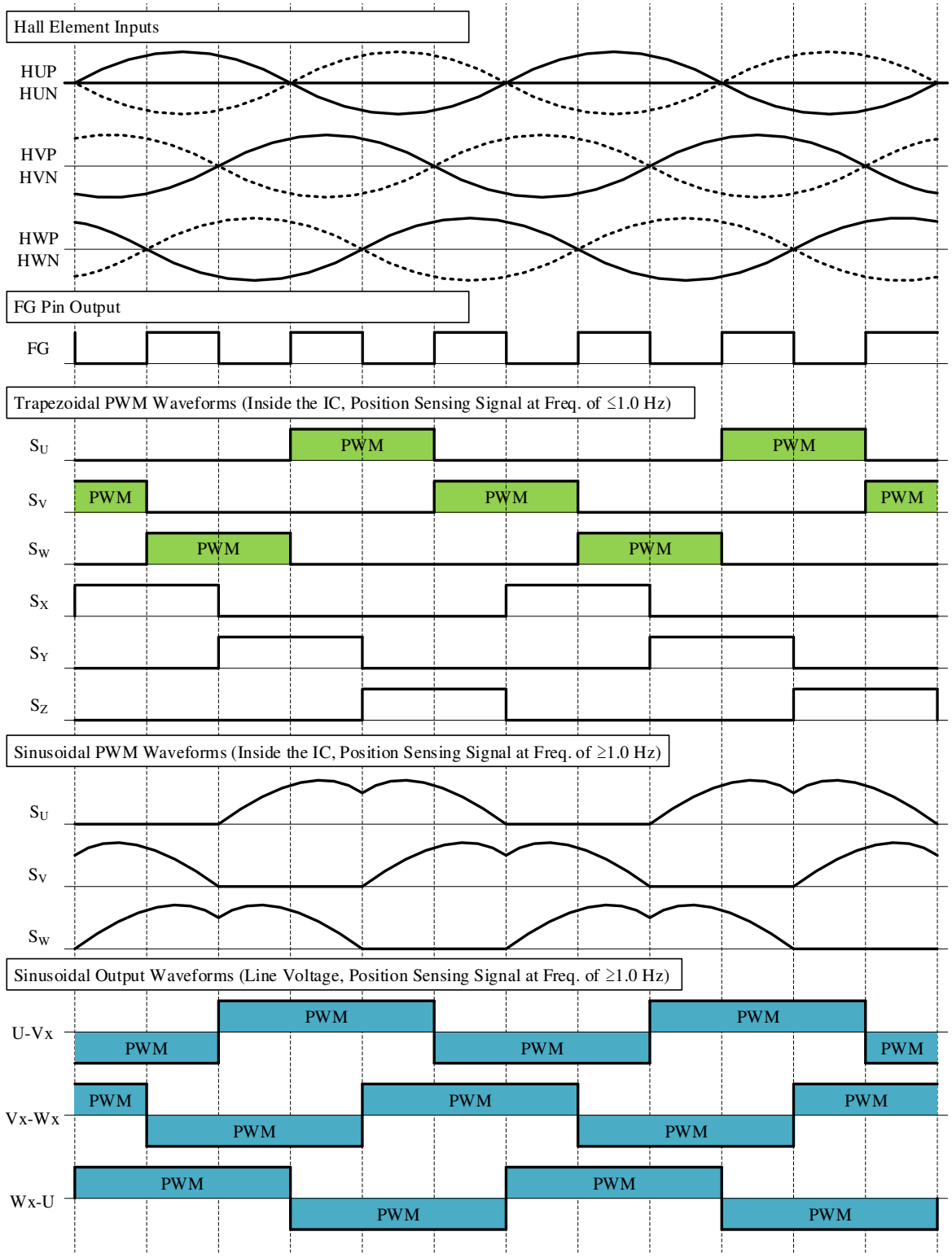


Figure 11-15. Operational Waveforms (Forward, No Phase Advance)

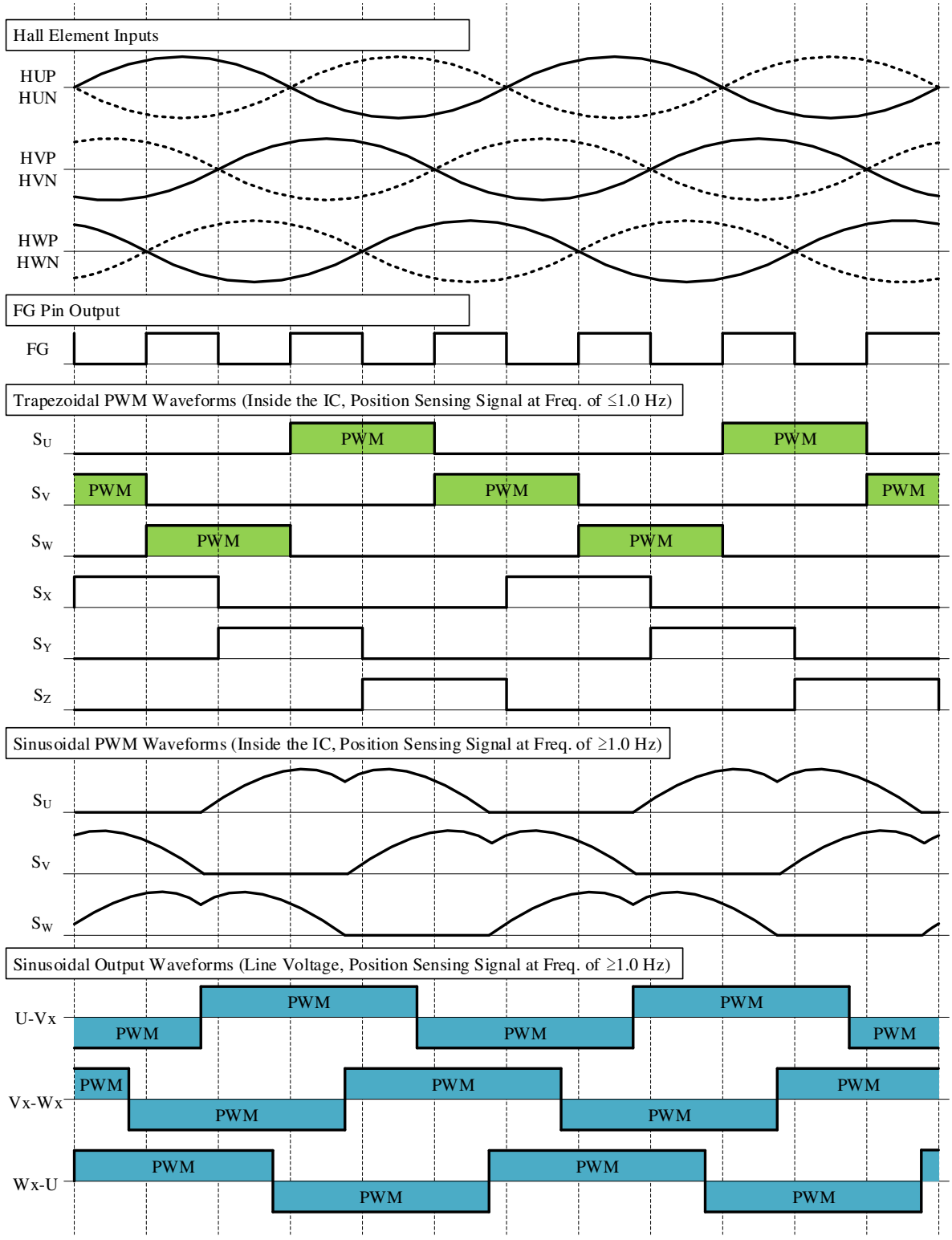


Figure 11-16. Operational Waveforms (Forward, Phase Advance by 15°)

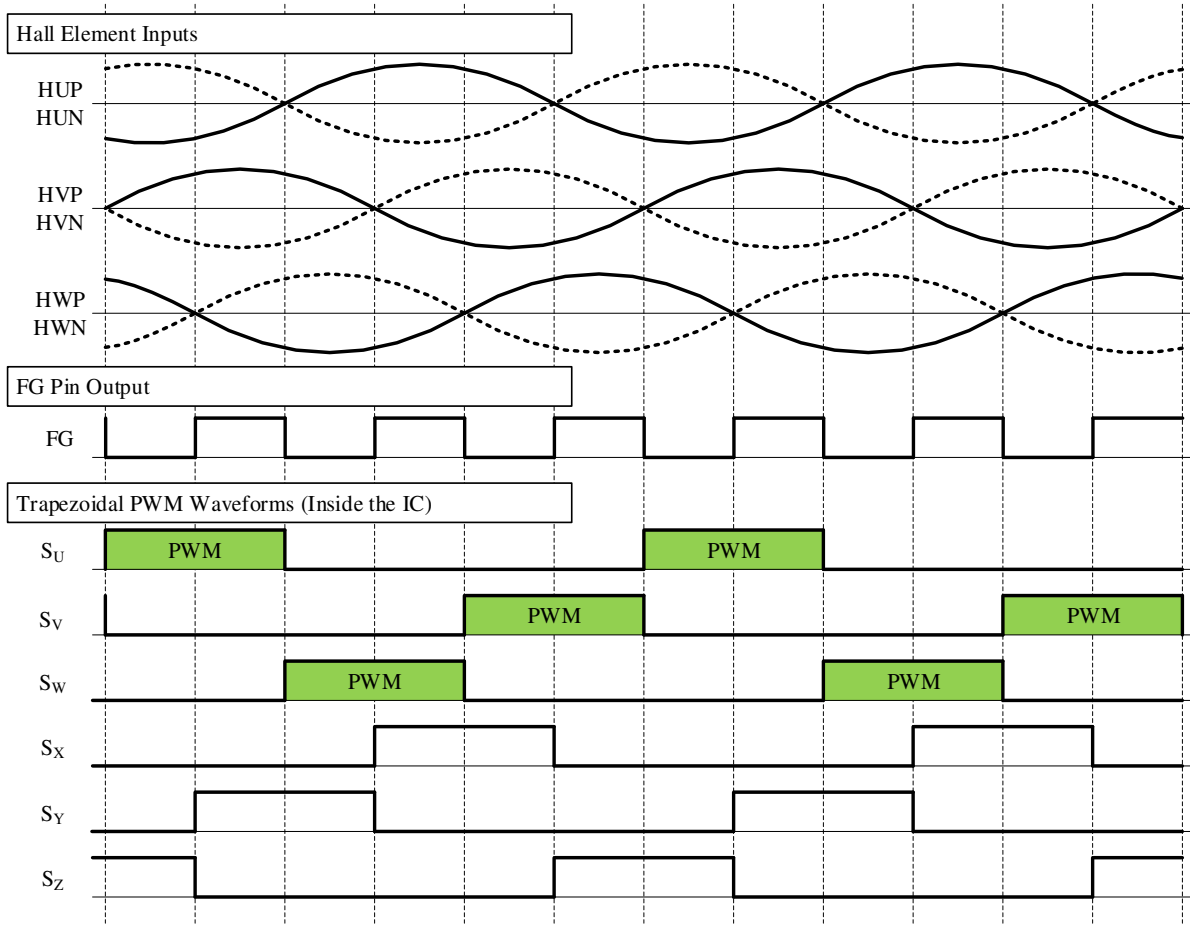


Figure 11-17. Operational Waveforms (Reverse)

11.6 Fault Signal Output

In case one or more of the following protections are actuated, an internal P-channel power MOSFET turns on, then the FO pin becomes logic high (about 5 V). In normal operation, the FO pin outputs a low signal.

For more details on the protections, see Section 11.7.

- VREG pin undervoltage lockout (UVLO_VREG)
- Overcurrent protection (OCP)
- Thermal shutdown (TSD)
- Motor lock protection (MLP)
- Reverse rotation detection
- Hall signal abnormality detection

The fault signal output time of the FO pin at OCP activation is defined as the OCP Hold Time, t_P = 15 ms (typ.), fixed by a built-in feature of the IC itself (see Section 11.7.3).

The external microcontroller receives a fault signal with its interrupt pin (INT), and must be programmed to shut off any input signals to the IC within the predetermined OCP hold time, t_P.

11.7 Protection Functions

This section describes the various protection circuits provided in the SIM2602M, such as those designed to detect a voltage drop across power supplies, an overcurrent condition, an abnormal motor state, and so on.

11.7.1 VREG Pin Undervoltage Lockout (UVLO_VREG)

When the VREG pin voltage decreases to V_{UVRL} = 3.60 V or less, the VREG pin undervoltage lockout (UVLO_VREG) circuit gets activated and turns off the high- and low-side transistors. When the VREG pin voltage increases to V_{UVRH} = 4.00 V or more, the IC releases the UVLO_VREG operation. Then, the high- and low-side transistors resume operating according to position sensing signals. During the UVLO_VREG operation, the FO pin becomes logic high and transmits fault signals.

11.7.2 Undervoltage Lockout for Power Supply (UVLO)

In case the gate-driving voltages of the output transistors decrease, their steady-state power dissipations increase. This overheating condition may cause permanent damage to the IC in the worst case. To prevent this event, the SIM2602M has the undervoltage lockout (UVLO) circuits for each of the high-side (the VBx pin) and the low-side (the VCC pin) power supplies.

11.7.2.1. VBx Pin (UVLO_VB)

When the voltage between the VBx and output (U, V1/V2, or W1/W2) pins (VBx–HSx) decreases to $V_{BS(OFF)}$ = 10.0 V or less, the UVLO_VB circuit gets activated and turns off the high-side transistors. When the voltage between the VBx and output pins increases to $V_{BS(ON)}$ = 10.5 V or more, the IC releases the UVLO_VB operation. Then, the high-side transistors resume operating according to position sensing signals.

11.7.2.2. VCC Pin (UVLO_VCC)

When the VCC pin voltage decreases to $V_{CC(OFF)}$ = 11.0 V or less, the UVLO_VCC circuit gets activated and turns off the high- and low-side transistors. When the VCC pin voltage increases to $V_{CC(ON)}$ = 11.5 V or more, the IC releases the UVLO_VCC operation. Then, the high- and low-side transistors resume operating according to position sensing signals.

11.7.3 Overcurrent Limit (OCL) and Overcurrent Protection (OCP)

The IC has two different protections against overcurrent conditions: the overcurrent limit (OCL) and the overcurrent protection (OCP). Figure 11-18 is an internal circuit diagram describing the OCP pin and its peripheral circuit. The OCP pin detects overcurrents with voltage across an external shunt resistor, R_S. Because the OCP pin is internally pulled up, the OCP pin voltage increases proportionally to a rise in the current running through the shunt resistor, R_S. When the shunt resistor, R_S, is open, the IC activates the OCP function.

Note that overcurrents are undetectable when one or more of the U, V1/V2, and W1/W2 pins or their traces are shorted to ground (ground fault). In case any of these pins falls into a state of ground fault, the output transistors may be destroyed.

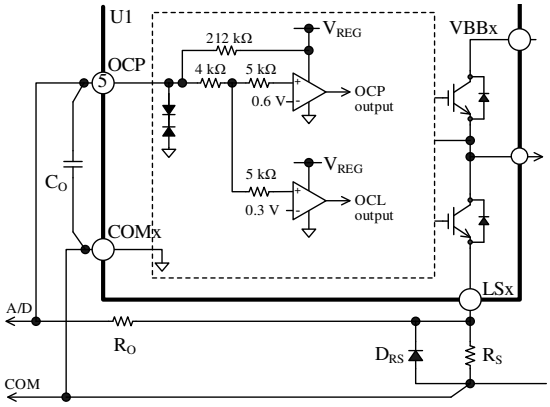


Figure 11-18. Internal Circuit Diagram of OCP Pin and Its Peripheral Circuit

The overcurrent limit (OCL) is a protection against relatively low overcurrent conditions. When the OCP pin voltage increases to V_{LIM} = 0.30 V or more, and remains in this condition for a period of a blanking time ($t_{BK(OCL)}$ = 2.3 µs) or longer, the IC turns off the high- and low-side transistors. The OCL operation is automatically released at each PWM cycle.

The overcurrent protection (OCP) is a protection against large inrush currents. When the OCP pin voltage increases to V_{TRIP} = 0.60 V or more, and remains in this condition for a period of a blanking time ($t_{BK(OCP)}$ = 0.8 µs) or longer, the OCP circuit is activated. Then, the high- and low-side transistors are turned off for a certain period of time (t_P = 15 ms). After that, the high- and low-side transistors resume operating according to position sensing signals. During the OCP operation, the FO pin goes logic high and sends fault signals.

The OCL and OCP are used for detecting abnormal conditions, such as an output transistor shorted. In case short-circuit conditions occur repeatedly, the output transistors can be destroyed. For this reason, motor operations must be controlled by the external microcontroller so that it can immediately stop the motor when fault signals are detected. If you need to resume the IC operation thereafter, set the IC to be resumed after a lapse of ≥2 seconds.

For proper shunt resistor setting, your application must meet the following:

- Use the shunt resistor that has a recommended resistance, R_S (see Section 2).
- Set the OCP pin input voltage to vary within the rated input voltages, $V_{IN(2)}$ (see Section 1).
- Keep the current through the output transistors below the rated output current (pulse), I_{OP} (see Section 1).

It is required to use a resistor with low internal inductance because high-frequency switching current will flow through the shunt resistor, R_S. In addition, choose a resistor with allowable power dissipation according to your application.

11.7.4 Thermal Shutdown (TSD)

The SIM2602M incorporates the thermal shutdown (TSD) circuit. In case of overheating (e.g., increased power dissipation due to overload, or elevated ambient temperature at the device), the IC shuts down the high- and low-side transistors.

The TSD circuit in the MIC for gate driver monitors temperatures (see Figure 6-1). When the junction temperature of the MIC for gate driver, $T_{J(DRV)}$, exceeds T_{DH} = 130 °C, the TSD circuit is activated. When $T_{J(DRV)}$ decreases to $T_{DH} - T_{D(HYS)}$ after the TSD activation, the shutdown condition is released. The output transistors then resume operating according to input signals. During the TSD operation, the FO pin becomes logic high and transmits fault signals. Note that junction temperatures of the output transistors themselves are not monitored; therefore, do not use the TSD function as an overtemperature prevention for the output transistors.

11.7.5 Motor Lock Protection (MLP)

When the state in which a position sensing signal stays unchanged within a rotation of 60° electrical angle persists for a motor lock hold time (t_{LD} = 5 s) or longer, the motor lock protection (MLP) circuit gets activated. Then, the high- and low-side transistors are turned off for a certain period of time (t_{LH} = 64 s). After that, the high- and low-side transistors resume operating according to position sensing signals.

During the MLP operation, the FO pin becomes logic high and transmits fault signals. Moreover, direct currents through the output transistors cause an increase in the junction temperatures of the output transistors. Therefore, care must be taken not to allow the junction temperatures to exceed the absolute maximum rating.

11.7.6 Reverse Rotation Detection

In case the motor rotates in a direction opposite to the preset direction, the reverse rotation detection function gets activated and puts the FO pin into a high state (i.e., a fault signal output). When the motor rotates in the preset direction, the FO pin is in a low state. When the IC detects a reverse rotation state during motor rotations, the motor driving system is immediately switched to the trapezoidal control before a rotation of 60° electrical angle completes.

Table 11-6. Motor Driving Controls during Reverse Rotation

CW/CCW Pin State	Motor Direction	Driving System
L (Forward)	Forward	Sinusoidal
	Reverse	Trapezoidal
H (Reverse)	Forward	Trapezoidal
	Reverse	Sinusoidal

11.7.7 Hall Signal Abnormality Detection

As Figure 11-19 shows, signals from the external Hall elements are input into the corresponding comparators. The IC then receives the comparator outputs as the motor positional information, i.e., position sensing signals.

When all the position sensing signals (HU, HV, HW) are either in a high or low state, the Hall signal abnormality detection function gets activated and turns off the high- and low-side transistors. When the IC

detects input states other than those above, each of the high- and low-side transistors responds in accordance with the input logic levels of the position sensing signals. For the truth tables for the position sensing signals and the output transistors, see Table 11-4 and Table 11-5. While the function is being enabled, the FO pin becomes logic high and sends fault signals.

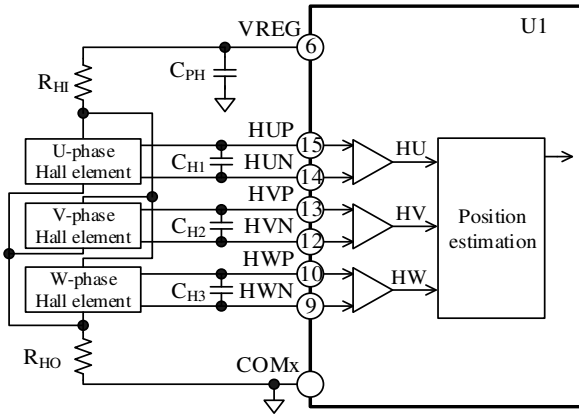


Figure 11-19. Internal Circuit Diagram of HxP and HxN Pins and Their Peripheral Circuit

12. Design Notes

12.1 PCB Pattern Layout

Figure 12-1 shows a schematic diagram of a motor drive circuit. The circuit consists of current paths having high frequencies and high voltages, which also bring about negative influences on IC operation, noise interference, and power dissipation. Therefore, PCB trace layouts and component placements play an important role in circuit designing. Current loops, which have high frequencies and high voltages, should be as small and wide as possible, in order to maintain a low-impedance state. In addition, ground traces should be as wide and short as possible so that radiated EMI levels can be reduced.

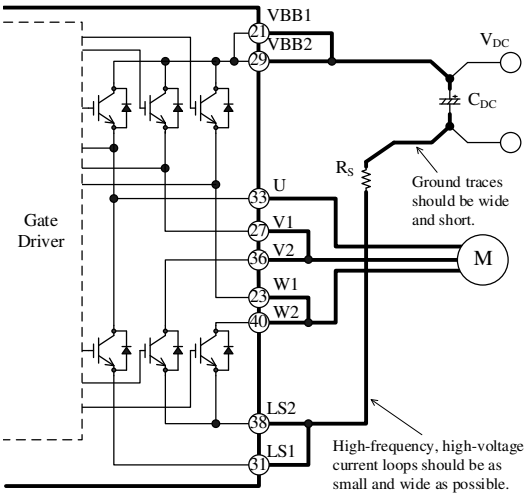


Figure 12-1. High-frequency, High-voltage Current Paths

12.2 Considerations in IC Characteristics Measurement

When measuring the leakage current of the output transistors incorporated in the IC, note that all of the output (U, V1, V2, W1, W2), LSx, and COMx pins must be appropriately connected. Otherwise, the output transistors may result in permanent damage. Also note that the gate and emitter of each output transistor should have the same potential during the leakage current measurement. Moreover, care should be taken during the measurement because each output transistor is connected as follows:

- All the high-side collectors are internally connected to the VBBx pin.
- In the U-phase, the high-side emitter and the low-side collector are internally connected to the U pin. (In the V- and W-phases, the high- and low-side transistors are unconnected inside the IC.)
- In the V- and W-phases, the low-side emitters are internally connected to the LS2 pin.
- The high-side gates are internally pulled down to the output pins.
- The low-side gates are internally pulled down to the COMx pin.

The following are circuit diagrams representing typical measurement circuits for breakdown voltage: Figure 12-2 shows the high-side transistor (Q_{1H}) in the U-phase; Figure 12-3 shows the low-side transistor (Q_{1L}) in the U-phase. And all the pins that are not represented in these figures are open. When measuring the high-side transistors, leave all the non-measuring pins open. When measuring the low-side transistors, connect only the measuring LSx pin to the COMx pin and leave the other pins open.

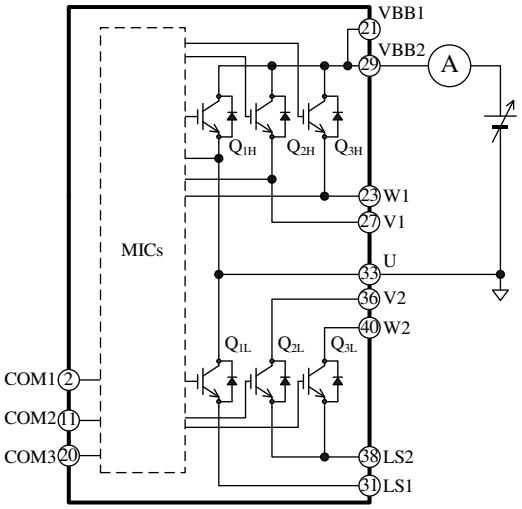


Figure 12-2. Typical Measurement Circuit for High-side Transistor (Q_{1H}) in U-phase

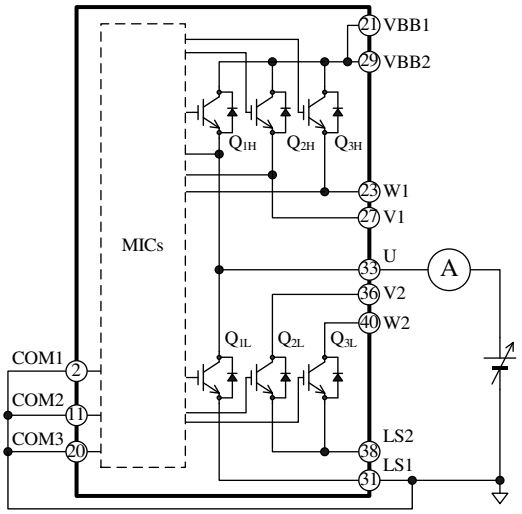


Figure 12-3. Typical Measurement Circuit for Low-side Transistor (Q_{1L}) in U-phase

12.3 Considerations in Heatsink Mounting

The following are the key considerations and the guidelines for mounting a heatsink:

- A pair of a metric screw of M2.5 and a plain washer of 6.0 mm (φ) must be used. When tightening the screws, use a torque screwdriver and tighten them within the range of screw torque defined in Section 4. Be sure to avoid uneven tightening. Temporarily tighten the two screws first, then tighten them equally on both sides until the specified screw torque is reached.
- When mounting a heatsink, it is recommended to use silicone greases. If a thermally conductive sheet or an electrically insulating sheet is used, package cracks may be occurred due to creases at screw tightening. Therefore, you should conduct thorough evaluations before using these materials.
- When applying a silicone grease, make sure that there are no foreign substances between the IC and a heatsink. Extreme care should be taken not to apply a silicone grease onto any device pins as much as possible. The following requirements must be met for proper grease application:
  - Grease thickness: 100 μm
  - Heatsink flatness: ±100 μm
  - Apply a silicone grease within the area indicated in Figure 12-4, below.

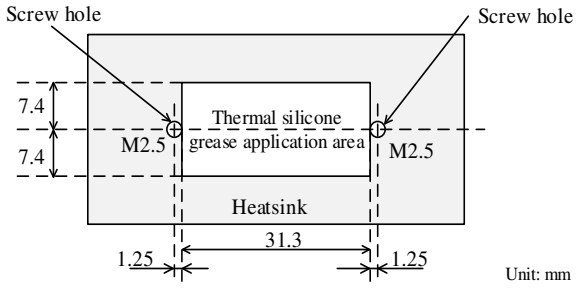


Figure 12-4. Reference Application Area for Thermal Silicone Grease

13. Calculating Power Losses and Estimating Junction Temperature

This section describes the procedures to calculate power losses in switching transistors, and to estimate a junction temperature. Note that the descriptions listed here are applicable to the SIM2602M, which is controlled by a 3-phase sine-wave PWM driving strategy.

For quick and easy references, we offer calculation support tools online. Please visit our website to find out more.

- DT0052: SIM2602M Calculation Tool
  https://www.semicon.sanken-ele.co.jp/en/calc-tool/igbtall_caltool_en.html

Total power loss in an IGBT can be obtained by taking the sum of steady-state loss, P_{ON}, and switching loss, P_{SW}. The following subsections contain the mathematical procedures to calculate these losses (P_{ON} and P_{SW}) and the junction temperature of all IGBTs operating.

13.1.1 IGBT Steady-state Loss, P_{ON}

Steady-state loss in an IGBT can be computed by using the $V_{CE(SAT)}$ vs. I_C curves, listed in Section 14.3.1. As expressed by the curves in Figure 13-1, linear approximations at a range the I_C is actually used are obtained by: $V_{CE(SAT)} = \alpha \times I_C + \beta$. The values gained by the above calculation are then applied as parameters in Equation (1), below. Hence, the equation to obtain the IGBT steady-state loss, P_{ON}, is:

$$P_{ON} = \frac{1}{2\pi}\int_0^{\pi} V_{CE(SAT)}(\varphi) \times I_C(\varphi) \times DT \times d\varphi$$

$$= \frac{1}{2}\alpha\left(\frac{1}{2} + \frac{4}{3\pi}M \times \cos\theta\right) {I_M}^2 + \frac{\sqrt{2}}{\pi}\beta\left(\frac{1}{2} + \frac{\pi}{8}M \times \cos\theta\right) I_M . \quad (1)$$

Where:

$V_{CE(SAT)}$ is the collector-to-emitter saturation voltage of the IGBT (V),
I_C is the collector current of the IGBT (A),
DT is the duty cycle, which is given by

$$DT = \frac{1 + M \times \sin(\varphi + \theta)}{2},$$

M is the modulation index (0 to 1),
cosθ is the motor power factor (0 to 1),
I_M is the effective motor current (A),
α is the slope of the linear approximation in the $V_{CE(SAT)}$ vs. I_C curve, and
β is the intercept of the linear approximation in the $V_{CE(SAT)}$ vs. I_C curve.

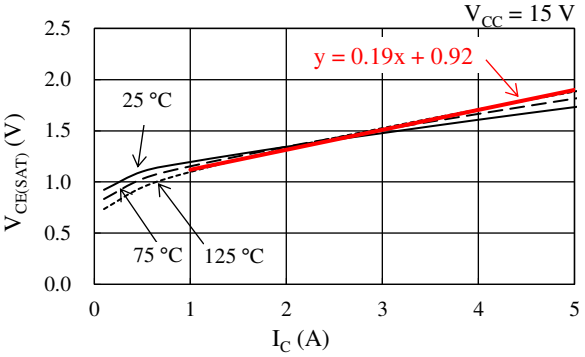


Figure 13-1. Linear Approximate Equation of $V_{CE(SAT)}$ vs. I_C

13.1.2 IGBT Switching Loss, P_{SW}

Switching loss in an IGBT, P_{SW}, can be calculated by Equation (2), letting I_M be the effective current value of the motor:

$$P_{SW} = \frac{\sqrt{2}}{\pi} \times f_C \times \alpha_E \times I_M \times \frac{V_{DC}}{300}. \quad (2)$$

Where:

f_C is the PWM carrier frequency (Hz),
V_{DC} is the main power supply voltage (V), i.e., the VBBx pin input voltage, and
α_E is the slope on the switching loss curve (see Section 14.3.2).

13.1.3 Estimating Junction Temperature of IGBT

The junction temperature of all IGBTs operating, T_J, can be estimated with Equation (3):

$$T_J = R_{(J-C)Q} \times \{(P_{ON} + P_{SW}) \times 6\} + T_C . \quad (3)$$

Where:

$R_{(J\text{-}C)Q}$ is the junction-to-case thermal resistance (°C/W) of all the IGBTs operating, and
T_C is the case temperature (°C), measured at the point defined in Figure 3-2.

14. Performance Curves

14.1 Transient Thermal Resistance Curves

The following graphs represent transient thermal resistance (the ratios of transient thermal resistance), with steady-state junction-to-case thermal resistance = 1. Note that the graph representing that of the IGBT-embedded device shows only IGBT characteristics; no freewheeling diode characteristics are included.

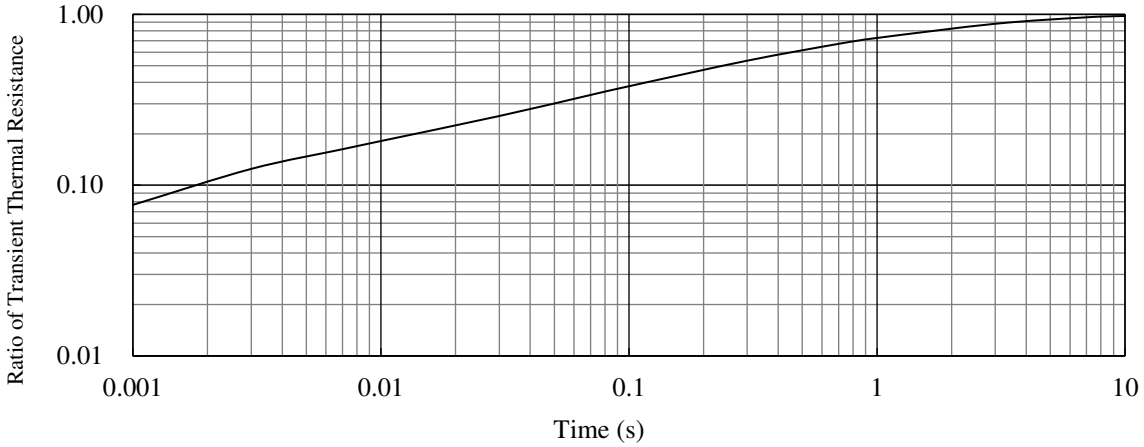


Figure 14-1. Transient Thermal Resistance

14.2 Performance Curves of Control Parts

Figure 14-2 to Figure 14-18 provide performance curves of the control parts integrated in the SIM2602M, including variety-dependent characteristics and thermal characteristics. T_J represents the junction temperature of the control parts.

Table 14-1. Typical Characteristics of Control Parts

Figure Number	Figure Caption
Figure 14-2	Logic Supply Current, I_{CC} vs. T_C
Figure 14-3	Logic Supply Current, I_{CC} vs. VCC Pin Voltage, V_{CC}
Figure 14-4	Logic Supply Current in 1-phase Operation (V_{SP} = 0 V), I_{BS} vs. T_C
Figure 14-5	Logic Supply Current in 1-phase Operation (V_{SP} = 5.5 V), I_{BS} vs. T_C
Figure 14-6	High-side Logic Operation Start Voltage, $V_{BS(ON)}$ vs. T_C
Figure 14-7	High-side Logic Operation Stop Voltage, $V_{BS(OFF)}$ vs. T_C
Figure 14-8	Low-side Logic Operation Start Voltage, $V_{CC(ON)}$ vs. T_C
Figure 14-9	Low-side Logic Operation Stop Voltage, $V_{CC(OFF)}$ vs. T_C
Figure 14-10	UVLO_VB Filtering Time vs. T_C
Figure 14-11	UVLO_VCC Filtering Time vs. T_C
Figure 14-12	High Level Input Current 1 (LA, MLP, CW/CCW, FGSEL, or VSP Pin), I_{IN1} vs. T_C
Figure 14-13	High Level Input Current 2 (OCP Pin), I_{IN2} vs. T_C
Figure 14-14	VREG Pin Voltage, V_{REG} vs. T_C
Figure 14-15	Current Limit Reference Voltage, V_{LIM} vs. T_C
Figure 14-16	OCL Blanking Time, $t_{BK(OCL)}$ + Propagation Delay, t_D vs. T_C
Figure 14-17	OCP Threshold Voltage, V_{TRIP} vs. T_C
Figure 14-18	OCP Hold Time, t_P vs. T_C

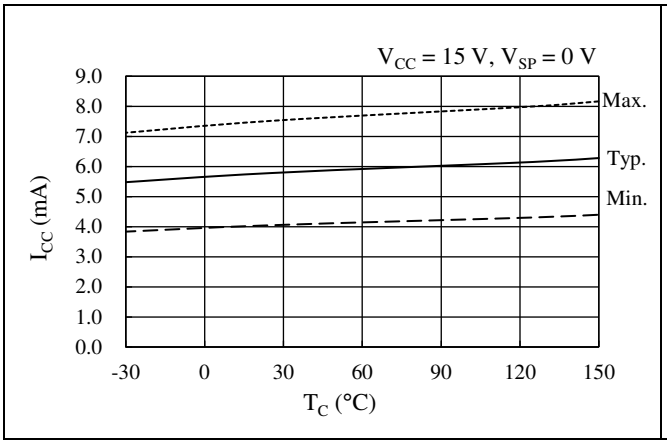


Figure 14-2. Logic Supply Current, I_{CC} vs. T_C

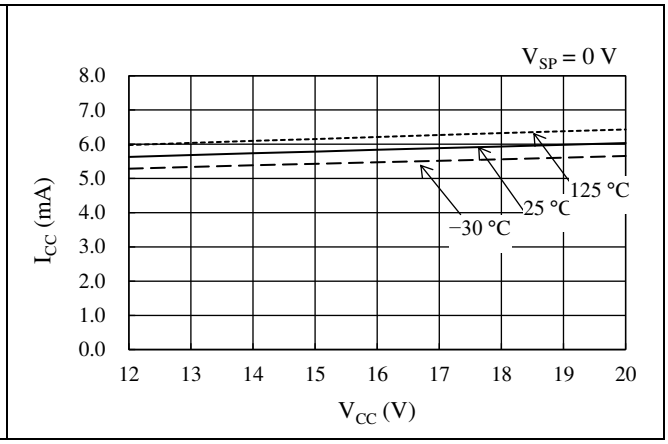


Figure 14-3. Logic Supply Current, I_{CC} vs. VCC Pin Voltage, V_{CC}

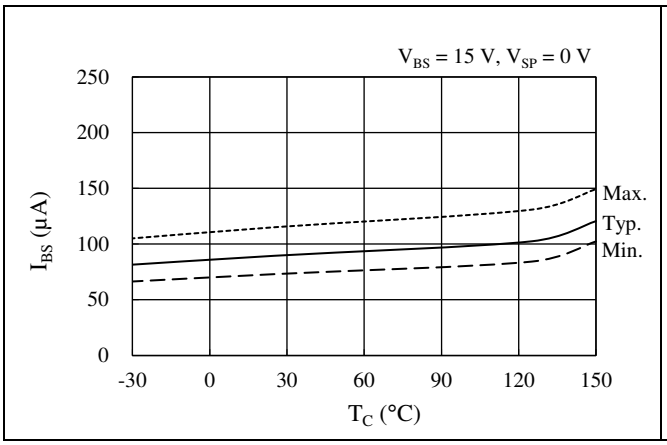


Figure 14-4. Logic Supply Current in 1-phase Operation (V_{SP} = 0 V), I_{BS} vs. T_C

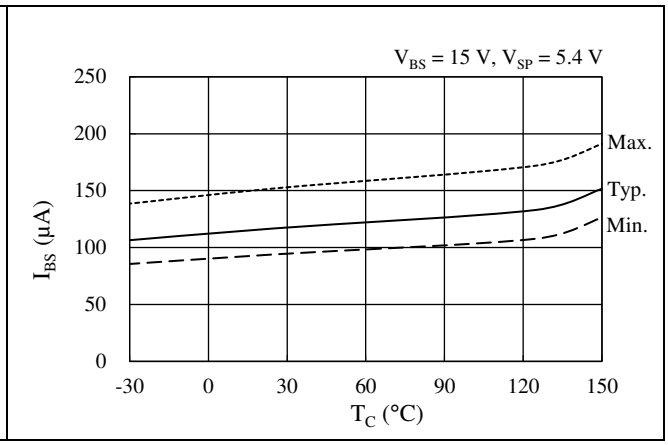


Figure 14-5. Logic Supply Current in 1-phase Operation (VSP = 5.5 V), I_{BS} vs. T_C

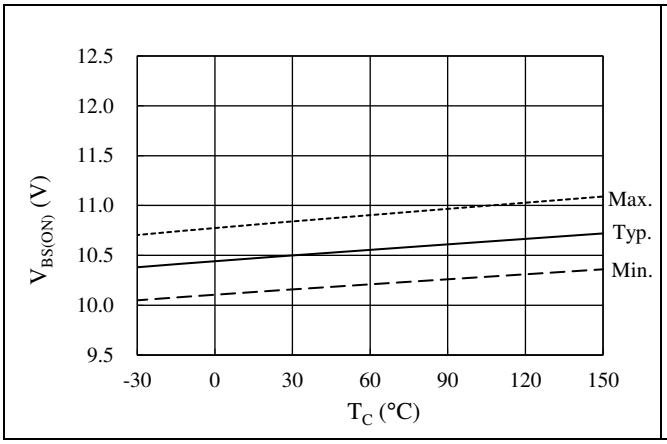


Figure 14-6. High-side Logic Operation Start Voltage, $V_{BS(ON)}$ vs. T_C

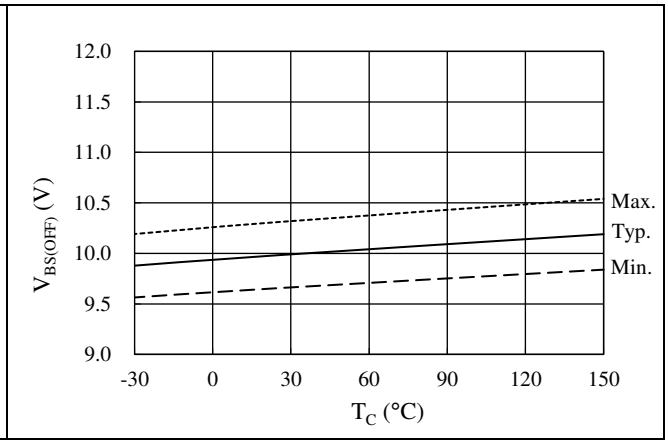


Figure 14-7. High-side Logic Operation Stop Voltage, $V_{BS(OFF)}$ vs. T_C

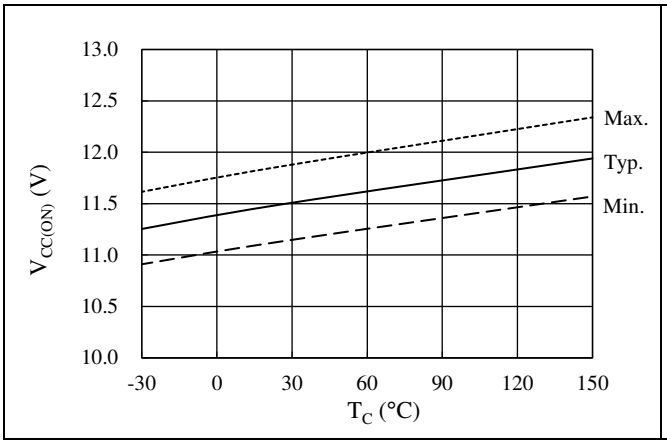


Figure 14-8. Low-side Logic Operation Start Voltage, $V_{CC(ON)}$ vs. T_C

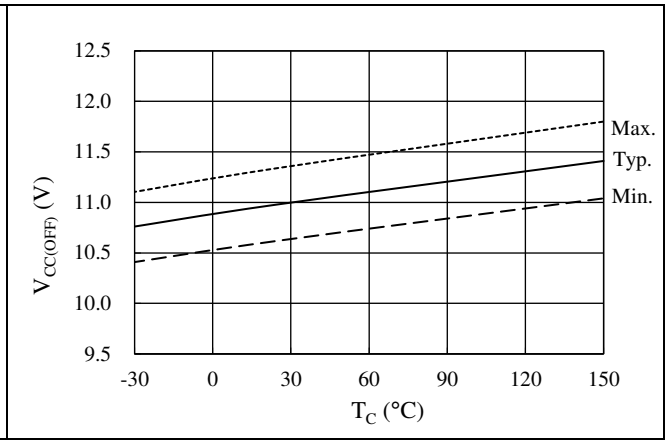


Figure 14-9. Low-side Logic Operation Stop Voltage, $V_{CC(OFF)}$ vs. T_C

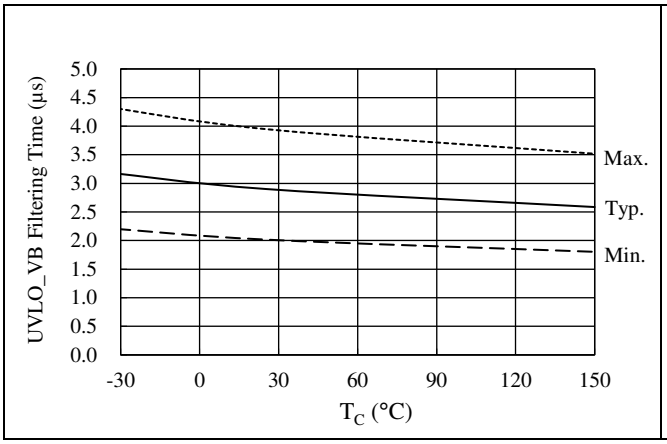


Figure 14-10. UVLO_VB Filtering Time vs. T_C

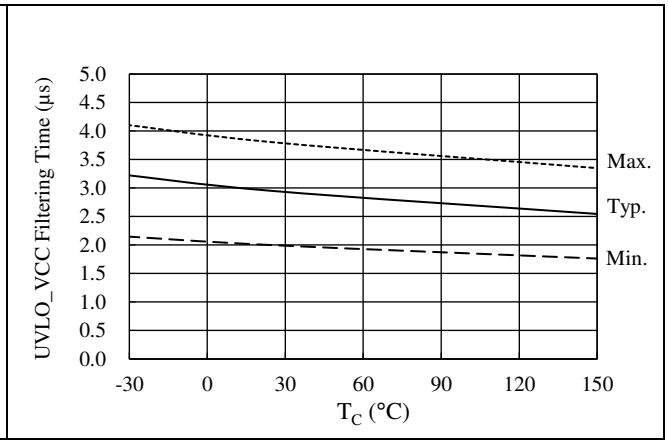


Figure 14-11. UVLO_VCC Filtering Time vs. T_C

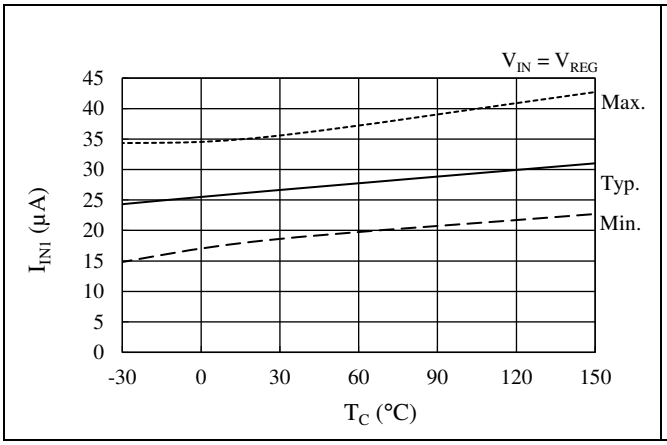


Figure 14-12. High Level Input Current 1 (LA, MLP, CW/CCW, FGSEL, or VSP Pin), I_{IN1} vs. T_C

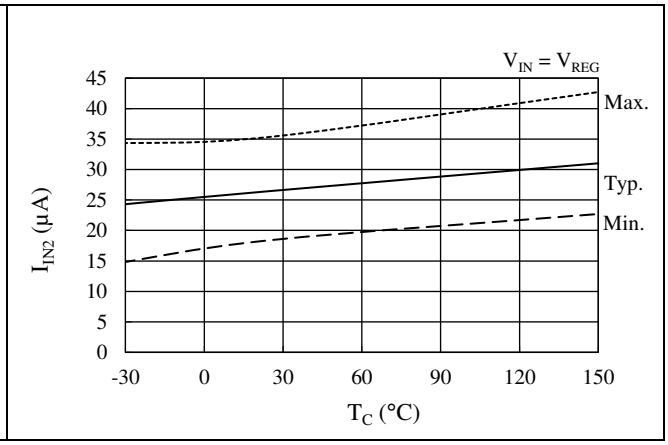


Figure 14-13. High Level Input Current 2 (OCP Pin), I_{IN2} vs. T_C

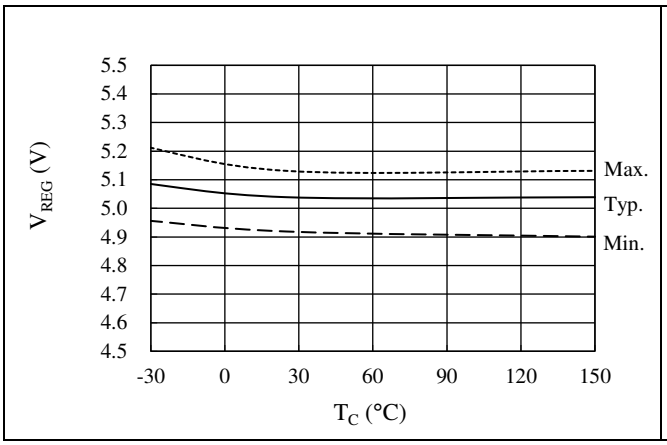


Figure 14-14. VREG Pin Voltage, V_{REG} vs. T_C

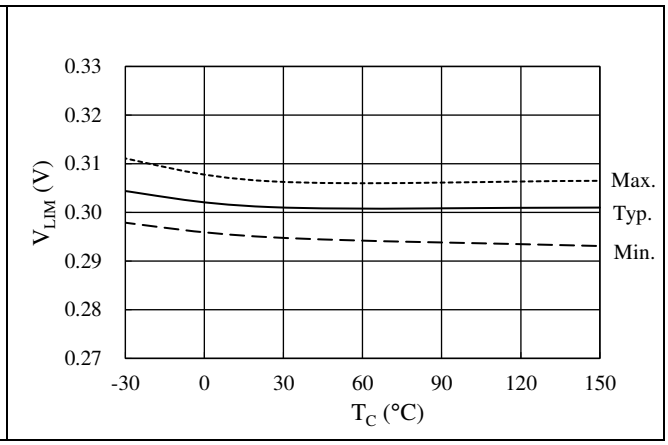


Figure 14-15. Current Limit Reference Voltage, V_{LIM} vs. T_C

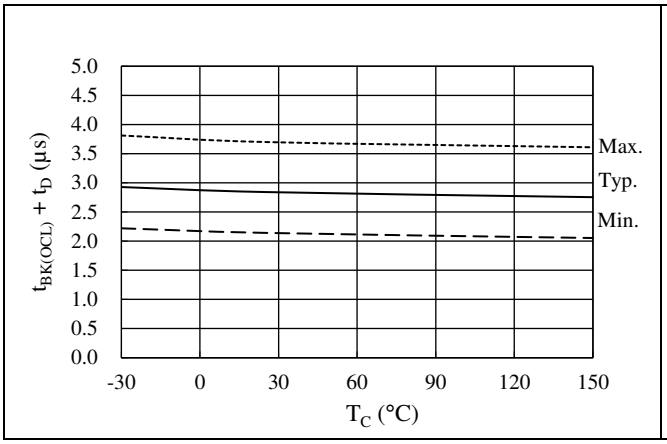


Figure 14-16. OCL Blanking Time, $t_{BK(OCL)}$ + Propagation Delay, t_D vs. T_C

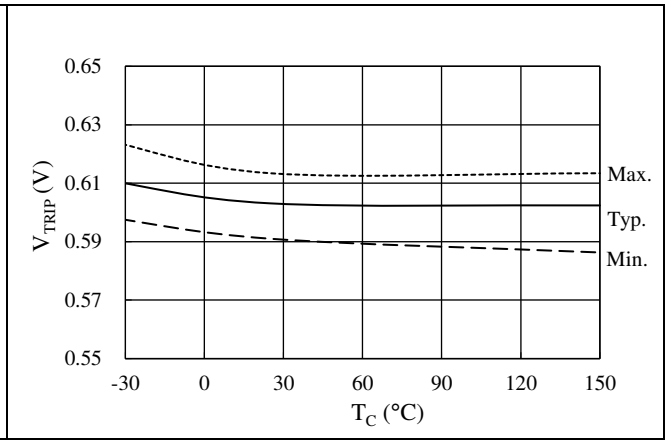


Figure 14-17. OCP Threshold Voltage, V_{TRIP} vs. T_C

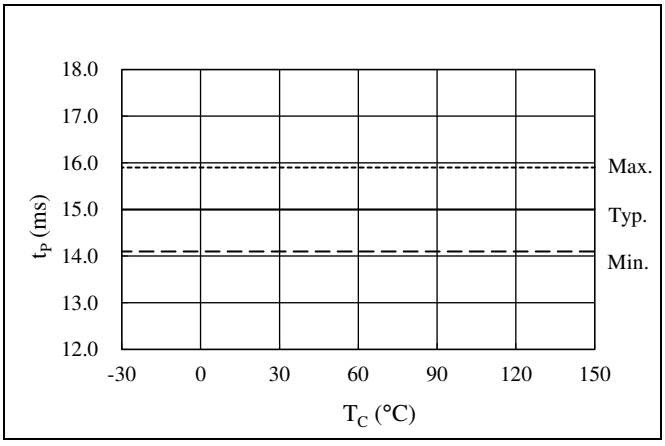


Figure 14-18. OCP Hold Time, t_P vs. T_C

14.3 Performance Curves of Output Parts

14.3.1 Transistor Characteristics

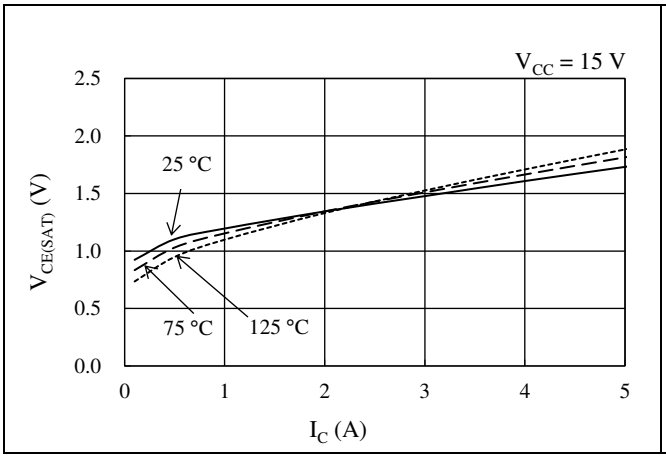


Figure 14-19. IGBT $V_{CE(SAT)}$ vs. I_C

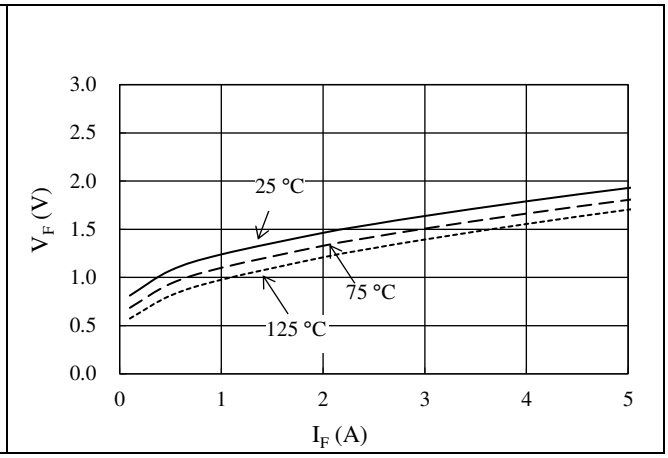


Figure 14-20. Freewheeling Diode V_F vs. I_F

14.3.2 Switching Losses

Conditions: VBBx pin voltage = 300 V, half-bridge circuit with inductive load.
Switching Loss, E, is the sum of turn-on loss and turn-off loss.

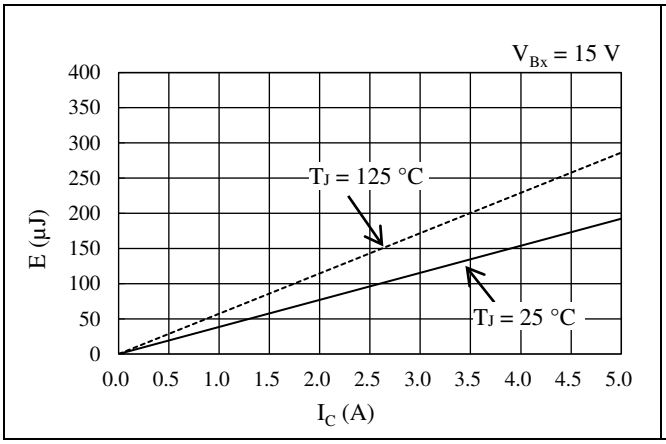


Figure 14-21. High-side Switching Loss

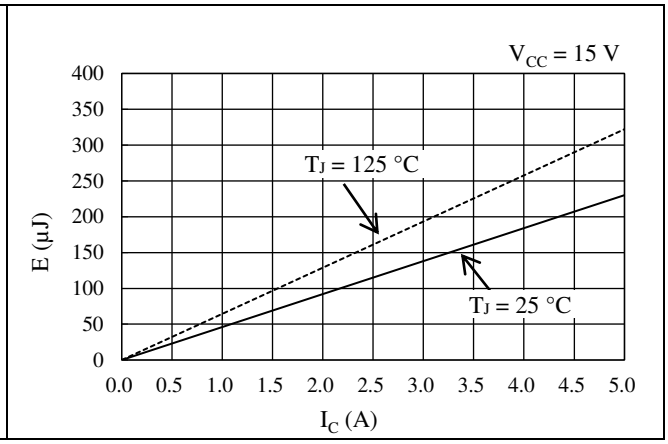


Figure 14-22. Low-side Switching Loss

14.4 Allowable Effective Current Curves

The following curves represent allowable effective currents in 3-phase sine-wave PWM driving with parameters such as typical $R_{DS(ON)}$ or $V_{CE(SAT)}$, and typical switching losses.

Operating conditions: VBBx pin input voltage, V_{DC} = 300 V; VCC pin input voltage, V_{CC} = 15 V; modulation index, M = 0.9; motor power factor, cosθ = 0.8; junction temperature, T_J = 150 °C.

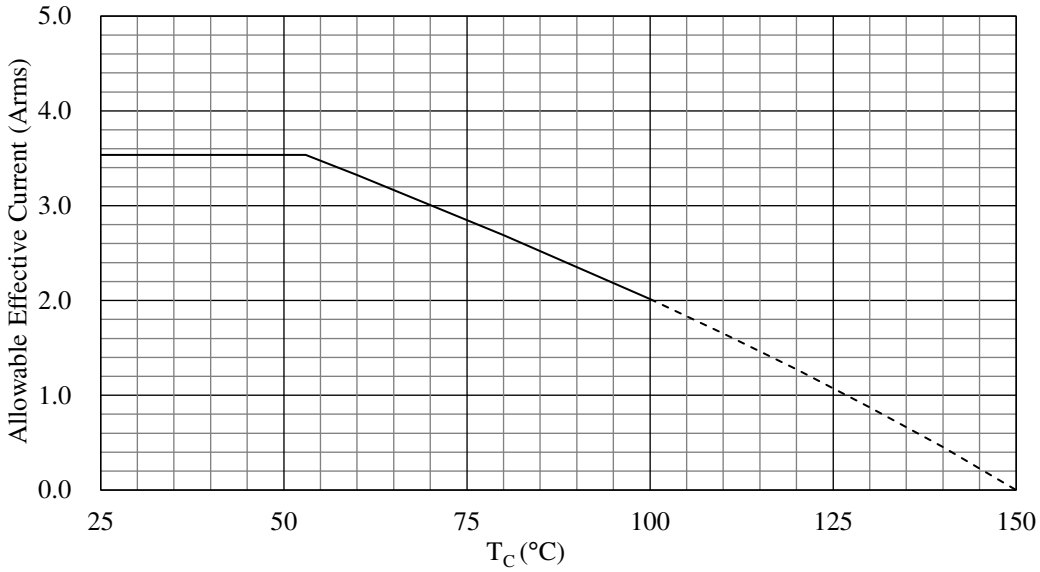


Figure 14-23. Allowable Effective Current (f_C = 17 kHz)

14.5 Short Circuit SOA (Safe Operating Area)

Conditions: $V_{DC} \leq 400$ V, 13.5 V $\leq V_{CC} \leq$ 16.5 V, T_J = 125 °C, 1 pulse.

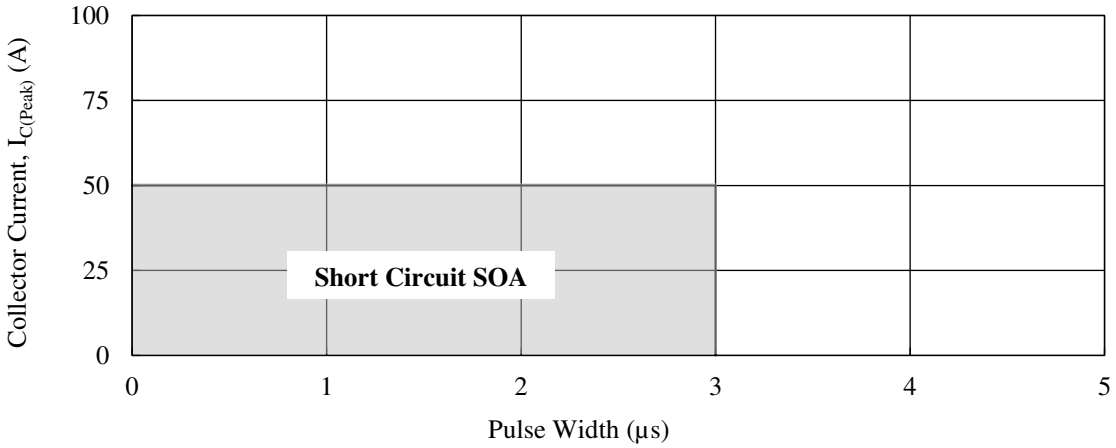
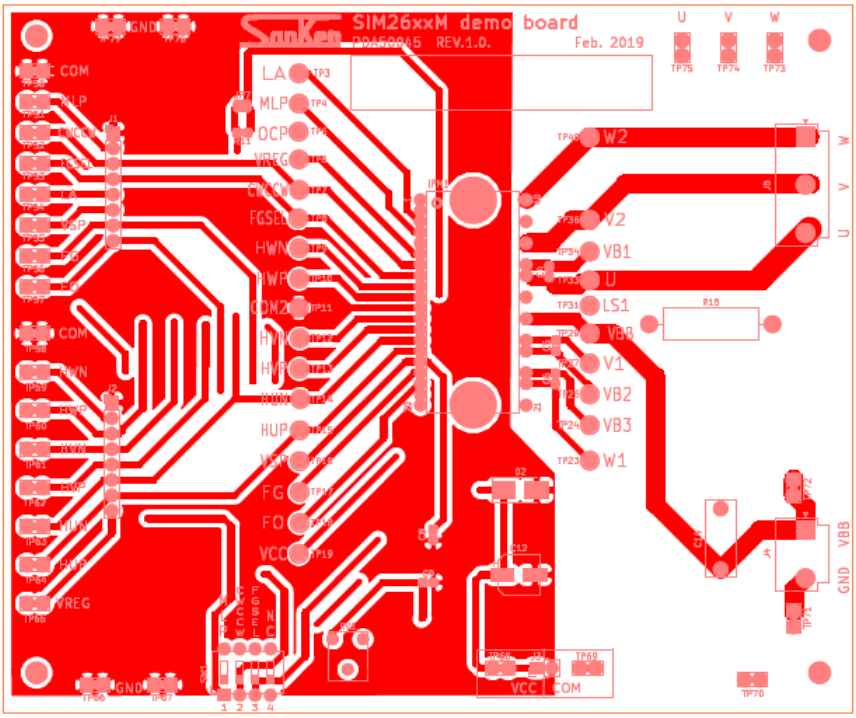


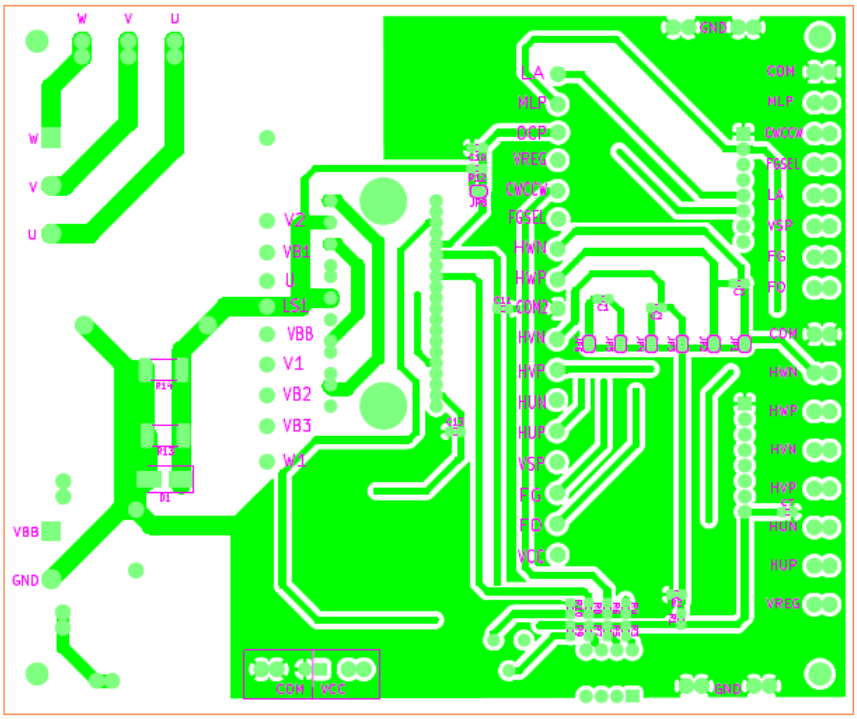
Figure 14-24. Short Circuit SOA

15. Pattern Layout Example

This section contains the schematic diagrams of a PCB pattern layout example using an SIM2602M device. For details on the land pattern example of the IC, see Section 9.



(Top View)



(Bottom View)

Figure 15-1. Pattern Layout Example

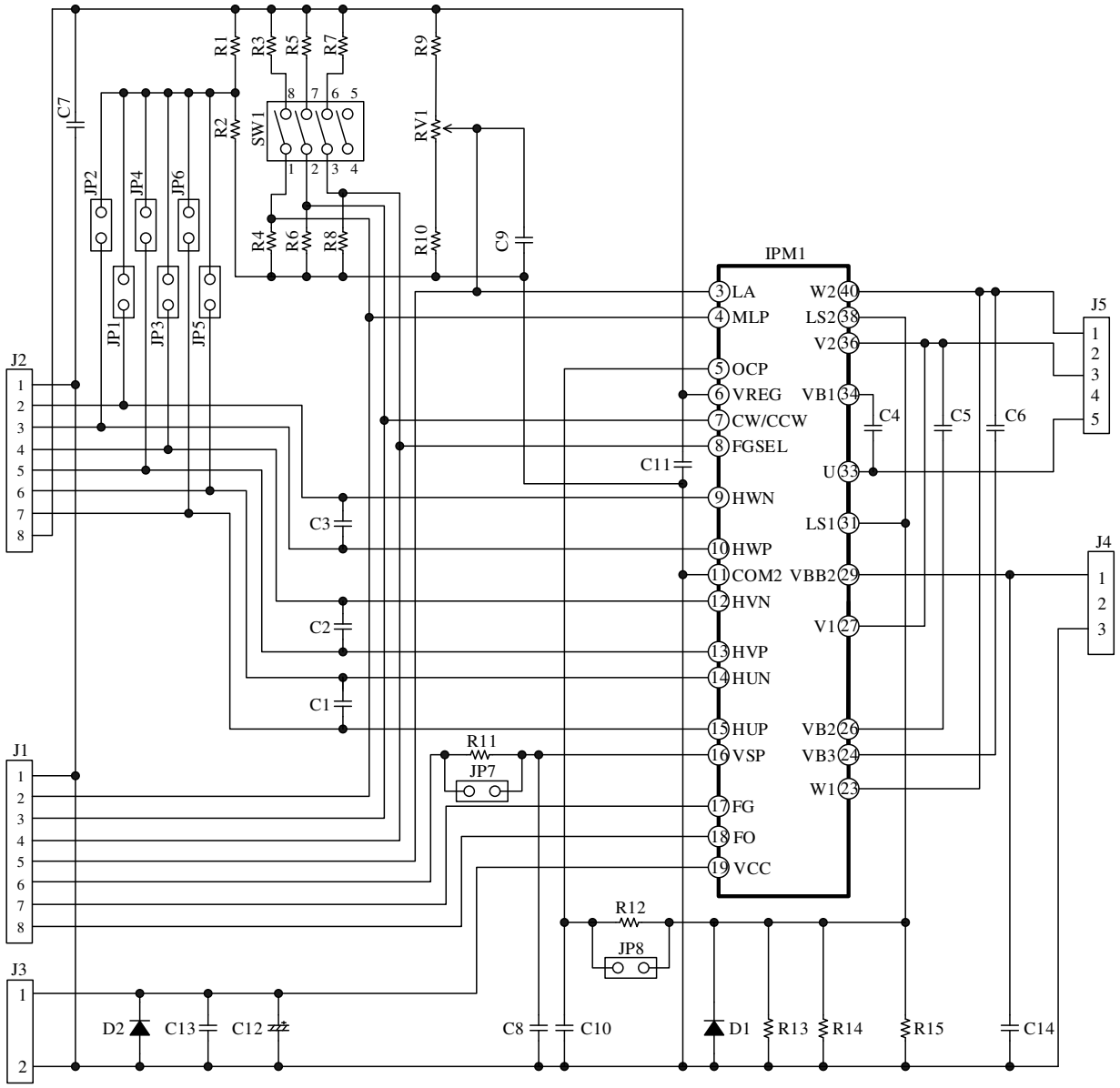


Figure 15-2. Circuit Diagram of PCB Pattern Layout Example

16. Typical Motor Driver Application

This section contains the information on the typical motor driver application (which uses signals input from the Hall elements) listed in the previous section, including a circuit diagram, specifications, and the bill of the materials used.

- **Motor Driver Specifications**

IC	SIM2602M
Main Supply Voltage, V_{DC}	300 VDC (typ.)
Rated Output Power	150 W

- **Circuit Diagram**

See Figure 15-2.

- **Bill of Materials**

Symbol	Part Type	Ratings	Symbol	Part Type	Ratings
C1[1]	Ceramic	Open	R6	General	Open
C2[1]	Ceramic	Open	R7	General	Short
C3[1]	Ceramic	Open	R8	General	Open
C4	Ceramic	1 µF, 35 V	R9	General	Short
C5	Ceramic	1 µF, 35 V	R10	General	1 kΩ, 0.25 W
C6	Ceramic	1 µF, 35 V	R11[2]	General	Open
C7	Ceramic	0.1 µF, 35 V	R12	General	100 Ω, 0.25 W
C8	Ceramic	0.1 µF, 35 V	R13	Metal plate	0.33 Ω, 1 W
C9	Ceramic	0.1 µF, 35 V	R14	Metal plate	0.33 Ω, 1 W
C10	Ceramic	2200 pF, 35 V	R15	Metal plate	Open
C11	Ceramic	0.1 µF, 35 V	RV1	Trimmer	10 kΩ, 0.25 W
C12	Electrolytic	100 µF, 35 V	SW1	Switch	1 × 04
C13	Ceramic	0.1 µF, 35 V	JP1[3][4]	Jumper	Open
C14	Ceramic	0.1 µF, 630 V	JP2[3][4]	Jumper	Open
J1	Pin header	1 n he	JP3[3][4]	Jumper	Open
J2	Pin header	1 n he	JP4[3][4]	Jumper	Open
J3	Pin header	1 n he	JP5[3][4]	Jumper	Open
J4	Pin header	Equiv. to B2P3-VH	JP6[3][4]	Jumper	Open
J5	Pin header	Equiv. to B3P5-VH	JP7[5]	Jumper	Short
R1	General	2.2 kΩ, 0.25 W	JP8	Jumper	Open
R2	General	2.2 kΩ, 0.25 W	D1	General	1 A, 50 V
R3	General	Short	D2	Zener	V_Z = 20 V, 0.5 W
R4	General	Open	IPM1	IC	SIM2602M
R5	General	Short			

[1] Refers to a noise filter capacitor for Hall element signals; should be connected as needed.
[2] Refers to a noise filter resistor for a motor speed control signal input to the VSP pin; should be connected as needed.
[3] When inputting Hall IC signals for detecting a south pole: set JP1, JP3, JP5 = short; set JP2, JP4, JP6 = open.
[4] When inputting Hall IC signals for detecting a north pole: set JP1, JP3, JP5 = open; set JP2, JP4, JP6 = short.
[5] Should be opened when R11 is connected; should be shorted when R11 is not connected.

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