19-2911 Rev 3; 8/06

EVALUATION KIT AVAILABLE

EEPROM-Programmable TFT VCOM Calibrator

General Description

The MAX1512 is a programmable VCOM-adjustment solution for thin-film transistor (TFT) liquid-crystal displays (LCDs). The MAX1512 simplifies the labor-intensive VCOM-adjustment process and replaces mechanical potentiometers, which significantly reduces labor costs, increases reliability, and enables automation.

The MAX1512 attaches to an external resistive voltage-divider and sinks a programmable current to set the VCOM voltage level. An internal 7-bit digital-to-analog converter (DAC) controls the sink current. The DAC is ratiometric relative to AVDD and is guaranteed to be monotonic over all operating conditions. This VCOM calibrator IC includes an EEPROM to store the desired VCOM voltage level. The EEPROM can be programmed repeatedly, giving TFT LCD manufacturers the flexibility to calibrate the display panel as many times as the manufacturing process requires.

The IC features a single-wire interface between the LCD panel and the programming circuit. The single-wire interface delivers both programming power and DAC-adjustment commands to minimize changes to panel connectors and production equipment. The MAX1512 is available in an 8-pin 3mm x 3mm TDFN package. A complete evaluation kit is available to simplify evaluation and production development.

Applications

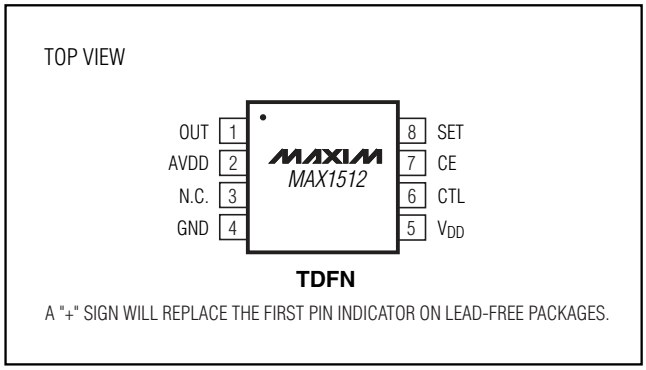
LCD Panels

Notebook Computers

Monitors

LCD TVs

Pin Configuration



*Patent Pending.

Features

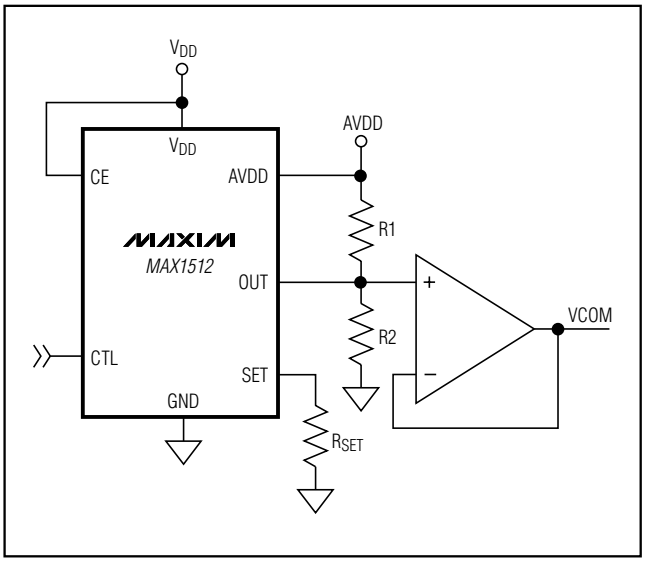
- **7-Bit Adjustable Sink-Current Output**
- **Resistor-Adjustable Full-Scale Range**
- **Guaranteed Monotonic Output Over Operating Range**
- **Single-Wire Adjustment and Programming***
- **EEPROM Stores VCOM Setting**
- **Interface Enable/Disable Control (CE)**
- **2.6V to 3.6V Logic Supply-Voltage Operating Range (V_{DD})**
- **4.5V to 20V Analog Supply-Voltage Range (V_{AVDD})**
- **V_{DD} UVLO Protection**
- **8-Pin 3mm x 3mm TDFN (0.8mm max)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1512ETA	-40°C to +85°C	8 TDFN 3mm x 3mm
MAX1512ETA+	-40°C to +85°C	8 TDFN 3mm x 3mm

+Denotes lead-free package.

Typical Operating Circuit



EEPROM-Programmable TFT VCOM Calibrator

ABSOLUTE MAXIMUM RATINGS

V_{DD}, SET, CE to GND .....-0.3V to +4V
OUT to GND .....-0.3V to +14V
AVDD to GND .....-0.3V to +24V
CTL to GND .....-0.3V to +16V
Continuous Power Dissipation (T_A = +70°C) .....
8-Pin Thin QFN 3mm x 3mm (derate 24.4mW/°C above +70°C) 1951mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V_{DD} = 3V, V_{AVDD} = 10V, V_{OUT} = 5V, R_{SET} = 30.1kΩ, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SINK-CURRENT ADJUSTMENT						
SET Voltage Resolution			7			Bits
SET Differential Nonlinearity		Guaranteed monotonic	-1		+1	LSB
SET Zero-Scale Error			-1	+1	+2	LSB
SET Full-Scale Error			-12		+12	LSB
SET Current	I_{SET}				120	µA
SET External Resistance (Note 2)	R_{SET}	To GND, V_{AVDD} = 20V	10		200	kΩ
		To GND, V_{AVDD} = 4.5V	2.25		45.00	
V_{SET} / V_{AVDD} Voltage Ratio		DAC full scale		0.05		V/V
V_{SET} / V_{AVDD} Factory-Set Voltage Ratio			0.024	0.025	0.026	V/V
V_{DD} SUPPLY						
V_{DD} Supply Range	V_{DD}		2.6		3.6	V
V_{DD} Supply Current	I_{DD}	CE = V_{DD}		32	55	µA
		CE = GND		12	20	
V_{DD} Power-On Reset Threshold		Rising edge	2.2	2.5	2.7	V
		Falling edge	2.1	2.4	2.6	
V_{DD} Power-On Reset Hysteresis				100		mV
CONTROL AND PROGRAMMING						
CE Input Low Voltage		2.6V < V_{DD} < 3.6V			0.4	V
CE Input High Voltage		2.6V < V_{DD} < 3.6V	1.6			V
CE Startup Time		(Note 3)			1	ms
CTL High Voltage		2.6V < V_{DD} < 3.6V	0.70 x V_{DD}		0.82 x V_{DD}	V
CTL Float Voltage		2.6V < V_{DD} < 3.6V	0.40 x V_{DD}		0.62 x V_{DD}	V
CTL Low Voltage		2.6V < V_{DD} < 3.6V	0.20 x V_{DD}		0.32 x V_{DD}	V
CTL Rejected Pulse Width			20			µs
CTL Minimum Pulse Width					200	µs
CTL Minimum Time Between Pulses					10	µs
CTL Input Current		CTL = GND	-10			µA
		CTL = V_{DD}			10	

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{DD} = 3V, V_{AVDD} = 10V, V_{OUT} = 5V, R_{SET} = 30.1kΩ, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CTL EEPROM Program Voltage	V_{PP}	(Note 3)	15.25	15.5	15.75	V
OUTPUT VOLTAGE						
OUT Leakage Current		V_{DD} = 2.1V		1		nA
OUT Settling Time		To ±0.5 LSB error band		20		µs
V_{OUT} Voltage Range	V_{OUT}		V_{SET} + 0.5V		13	V
AVDD SUPPLY						
V_{AVDD} Supply Range	V_{AVDD}		4.5		20.0	V
AVDD Operating Current	I_{AVDD}	V_{DD} = 2.1V, V_{AVDD} = 20V		0.04		µA
		V_{AVDD} = 20V		10	20	

ELECTRICAL CHARACTERISTICS

(V_{DD} = 3V, V_{AVDD} = 10V, V_{OUT} = 5V, R_{SET} = 30.1kΩ, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SINK-CURRENT ADJUSTMENT						
SET Differential Nonlinearity		Guaranteed monotonic	-1		+1	LSB
SET Zero-Scale Error			-1		+2	LSB
SET Full-Scale Error			-12		+12	LSB
SET Current	I_{SET}				120	µA
SET External Resistance (Note 2)	R_{SET}	To GND, V_{AVDD} = 20V	10		200	kΩ
		To GND, V_{AVDD} = 4.5V	2.25		45.00	
V_{DD} SUPPLY						
V_{DD} Supply Range	V_{DD}		2.6		3.6	V
V_{DD} Supply Current	I_{DD}	CE = V_{DD}			55	µA
		CE = GND			20	
V_{DD} Power-On Reset Threshold		Rising edge	2.2		2.7	V
		Falling edge	2.1		2.6	
CONTROL AND PROGRAMMING						
CE Input Low Voltage		2.6V < V_{DD} < 3.6V			0.4	V
CE Input High Voltage		2.6V < V_{DD} < 3.6V	1.6			V
AVDD SUPPLY						
V_{AVDD} Supply Range	V_{AVDD}		4.5		20.0	V
AVDD Operating Current	I_{AVDD}	V_{AVDD} = 20V			20	µA

Note 1: Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed through correlation using standard quality control (SQC) methods.

Note 2: SET external resistor range is verified at DAC full scale.

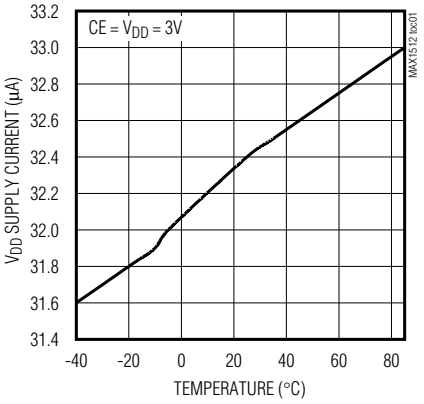
Note 3: Guaranteed by design. Not production tested.

EEPROM-Programmable TFT VCOM Calibrator

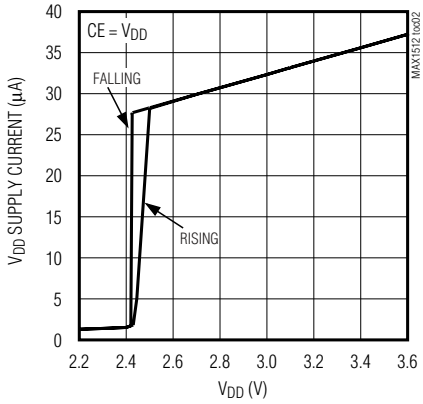
Typical Operating Characteristics

(Circuit of Figure 1, V_{DD} = 3V, V_{AVDD} = 10V, V_{OUT} = 5V, R_{SET} = 24.9kΩ, T_A = +25°C, DAC half scale, unless otherwise noted.)

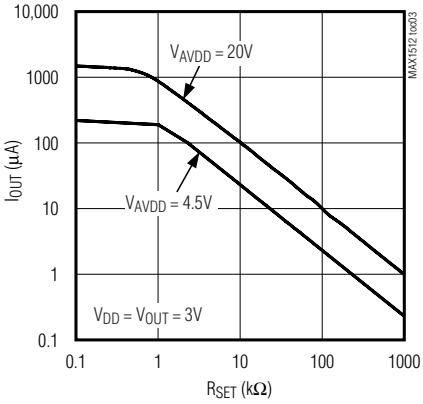
V_{DD} SUPPLY CURRENT vs. TEMPERATURE



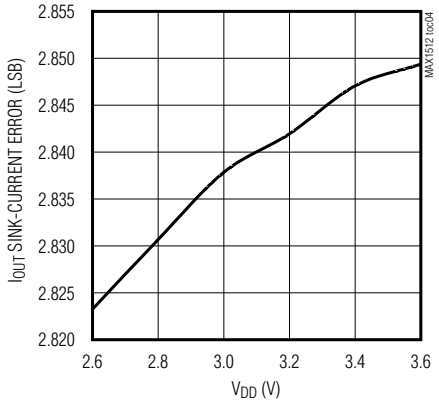
V_{DD} SUPPLY CURRENT vs. V_{DD}



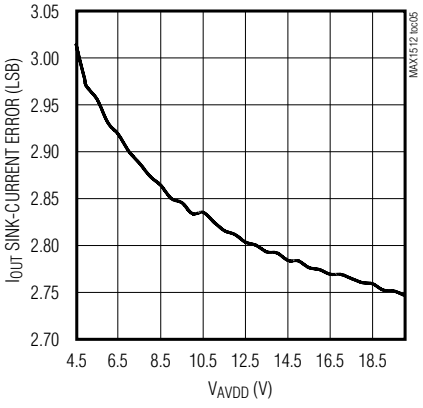
I_{OUT} vs. R_{SET}



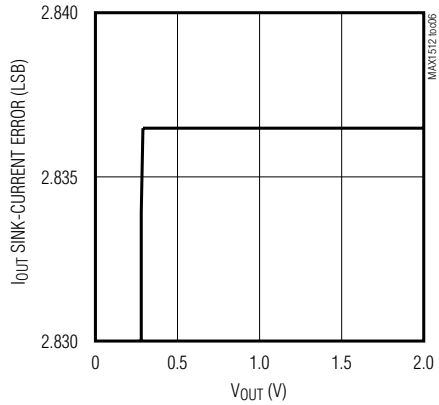
I_{OUT} SINK-CURRENT ERROR vs. V_{DD}



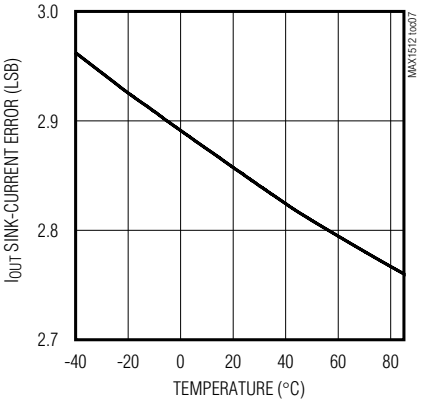
I_{OUT} SINK-CURRENT ERROR vs. V_{AVDD}



I_{OUT} SINK-CURRENT ERROR vs. V_{OUT}



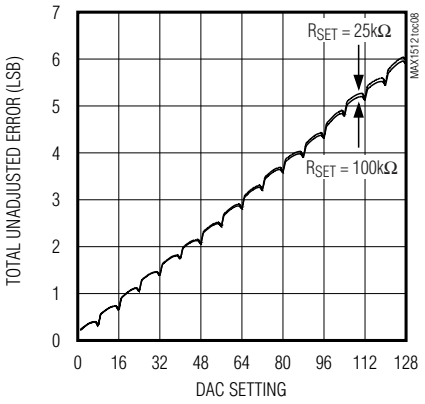
I_{OUT} SINK-CURRENT ERROR vs. TEMPERATURE



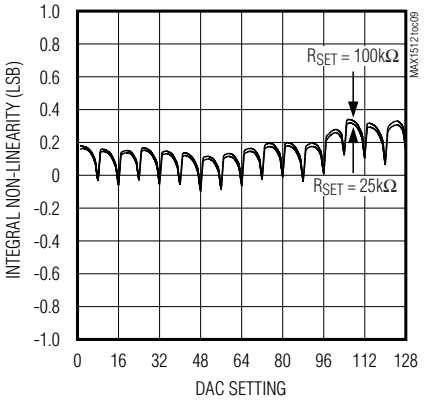
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{DD} = 3V, V_{AVDD} = 10V, V_{OUT} = 5V, R_{SET} = 24.9kΩ, T_A = +25°C, DAC half scale, unless otherwise noted.)

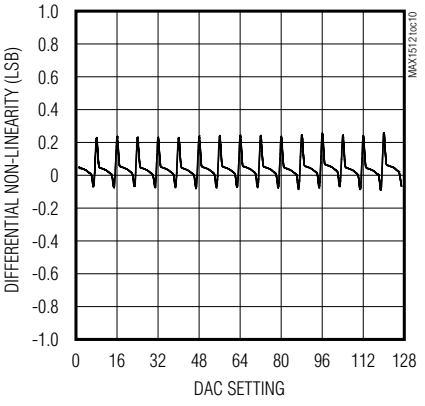
TOTAL UNADJUSTED ERROR vs. DAC SETTING



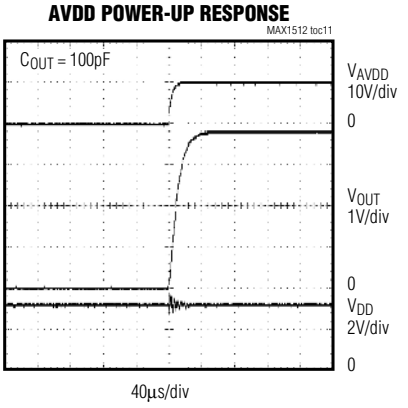
INTEGRAL NONLINEARITY vs. DAC SETTING



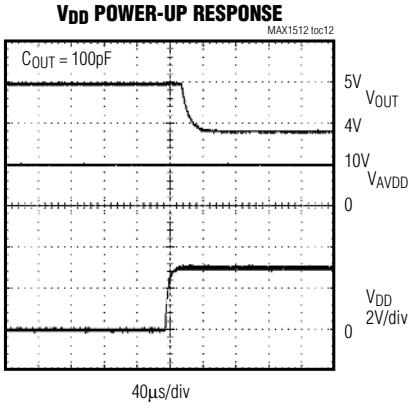
DIFFERENTIAL NONLINEARITY vs. DAC SETTING



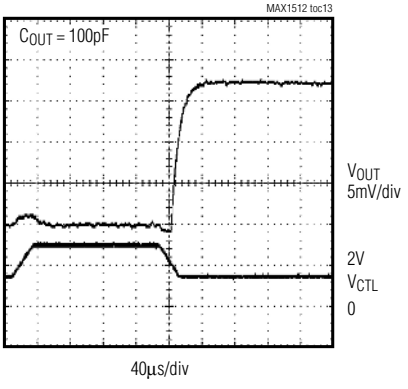
AVDD POWER-UP RESPONSE



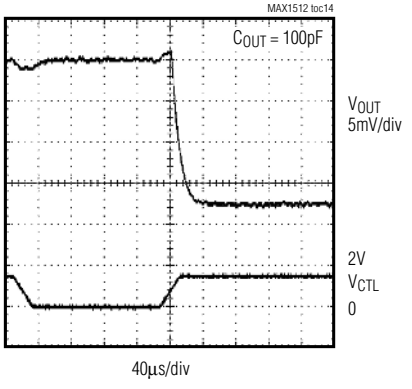
V_{DD} POWER-UP RESPONSE



SINGLE LSB STEP-UP RESPONSE



SINGLE LSB STEP-DOWN RESPONSE



EEPROM-Programmable TFT VCOM Calibrator

Pin Description

PIN	NAME	FUNCTION
1	OUT	Adjustable Sink-Current Output. OUT connects to the resistive voltage-divider between AVDD and GND that sets the VCOM voltage. I_{OUT} lowers the divider voltage by an adjustable amount. See the SET pin description.
2	AVDD	High-Voltage Analog Supply. Connects to the panel source-driver supply rail.
3	N.C.	No Connect. Not internally connected.
4	GND	Ground
5	V_{DD}	Supply Input. +2.6V to +3.6V input range.
6	CTL	VCOM Adjustment and EEPROM Programming Control. CTL sets the internal DAC code and programs the EEPROM. A pulse-control method is used to adjust the VCOM level. See the *VCOM Adjustment (CTL)* section. To program the DAC setting into the EEPROM as the power-on default, drive CTL to the EEPROM programming voltage using the correct timing and voltage ramp rates. See the *EEPROM Programming (CTL)* section.
7	CE	Control Interface Enable. Connect CE to V_{DD} to enable the CTL input. Connect CE to GND to disable the CTL input and reduce the supply current.
8	SET	Full-Scale Sink-Current Adjustment Input. Connect a resistor, R_{SET}, from SET to GND to set the full-scale adjustable sink current. The full-scale adjustable sink current is equal to: $\left(\frac{V_{AVDD}}{20 \times R_{SET}}\right)$ I_{OUT} is equal to the current through R_{SET}.

Detailed Description

The MAX1512 is a solid-state alternative to mechanical potentiometers used for adjusting the LCD backplane voltage (VCOM) in TFT LCD displays. The MAX1512 attaches to an external resistive voltage-divider and sinks a programmable current (I_{OUT}), which sets the VCOM level (Figure 1). An internal 7-bit DAC controls the sink current and allows the user to increase or decrease the VCOM level (Figure 2). The DAC is ratiometric relative to AVDD and is monotonic over all operating conditions. The user can store the DAC setting in an internal EEPROM. On power-up, the EEPROM presets the DAC to the last stored setting. The single-wire interface between the LCD panel and the programming circuit adjusts the DAC, programs the EEPROM, and provides programming power.

The resistive voltage-divider and the AVDD supply set the maximum value of VCOM. The MAX1512 sinks current from the voltage-divider to reduce the VCOM level. The external resistor R_{SET} sets the full-scale sink current and the minimum value of VCOM.

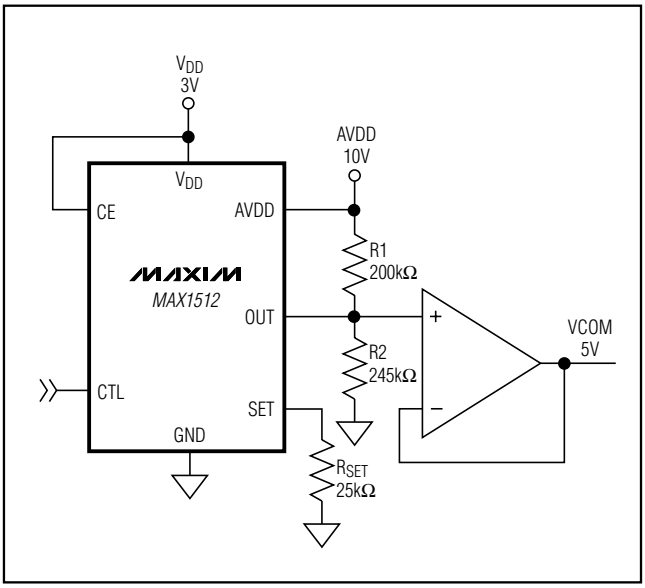


Figure 1. Standard Application Circuit

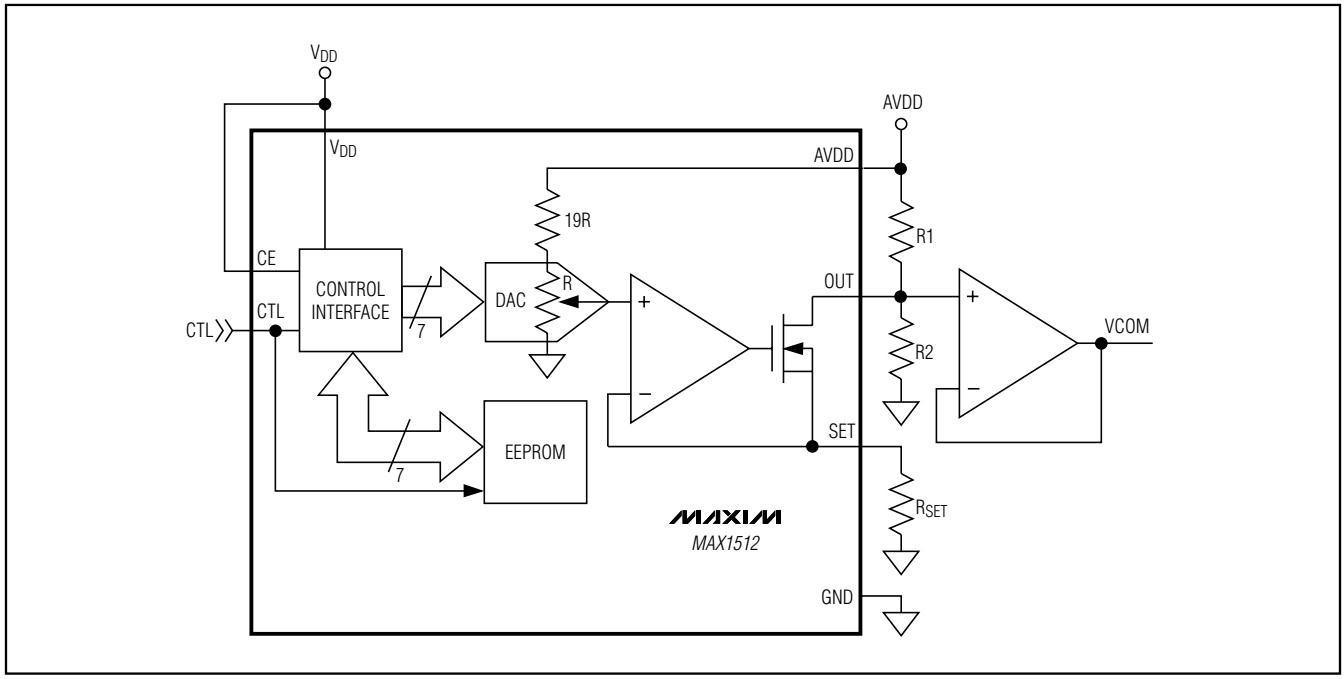


Figure 2. Simplified Functional Diagram

Setting the VCOM Adjustment Range (R_{SET})

The external resistive voltage-divider sets the maximum value of the VCOM adjustment range. R_{SET} sets the full-scale sink current, I_{OUT}, which determines the minimum value of the VCOM adjustment range. Large R_{SET} values increase resolution but decrease the VCOM adjustment range. Calculate R1, R2, and R_{SET} using the following procedure:

1) Choose the maximum VCOM level (V_{MAX}), the minimum VCOM level (V_{MIN}), and the AVDD supply voltage (V_{AVDD}).
2) Calculate the R1 / R2 ratio:

$$\frac{R1}{R2} \cong \frac{V_{AVDD}}{V_{MAX}} - 1$$

3) Calculate the R1 / R_{SET} ratio:

$$\frac{R1}{R_{SET}} \cong \frac{(V_{MAX} - V_{MIN})}{V_{MAX}} \times 20$$

4) Choose R_{SET} according to the limits shown in the *Electrical Characteristics* section and calculate the values for R1 and R2.
5) The resulting resolution is:

$$\text{Resolution} = \frac{(V_{MAX} - V_{MIN})}{127}$$

A complete design example is given below:

1) V_{MAX} = 5V, V_{MIN} = 3V, V_{AVDD} = 10V

2) $$\frac{R1}{R2} \cong \frac{10}{5} - 1 = 1$$

3) $$\frac{R1}{R_{SET}} = 20 \times \frac{(5-3)}{5} = 8$$

4) If R_{SET} = 24.9kΩ, then R1 = 200kΩ and R2 = 200kΩ
5) Resolution = 15.75mV

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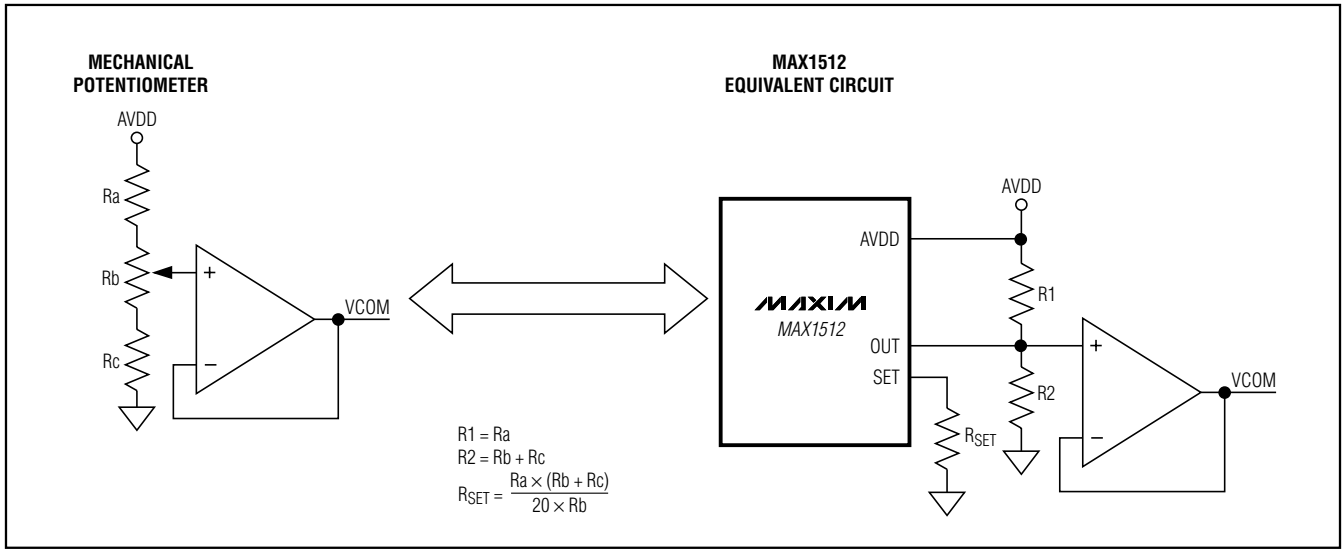

Figure 3. Replacement of Mechanical/Potentiometer Circuit

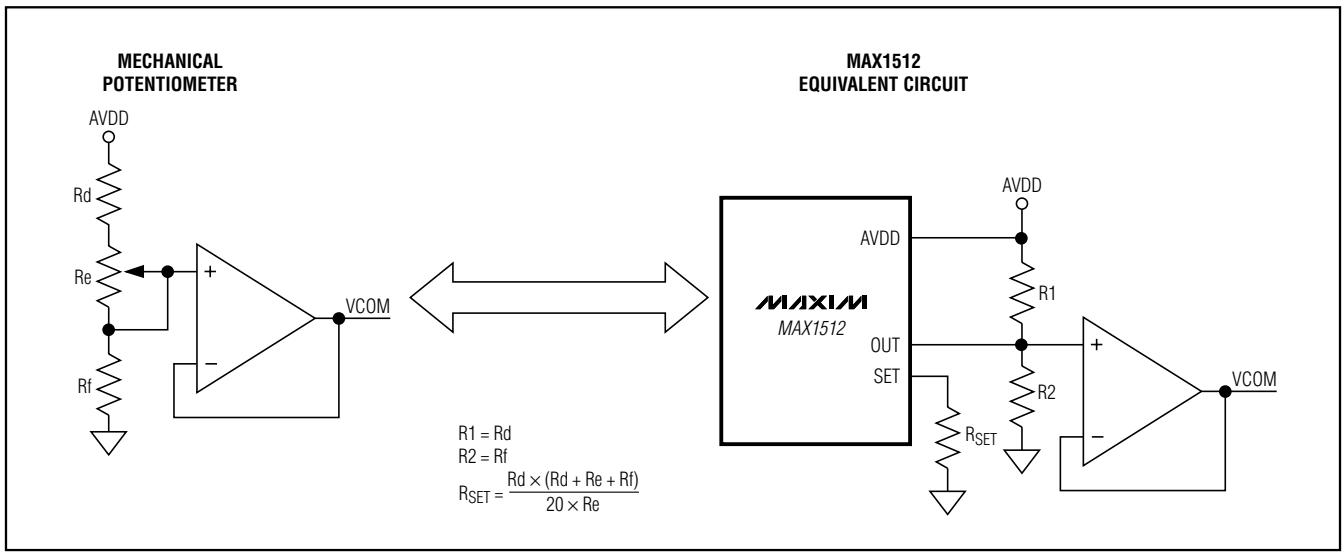

Figure 4. Replacement of Mechanical/Potentiometer Circuit

Translating Existing Potentiometer Circuits

Existing VCOM adjustment circuits using conventional mechanical potentiometers can be translated into MAX1512 circuits. Figures 3 and 4 show two common adjustment circuits and their equivalent MAX1512 circuits.

Interface Enable/Disable (CE)

The MAX1512 control interface can be disabled to reduce the V_{DD} supply current. Connect CE to GND to reduce the typical supply current from 32µA to 12µA. Connect CE to V_{DD} to enable the control interface.

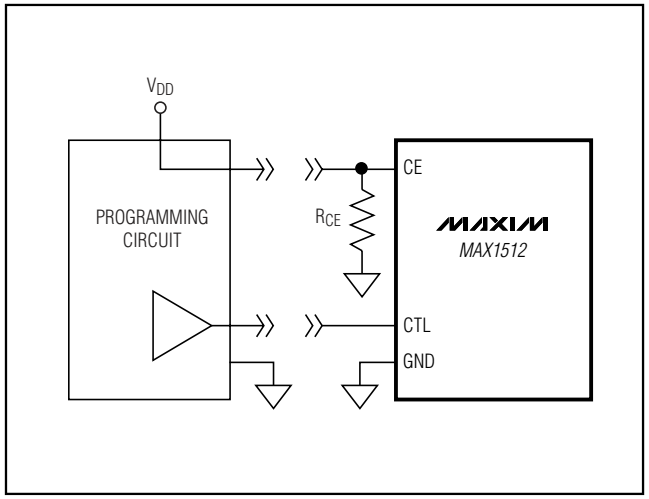

Figure 5. Optional Circuit to Drive CE

The programming circuit in Figure 5 drives CE high to enable the CTL input when it is connected. When the programming circuit is not connected, CE is pulled low through resistor R_{CE}, which disables the CTL input. The CTL input is relatively immune to noise and brief voltage transients. It can be safely left continuously enabled if higher supply current is acceptable.

VCOM Adjustment (CTL)

Pulse CTL low for more than 200µs to increment the DAC setting, which increases the OUT sink current and lowers the VCOM level by 1 least-significant bit (LSB) (Figure 6). Similarly, pulse CTL high for more than 200µs to decrement the DAC setting, which decreases the OUT sink current and increases the VCOM level by 1 LSB.

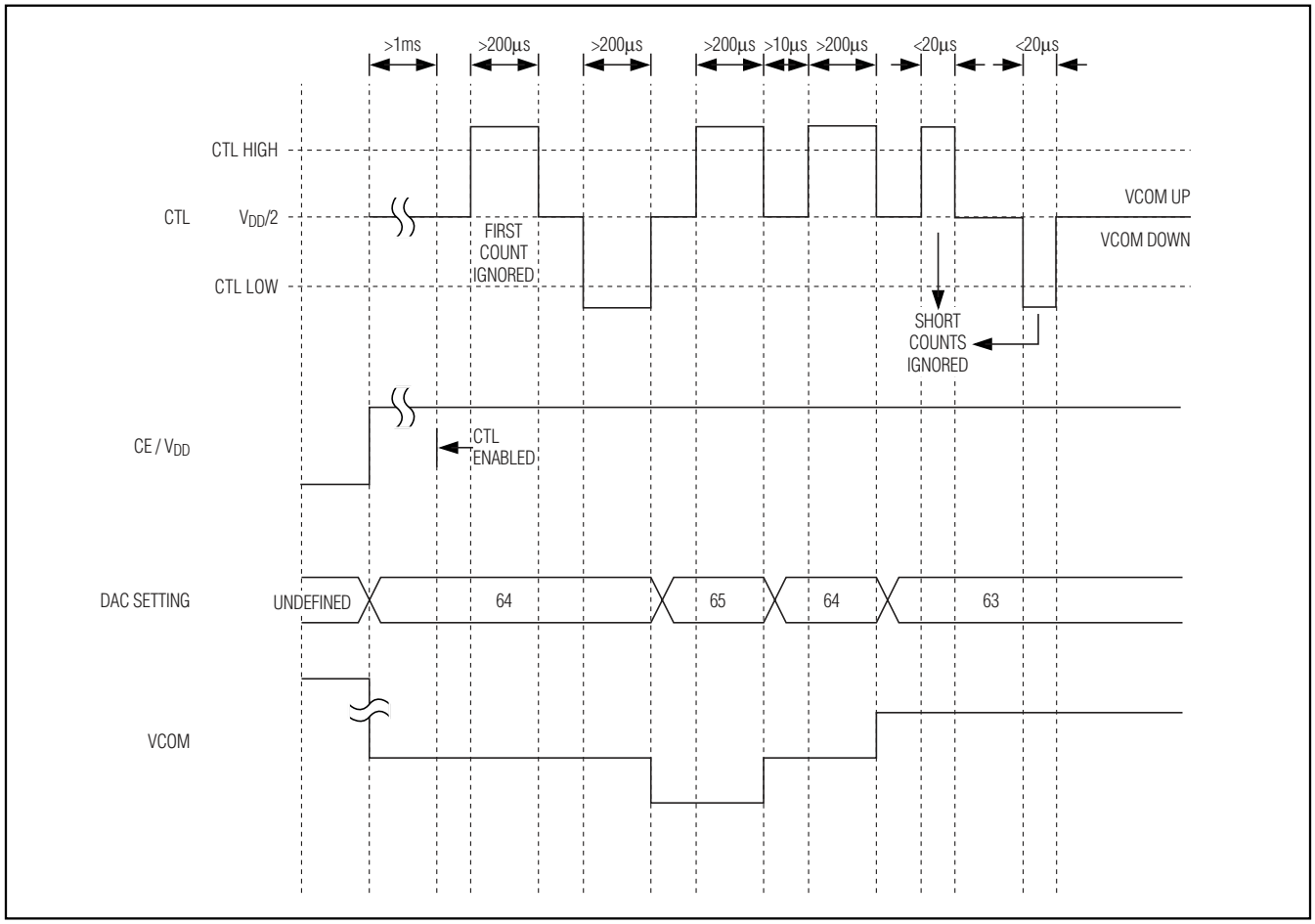

Figure 6. VCOM Adjustment

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To avoid unintentional VCOM adjustment, the MAX1512 is guaranteed to reject CTL pulses shorter than 20µs. In addition, to avoid the possibility of a single false pulse caused by power-up sequencing between V_{DD} and CTL, the very first pulse is ignored.

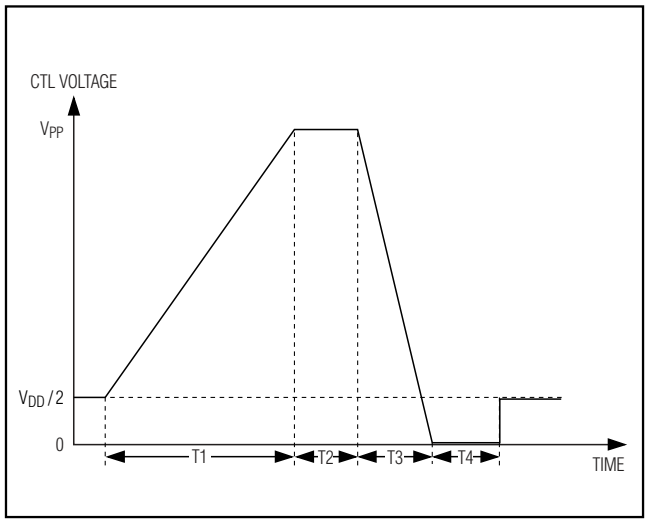


Figure 7. EEPROM Programming

EEPROM Programming (CTL)

To program the EEPROM, apply the EEPROM programming waveform through the CTL interface (Figure 7). The control interface delivers programming power and DAC adjustment commands on the same wire. This single-wire approach minimizes the number of connections from the programming circuit to the LCD panel.

To apply the EEPROM programming waveform, carefully ramp CTL from midscale (V_{DD} / 2) to the programming voltage, V_{PP}, in 7.5ms as shown in Figure 7. If the ramp is generated digitally, use at least 45 steps to achieve the required 320mV ramp resolution. During the ramp time, VCOM adjustment is disabled and the EEPROM cells are biased in preparation for programming. After reaching V_{PP}, hold CTL at V_{PP} for 1ms. During the EFPROM program time, the EEPROM stores the DAC setting. Next, drive CTL to ground in less than 1ms and hold for at least 200µs. Finally, drive CTL to V_{DD} / 2 to complete the write cycle. The EEPROM is factory set to half scale. Follow the *EEPROM Programming Specifications* in Table 1 to guarantee reliable EEPROM programming. Violating the specifications can damage the EEPROM or affect data retention.

A complete evaluation kit is available to simplify evaluation and production development.

Table 1. EEPROM Programming Specifications

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
CTL Programming Voltage	V_{PP}	15.25	15.5	15.75	V
CTL Programming Ramp	T1	7.0	7.5	8.0	ms
EEPROM Program Time	T2	0.9	1.0	1.1	ms
V_{PP} Fall Time	T3	10		1000	µs
Done Hold Time	T4	200			µs

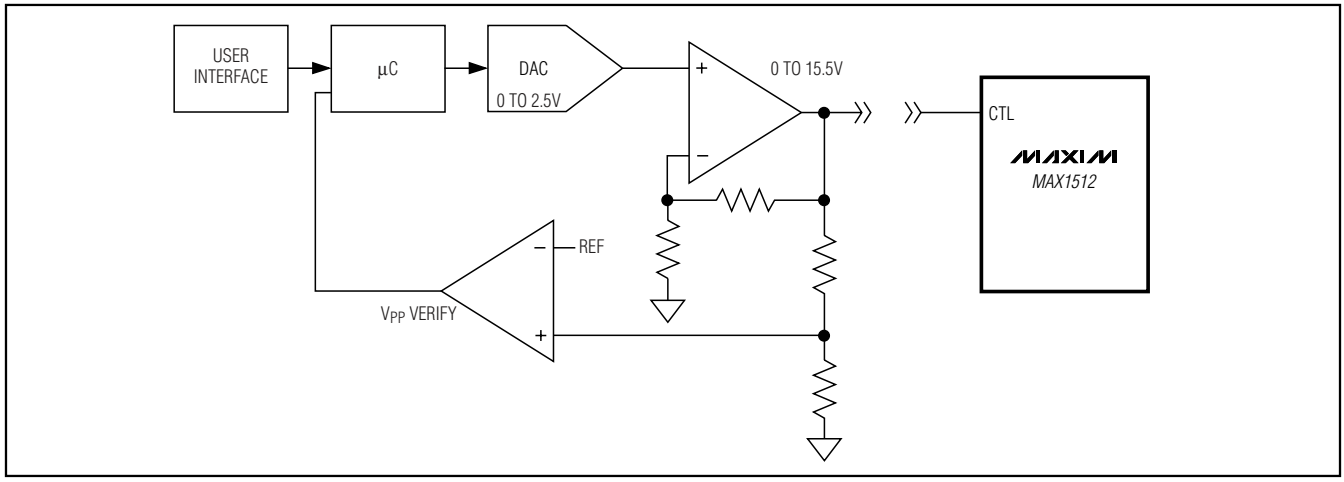


Figure 8. Conceptual Programming Circuit

Applications Information

The VCOM adjustment and the EEPROM programming must be performed with an external programming circuit. Refer to the MAX1512 evaluation kit for a complete programming circuit solution.

Use a circuit similar to the conceptual diagram shown in Figure 8 to drive CTL. The accuracy of the programming voltage (V_{PP}) is critical for proper MAX1512 data retention. The use of a comparator is recommended to verify the correct programming voltage has been reached. A complete design example of a CTL programming circuit is presented in the MAX1512 evaluation kit data sheet.

Electrostatic Discharge (CTL, CE)

Often, CTL and CE are exposed at the panel connector and are therefore subject to electrostatic discharge (ESD). Resistor-capacitor (RC) filters can be employed at these inputs to improve their ESD performance (Figure 9).

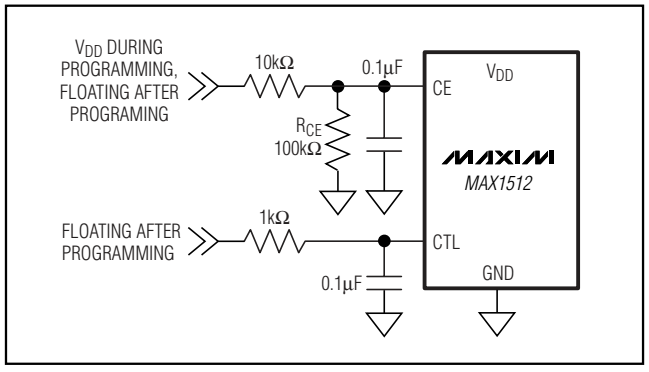


Figure 9. Improved EOS/Surge Performance

If the CE panel connector is to be left floating after programming, be sure to include a resistor to ground (R_{CE}) to ensure a valid logic-low on CE. The time constant for a CE filter is not critical but the driving resistor must have a much lower resistance than RCE to properly drive CE.

If a filter is used at the CTL panel connector, its RC time-constant should be short enough to avoid interfering with CTL pulses or EEPROM programming timing. A time constant less than 200µs does not interfere with EEPROM programming. To avoid interfering with CTL pulses, make the time constant small compared to the CTL pulsewidth used.

Leakage Current (CTL)

The CTL pin is internally biased to V_{DD} / 2, but it is sensitive to leakage currents above 0.1µA. When CTL is not driven, avoid leakage currents around the CTL pin. Otherwise, reinforce the V_{DD} / 2 set point with an external resistive voltage-divider.

Layout Information

Use the following guidelines for good layout:

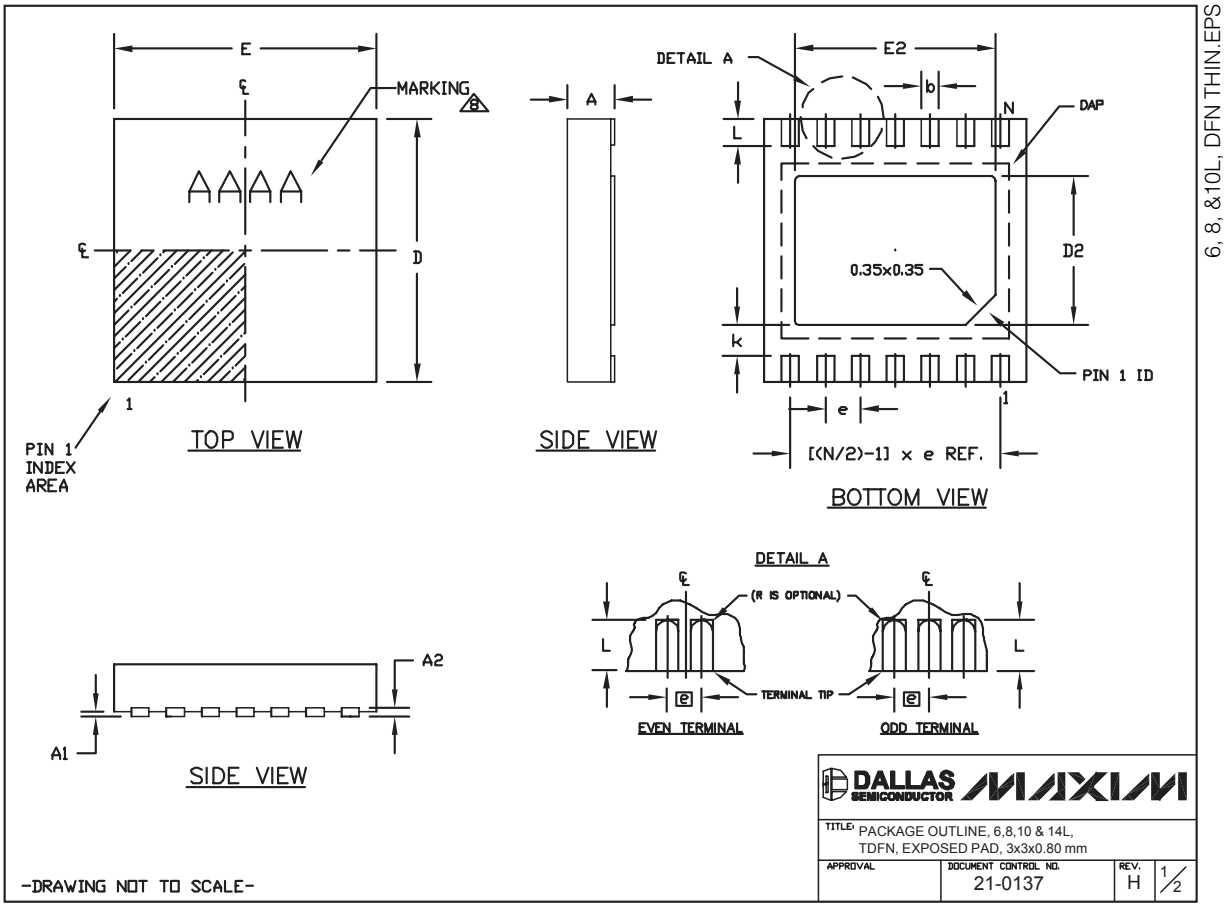
- Place the VCOM buffer and the R1/R2 voltage-divider close to the OUT pin (Figure 1). Keep the VCOM buffer and the R1/R2 voltage-divider close to each other.
- Place R_{SET} close to SET.
- In noisy environments, bypass capacitors may be desired on V_{DD} and/or V_{AVDD}. Keep any bypass capacitors close to the IC with short connections to the pins.

Refer to the MAX1512 evaluation kit for an example of proper board layout.

EEPROM-Programmable TFT VCOM Calibrator

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS		
SYMBOL	MIN.	MAX.
A	0.70	0.80
D	2.90	3.10
E	2.90	3.10
A1	0.00	0.05
L	0.20	0.40
k	0.25 MIN.	
A2	0.20 REF.	

PACKAGE VARIATIONS							
PKG. CODE	N	D2	E2	e	JEDEC SPEC	b	[(N/2)-1] x e
T633-1	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF
T633-2	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF
T833-1	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T833-2	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T833-3	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T1033-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1033-2	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1433-1	14	1.70±0.10	2.30±0.10	0.40 BSC	- - - -	0.20±0.05	2.40 REF
T1433-2	14	1.70±0.10	2.30±0.10	0.40 BSC	- - - -	0.20±0.05	2.40 REF

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2", AND T1433-1 & T1433-2.
6. "N" IS THE TOTAL NUMBER OF LEADS.
7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
8. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 6,8,10 & 14L, TDFN, EXPOSED PAD, 3x3x0.80 mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0137	H	2/2

Revision History

Pages changes at Rev 3: 1, 11, 12