

- Reads and Writes Can Be Asynchronous or Coincident
- Organization:
  - SN74ACT7200L – 256 × 9
  - SN74ACT7201LA – 512 × 9
  - SN74ACT7202LA – 1024 × 9
- Fast Data Access Times of 15 ns
- Read and Write Frequencies up to 40 MHz
- Bit-Width and Word-Depth Expansion
- Fully Compatible With the IDT7200/7201/7202
- Retransmit Capability
- Empty, Full, and Half-Full Flags
- TTL-Compatible Inputs
- Available in 28-Pin Plastic DIP (NP), Small-Outline (DV), and 32-Pin Plastic J-Leaded Chip-Carrier (RJ) Packages

**description**

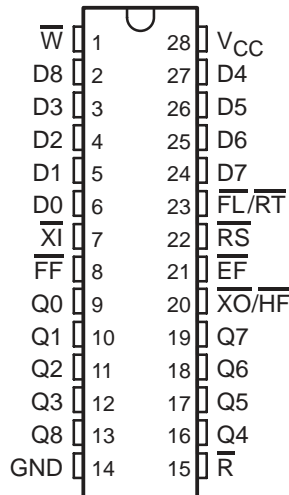
The SN74ACT7200L, SN74ACT7201LA, and SN74ACT7202LA are constructed with dual-port SRAM and have internal write and read address counters to provide data throughput on a first-in, first-out (FIFO) basis. Write and read operations are independent and can be asynchronous or coincident. Empty and full status flags prevent underflow and overflow of memory, and depth-expansion logic allows combining the storage cells of two or more devices into one FIFO. Word-width expansion is also possible.

Data is loaded into memory by the write-enable ( $\overline{W}$ ) input and unloaded by the read-enable ( $\overline{R}$ ) input. Read and write cycle times of 25 ns (40 MHz) are possible with data access times of 15 ns.

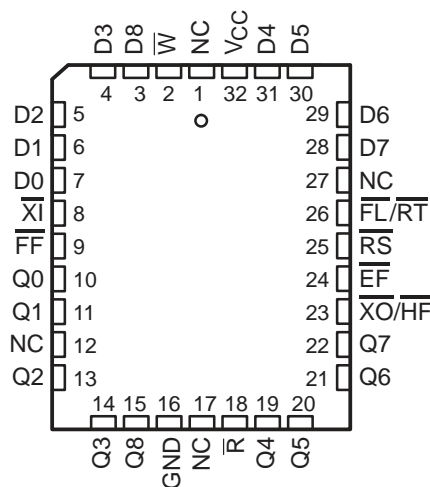
These devices are particularly suited for providing a data channel between two buses operating at asynchronous rates. Applications include use as rate buffers from analog-to-digital converters in data-acquisition systems, temporary storage elements between buses and magnetic or optical memories, and queues for communication systems. A 9-bit-wide data path is provided for the transmission of byte data plus a parity bit or packet-framing information. The read pointer can be reset independently of the write pointer for retransmitting previously read data when a device is not used in depth expansion.

The SN74ACT7200L, SN74ACT7201LA, and SN74ACT7202LA are characterized for operation from 0°C to 70°C.

DV OR NP PACKAGE (TOP VIEW)



RJ PACKAGE (TOP VIEW)



NC – No internal connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



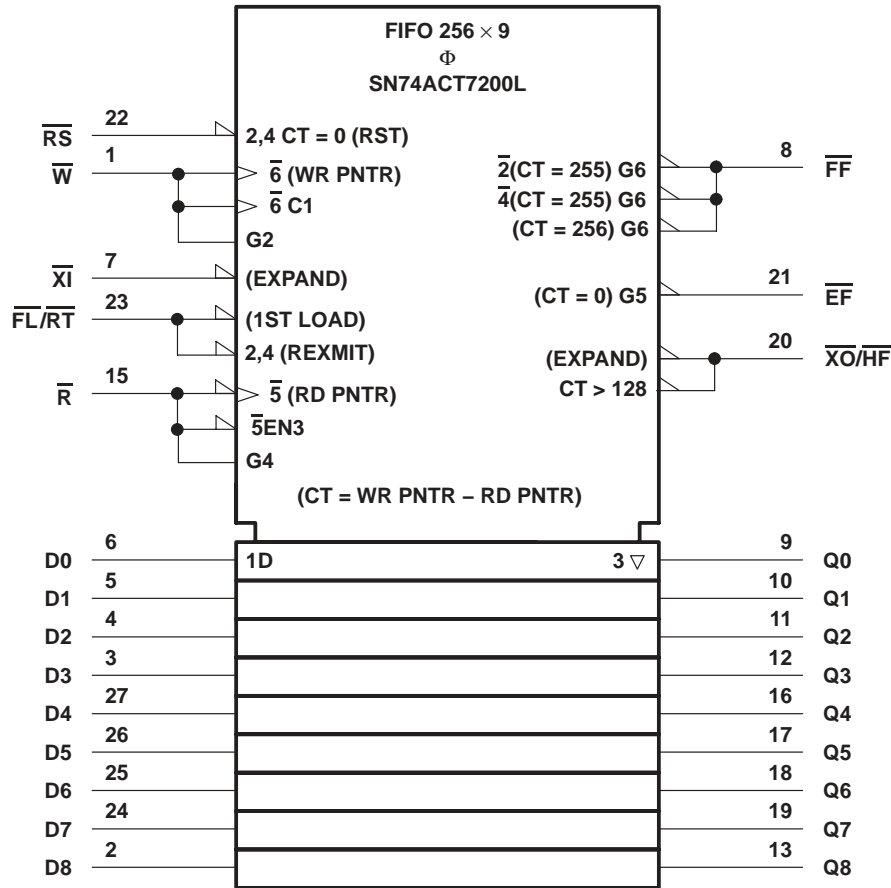
# SN74ACT7200L, SN74ACT7201LA, SN74ACT7202LA

256 × 9, 512 × 9, 1024 × 9

## ASYNCHRONOUS FIRST-IN, FIRST-OUT MEMORIES

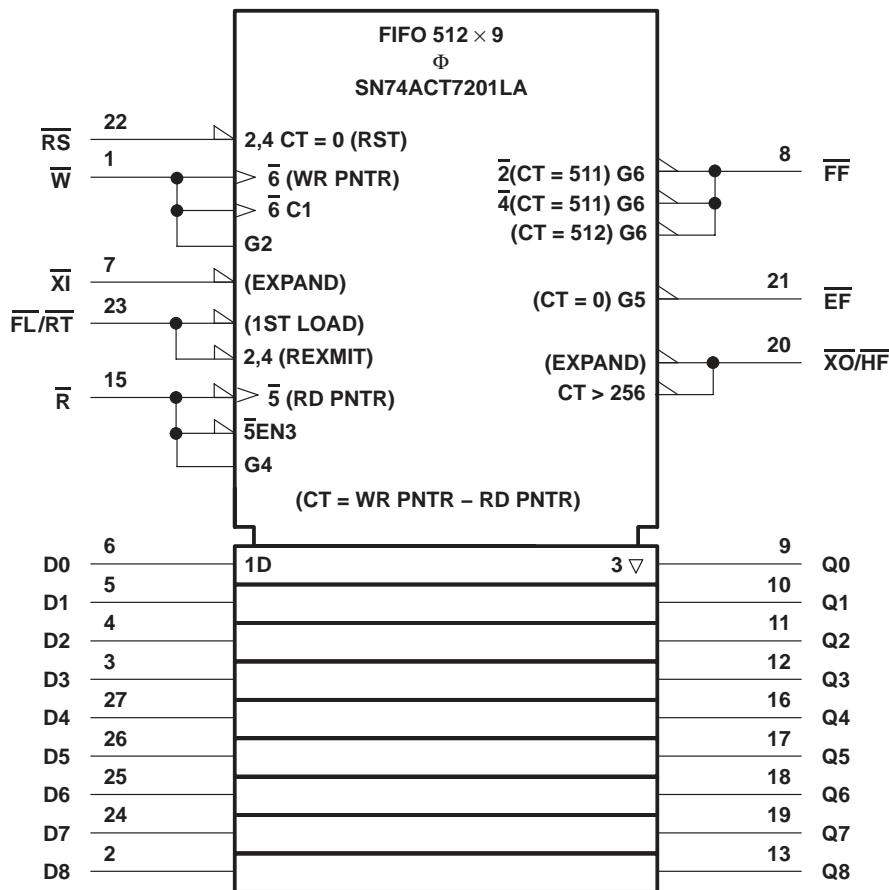
SCAS221A – FEBRUARY 1993 – REVISED SEPTEMBER 1995

### SN74ACT7200L logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DV and NP packages.

SN74ACT7201LA logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DV and NP packages.

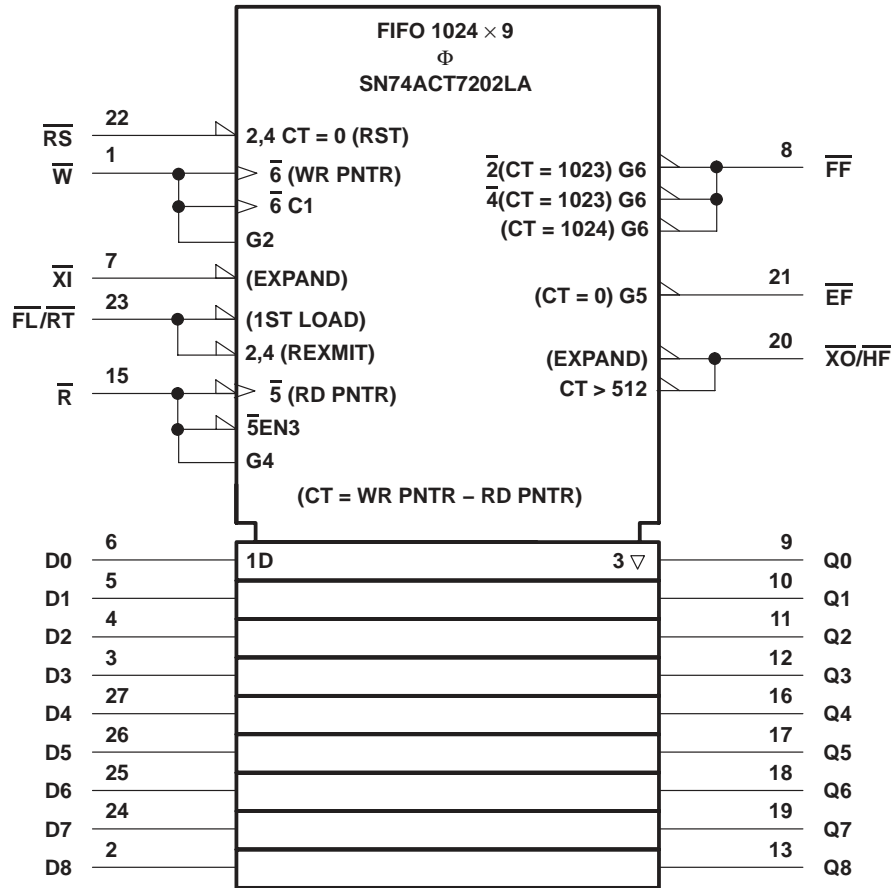
**SN74ACT7200L, SN74ACT7201LA, SN74ACT7202LA**

**256 × 9, 512 × 9, 1024 × 9**

**ASYNCHRONOUS FIRST-IN, FIRST-OUT MEMORIES**

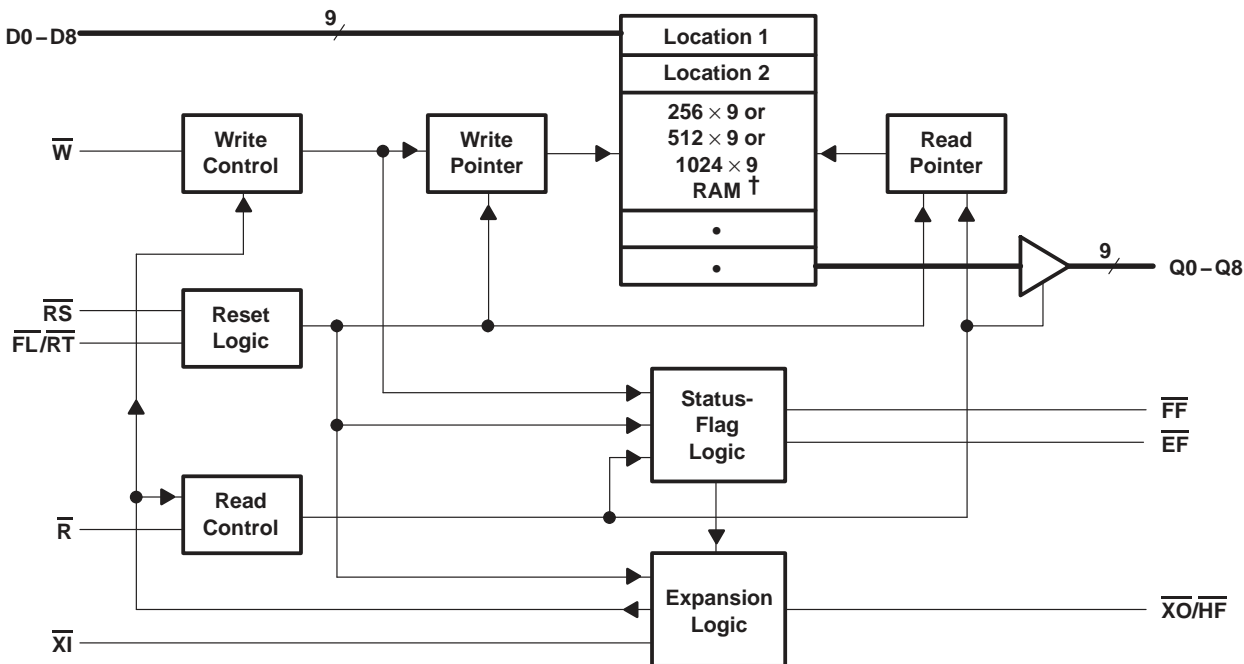
SCAS221A – FEBRUARY 1993 – REVISED SEPTEMBER 1995

**SN74ACT7202LA logic symbol†**



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DV and NP packages.

functional block diagram



† 256 × 9 for SN74ACT7200L; 512 × 9 for SN74ACT7201LA; 1024 × 9 for SN74ACT7202LA

RESET AND RETRANSMIT FUNCTION TABLE  
(single-device depth; single-or multiple-device width)

INPUTS			INTERNAL TO DEVICE		OUTPUTS			FUNCTION
RS̄	FL/RT̄	XĪ	READ POINTER	WRITE POINTER	EF̄	FF̄	XO/HF̄	
L	X	L	Location zero	Location zero	L	H	H	Reset device
H	L	L	Location zero	Unchanged	X	X	X	Retransmit
H	H	L	Increment if EF̄ high	Increment if FF̄ high	X	X	X	Read/write

RESET AND FIRST-LOAD FUNCTION TABLE  
(multiple-device depth; single-or multiple-device width)

INPUTS			INTERNAL TO DEVICE		OUTPUTS		FUNCTION
RS̄	FL/RT̄	XĪ	READ POINTER	WRITE POINTER	EF̄	FF̄	
L	L	‡	Location zero	Location zero	L	H	Reset first device
L	H	‡	Location zero	Location zero	L	H	Reset all other devices
H	X	‡	X	X	X	X	Read/write

‡ XĪ is connected to XO/HF̄ of the previous device in the daisy chain (see Figure 15).

# SN74ACT7200L, SN74ACT7201LA, SN74ACT7202LA

256 × 9, 512 × 9, 1024 × 9

## ASYNCHRONOUS FIRST-IN, FIRST-OUT MEMORIES

SCAS221A – FEBRUARY 1993 – REVISED SEPTEMBER 1995

### Terminal Functions

TERMINAL NAME	I/O	DESCRIPTION
D0–D8	I	Data inputs
$\overline{EF}$	O	Empty-flag output. $\overline{EF}$ is low when the read pointer is equal to the write pointer, inhibiting any operation initiated by a read cycle. When the FIFO is empty, a data word can be read automatically at Q0–Q8 by holding $\overline{R}$ low when loading the data word with a low-level pulse on $\overline{W}$ .
$\overline{FF}$	O	Full-flag output. $\overline{FF}$ is low when the write pointer is one location less than the read pointer, indicating that the device is full and inhibiting any operation initiated by a write cycle. $\overline{FF}$ goes low when the number of writes after reset exceeds the number of reads by 256 for the SN74ACT7200L, 512 for the SN74ACT7201LA, and 1024 for the SN74ACT7202LA. When the FIFO is full, a data word can be written automatically into memory by holding $\overline{W}$ low while reading out another data word with a low-level pulse on $\overline{R}$ .
$\overline{FL/RT}$	I	First-load/retransmit input. $\overline{FL/RT}$ performs two separate functions. When cascading two or more devices for word-depth expansion, $\overline{FL/RT}$ is tied to ground on the first device in the daisy chain to indicate that it is the first device loaded and unloaded; it is tied high on all other devices in the depth-expansion chain. A device is not used in depth expansion when its expansion ( $\overline{XI}$ ) input is tied to ground. In that case, $\overline{FL/RT}$ acts as a retransmit enable. A retransmit operation is initiated when $\overline{FL/RT}$ is pulsed low. This sets the internal read pointer to the first location and does not affect the write pointer. $\overline{R}$ and $\overline{W}$ must be at a high logic level during the low-level $\overline{FL/RT}$ retransmit pulse. Retransmit should be used only when less than 256/512/1024 writes are performed between resets; otherwise, an attempt to retransmit can cause the loss of unread data. The retransmit function can affect $\overline{XO/HF}$ depending on the relative locations of the read and write pointers.
GND		Ground
Q0–Q8	O	Data outputs. Q0–Q8 are in the high-impedance state when $\overline{R}$ is high or the FIFO is empty.
$\overline{R}$	I	Read-enable input. A read cycle begins on the falling edge of $\overline{R}$ if $\overline{EF}$ is high. This activates Q0–Q8 and shifts the next data value to this bus. The data outputs return to the high-impedance state as $\overline{R}$ goes high. As the last stored word is read by the falling edge of $\overline{R}$ , $\overline{EF}$ transitions low but Q0–Q8 remain active until $\overline{R}$ returns high. When the FIFO is empty, the internal read pointer is unchanged by a pulse on $\overline{R}$ .
$\overline{RS}$	I	Reset input. A reset is performed by taking $\overline{RS}$ low. This initializes the internal read and write pointers to the first location and sets $\overline{EF}$ low, $\overline{FF}$ high, and $\overline{HF}$ high. Both $\overline{R}$ and $\overline{W}$ must be held high for a reset during the window shown in Figure 7. A reset is required after power up before a write operation can take place.
$V_{CC}$		Supply voltage
$\overline{W}$	I	Write-enable input. A write cycle begins on the falling edge of $\overline{W}$ if $\overline{FF}$ is high. The value on D0–D8 is stored in memory as $\overline{W}$ returns high. When the FIFO is full, $\overline{FF}$ is low, inhibiting $\overline{W}$ from performing any operation on the device.
$\overline{XI}$	I	Expansion-in input. $\overline{XI}$ performs two functions. $\overline{XI}$ is tied to ground to indicate that the device is not used in depth expansion. When the device is used in depth expansion, $\overline{XI}$ is connected to the expansion-out ( $\overline{XO}$ ) output of the previous device in the depth-expansion chain.
$\overline{XO/HF}$	O	Expansion-out/half-full-flag output. $\overline{XO/HF}$ performs two functions. When the device is not used in depth expansion (i.e., when $\overline{XI}$ is tied to ground), $\overline{XO/HF}$ indicates when half the memory locations are filled. After half of the memory is filled, the falling edge on $\overline{W}$ for the next write operation drives $\overline{XO/HF}$ low. $\overline{XO/HF}$ remains low until a rising edge of $\overline{R}$ reduces the number of words stored to exactly half of the total memory. When the device is used in depth expansion, $\overline{XO/HF}$ is connected to $\overline{XI}$ of the next device in the daisy chain. $\overline{XO/HF}$ drives the daisy chain by sending a pulse to the next device when the previous device reaches the last memory location.



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$ (see Note 1)	–0.5 V to 7 V
Input voltage range (any input), $V_I$	–0.5 V to 7 V
Continuous output current, $I_O$	50 mA
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, $T_A$	0°C to 70°C
Storage temperature range, $T_{Stg}$	–55°C to 125°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

**recommended operating conditions**

	MIN	NOM	MAX	UNIT
$V_{CC}$ Supply voltage	4.5	5	5.5	V
$V_{IH}$ High-level input voltage	$\overline{XI}$	2.6		V
	Other inputs	2		
$V_{IL}$ Low-level input voltage			0.8	V
$I_{OH}$ High-level output current			–2	mA
$I_{OL}$ Low-level output current			8	mA
$T_A$ Operating free-air temperature	0		70	°C

**electrical characteristics over recommended operating free-air temperature range,  $V_{CC} = 5.5$  V (unless otherwise noted)**

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{OH}$	$V_{CC} = 4.5$ V,	$I_{OH} = -2$ mA	2.4			V
$V_{OL}$	$V_{CC} = 4.5$ V,	$I_{OL} = 8$ mA			0.4	V
$I_{OZH}$	$V_O = V_{CC}$ ,	$\overline{R} \geq V_{IH}$			±10	µA
$I_{OZL}$	$V_O = 0.4$ V,	$\overline{R} \geq V_{IH}$			±10	µA
$I_I$	$V_I = 0$ to 5.5 V		–1		1	µA
$I_{CC1}‡$	$t_a = 15$ and 25 ns				125 <sup>¶</sup>	mA
	$t_a = 35$ and 50 ns			50	80	
$I_{CC2}‡$	$t_a = 15$ and 25 ns		$\overline{R}$ , $\overline{W}$ , $\overline{RS}$ , and $\overline{FL/RT}$ at $V_{IH}$			15
	$t_a = 35$ and 50 ns					
$I_{CC3}‡$	$t_a = 15$ and 25 ns		$V_I = V_{CC} - 0.2$ V			0.5
	$t_a = 35$ and 50 ns					
$C_i$ §	$V_I = 0$ ,	$T_A = 25^\circ\text{C}$ ,	$f = 1$ MHz		8	pF
$C_o$ §	$V_O = 0$ ,	$T_A = 25^\circ\text{C}$ ,	$f = 1$ MHz		8	pF

‡  $I_{CC1}$  = supply current;  $I_{CC2}$  = standby current;  $I_{CC3}$  = power-down current.  $I_{CC}$  measurements are made with outputs open (only capacitive loading).

§ This parameter is sampled and not 100% tested.

¶ Tested at  $f_{clock} = 20$  MHz



**SN74ACT7200L, SN74ACT7201LA, SN74ACT7202LA**

**256 × 9, 512 × 9, 1024 × 9**

**ASYNCHRONOUS FIRST-IN, FIRST-OUT MEMORIES**

SCAS221A – FEBRUARY 1993 – REVISED SEPTEMBER 1995

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	FIGURE	'ACT7200L-15 'ACT7201LA-15 'ACT7202LA-15		'ACT7200L-25 'ACT7201LA-25 'ACT7202LA-25		'ACT7201LA-35† 'ACT7202LA-35†		'ACT7200L-50 'ACT7201LA-50 'ACT7202LA-50		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub> Clock frequency, $\overline{R}$ or $\overline{W}$		40		28.5		22.2		15		MHz
t <sub>c(R)</sub> Cycle time, read	1(a)	25		35		45		65		ns
t <sub>c(W)</sub> Cycle time, write	1(b)	25		35		45		65		ns
t <sub>c(RS)</sub> Cycle time, reset	7	25		35		45		65		ns
t <sub>c(RT)</sub> Cycle time, retransmit	4	25		35		45		65		ns
t <sub>w(RL)</sub> Pulse duration, $\overline{R}$ low	1(a)	15		25		35		50		ns
t <sub>w(WL)</sub> Pulse duration, $\overline{W}$ low	1(b)	15		25		35		50		ns
t <sub>w(RH)</sub> Pulse duration, $\overline{R}$ high	1(a)	10		10		10		15		ns
t <sub>w(WH)</sub> Pulse duration, $\overline{W}$ high	1(b)	10		10		10		15		ns
t <sub>w(RT)</sub> Pulse duration, $\overline{FL/RT}$ low	4	15		25		35		50		ns
t <sub>w(RS)</sub> Pulse duration, $\overline{RS}$ low	7	15		25		35		50		ns
t <sub>w(XIL)</sub> Pulse duration, $\overline{XI}$ low	10	15		25		35		50		ns
t <sub>w(XIH)</sub> Pulse duration, $\overline{XI}$ high	10	10		10		10		10		ns
t <sub>su(D)</sub> Setup time, data before $\overline{W}$ ↑	1(b), 6	11		15		18		30		ns
t <sub>su(RT)</sub> Setup time, $\overline{R}$ and $\overline{W}$ high before $\overline{FL/RT}$ ↑‡	4	15		25		35		50		ns
t <sub>su(RS)</sub> Setup time, $\overline{R}$ and $\overline{W}$ high before $\overline{RS}$ ↑‡	7	15		25		35		50		ns
t <sub>su(XI-R)</sub> Setup time, $\overline{XI}$ low before $\overline{R}$ ↓	10	10		10		10		15		ns
t <sub>su(XI-W)</sub> Setup time, $\overline{XI}$ low before $\overline{W}$ ↓	10	10		10		10		15		ns
t <sub>h(D)</sub> Hold time, data after $\overline{W}$ ↑	1(b), 6	0		0		0		5		ns
t <sub>h(E-R)</sub> Hold time, $\overline{R}$ low after $\overline{EF}$ ↑	5, 11	15		25		35		50		ns
t <sub>h(F-W)</sub> Hold time, $\overline{W}$ low after $\overline{FF}$ ↑	6, 12	15		25		35		50		ns
t <sub>h(RT)</sub> Hold time, $\overline{R}$ and $\overline{W}$ high after $\overline{FL/RT}$ ↑	4	10		10		10		15		ns
t <sub>h(RS)</sub> Hold time, $\overline{R}$ and $\overline{W}$ high after $\overline{RS}$ ↑	7	10		10		10		15		ns

† Released in RJ package only

‡ These values are characterized but not currently tested.





switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figure 13)

PARAMETER	FIGURE	'ACT7200L-15 'ACT7201LA-15 'ACT7202LA-15		'ACT7200L-25 'ACT7201LA-25 'ACT7202LA-25		'ACT7201LA-35† 'ACT7202LA-35†		'ACT7200L-50 'ACT7201LA-50 'ACT7202LA-50		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>a</sub>	Access time, $\overline{R}\downarrow$ or $\overline{EF}\uparrow$ to data out valid	1(a), 3, 5	15	25	35	50	ns			
t <sub>v(RH)</sub>	Valid time, data out valid after $\overline{R}\uparrow$	1(a)	5	5	5	5	ns			
t <sub>en(R-QX)</sub>	Enable time, $\overline{R}\downarrow$ to Q outputs at low impedance‡	1(a)	5	5	10	10	ns			
t <sub>en(W-QX)</sub>	Enable time, $\overline{W}\uparrow$ to Q outputs at low impedance‡§	5	5	5	5	15	ns			
t <sub>dis(R)</sub>	Disable time, $\overline{R}\uparrow$ to Q outputs at high impedance‡	1(a)	15	18	20	30	ns			
t <sub>w(FH)</sub>	Pulse duration, $\overline{FF}$ high in automatic write mode	6	15	25	30	45	ns			
t <sub>w(EH)</sub>	Pulse duration, $\overline{EF}$ high in automatic read mode	5	15	25	30	45	ns			
t <sub>pd(W-F)</sub>	Propagation delay time, $\overline{W}\downarrow$ to $\overline{FF}$ low	2	15	25	30	45	ns			
t <sub>pd(R-F)</sub>	Propagation delay time, $\overline{R}\uparrow$ to $\overline{FF}$ high	2, 6, 12	15	25	30	45	ns			
t <sub>pd(RS-F)</sub>	Propagation delay time, $\overline{RS}\downarrow$ to $\overline{FF}$ high	7	25	35	45	65	ns			
t <sub>pd(RS-HF)</sub>	Propagation delay time, $\overline{RS}\downarrow$ to $\overline{XO}/\overline{HF}$ high	7	25	35	45	65	ns			
t <sub>pd(W-E)</sub>	Propagation delay time, $\overline{W}\uparrow$ to $\overline{EF}$ high	3, 5, 11	15	25	30	45	ns			
t <sub>pd(R-E)</sub>	Propagation delay time, $\overline{R}\downarrow$ to $\overline{EF}$ low	3	15	25	30	45	ns			
t <sub>pd(RS-E)</sub>	Propagation delay time, $\overline{RS}\downarrow$ to $\overline{EF}$ low	7	25	35	45	65	ns			
t <sub>pd(W-HF)</sub>	Propagation delay time, $\overline{W}\downarrow$ to $\overline{XO}/\overline{HF}$ low	8	25	35	45	65	ns			
t <sub>pd(R-HF)</sub>	Propagation delay time, $\overline{R}\uparrow$ to $\overline{XO}/\overline{HF}$ high	8	25	35	45	65	ns			
t <sub>pd(R-XOL)</sub>	Propagation delay time, $\overline{R}\downarrow$ to $\overline{XO}/\overline{HF}$ low	9	15	25	35	50	ns			
t <sub>pd(W-XOL)</sub>	Propagation delay time, $\overline{W}\downarrow$ to $\overline{XO}/\overline{HF}$ low	9	15	25	35	50	ns			
t <sub>pd(R-XOH)</sub>	Propagation delay time, $\overline{R}\uparrow$ to $\overline{XO}/\overline{HF}$ high	9	15	25	35	50	ns			
t <sub>pd(W-XOH)</sub>	Propagation delay time, $\overline{W}\uparrow$ to $\overline{XO}/\overline{HF}$ high	9	15	25	35	50	ns			
t <sub>pd(RT-FL)</sub>	Propagation delay time, $\overline{FL}/\overline{RT}\downarrow$ to $\overline{HF}$ , $\overline{EF}$ , $\overline{FF}$ valid	4	25	35	45	65	ns			

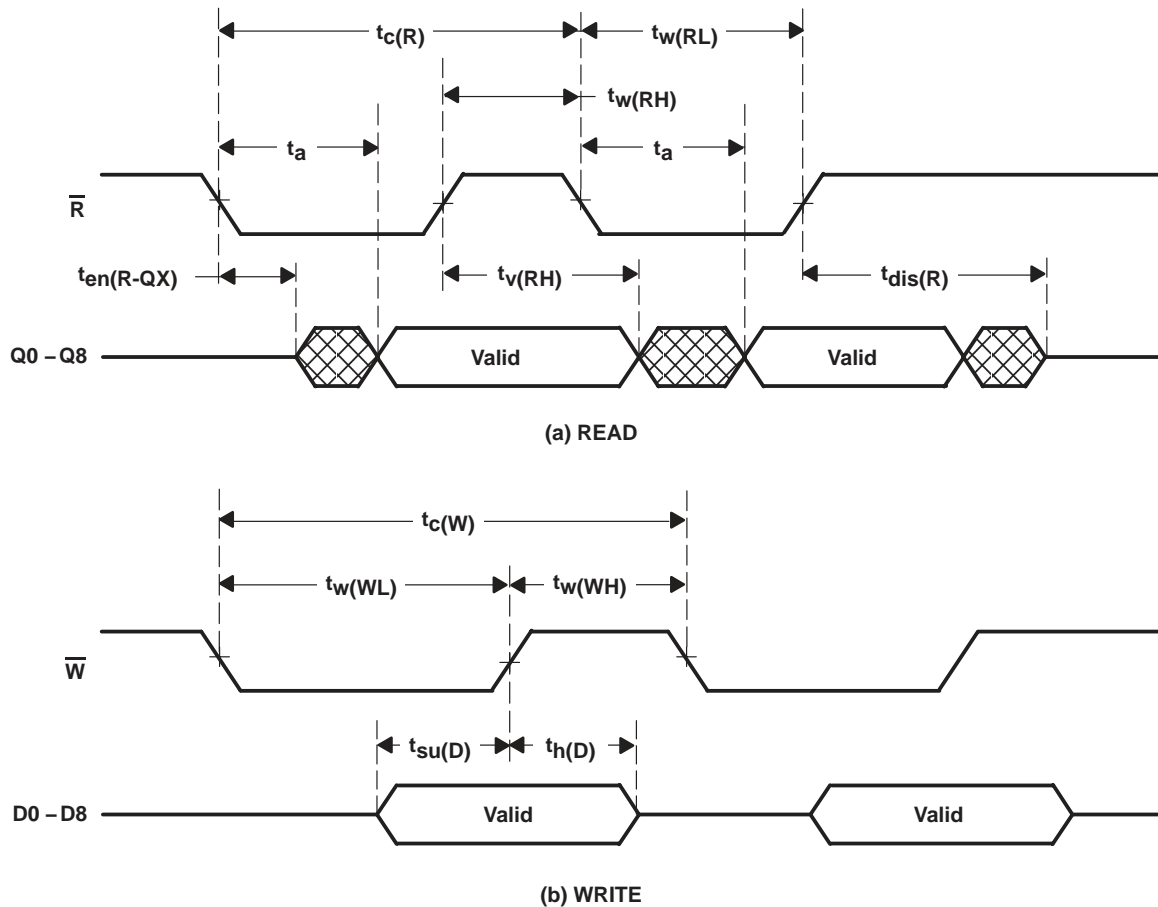
† Released in RJ package only

‡ These values are characterized but not currently tested.

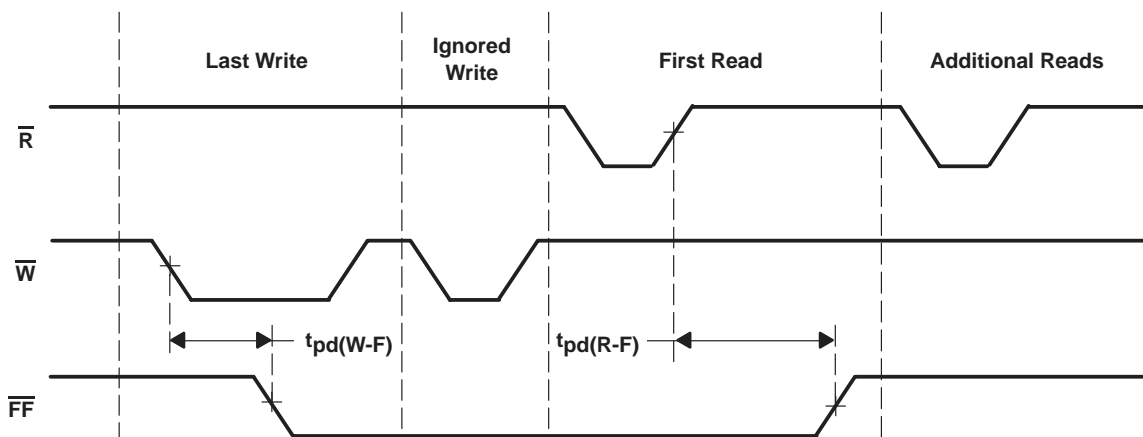
§ Only applies when data is automatically read (see Figure 5)



**PARAMETER MEASUREMENT INFORMATION**



**Figure 1. Asynchronous Waveforms**



**Figure 2. Full-Flag Waveforms**

PARAMETER MEASUREMENT INFORMATION

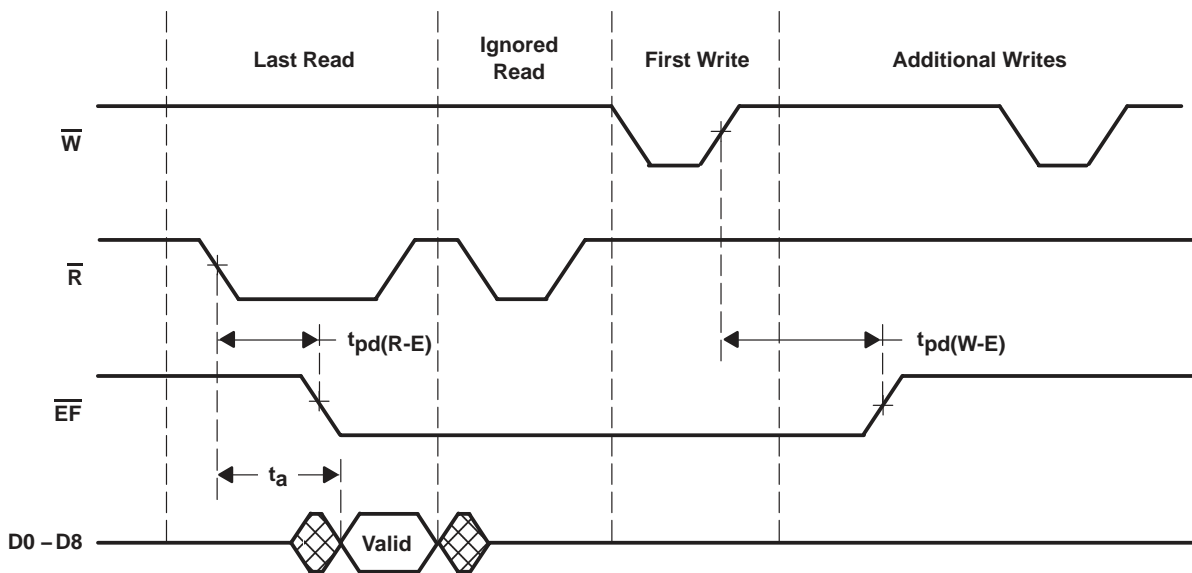
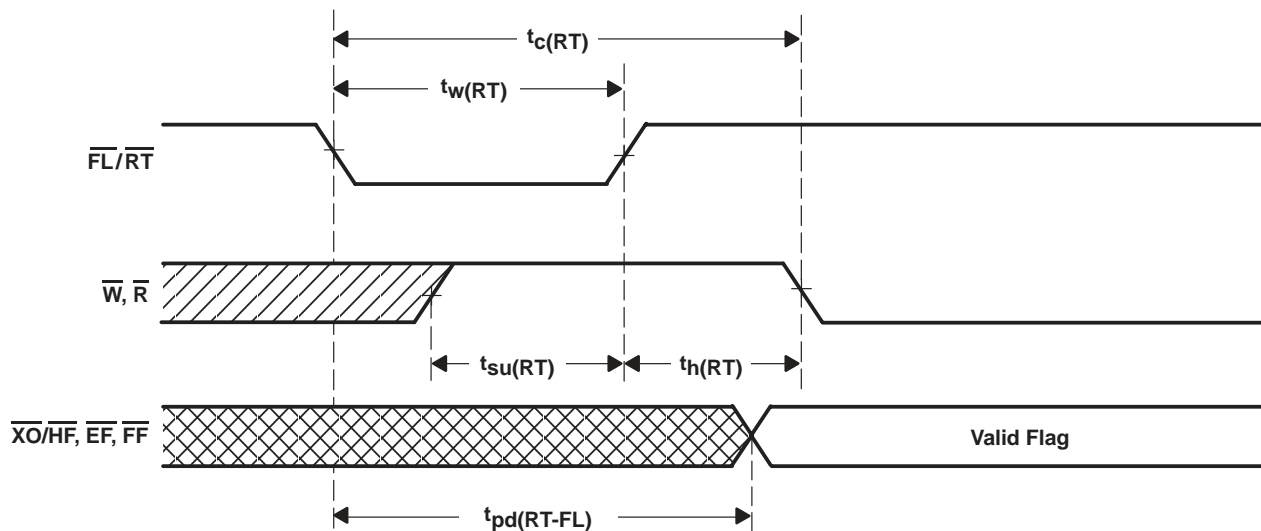


Figure 3. Empty-Flag Waveforms



NOTE A: The  $\overline{EF}$ ,  $\overline{FF}$ , and  $\overline{X0/HF}$  status flags are valid after completion of the retransmit cycle.

Figure 4. Retransmit Waveforms

PARAMETER MEASUREMENT INFORMATION

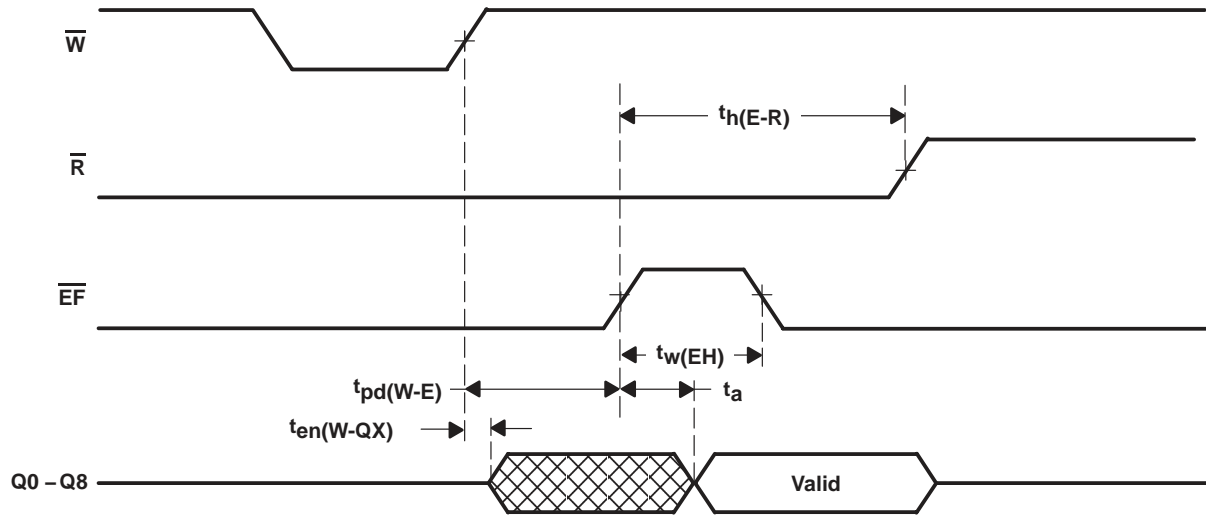


Figure 5. Automatic-Read Waveforms

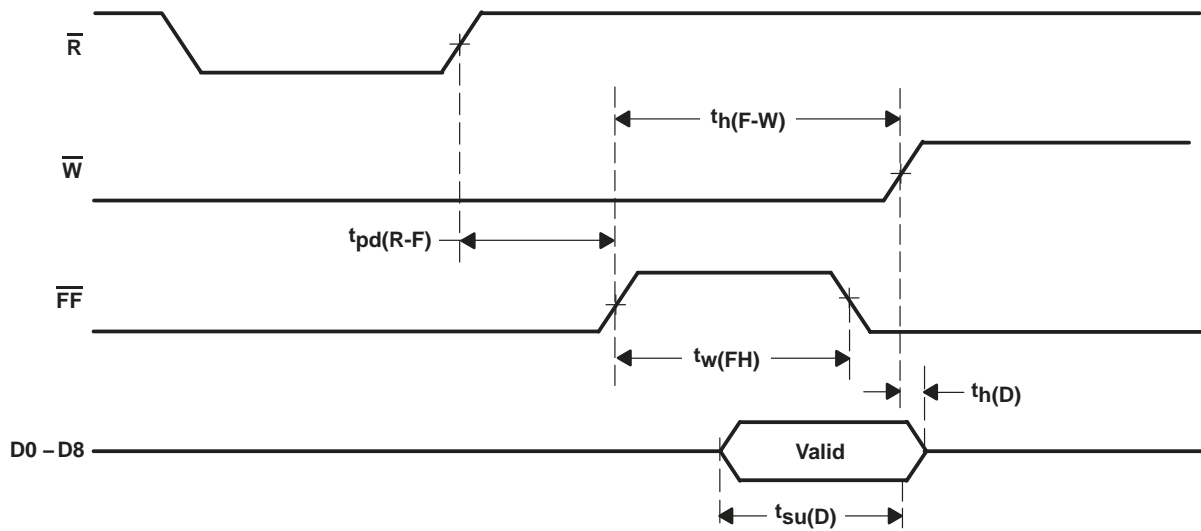


Figure 6. Automatic-Write Waveforms

PARAMETER MEASUREMENT INFORMATION

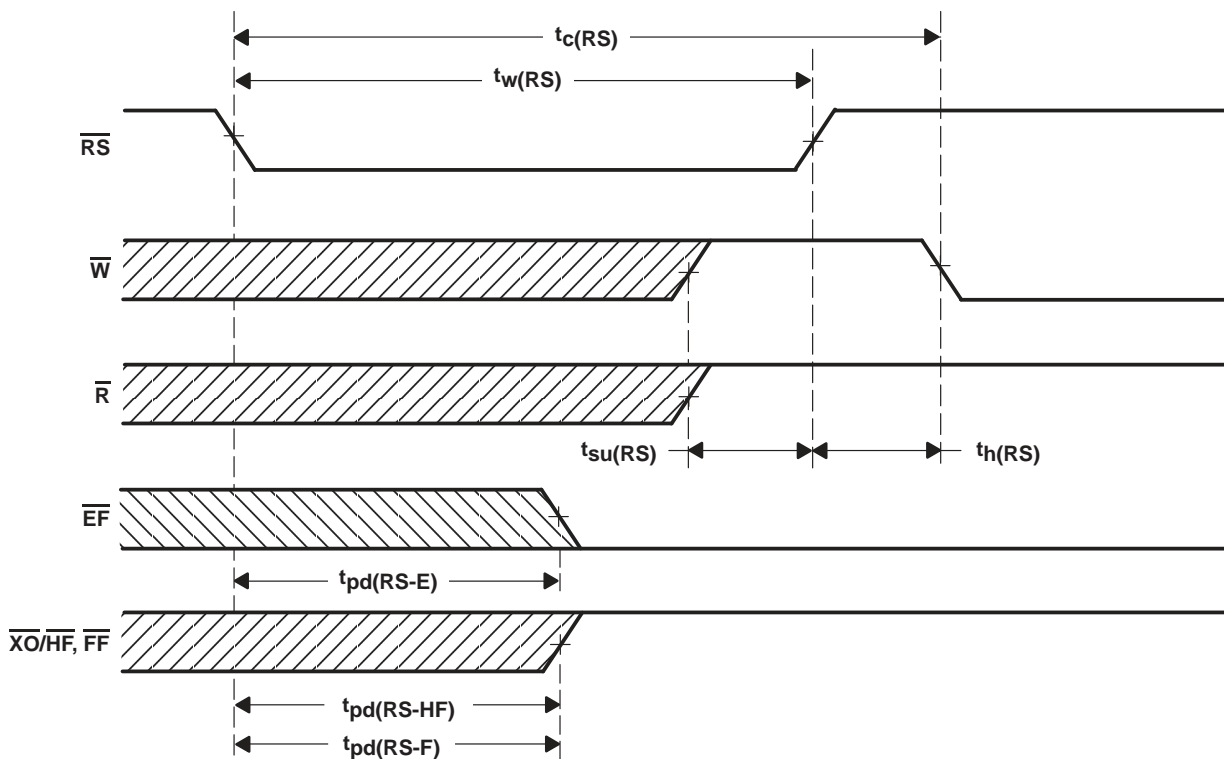


Figure 7. Master-Reset Waveforms

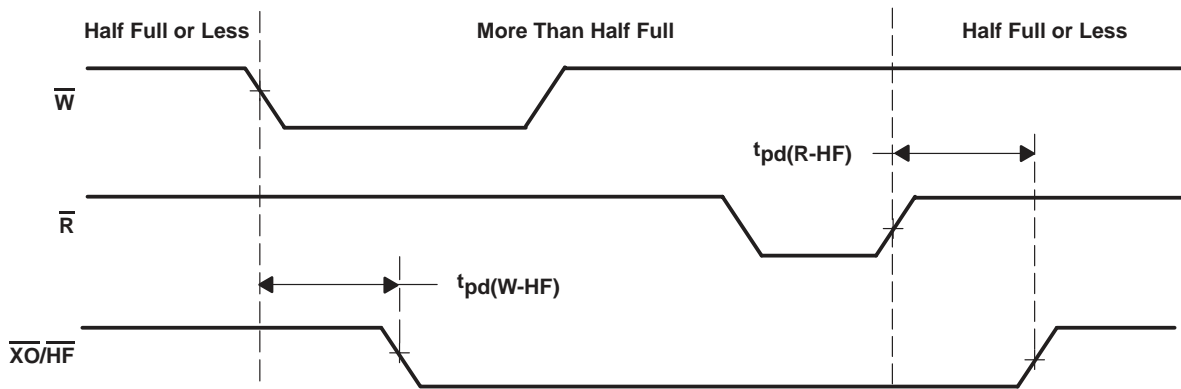


Figure 8. Half-Full Flag Waveforms

PARAMETER MEASUREMENT INFORMATION

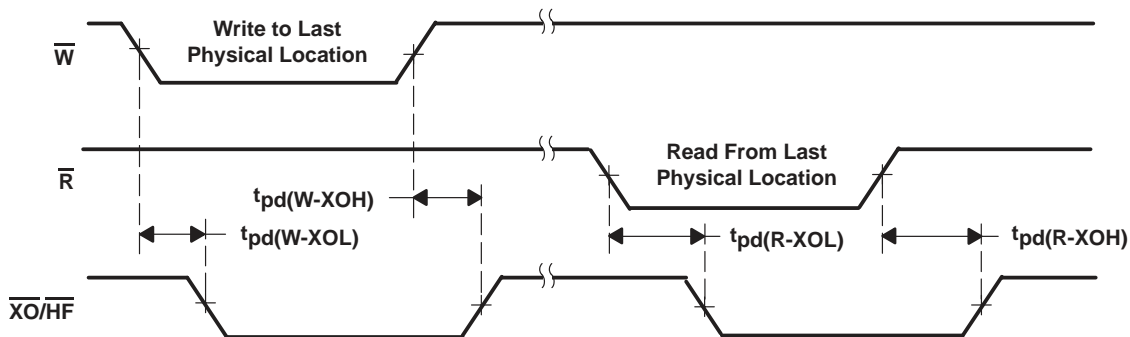


Figure 9. Expansion-Out Waveforms

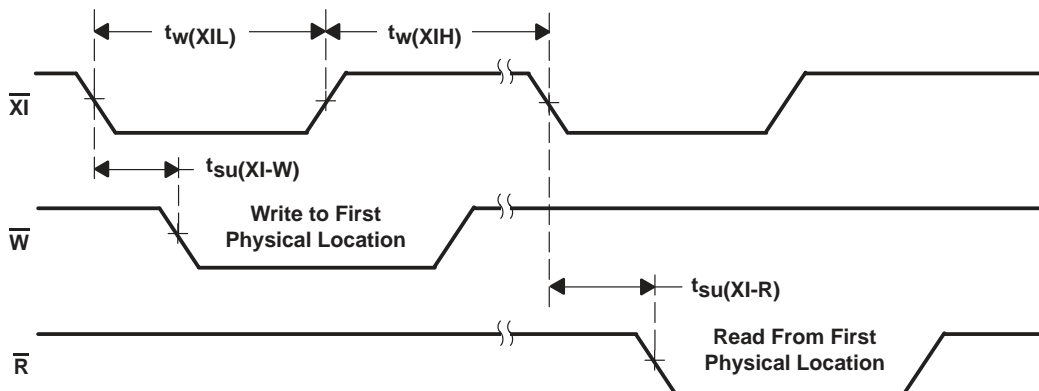


Figure 10. Expansion-In Waveforms

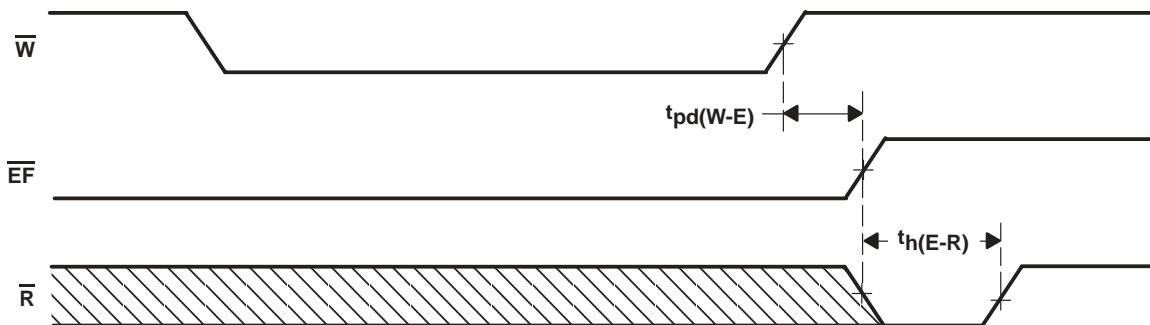


Figure 11. Minimum Timing for an Empty-Flag Coincident-Read Pulse

PARAMETER MEASUREMENT INFORMATION

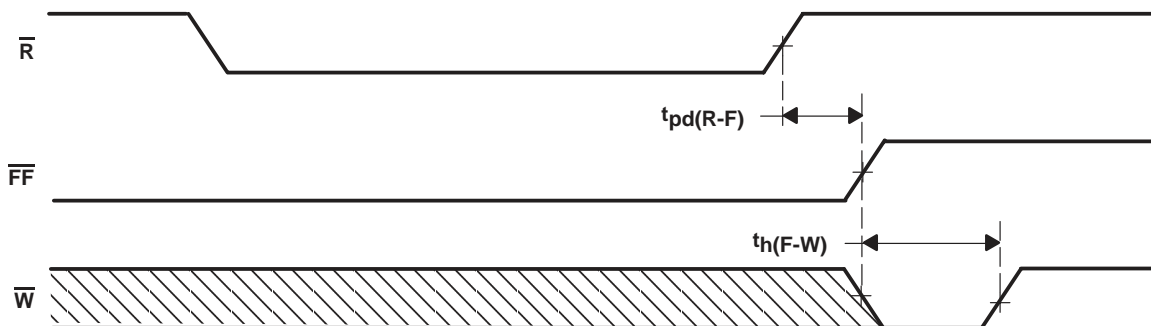
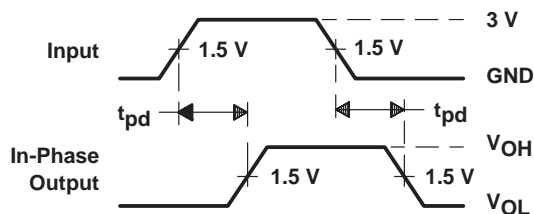
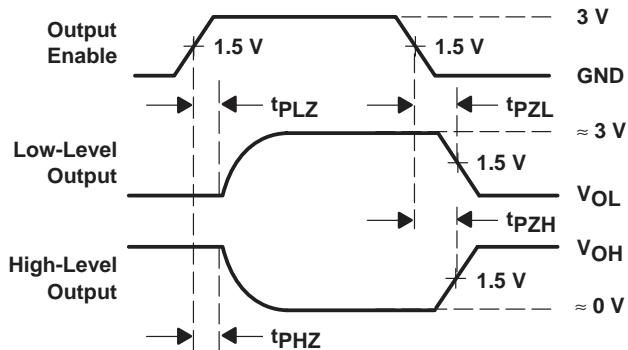
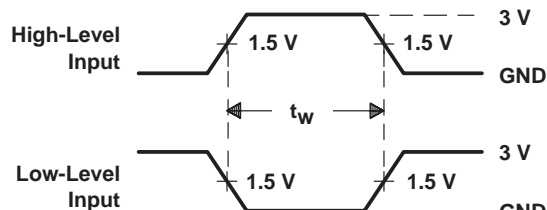
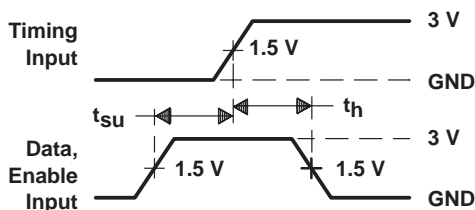
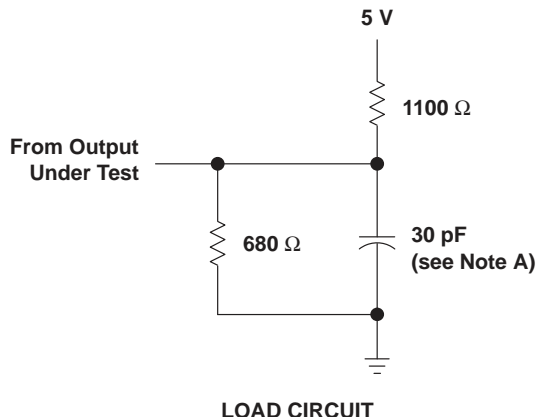


Figure 12. Minimum Timing for a Full-Flag Coincident-Write Pulse

**PARAMETER MEASUREMENT INFORMATION**



NOTE A: Includes probe and jig capacitance

**Figure 13. Load Circuit and Voltage Waveforms**



---

## APPLICATION INFORMATION

Combining two or more devices to create one FIFO with a greater number of memory bits is accomplished in two different ways. Width expansion increases the number of bits in each word by connecting FIFOs with the same depth in parallel. Depth expansion uses the built-in expansion logic to daisy-chain two or more devices for applications requiring more than 256, 512, or 1024 words of storage. Width expansion and depth expansion can be used together.

### width expansion

Word-width expansion is achieved by connecting the corresponding input control to multiple devices with the same depth. Status flags ( $\overline{EF}$ ,  $\overline{FF}$ , and  $\overline{HF}$ ) can be monitored from any one device. Figure 14 shows two FIFOs in a width-expansion configuration. Both devices have their expansion-in ( $\overline{XI}$ ) inputs tied to ground. This disables the depth-expansion function of the device, allowing the first-load/retransmit ( $\overline{FL}/\overline{RT}$ ) input to function as a retransmit ( $\overline{RT}$ ) input and the expansion-out/half-full ( $\overline{XO}/\overline{HF}$ ) output to function as a half-full ( $\overline{HF}$ ) flag.

### depth expansion

The SN74ACT7200L/7201LA/7202LA is easily expanded in depth. Figure 15 shows the connections used to depth expand three SN74ACT7200L/7201LA/7202LA devices. Any depth can be attained by adding additional devices to the chain. The SN74ACT7200L/7201LA/7202LA operates in depth expansion under the following conditions:

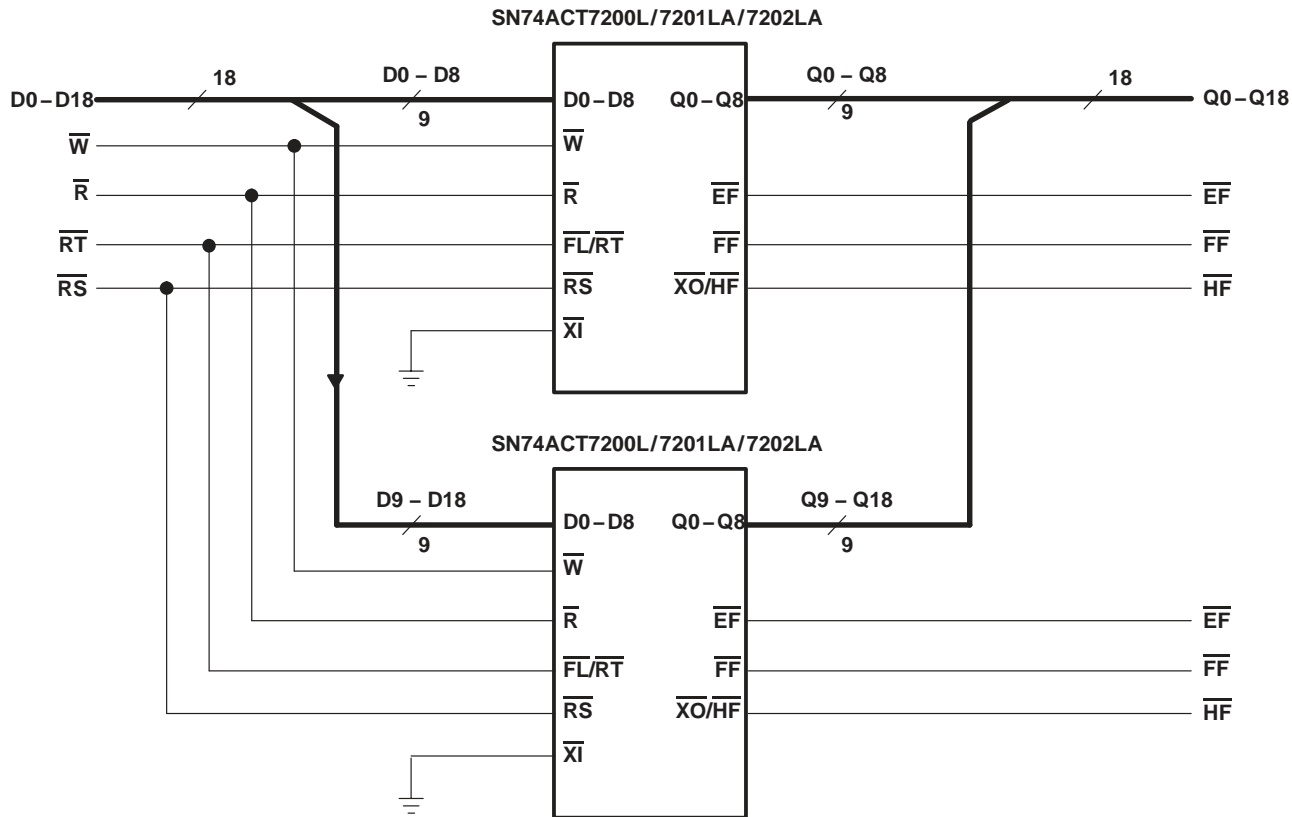
- The first device in the chain is designated by tying  $\overline{FL}$  to ground.
- All other devices must have their  $\overline{FL}$  inputs at a high logic level.
- $\overline{XO}$  of each device must be tied to  $\overline{XI}$  of the next device.
- External logic is needed to generate a composite  $\overline{FF}$  and  $\overline{EF}$ . All  $\overline{FF}$  outputs must be ORed together and all  $\overline{EF}$  outputs must be ORed together.
- $\overline{RT}$  and  $\overline{HF}$  functions are not available in the depth-expanded configuration.

### combined depth and width expansion

Both expansion techniques can be used together to increase depth and width. This is done by first creating depth-expanded units and then connecting them in a width-expanded configuration (see Figure 16).

**SN74ACT7200L, SN74ACT7201LA, SN74ACT7202LA**  
**256 × 9, 512 × 9, 1024 × 9**  
**ASYNCHRONOUS FIRST-IN, FIRST-OUT MEMORIES**  
 SCAS221A – FEBRUARY 1993 – REVISED SEPTEMBER 1995

**APPLICATION INFORMATION**



**Figure 14. Word-Width Expansion: 256/512/1024 Words × 18 Bits**

APPLICATION INFORMATION

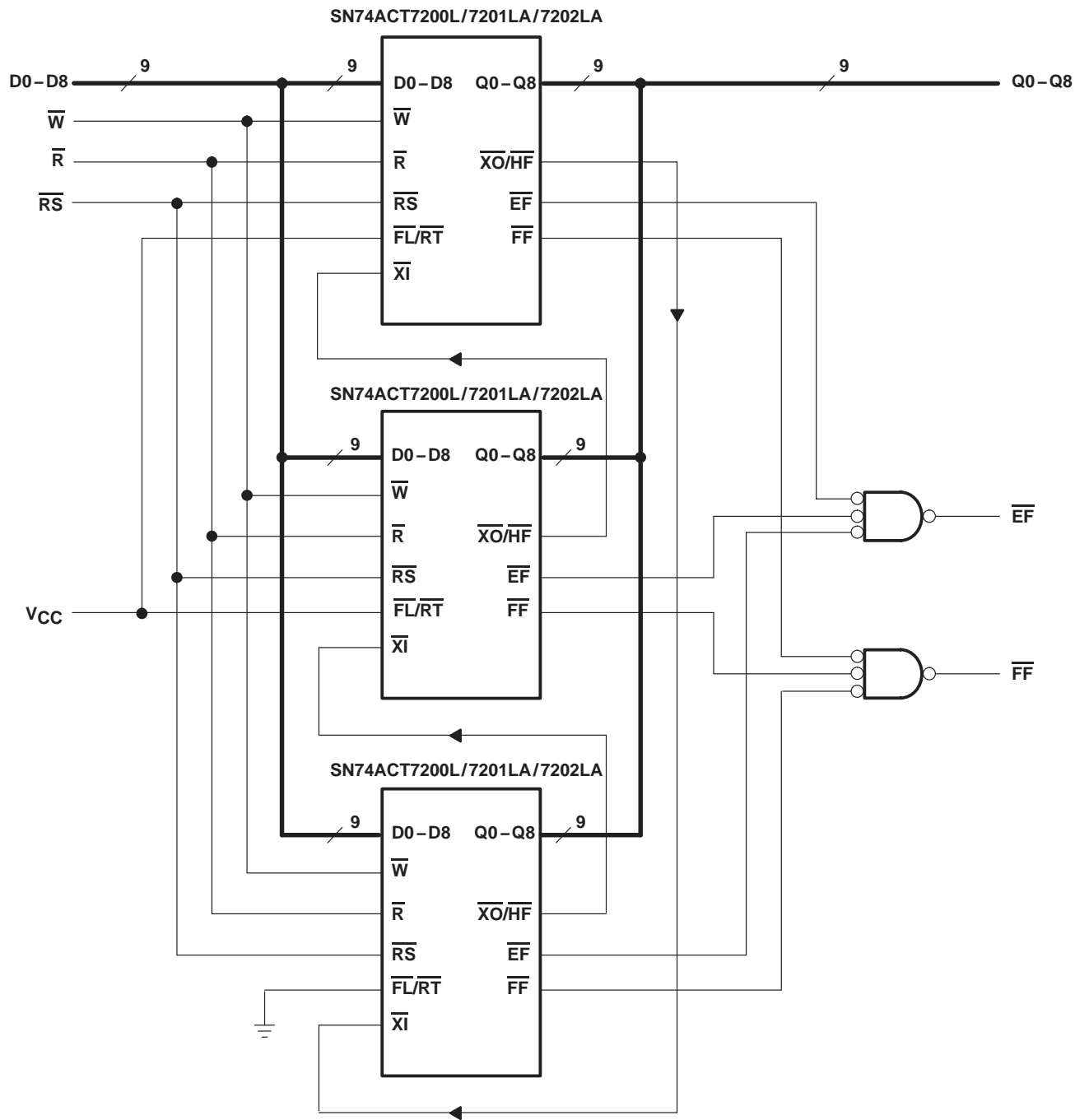


Figure 15. Word-Depth Expansion: 768/1536/3072 Words × 9 Bits

APPLICATION INFORMATION

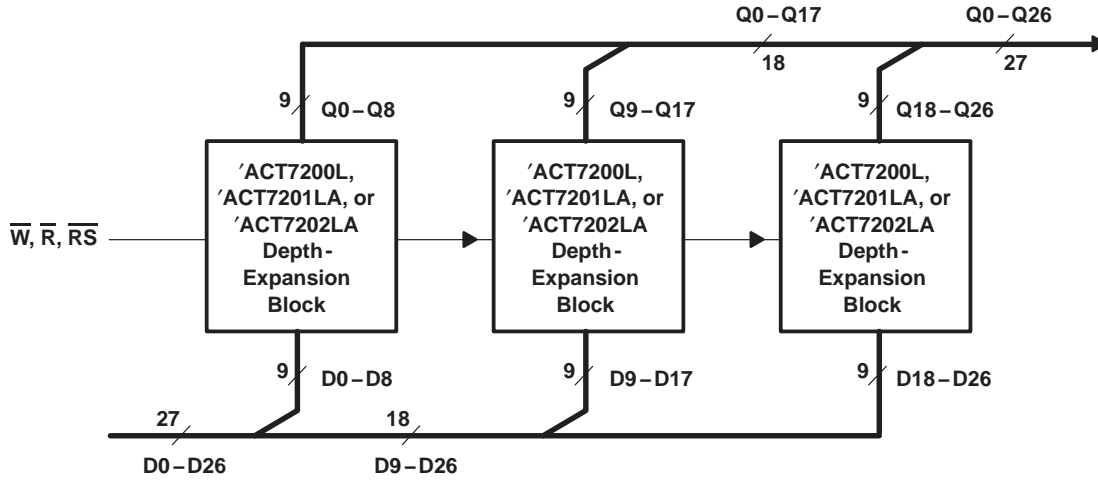


Figure 16. Word-Depth Plus Word-Width Expansion

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

### Products

Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
RF/IF and ZigBee® Solutions	<a href="http://www.ti.com/lprf">www.ti.com/lprf</a>

### Applications

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Automotive	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
Broadband	<a href="http://www.ti.com/broadband">www.ti.com/broadband</a>
Digital Control	<a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Military	<a href="http://www.ti.com/military">www.ti.com/military</a>
Optical Networking	<a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
Video & Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
Wireless	<a href="http://www.ti.com/wireless">www.ti.com/wireless</a>

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2008, Texas Instruments Incorporated