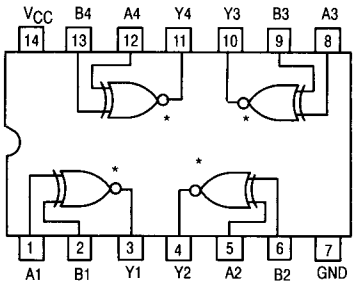
MOTOROLA

Quad 2-Input Exclusive NOR Gate

ELECTRICALLY TESTED PER:
MIL-M-38510/30303

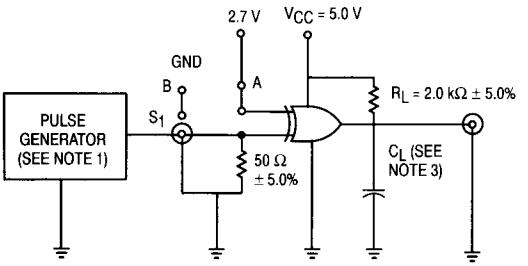
Military 54LS266

LOGIC DIAGRAM

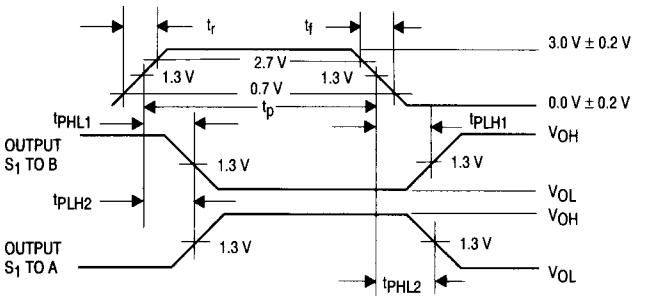


*OPEN COLLECTOR OUTPUTS

AC TEST CIRCUIT



WAVEFORMS



NOTES:
1. The generator has the following characteristics: $t_f \leq 6.0$ ns, $t_r = 15$ ns: PRR ≤ 1.0 MHz, $t_p = 0.5$ µs, $Z_{OUT} = 50\ \Omega$.
2. Each gate tested separately.
3. $C_L = 50$ pF ±10% including scope probe, wiring and stray capacitance, without package in test fixture.
4. Voltage measurements are to be made with respect to network ground terminal.
5. $R_L = 2.0$ kΩ ± 5.0%.

AVAILABLE AS:

1) JAN: JM38510/30303BXA
2) SMD: N/A
3) 883: 54LS266/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: C
CERFLAT: D
LCC: 2

THE LETTER "M" APPEARS BEFORE THE / ON LCC.

PIN ASSIGNMENTS

FUNCT.	DIL 632-08	FLATS 717-04	LCC 756A-02	BURN-IN (COND. A)
A1	1	1	2	VCC
B1	2	2	3	VCC
Y1	3	3	4	VCC
Y2	4	4	6	VCC
A2	5	5	8	VCC
B2	6	6	9	VCC
GND	7	7	10	GND
A3	8	8	12	VCC
B3	9	9	13	VCC
Y3	10	10	14	VCC
Y4	11	11	16	VCC
A4	12	12	18	VCC
B4	13	13	19	VCC
VCC	14	14	20	VCC

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

TRUTH TABLE

Inputs		Output
A	B	Z
0	0	1
0	1	0
1	0	0
1	1	1

5

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V, I_{OL} = 4.0 mA, V_{IL} = 0.7 V, other input = 2.0 V, or per truth table.
V_{IC}	Input Clamping Voltage		− 1.5					V	V_{CC} = 4.5 V, I_{IN} = − 18 mA, other input is open.
I_{CEX}	Open Collector Input Current		100		100		100	µA	V_{CC} = 4.5 V, V_{OUT} = 5.5 V, V_{IL} = 0.7 V, other input = 0.7 V, or per truth table.
I_{IH}	Logical "1" Input Current		40		40		40	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other input = GND.
I_{IHH}	Logical "1" Input Current		200		200		200	µA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V, other input = GND.
I_{IL}	Logical "0" Input Current	− 300	− 760	− 300	− 760	− 300	− 760	µA	V_{CC} = 5.5 V, V_{IN} = 0.4 V, other input = 5.5 V.
I_{CC}	Power Supply Current		13		13		13	mA	V_{CC} = 5.5 V, V_{IN} = 4.5 V, other input = GND.
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.7		0.7		0.7	V	V_{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V_{CC} = 5.0 V, V_{INL} = 0.4 V, and V_{INH} = 2.5 V.

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL1} t_{PHL1}	Propagation Delay /Data-Output Output High-Low	2.0 —	40 30	2.0 —	45 40	2.0 —	45 40	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ V_{CC} = 5.0 V, C_L = 15 pF, R_L = 2.0 kΩ
t_{PLH1} t_{PLH1}	Propagation Delay /Data-Output Output Low-High	2.0 —	45 30	2.0 —	56 51	2.0 —	56 51	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ V_{CC} = 5.0 V, C_L = 15 pF, R_L = 2.0 kΩ
t_{PHL2} t_{PHL2}	Propagation Delay /Data-Output Output Low-High	2.0 —	40 30	2.0 —	45 40	2.0 —	45 40	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ V_{CC} = 5.0 V, C_L = 15 pF, R_L = 2.0 kΩ
t_{PLH2} t_{PLH2}	Propagation Delay /Data-Output Output Low-High	2.0 —	45 30	2.0 —	56 51	2.0 —	56 51	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ V_{CC} = 5.0 V, C_L = 15 pF, R_L = 2.0 kΩ

NOTE:
1. The limits specified for C_L = 15 pF are guaranteed but not tested.