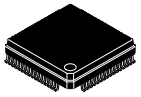
Document Number: MC33789
Rev. 4.0, 9/2014

Airbag System Basis Chip (SBC) with Power Supply and PSI5 Sensor Interface

33789

AUTO RESTRAINT



AE SUFFIX (PB-FREE)
EXPOSED PAD
98ASA10763D
64-PIN LQFP

The 33789, a SafeAssure SMARTMOS solution, is a mixed signal IC for airbag safety applications. The 33789 provides a cost effective and flexible system IC solution across the range of airbag partitions used in cars and other vehicles.

The 33789 connects to the 12 V vehicle battery and supplies the multiple voltages of a typical airbag system. The 33789 can detect switched input states, communicate with both local and remote crash sensors. It offers an industry standard interface (SPI) and four PSI5 master interfaces. The 33789 has a dedicated safing state machine that complements the airbag's MCU hardware/ software safing approach. Also included are a diagnostic - self protection capability and a programmable analog interface accessible by the system MCU.

The 33789 is well suited for use in low to high end airbag systems by allowing the designer to scale a design for the number of firing loops needed while providing enhanced safety and system reliability.

Features

- Designed to operate 5.2 V ≤ V_{PWR} ≤ 20 V, up to a 40 V transient
- Safing state machine with programmable sensing thresholds
- Two configurable high-side/low-side drivers with PWM capability
- Four PSI5 satellite sensor master interfaces
- Self-protected and diagnostic capability
- Watchdog and system Power ON Reset (POR)
- Supports complete airbag system power supply architecture, including system power mode control, supplies for squib firing (33 V), satellite sensors (6.3 V), and local ECU sensors and ECU logic circuits (5.0 V)
- Nine configurable switch input monitors for simple switch and Hall- effect sensor interfaces with internal power supply
- 16-bit SPI interface
- LIN 2.1 physical layer interface

Applications

- Airbag safety

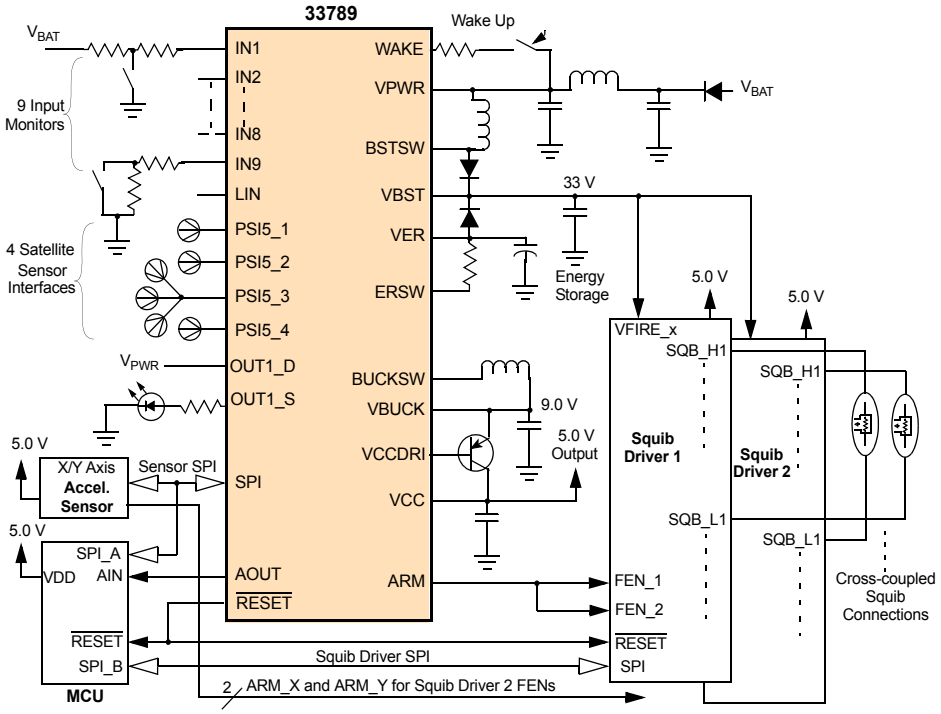


Figure 1. 33789 Simplified Application Diagram

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

ORDERABLE PARTS

This section describes the part numbers available to be purchased along with their differences. Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to http://www.freescale.com and perform a part number search for the following device numbers.

Table 1. Orderable Part Variations

Part Number	Notes	Temperature (T_A)	Package
MCZ33789BAE	(1)	-40 °C to 125 °C	64 LQFP EP

Notes

1. To order parts in Tape & Reel, add the R2 suffix to the part number.

INTERNAL BLOCK DIAGRAM

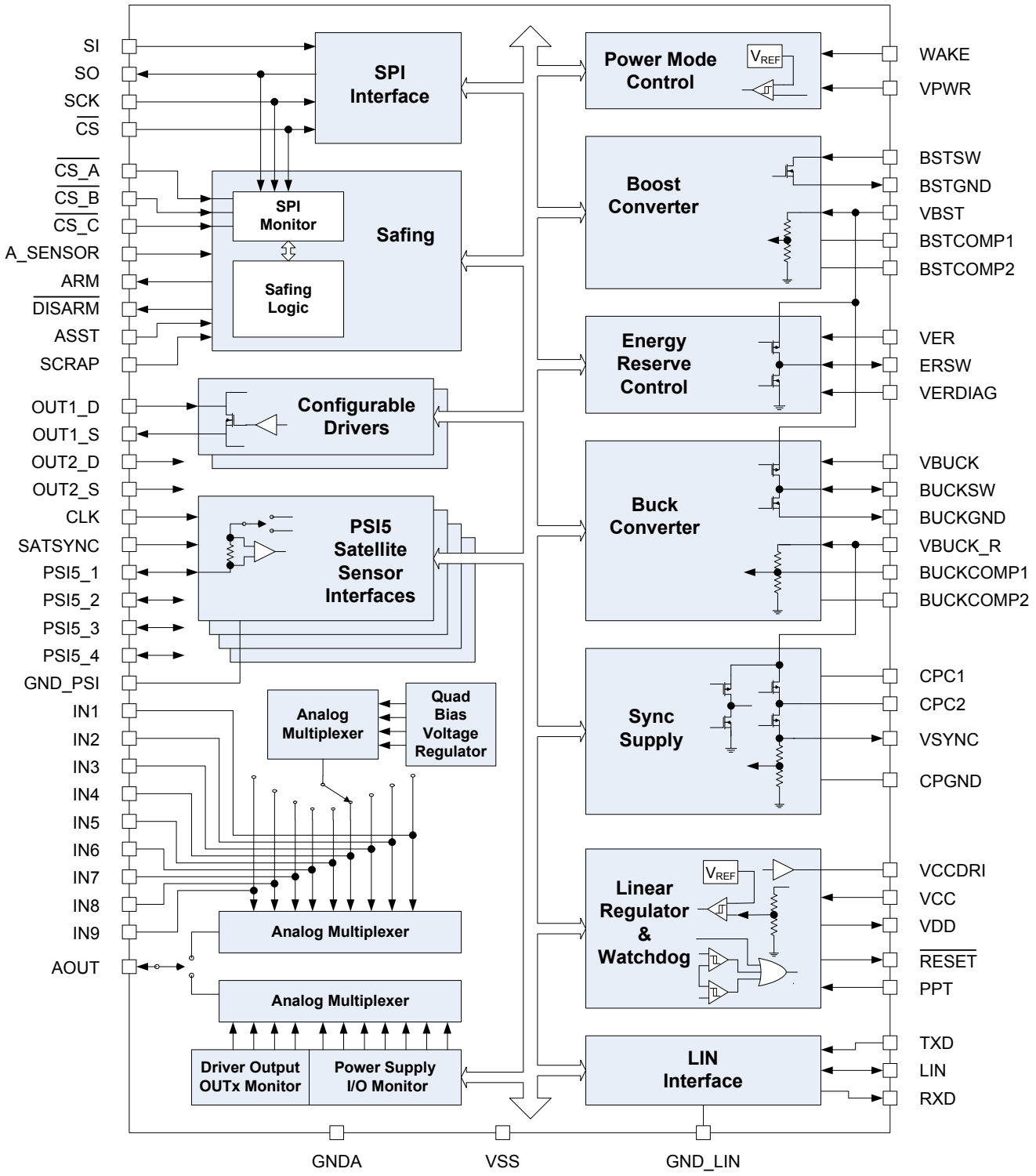


Figure 2. 33789 Simplified Internal Block Diagram

PIN CONNECTIONS

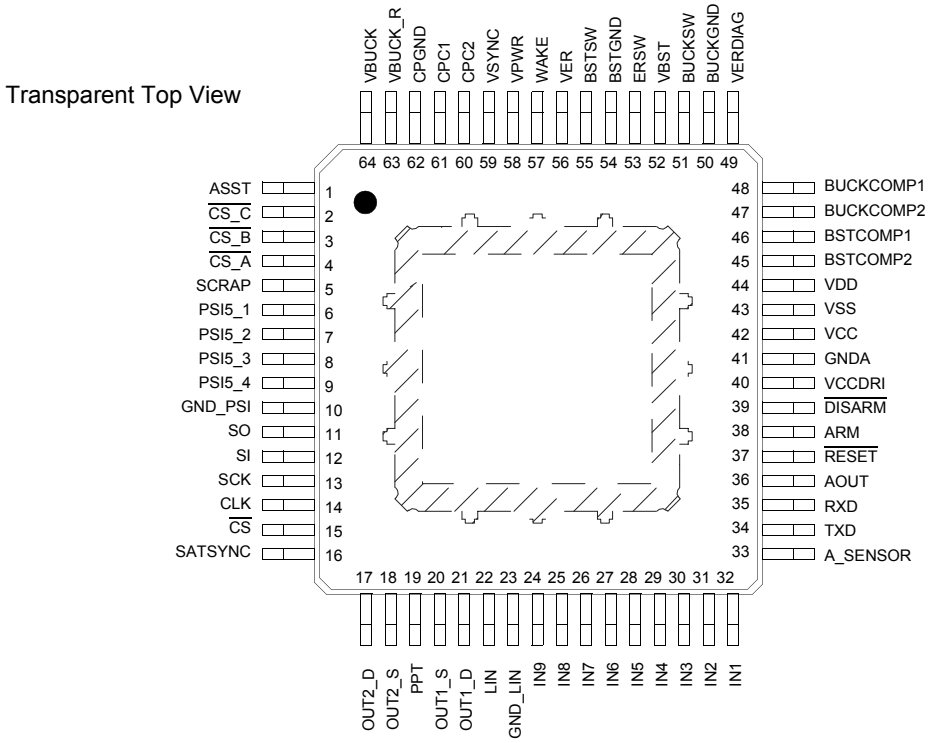


Figure 3. 33789 Pin Connections

A functional description of each pin can be found in the Functional Pin Description section beginning on page 26.

Table 2. 33789 Pin Definitions

Pin Number	Pin Name	Pin Function	Formal Name	Definition
1	ASST	Input	Analog Sensor Self-test	Active high input to initiate analog sensor self-test
2	$\overline{\text{CS\_C}}$	Input	Chip Select C	Active low SPI monitor chip select input dedicated for on-board sensor C.
3	$\overline{\text{CS\_B}}$	Input	Chip Select B	Active low SPI monitor chip select input dedicated for on-board sensor B
4	$\overline{\text{CS\_A}}$	Input	Chip Select A	Active low SPI monitor chip select input dedicated for on-board sensor A
5	SCRAP	Input	Scrap	Scrap command input
6	PSI5_1	Input/Output	PSI5 Interface 1	PSI5 standard interface 1 as satellite sensor channel 1
7	PSI5_2	Input/Output	PSI5 Interface 2	PSI5 standard interface 2 as satellite sensor channel 2
8	PSI5_3	Input/Output	PSI5 Interface 3	PSI5 standard interface 3 as satellite sensor channel 3
9	PSI5_4	Input/Output	PSI5 Interface 4	PSI5 standard interface 4 as satellite sensor channel 4
10	GND_PSI	Ground	PSI Ground	Dedicated ground point for PSI5 sensor
11	SO	Output	SPI Data Out	SPI data output
12	SI	Input	SPI Data In	SPI data input
13	SCK	Input	SPI Clock	SPI clock input
14	CLK	Input	Satellite Sensor Clock	Clock input for the PSI5 sensor interface(s) running in synchronous operation mode
15	$\overline{\text{CS}}$	Input	SPI Chip Select	Active low SPI chip select input from MCU, also used for satellite channels on SPI monitor

Table 2. 33789 Pin Definitions (continued)

Pin Number	Pin Name	Pin Function	Formal Name	Definition
16	SATSYNC	Input	Satellite Sync-pulse Trigger	Satsync command input from MCU to trigger PSI5 Sync-pulse
17	OUT2_D	Output	Output Driver2 Drain	Drain pin of the configurable driver2 outputs
18	OUT2_S	Output	Output Driver2 Source	Source pin of the configurable driver2 outputs
19	PPT	Input	Production Programming and Testing	Active high input to enable test-mode for production programming and testing. Not for application
20	OUT1_S	Output	Output Driver1 Source	Source pin of the configurable driver1 outputs
21	OUT1_D	Output	Output Driver1 Drain	Drain pin of the configurable driver1 outputs
22	LIN	Input/output	LIN Interface	LIN interface. It can be configured as a bi-directional pin which represents the single-wire bus transmitter and receiver
23	GND_LIN	Ground	LIN Ground	Dedicated ground point for a bi-directional pin which represents the single-wire bus transmitter and receiver
24	IN9	Input	Input Monitor Port 9	Port 9 of input monitor for DC sensor
25	IN8	Input	Input Monitor Port 8	Port 8 of input monitor for DC sensor
26	IN7	Input	Input Monitor Port 7	Port 7 of input monitor for DC sensor
27	IN6	Input	Input Monitor Port 6	Port 6 of input monitor for DC sensor
28	IN5	Input	Input Monitor Port 5	Port 5 of input monitor for DC sensor
29	IN4	Input	Input Monitor Port 4	Port 4 of input monitor for DC sensor
30	IN3	Input	Input Monitor Port 3	Port 3 of input monitor for DC sensor
31	IN2	Input	Input Monitor Port 2	Port 2 of input monitor for DC sensor
32	IN1	Input	Input Monitor Port 1	Port 1 of input monitor for DC sensor
33	A_SENSOR	Input	Analog Sensor Input	Analog sensor input for safing
34	TXD	Input	Data Input from UART	Logic-level data input from MCU UART transmitter for LIN/K-line
35	RXD	Output	Data Output to UART	Logic-level data output to MCU UART receiver for LIN/K-line
36	AOUT	Output	Analog Output	Analog output to send MCU scaled, multiplexed and buffered analog signals for diagnosis
37	$\overline{\text{RESET}}$	Output	Reset	Active low reset output
38	ARM	Output	Arm Enable	Active high safing enable signal to squib driver
39	$\overline{\text{DISARM}}$	Output	Arm Disable	Active low safing enable signal to squib driver
40	VCCDRI	Output	V_{CC} Bypass Transistor Drive	Linear regulator drive output to control an external PNP transistor for 5.0 V V_{CC} output
41	GNDA	Ground	Analog Ground	Analog ground
42	VCC	Input	V_{CC} Input	5.0 V V_{CC} input for monitoring and internal supply
43	VSS	Ground	Digital Ground	Digital ground
44	VDD	Output	Digital Power Supply Output	2.5 V linear regulator output for output capacitor connection.
45	BSTCOMP2	Input	Boost Compensation pin2	Connection 2 to the boost converter compensation network
46	BSTCOMP1	Input	Boost Compensation pin1	Connection 1 to the boost converter compensation network
47	BUCKCOMP2	Input	Buck Compensation pin2	Connection 2 to the buck converter compensation network
48	BUCKCOMP1	Input	Buck Compensation pin1	Connection 1 to the buck converter compensation network

Table 2. 33789 Pin Definitions (continued)

Pin Number	Pin Name	Pin Function	Formal Name	Definition
49	VERDIAG	Input	Energy Reserve Diagnosis	AC coupled energy reserve diagnostic input
50	BUCKGND	Ground	Buck Converter Ground	Ground return of the buck converter, buck switch ground
51	BUCKSW	Output	Buck Switch	Buck switch driver output to connect buck inductor
52	VBST	Input	Boost Voltage Input	Boost voltage input for boost loop feedback and source of buck converter, same voltage as boost output
53	ERSW	Output	Energy Reserve Switch	Storage driver output to control the energy reserve capacitor charging
54	BSTGND	Ground	Boost Converter Ground	Ground return of the boost converter, buck switch ground
55	BSTSW	Output	Boost Switch	Boost switch driver output to connect boost inductor
56	VER	Input	Energy Reserve Voltage	Energy reserve voltage input for the storage capacitor charge control and energy reserve monitor
57	WAKE	Input	Wake-up	Wake-up signal input to start-up boost and buck converters
58	VPWR	Input	Power Supply	Battery voltage power supply input
59	VSYNC	Input/output	Sensor Sync Power Supply	Satellite sensor sync voltage supply charge/discharge connection
60	CPC2	Output	Charge Pump Capacitor Pin2	Charge pump capacitor pin2
61	CPC1	Output	Charge Pump Capacitor Pin1	Charge pump capacitor pin1
62	CPGND	Ground	Charge Pump Ground	Charge pump ground
63	VBUCK_R	Input	Buck Converter Redundant Input	Redundant buck converter input to supply current for charge pump
64	VBUCK	Input	Buck Converter Input	Buck converter input for buck loop feedback and current source of charge pump

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 3. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
ELECTRICAL RATINGS			
Supply Input Voltage	V_{PWR}	-0.3 to 40	V
Wake-up Input Voltage	V_{WAKE}	-16 to 40	V
Supply Voltage - 1	V_{BST}, V_{BSTSW}, V_{BUCKSW}, V_{ERSW}, V_{ER}	-0.3 to 40	V
Supply Voltage - 2	V_{SYNC}, V_{CPC2}	-0.3 to 20	V
Supply Voltage - 3	V_{CPC1}, V_{BUCK}, V_{BUCK_R}, V_{CCDRI}	-0.3 to 10	V
Supply Voltage - 4	V_{ERDIAG}	-0.3 to 7	V
Supply Voltage - 5	V_{CC}	-0.3 to 5.5	V
Supply Voltage - 6	V_{DD}, $V_{BSTCOMP1}$, $V_{BSTCOMP2}$, $V_{BUCKCOMP1}$, $V_{BUCKCOMP2}$	-0.3 to 3	V
LIN Interface Voltage	V_{LIN}	-27 to 40	V
I/O Voltage - 1	V_{OUT1_D}, V_{OUT1_S}, V_{OUT2_D}, V_{OUT2_S}	-1 to 40	V
I/O Voltage - 2	V_{IN1} ~ V_{IN9}, V_{PSI5_1} ~ V_{PSI5_4}	-1 to 20	V
I/O Voltage - 3	V_{ARM}, $V_{\overline{DISARM}}$, V_{PPT}	-0.3 to 10	V
I/O Voltage - 4	V_{A_SENSOR}, V_{AOUT}, V_{ASST}, V_{SCRAP}, $V_{\overline{RESET}}$, V_{TXD}, V_{RXD}, V_{SI}, V_{SO}, V_{SCK}, V_{CLK}, $V_{\overline{CS}}$, $V_{\overline{CS\_A}}$, $V_{\overline{CS\_B}}$, $V_{\overline{CS\_C}}$, $V_{SATSYNC}$	-0.3 to 5.5	V
GND Shift	V_{SS}, V_{GND_LIN}, V_{CPGND}, V_{GND_PSI}	-0.3 to 0.3	V
LIN Bus Voltage[2] Normal Operation (DC) Transient (Coupled Through 1.0 nF Capacitor, according to ISO7637-2 & ISO7637-3) (See Table 4 and Figure 4) - Pulse 1 (test up to the limit for Damage - Class C[1]) - Pulse 2a (test up to the limit for Damage - Class C[1]) - Pulse 3a (test up to the limit for Damage - Class C[1]) - Pulse 3b (test up to the limit for Damage - Class C[1])	$V_{BUS(SS)}$ $V_{BUS(S1)}$ $V_{BUS(S2A)}$ $V_{BUS(S3A)}$ $V_{BUS(S3B)}$	-27 to 40 -100 +75 -150 +100	V

Notes

1. Class C: At least one function of the transceiver stops working properly during the test, and will return to the proper operation automatically when the exposure to the disturbance has ended. No physical damage of the IC occurs.
2. The LIN bus voltage is applied on the LIN pin as V_{LIN} during tests.

Table 3. Maximum Ratings *(continued)*

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
ESD Capability			
AECQ100			
Human Body Model - JESD22/A114[3]			
All pins	V_{ESD1-1}	±2.0 k	
Charge Device Model - JESD22/C101[3]			
Corner pins	V_{ESD2-1}	±750	
VCCDRI pin	V_{ESD2-2}	±400	V
All other pins	V_{ESD2-3}	±500	
Additional for LIN Conformance			
Contact Discharge, Unpowered[4]			
LIN pin without capacitor	V_{LIN_ESD1-1}	±6.0 k	
LIN pin with 220 pF capacitor	V_{LIN_ESD1-2}	±6.0 k	
LIN pin with 220 pF capacitor and indirect ESD coupling (according to ISO10605 - Annex F)	V_{LIN_ESD1-3}	±8.0 k	
THERMAL RATINGS			
Operating Temperature			
Junction Temperature	T_J	-40 to 150	°C
Case (Exposed Pad) Temperature	T_C	-40 to 125	
Storage Temperature	T_{STG}	-65 to +150	°C
Peak Package Reflow Temperature During Reflow[5], [6]	T_{PPRT}	Note 6	°C
THERMAL RESISTANCE			
Junction to Ambient (Natural Convection)	θ_{JA}	26	°C/W
Junction to Case (Exposed Pad)	θ_{JC}	1.5	°C/W

Notes

3. ESD testing is performed in accordance with the Human Body Model (HBM) (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), and the Charge Device Model (CDM) (C_{ZAP} = 4.0 pF).
4. According to “Hardware Requirements for LIN, CAN, and Flexray Interfaces in Automotive Applications” specification Rev. 1.1/December 2, 2009 (C_{ZAP} = 150 pF, R_{ZAP} = 330 Ω).
5. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
6. Freescale’s Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts (i.e. MC33xxxD enter 33xxx), and review parametrics.

Table 4. Limits / Maximum Test Voltage for LIN Pin Transient Immunity Tests

Test Pulse	V_S [V]	Pulse Repetition Frequency [Hz] ($1/T_1$)	Test Duration [min]	R_i [W]	Remarks
1	-100	2	10	10	t_2 = 0s
2a	+75	2	10	2	
3a	-150	10	10	50	
3b	+100	10	10	50	

Notes

7. V_{SUP} is applied on the VPWR pin as a test condition.

The I/V characteristic and leakage of the pin is performed before and after the test.

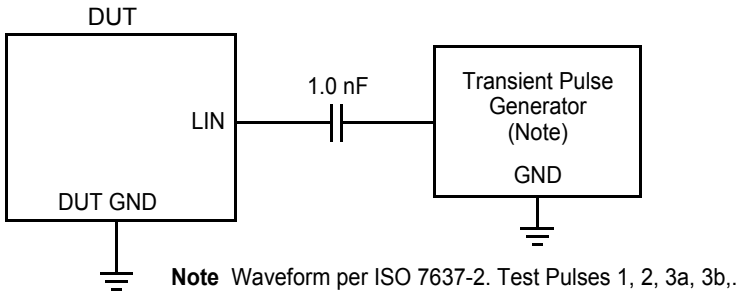
The supply pins and LIN must pass the V_S voltage level specified in Table 4 without damage.

The failure validation during test is evaluated at RxD.

Tests perform in Normal mode on LIN (Failure on RxD), V_{SUP} (Failure on LIN)(7).

The voltage level found is for information only.

Failure criteria on RxD in Normal Mode: ±0.9 V and ±7.5 µs



Note Waveform per ISO 7637-2. Test Pulses 1, 2, 3a, 3b,.

Figure 4. Test Circuit for Transient Test Pulses (LIN)

STATIC ELECTRICAL CHARACTERISTICS

Table 5. Static Electrical Characteristics

Characteristics noted under conditions 7.0 V ≤ V_{SUP}[8] ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
POWER MANAGEMENT						
V_{PWR}	Power Supply Input Voltage Normal Operation	5.2	-	20	V	
V_{WAKE_TH}	Wake-up Threshold Voltage Normal V_{PWR} Range	0.3* V_{PWR}	0.5* V_{PWR}	0.7* V_{PWR}	V	
R_{WAKE}	Wake-up Input Internal Pull-down Resistance	120	200	320	kΩ	
V_{BST}	Boost Converter Output Voltage Normal V_{PWR} Range, 0 ≤ I_{BST} ≤ Max. I_{BST}	31.6	33.3	35	V	
V_{BST_OV}	Boost Overvoltage Threshold	36	38	40	V	
$V_{BST\_OV\_CLMP}$	Boost Overvoltage Clamping Boost operating with active clamping	40	43	46	V	
$V_{BST\_OV\_HYS}$	Boost Overvoltage Hysteresis	2.2	2.6	3.0	V	
V_{BST_UV}	Low V_{PWR} as Boost Undervoltage Lockout Threshold and IGNSTAT Detect Threshold	4.7	4.95	5.2	V	
$V_{BST\_UV\_HYS}$	Boost Undervoltage Hysteresis	0.3	0.5	0.8	V	
R_{BSTSW_ON}	Boost Switch Transistor On Resistance	-	-	550	mΩ	
I_{BSTSW_LMT}	Boost Switch Current Limit	1.3	1.5	1.8	A	
T_{SW_SHDN}	Power Switch Thermal Shutdown	155	175	195	°C	
T_{SW_HYST}	Power Switch Thermal Shutdown Hysteresis	15	-	30	°C	
ESR_{CERM}	Energy Reserve Capacitor ESR Measurement Range	200	-	600	mΩ	
-	C_{ER} ESR Measurement Tolerance	-50	-	50	mΩ	
-	C_{ER} Capacitance Measurement Tolerance	-15	-	15	%	
$R_{ERSW\_CH\_ON}$	C_{ER} Charge Transistor On Resistance	3.0	10	14	Ω	
$I_{ERSW\_CH\_SHDN}$	C_{ER} Charge Transistor Overcurrent Shutdown Threshold	400	550	800	mA	
$R_{ERSW\_DISCH\_ON}$	C_{ER} Discharge Transistor On Resistance	2.0	5.5	8.0	Ω	
$I_{ERSW\_DISCH\_SHDN}$	C_{ER} Discharge Transistor Overcurrent Shutdown Threshold	350	450	800	mA	
I_{ERSW_LEAK}	ERSW Pin Leakage Current	-	-	250	nA	
I_{VER_LEAK}	VER Pin Leakage Current	-	-	200	μA	
V_{ER_RESD}	C_{ER} Residual Voltage after 10 s Discharge	-	-	2.5	V	
V_{BUCK}	Buck Converter Output Voltage 10 V ≤ V_{BST} ≤ 40 V, 100 mA ≤ I_{BUCK} ≤ I_{BUCK_C}	8.73	9.0	9.27	V	
$V_{BUCK\_OV\_SHDN}$	Buck Converter Output Overvoltage Shutdown Threshold	9.6	10	10.8	V	
V_{BUCK_UV}	Low V_{BST} as Buck Converter Start-up Threshold	13.5	15.5	17.5	V	
V_{BUCK_RIPL}	Buck Converter Output Ripple Voltage 6.0 V ≤ V_{PRW} ≤40 V, 100 mA ≤ I_{BUCK} ≤ I_{BUCK_C}	-	-	460	mV_{PP}	

Notes

8. V_{SUP} is applied on the VPWR pin as a test condition.

Table 5. Static Electrical Characteristics (continued)

Characteristics noted under conditions 7.0 V ≤ V_{SUP}[8] ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
POWER MANAGEMENT (CONTINUED)						
I_{BUCK_C}	Buck Converter Output Current Capability	400	-	-	mA	
V_{BUCK_LOAD}	Buck Converter Load Regulation I_{BUCK} = 100 mA, ΔI_{BUCK} = 100 mA I_{BUCK} = 300 mA, ΔI_{BUCK} = 100 mA	 - -	 5.0 4.0	 8.0 6.0	mV	
$I_{BUCKSW\_HS\_LMT}$	Buck High-side Switch Current Limit	500	800	1100	mA	
V_{SYNC}	Sync Supply Output Voltage 6.0 V ≤ V_{PRW} ≤ 40 V	15	-	2x V_{BUCK}	V	
V_{SYNC_RIPL}	Sync Supply Output Ripple Voltage 6.0 V ≤ V_{PRW} ≤ 40 V	-	-	300	mV_{PP}	
I_{SYNC_C}	Sync Supply Output Current Capability	20	-	-	mA	
I_{SYNC_OC}	Sync Switch Overcurrent Protection Limit	65	-	150	mA	
V_{CC}	V_{CC} Supply Output Voltage 6.0 V ≤ V_{BUCK} ≤ 9.5 V, 0 ≤ I_{CC} ≤ 200 mA	4.85	5.0	5.15	V	
-	V_{CC} Supply Line Regulation V_{PWR-AC} = 200 mV_{PP}, f_{PWR-AC} ≤ 500 kHz	20	-	-	dB	
-	V_{CC} Supply Load Regulation I_{CC-DC} = 0.8* I_{CC_MAX}, ΔI_{CC} = 50 mA	-	-	10	mV	
V_{CC_NOISE}	V_{CC} Supply Noise Voltage	-	5.0	20	mV_{PP}	
I_{VCCDRI_LMT}	V_{CC} Base Driver Current Limit T_A = 25°C, Temperature coefficient = 300 ppm/ °C (typ.)	9.0	13.5	22	mA	
V_{BUCK_VCC}	Minimum V_{BUCK} Voltage for V_{CC} Operation	-	-	6.0	V	
V_{BST_VCC}	Minimum V_{BST} Voltage for V_{CC} Operation	-	-	7.0	V	
V_{DD}	V_{DD} Supply Voltage	-	2.5	-	V	
RESET AND WATCHDOG						
$V_{\overline{RESET}\_H}$	Reset Output High $I_{\overline{RESET}}$ = -2.0 mA	V_{CC} - 0.4	-	V_{CC}	V	
$V_{\overline{RESET}\_L}$	Reset Output Low $I_{\overline{RESET}}$ = 2.0 mA	0.0	-	0.4	V	
V_{CC_OP}	Rising V_{CC} Threshold for Reset Operation	-	-	1.5	V	
V_{CC_OV}	V_{CC} Overvoltage for Reset	5.2	-	5.5	V	
V_{CC_UV}	V_{CC} Undervoltage for Reset	4.5	-	4.80	V	
$V_{CC\_VM\_HYS}$	V_{CC} Voltage Monitor Threshold Hysteresis	30	-	-	mV	
V_{DD_OV}	V_{DD} Overvoltage for Reset	2.7	-	3.0	V	
V_{DD_UV}	V_{DD} Undervoltage for Reset	1.85	1.90	2.10	V	
$V_{GNDA\_GND\_LIN\_TH}$	GNDA to GND_LIN Voltage Difference to Activate Open GNDA Detection	0.3	-	0.8	V	

Table 5. Static Electrical Characteristics (continued)

Characteristics noted under conditions 7.0 V ≤ V_{SUP}[8] ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
SATELLITE SENSOR INTERFACE						
$I_{SAT\_BUS\_SUP\_Q}$	Satellite Bus Supply Quiescent Current	-	-	2.2	mA	
$I_{SAT\_BUS\_SUP}$	Satellite Bus Supply Operation Current	-	-	4.0	mA	
$I_{SAT\_SYNC\_SUP\_Q}$	Sync Supply Quiescent Current	-	-	1.0	mA	
$I_{SAT\_SYNC\_SUP}$	Sync Supply Operation Current	-	-	1.0	mA	
$I_{SAT\_VCC\_Q}$	Satellite Logic Supply Quiescent Current	-	-	1.0	mA	
I_{SAT_VCC}	Satellite Logic Supply Operation Current	-	-	3.0	mA	
V_{SAT_OUT}	Satellite Interface DC Output Operation Voltage 0 ≤ I_{SAT_OUT} ≤ 65 mA	5.8	6.3	6.7	V	
$V_{SAT\_OUT\_DIS}$	Satellite Interface DC Output Disable Voltage I_{SAT_OUT} = 0 mA	-	-	0.5	V	
$P_{SRRSAT\_BUS\_SUP}$	Satellite Interface Ripple Rejection from Bus Supply 50 kHz ≤ f_{RIPL} ≤ 280 kHz 280 kHz ≤ f_{RIPL} ≤ 560 kHz	30 20	- -	- -	dB	
V_{SAT_RIPL}	Satellite Interface Ripple Voltage due to Current Modulation (typical application configuration)	-	-	200	mV_{PP}	
$V_{SAT\_SYNC\_ABS}$	Sync Pulse Absolute Voltage	10	-	12	V	
$V_{SAT\_SYNC\_STEP}$	Sync Pulse Voltage Step	V_{SAT_OUT} + 4.3	-	V_{SAT_OUT} + 5.5	V	
$V_{SATSYNC\_L}$	SATSYNC Input Low Voltage	-0.3	-	1.0	V	
$V_{SATSYNC\_H}$	SATSYNC Input High Voltage	2.0	-	V_{CC}+0.3	V	
$I_{SATSYNC\_PULLDN}$	SATSYNC Input Pull-down Current	10	-	50	µA	
I_{SAT}	Satellite Interface Operational Current Range	0.0	-	65	mA	
$I_{SAT\_PD\_LIM}$	Satellite Interface Pull-down Current Limit	27	-	60	mA	
I_{SAT_OC}	Satellite Interface Overcurrent Limit	70	-	120	mA	
$I_{SAT\_Q\_RANGE\_MIN}$	Minimum Satellite Quiescent Current Adaptation Level	1.9	-	3.8	mA	
$I_{SAT\_Q\_RANGE\_MAX}$	Maximum Satellite Quiescent Current Adaptation Level	35	-	50	mA	
$I_{SAT\_Q\_SINGLE}$	Satellite Quiescent Current for Single Satellite Synchronous Satsync-steered Mode	4.0	-	18.5	mA	
$I_{SAT\_Q\_DUAL}$	Satellite Quiescent Current for Dual Satellite Synchronous Satsync-steered Mode	8.0	-	26.5	mA	
$I_{SAT\_Q\_TOTAL}$	Total Bus Quiescent Current Synchronous TDM Mode	4.0	-	35	mA	
-	Satellite Quiescent Current Detect Accuracy 4.0 mA = Current Threshold = 14 mA 14 mA = Current Threshold = 35 mA	-10 -6.0	- -	10 6.0	%	
I_{SAT_MOD}	Satellite Sensor Modulation Current	20	-	30	mA	
$I_{SAT\_TH\_RANGE}$	Satellite Data Comparator Current Threshold Range	15.75	-	48.25	mA	
$I_{SAT\_TH\_OFS}$	Satellite Data Comparator Threshold Current Offset	11.25	12.5	13.75	mA	
$I_{SAT\_TH\_HYST}$	Satellite Data Detection Current Threshold Hysteresis	2.0	-	3.5	mA	

Table 5. Static Electrical Characteristics (continued)

Characteristics noted under conditions 7.0 V ≤ V_{SUP}[8] ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
SYNC PULSE LIMITS FOR SYNCHRONOUS TDM MODE (SEE Figure 5. SYNCHRONOUS TDM MODE SYNC PULSE TIMING)						
V_{t0}	Sync Slope Reference Voltage	-	0.5	-	V	
V_{t2}	Sync Signal Sustain Voltage	4.3	-	5.5	V	
DC SENSOR INTERFACE						
I_{DCREG_LMT}	DC Sensor Supply Regulator Current Limit	30	-	55	mA	
$I_{DCREG\_OC\_DIFF}$	Current Difference Between the Regulator Overcurrent Detection Threshold and the Regulator Current Limit $I_{DCREG\_OC\_DIFF} = I_{DCREG\_LMT} - I_{DCREG\_OC}$	1.0	9.0	18	mA	(9)
V_1	Regulated Output Voltage 1	1.35	1.5	1.73	V	
V_2	Regulated Output Voltage 2	2.25	2.5	2.75	V	
V_3	Regulated Output Voltage 3	4.5	5.0	5.5	V	
V_4	Regulated Output Voltage 4	5.85	6.5	7.15	V	
-	Output Voltage Overshoot When Changing the Setting Measured as Percentage of the Voltage Step	-	-	25	%	
R_{DCREG_FBK}	Regulator Feedback Load Resistance	100	200	300	kΩ	
Th_{DCREG_SD}	Regulator Thermal Shutdown Temperature	155	175	195	°C	
Th_{DCREG_HYS}	Regulator Thermal Shutdown Hysteresis	15	-	30	°C	
C_{INx}	INx Load Capacitance	12.5	-	220	nF	
K_{CONV}	DC Sensor Interface Current to Voltage Conversion Factor (See Figure 21) I_{INx}: 2.5 mA ~ 25 mA	0.163	0.177	0.190	V/mA	
V_{CONV_NLIN}	DC Sensor Interface Current to Voltage Conversion Nonlinearity	-	-	20	mV_{RMS}	
$V_{INx\_I\_OFS}$	Current Measurement Output Offset Voltage I_{INx} = 0, C_{INx} = 0.22 nF, R_{INx} = 1.0 MΩ V_1 = 1.5 V V_2 = 2.5 V V_3 = 5.0 V V_4 = 6.5 V	0.0 0.0 0.0 0.0	28 29 33 38	50 55 60 65	mV	
V_{INx_OFS}	INx Pin Offset Voltage Voltage Source not Enable and I_{INx} = 0	-	-	1.0	V	
I_{INx_PULLDN}	INx Active Pull-down Current 2.0 V ≤ V_{INx} ≤ 7.15 V and INx is not selected	-110	-85	-30	µA	

Notes

9. I_{DCREG_OC} is the regulator overcurrent detection threshold to trigger the regulator switch between a voltage source and a current source.

Table 5. Static Electrical Characteristics (continued)

Characteristics noted under conditions 7.0 V ≤ V_{SUP}[8] ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
ANALOG OUTPUT						
V_{AOUT}	Analog Output Voltage	GND	-	V_{CC}	V	
V_{AOUT_OFS}	Analog Buffer Offset	-20	-	20	mV	
A	Analog Output Buffer Gain For Output Voltage Monitors For DC Sensor Interface INx Voltage Monitors	 0.99 0.48	 1.0 0.5	 1.01 0.52		
K_1	Scale Factor of Pin VBST Monitor V_{BST} ≤ 35 V	8.0	8.5	9.1		
K_2	Scale Factor of Pin VER Monitor V_{ER} ≤ 35 V	8.0	8.5	9.1		
K_3	Scale Factor of Pin VERDIAG Monitor	4.5	5.0	5.5		
K_4	Scale Factor of Pin VBUCK Monitor V_{BUCK} ≤ 10 V	2.6	2.8	2.9		
K_5	Scale Factor of Pin VSYNC Monitor V_{SYNC} ≤ 20 V	4.5	5.0	5.5		
K_6	Scale Factor of Pin VPWR Monitor V_{PWR} ≤ 20 V	5.2	5.6	5.9		
K_7	Scale Factor of Pin OUTx_D Monitor	5.2	5.6	5.9		
K_8	Scale Factor of Pin OUTx_S Monitor	5.2	5.6	5.9		
CONFIGURABLE DRIVERS						
$V_{OUTx\_S\_ON\_HS}$	Drain-Source On Voltage in High-side Driver Configuration V_{OUTx_D} = 18 V, I_{OUTx_S} = 70 mA	V_{OUTx_D} – 0.5	-	V_{OUTx_D}	V	
$V_{OUTx\_D\_ON\_LS}$	Drain-Source On Voltage in Low-side Driver Configuration V_{OUTx_S} = 0 V, I_{OUTx_D} = 70 mA	V_{OUTx_S}	-	V_{OUTx_S} + 0.5	V	
$I_{OUTx\_S\_LMT}$	High-side Driver Current Limit V_{OUTx_D} = 18 V, V_{OUTx_S} = 0 V	70	-	110	mA	
$I_{OUTx\_D\_LMT}$	Low-side Driver Current Limit V_{OUTx_D} = 18 V, V_{OUTx_S} = 0 V	-110	-	-70	mA	
Th_{OUTx_SD}	Driver Thermal Shutdown Temperature	155	175	195	°C	
Th_{OUTx_HYS}	Driver Thermal Shutdown Hysteresis	15	-	30	°C	
$I_{OUTx\_D\_LEAK\_GND}$	Drain Leakage to GND $V_{\overline{RESET}}$ = 0 V, or in Sleep Mode, V_{OUTx_D} = 0 V $V_{\overline{RESET}}$ = 5 V, V_{PWR} = 18 V, Driver Off, V_{OUTx_D} = 0 V	 -1.0 45	 - -	 1.0 100	µA	
$I_{OUTx\_D\_LEAK\_BAT}$	Drain Leakage to Battery $V_{\overline{RESET}}$ = 0 V, V_{OUTx_D} = V_{PWR} $V_{\overline{RESET}}$ = 5.0 V, V_{PWR} =18 V, Driver Off, V_{OUTx_D} = 18 V	 -1.0 -100	 - -	 1.0 -45	µA	
$V_{OUTx\_D\_OPEN}$	Open Drain Voltage $V_{\overline{RESET}}$ = 5.0 V, Driver Off	0.4 x V_{PWR}	-	0.6 x V_{PWR}	V	
$I_{OUTx\_S\_LEAK\_GND}$	Source Leakage to GND $V_{\overline{RESET}}$ = 0 V, or in Sleep Mode, V_{OUTx_S} = 0 V $V_{\overline{RESET}}$ = 5.0 V, V_{PWR} = 18 V, Driver Off, V_{OUTx_S} = 0 V	 -1.0 50	 - -	 1.0 100	µA	

Table 5. Static Electrical Characteristics (continued)

Characteristics noted under conditions 7.0 V ≤ V_{SUP}[8] ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
CONFIGURABLE DRIVERS (CONTINUED)						
$I_{OUTx\_S\_LEAK\_BAT}$	Source Leakage to Battery $V_{\overline{RESET}}$ = 0 V, V_{OUTx_S} = V_{PWR} $V_{\overline{RESET}}$ = 5.0 V, V_{PWR} = 18 V, Driver Off, V_{OUTx_S} = 18 V	0.0 -100	- -	300 -50	µA	
$V_{OUTx\_S\_OPEN}$	Open Source Voltage $V_{\overline{RESET}}$ = 5.0 V, Driver Off	0.4 x V_{PWR}	-	0.6 x V_{PWR}	V	
$V_{TH\_2/3}$	2/3 V_{PWR} Comparator Threshold for Diagnostics 6.0 V ≤ V_{PWR} ≤ 18 V	0.6 x V_{PWR}	0.666 x V_{PWR}	0.734 x V_{PWR}	V	
$V_{TH\_1/3}$	1/3 V_{PWR} Comparator Threshold for Diagnostics 6.0 V ≤ V_{PWR} ≤ 18 V	0.266 x V_{PWR}	0.333 x V_{PWR}	0.4 x V_{PWR}	V	
D_{OUTx}	PWM Duty Cycle Fixed Frequency = 128 Hz, Increment step = 1.6%	0.0	-	100	%	
GENERAL LOGIC INPUTS: $\overline{CS}$, $\overline{CS\_X}$, SCK, SI, ASST, SCRAP, CLK						
V_{LGIN_H}	Logic Input High	2.0	-	V_{CC} + 0.3	V	
V_{LGIN_L}	Logic Input Low	-0.3	-	1.0	V	
I_{LGIN_PULLUP}	Logic Input Pull-up Current For $\overline{CS}$: V_{LGIN} = $V_{\overline{CS}}$ ≤ 2.0 V For others: V_{LGIN} ≤ 4.5 V	10	-	50	µA	
I_{LGIN_LEAK}	Logic Input Leakage V_{LGIN} = V_{DD}	-2.0	-	5.0	µA	
SPI (OTHERS) AND SPI MONITOR INTERFACE						
V_{SO_L}	SO Voltage Low I_{SO} = 0.5 mA	-	-	0.4	V	
V_{SO_H}	SO Voltage High I_{SO} = -0.2 mA	V_{CC} - 0.4	-	V_{CC}	V	
ANALOG SENSOR INPUT						
V_{IN_ANA}	Analog Sensor Input Voltage	0.0	-	V_{CC}	V	
I_{IN_ANA}	Analog Sensor Input Pull-down Current	2.0	-	8.0	µA	
ARM ENABLE / DISABLE OUTPUTS						
V_{ARM_H}	ARM / $\overline{DISARM}$ Output High	V_{CC} - 0.4	-	V_{CC}	V	
V_{ARM_L}	ARM / $\overline{DISARM}$ Output Low	0.0	-	0.4	V	
I_{ARM_LEAK}	ARM / $\overline{DISARM}$ Output High-impedance Leakage	-2.0	-	2.0	µA	
PRODUCTION PROGRAM AND TEST INPUT						
R_{PPT_IN}	PPT Input Pull-down Resistance	100	230	400	kΩ	
V_{PPT_TEST}	PPT Input Test Mode Enable Threshold	4.0	4.5	5.0	V	

Table 5. Static Electrical Characteristics (continued)

Characteristics noted under conditions 7.0 V ≤ V_{SUP}[8] ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
LIN TRANSCEIVER LOGIC INTERFACE						
V_{RXD_OL}	RXD Output Low Level Voltage I_{RXD_IN} ≤ 1.5 mA sinking current	0.0	—	0.9	V	
V_{RXD_OH}	RXD Output High Level Voltage I_{RXD_OUT} ≤ 250 µA source current	4.25	—	5.25	V	
V_{TXD_IL}	TXD Input Low Level Voltage	—	—	0.8	V	
V_{TXD_IH}	TXD Input High Level Voltage	2.0	—	—	V	
$V_{TXD\_IN\_HYST}$	TXD Input Threshold Voltage Hysteresis	100	300	600	mV	
I_{TXD_PULLUP}	TXD Pull-up Current Source 1.0 V < V_{TXD} < 3.5 V	-60	-35	-20	µA	
LIN TRANSCEIVER PHYSICAL LAYER [14],[12]						
V_{BAT}	Operating Voltage Range	8.0	–	18	V	(10)
V_{SUP}	Operating Supply Voltage Range	7.0	–	18	V	
$V_{SUP\_NON\_OP}$	Supply Voltage Range (within which the device is not destroyed)	-0.3	–	40	V	
I_{BUS_LIM}	Current Limitation for Driver Dominant State Driver ON, V_{BUS} = 18 V	40	90	200	mA	
$I_{BUS\_PAS\_DOM}$	Input Leakage Current at the Receiver Driver off; V_{BUS} = 0 V; V_{BAT} = 12 V	-1.0	–	–	mA	
$I_{BUS\_PAS\_REC}$	Leakage Output Current to GND Driver Off; 8.0 V < V_{BAT} < 18 V; 8.0 V < V_{BUS} < 18 V; V_{BUS} ≥ V_{BAT}; V_{BUS} ≥ V_{SUP}	–	–	20	µA	
$I_{BUS\_NO\_GND}$	Control Unit Disconnected from Ground GND_{DEVICE} = V_{SUP}; V_{BAT} = 12 V; 0 < V_{BUS} < 18 V	-1.0	–	1.0	mA	(11)
I_{BUSNO_BAT}	V_{BAT} Disconnected; V_{SUP_DEVICE} = GND; 0 V < V_{BUS} < 18 V	–	–	100	µA	(13)
V_{BUSDOM}	Receiver Dominant State	–	–	0.4* V_{SUP}	V	
V_{BUSREC}	Receiver Recessive State	0.6* V_{SUP}	–	–	V	
V_{BUS_CNT}	Receiver Threshold Center (V_{TH_DOM} + V_{TH_REC})/2	0.475* V_{SUP}	0.5* V_{SUP}	0.525* V_{SUP}	V	
V_{HYS}	Receiver Threshold Hysteresis (V_{TH_REC} - V_{TH_DOM})	–	–	0.175* V_{SUP}	V	
$V_{SERDIODE}$	Voltage Drop at the Serial Diode in Pull-up Path	0.4	–	1.0	V	
V_{SHIFT_BAT}	V_{BAT}_SHIFT	0.0	–	11.5%	V_{BAT}	
V_{SHIFT_GND}	GND_SHIFT	0.0	–	11.5%	V_{BAT}	
V_{UVL}, V_{UVH}	LIN Undervoltage Threshold (positive and negative)	5.9	–	6.7	V	
V_{UVHYST}	LIN Undervoltage Hysteresis (V_{UVL} - V_{UVH})	–	100	–	mV	

Table 5. Static Electrical Characteristics (continued)

Characteristics noted under conditions 7.0 V ≤ V_{SUP}[8] ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
LIN TRANSCEIVER PHYSICAL LAYER (CONTINUED) [14],[12]						
V_{BUSWU}	LIN Wake-up Threshold from Sleep Mode	–	4.3	5.0	V	
R_{SLAVE}	LIN Pull-up Resistor to V_{SUP}	20	40	60	kΩ	

Notes

10. Voltage range at the battery level, including the reverse battery diode.
11. Loss of local ground must not affect communication in the residual network.
12. In this LIN Physical Layer EC section, use VSUP to represent VPWR and use VBUS to represent VLIN, in order to be consistent with the LIN Protocol Specification, and other Freescale LIN product specifications.
13. Node has to sustain the current that can flow under this condition. The bus must remain operational under this condition.
14. Guaranteed by design.

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 6. Dynamic Electrical Characteristics

Characteristics noted under conditions 7.0 V ≤ V_{SUP}[15] ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
POWER MANAGEMENT						
t_{BSTSW}	Boost Switch Transistor Switching Time	20	50	150	ns	
t_{SYNCSW}	Sync Switch Transistor Switching Time	10	-	250	ns	
t_{VCC_RISE}	V_{CC} Voltage Rise Time From 0.1xV_{CC} to 0.9xV_{CC}	200	-	1800	µs	
$t_{VCC\_VM\_REJ}$	V_{CC} Voltage Monitor Deglitch Filter Time	45	50	55	µs	
$t_{VCC\_VM\_RST}$	V_{CC} Voltage Monitor Reset Time Delay	10	-	15	ms	
t_{WDW_MIN}	Watchdog Refresh Window Lower Limit	275	-	400	µs	
t_{WDW_MAX}	Watchdog Refresh Window Upper Limit	650	-	900	µs	
-	Reset Pin Activation Time for Watchdog Error	0.7	-	1.0	ms	
$f_{BST/BUCK}$	Boost and Buck Regulators Switch Frequency Low Speed Frequency High Speed Frequency	 133 232	 140 245	 147 258	kHz	(16)
f_{SYNC_CP}	Sync Supply Charge Pump Switch Frequency	-	160	-	kHz	
SATELLITE SENSOR INTERFACE PSI5						
f_{CLK}	Satellite Interface Input Clock Frequency Synchronous SATSYNC-steered mode Synchronous TDM mode	 3.92 3.98	 4.00 4.00	 4.08 4.02	MHz	
f_{SAT}	Satellite bit Rate Operation Range	118.75	125	131.25	kHz	
D_{SAT_IMOD}	Satellite Sensor Current Modulation Duty Cycle Synchronous SATSYNC-steered mode Synchronous TDM mode	 45 47	 - -	 55 53	%	
$t_{SAT\_IMOD\_FR}$	Satellite Sensor Current Signal Rising and Falling Time From 10% to 90% of Modulation Amplitude	0.5	-	1.0	µs	
SR_{SAT_IMOD}	Satellite Sensor Current Signal Slew Rate	16	-	48	mA/µs	
$t_{SAT\_SYNC\_FR}$	Sync Pulse Rising and Falling Time	3.0	4.0	6.0	µs	
$t_{SAT\_IQ\_FLT}$	Satellite Quiescent Current Sampling Filter Time Constant	-	60	-	µs	
$t_{SAT\_IQ\_DET}$	Satellite Quiescent Current Out of Range Detection Time	$3/f_{CLK}$	-	$4/f_{CLK}$	µs	
$t_{SAT\_OC\_DET}$	Satellite Current Overcurrent Detection Time	-	512	-	µs	
$t_{SAT\_OC\_SDDEL}$	Satellite Interface Overcurrent Shutdown Delay $t_{SATSYNC\_PER}$ = 500 µs, $t_{SAT\_OC\_DET}$ = 512 µs	3.5	-	4.0	ms	
$t_{SAT\_TH\_DEL\_\Delta}$	Satellite Data Detection Delay Difference Between Rising Edge and Falling Edge	-	-	250	ns	
$t_{SAT\_IQ\_INIT\_DEL}$	Initial Satellite Quiescent Current Measurement Delay	-	10	-	ms	
$t_{SAT\_IQ\_INIT\_DUR}$	Initial Satellite Quiescent Current Measurement Duration	-	35	-	ms	

Notes

15. V_{SUP} is applied on the VPWR pin as a test condition.
16. The switching frequency used for the Boost and Buck supplies is selectable via the SPI with a LIN_CONFIG command at either a low-speed or high-speed switching mode.

Table 6. Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions 7.0 V ≤ V_{SUP}[15] ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
SATELLITE SENSOR INTERFACE PSI5 (CONTINUED)						
$t_{SAT\_IQ\_DEL}$	Satellite Quiescent Current Measurement Delay	-	5.0	-	µs	
$t_{SAT\_IQ\_DUR}$	Satellite Quiescent Current Measurement Duration	-	3.0	-	µs	
$t_{SAT\_IQ\_DEL\_NA}$	Satellite Quiescent Current Measurement Delay with No Bus Activity	-	120	-	µs	
SYNC PULSE LIMITS FOR SYNCHRONOUS TDM MODE (SEE Figure 5. Synchronous TDM Mode Sync Pulse Timing)						
t_0	Reference Time Base	-	0.0	-	µs	
t_1	Sync Signal Earliest Start	-	-3.0	-	µs	
t_2	Sync Signal Sustain Start	0	7.0	-	µs	
-	Sync Rising Slope Slew Rate	0.43	-	1.5	V/µs	
-	Sync Falling Slope Slew Rate	-1.5	-	-	V/µs	
t_3	Sync Signal Sustain Time	-	16	-	µs	
t_4	Sync Discharge Time Limit	-	35	-	µs	
t_{SLOT1_START}	Start of First Sensor Data Word (Remaining discharge current < 2.0 mA)	44	-	-	µs	
SATELLITE TIMING LIMITS FOR SYNCHRONOUS TDM MODE (SEE Figure 6. Synchronous TDM Mode Satellite Interface Timing)						
t_{SYNC}	Sync Pulse Period	495	500	505	µs	
$t_{SATSYNC\_WIDTH}$	Satsync Input Pulse Width	40	-	-	µs	
t_{SLOT1_START}	Slot1 Start Time (relative to t_0)	-	44	-	µs	
t_{SLOT2_START}	Slot2Start Time (relative to t_0)	-	181.3	-	µs	
t_{SLOT3_START}	Slot3 Start Time (relative to t_0)	-	328.9	-	µs	
t_{SLOT3_END}	Slot3 End Time (relative to t_0)	-	492	-	µs	
t_{EMC}	Timing Variation Margin	-2.1	-	2.1	µs	
SATELLITE TIMING LIMITS FOR SYNCHRONOUS SATSYNC-STEERED MODE (SEE Figure 7. Synchronous Satsync-Steered Mode Satellite Interface Timing)						
t_{SAT_ACT}	PSI5_x Activation Time from Rising Edge of Chip Select (1)	1.0	-	10	µs	
$t_{SATSYNC\_PER}$	Satsync Period (2)	167	-	∞	µs	
$t_{SATSYNC\_PH1}$	Satsync Phase 1 Time (3)	-	200	-	µs	
$t_{SATSYNC\_PH0}$	Satsync Phase 0 Time (4)	-	170	-	µs	
$t_{SATSYNC\_S\_DEL}$	Satsync Sampling Delay Time (5) (1/ F_{SAT_CLK} to 3/ F_{SAT_CLK})	250	-	750	ns	
$t_{SAT\_SYNC\_WIDTH}$	Sync Pulse Width (6)	-	32	34	µs	
$t_{SAT\_STAGGER}$	Channel Stagger Time (7) (16/ F_{SAT_CLK})	-	4.0	-	µs	
$t_{SAT\_SYNC\_GEN\_DEL}$	SYNC Pulse Generation Delay (8)	-	-	2.5	µs	
$t_{SAT\_SYNC\_BLANK}$	Sync Blanking Time (Decoder disabled) (9)	-	69	-	µs	
$t_{SAT\_PHASE\_BLANK}$	Phase Transition Blanking Time (Manchester Decoder disabled) (10)	-	10	-	µs	
t_{SAT_MSG}	Message Time (11)	81.48	-	156.5	µs	

Table 6. Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions 7.0 V ≤ V_{SUP}[15] ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
DC SENSOR INTERFACE AND ANALOG OUTPUT						
t_{MEAS}	DC Sensor Measurement Duration	0.5	-	2.0	ms	
t_{DCREG_SET}	Supply Regulator Setting Time V_{INx} = 90% x V4 = 90% x 6.5 V, I_{Inx} = 20 mA, C_{Inx} = 10 nF	-	-	70	µs	
$\|dV_{Inx}/dt\|$	Regulator Output Switch Slew Rate	0.08	5.0	7.0	V/µs	
t_{AOUT_SETL}	Analog Output Settling Time C_L = 0.22 nF, R_L = 1.0 MΩ A_{OUT} = 90% final value A_{OUT} = 99% final value	 - -	 - -	 40 70	µs	
CONFIGURABLE DRIVERS						
$\|dV_{OUTx}/dt\|$	Driver Output Switching Slew Rate Control 6.0 V < V_{OUTx} <18 V, R_{LOAD} = 273 Ω, C_{LOAD} = 100 nF	135	190	210	mV/µs	
t_{LATCH_DELAY}	Delay for Comparator Latch (992/F_{CLK})	-	248	-	µs	
SPI AND SPI MONITOR INTERFACE (SEE Figure 8. SPI TIMING, WITH AN EXTERNAL PULL-UP OF 47 kΩ OR 110 MA ON DO)						
f_{SCK}	SCK Frequency	-	-	8.08	MHz	
t_{SCK_H}	SCK High Time (A)	1/2 t_{SCK} - 13	-	-	ns	
t_{SCK_L}	SCK High Time (B)	1/2 t_{SCK} - 13	-	-	ns	
t_{SCK}	SCK Period (C)	123.7	-	-	ns	
t_{FALL}	SCK Falling Time (D)	5.5	-	13	ns	
t_{RISE}	SCK Rising Time (E)	5.5	-	13	ns	
t_{SET}	SI Setup Time (F)	37	-	-	ns	
t_{HOLD}	SI Hold Time (G)	49	-	-	ns	
t_{ACC}	SO Access Time (H)	-	-	43	ns	
t_{VALID}	SO Valid Time after SCK (I)	-	-	30	ns	
t_{LAG}	SO Lag Time (J)	0.0	-	-	ns	
$t_{DISABLE}$	SO Disable Time (K)	-	-	750	ns	
$t_{\overline{CS}\_LEAD}$	$\overline{CS}$ Lead Time (L)	1/2 t_{SCK}	-	-	ns	
$t_{\overline{CS}\_LAG}$	$\overline{CS}$ Lag Time (M)	1/2 t_{SCK}	-	-	ns	
t_{TD}	Sequential Data Transfer Delay (N)	3/ F_{CLK}	-	-	µs	
ADDITIONAL COMMUNICATION LINE (ACL) INPUT FOR SCRAP						
t_{KEY_TOUT}	Scrap KEY Timeout	-	-	600	µs	
t_{ACL}	ACL Period	180	200	220	ms	
t_{ACL_H}	ACL Pulse High Time	126	140	154	ms	
t_{ACL_L}	ACL Pulse Low Time	54	60	66	ms	

Table 6. Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions 7.0 V ≤ V_{SUP}[15] ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
LIN PHYSICAL LAYER: DRIVER CHARACTERISTICS FOR NORMAL SLEW RATE - 20.0 KBIT/SEC ACCORDING TO THE LIN PHYSICAL LAYER SPECIFICATION[17], [18]						
D1	Duty Cycle 1: $TH_{REC(MAX)}$ = 0.744 * V_{SUP} $TH_{DOM(MAX)}$ = 0.581 * V_{SUP} D1 = $t_{BUS\_REC(MIN)}$/(2 x t_{BIT}), t_{BIT} = 50 µs, 7.0 V ≤ V_{SUP} ≤ 18 V	39.6	—	—	%	
D2	Duty Cycle 2: $TH_{REC(MIN)}$ = 0.422 * V_{SUP} $TH_{DOM(MIN)}$ = 0.284 * V_{SUP} D2 = $t_{BUS\_REC(MAX)}$/(2 x t_{BIT}), t_{BIT} = 50 µs, 7.6 V ≤ V_{SUP} ≤ 18 V	—	—	58.1	%	
LIN PHYSICAL LAYER: DRIVER CHARACTERISTICS FOR SLOW SLEW RATE - 10.4 KBIT/SEC ACCORDING TO LIN PHYSICAL LAYER SPECIFICATION[17], [19]						
D3	Duty Cycle 3: $TH_{REC(MAX)}$ = 0.778 * V_{SUP} $TH_{DOM(MAX)}$ = 0.616 * V_{SUP} D3 = $t_{BUS\_REC(MIN)}$/(2 x t_{BIT}), t_{BIT} = 96 µs, 7.0 V ≤ V_{SUP} ≤ 18 V	41.7	—	—	%	
D4	Duty Cycle 4: $TH_{REC(MIN)}$ = 0.389 * V_{SUP} $TH_{DOM(MIN)}$ = 0.251 * V_{SUP} D4 = $t_{BUS\_REC(MAX)}$/(2 x t_{BIT}), t_{BIT} = 96 µs, 7.6 V ≤ V_{SUP} ≤ 18 V	—	—	59	%	
LIN PHYSICAL LAYER: RECEIVER CHARACTERISTICS [20]						
t_{REC_PD} t_{REC_SYM}	Propagation Delay and Symmetry Propagation Delay of Receiver, t_{REC_PD} = MAX (t_{REC_PDR}, t_{REC_PDF}) Symmetry of Receiver Propagation Delay, t_{REC_PDF} - t_{REC_PDR}	— -2.0	— —	6.0 2.0	µs	[21]
TXD TIMING						
t_{TXDDOM}	TXD Permanent Dominant State Delay	3.75	5.0	6.25	ms	[22]
t_{LIN_1STDOM}	First Dominant bit Delay The transmitter delay before sending the first dominant bit, after the transceiver is activated	—	50	80	µs	[23]

Notes

17. Bus load R_{BUS} and C_{BUS} 1.0 nF / 1.0 kΩ, 6.8 nF / 660 Ω, 10 nF / 500 Ω. Measurement thresholds: 50% of TXD signal to LIN signal threshold defined at each parameter. See Figure 9. In Figure 9, use VSUP to represent the VPWR pin, and use GND to represent both the GND and GND_LIN VLIN pins, in order to be consistent with LIN Protocol Specification, and other Freescale LIN product specifications.
18. See Figure 10.
19. See Figure 11.
20. V_{SUP} from 7.0 to 18 V, bus load R_{BUS} and C_{BUS} 1.0 nF / 1.0 kΩ, 6.8 nF / 660 Ω, 10 nF / 500 Ω. Measurement thresholds: 50% of TXD signal to LIN signal threshold defined at each parameter. See Figure 9.
21. See Figure 12.
22. The LIN is in Recessive state and the receiver is still active.
23. The First Dominant bit delay normally has no impact to LIN communication, but may need additional care on the software for ISO 9141 (K-line) communication initialization.

TIMING DIAGRAMS

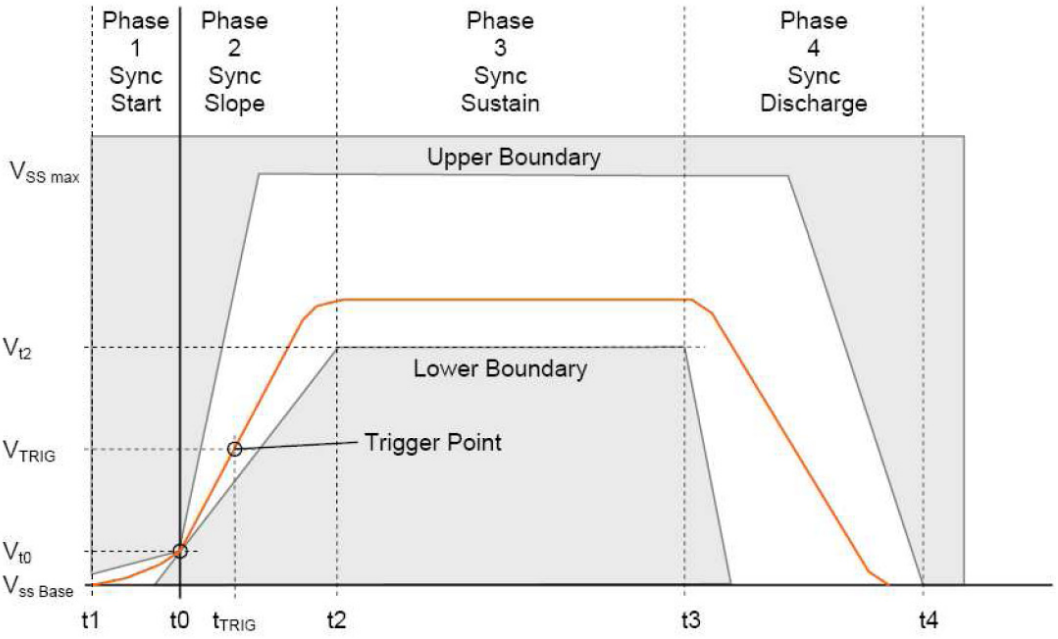


Figure 5. Synchronous TDM Mode Sync Pulse Timing

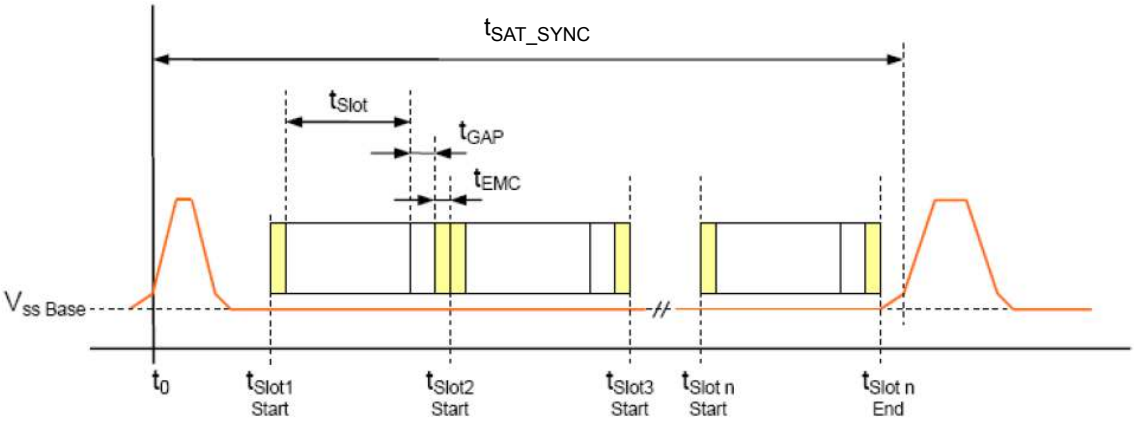


Figure 6. Synchronous TDM Mode Satellite Interface Timing

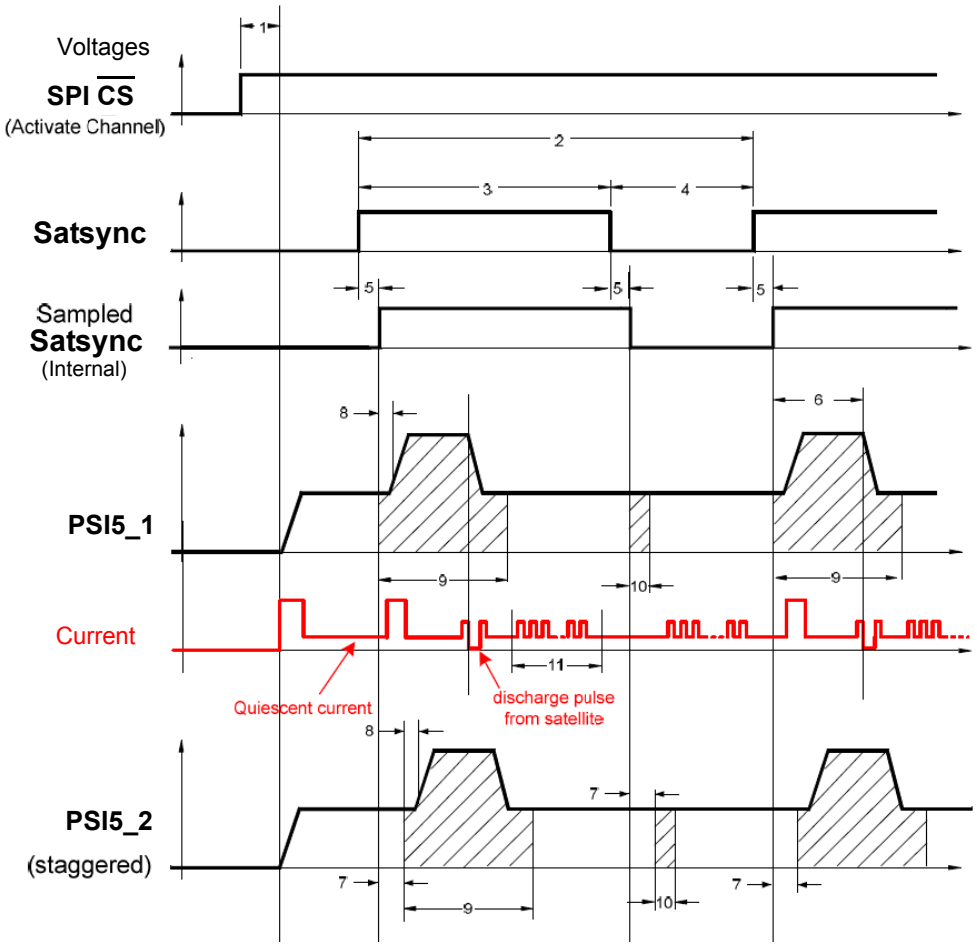


Figure 7. Synchronous Satsync-Steered Mode Satellite Interface Timing

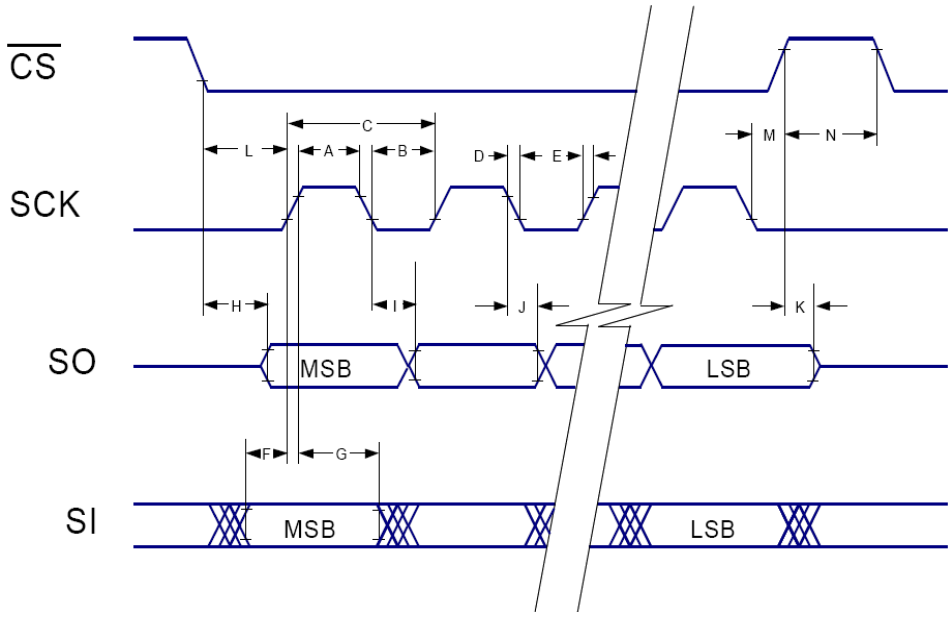
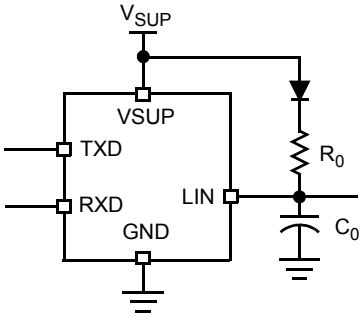


Figure 8. SPI Timing



Note R_0 and C_0: 1.0 kΩ/1.0 nF, 660 Ω/6.8 nF, and 500 Ω/10 nF.

Figure 9. Test Circuit for Timing Measurements

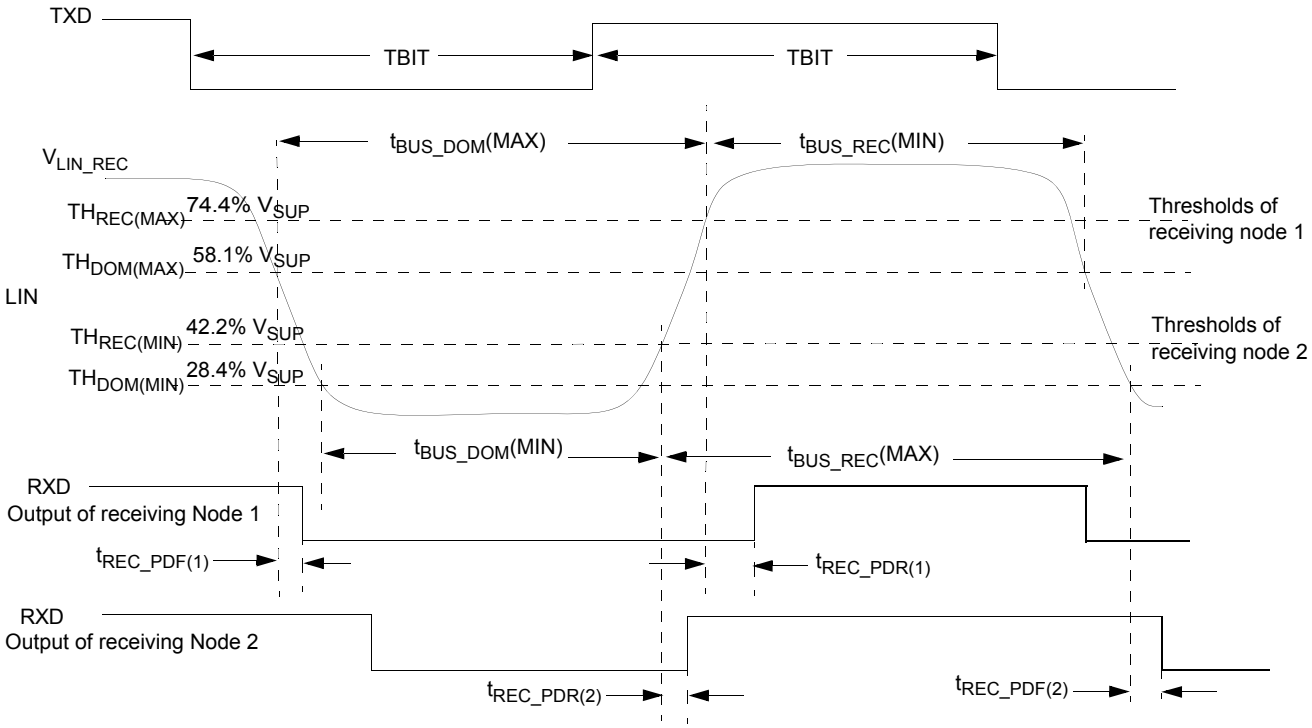


Figure 10. LIN Timing Measurements for Normal Baud Rate

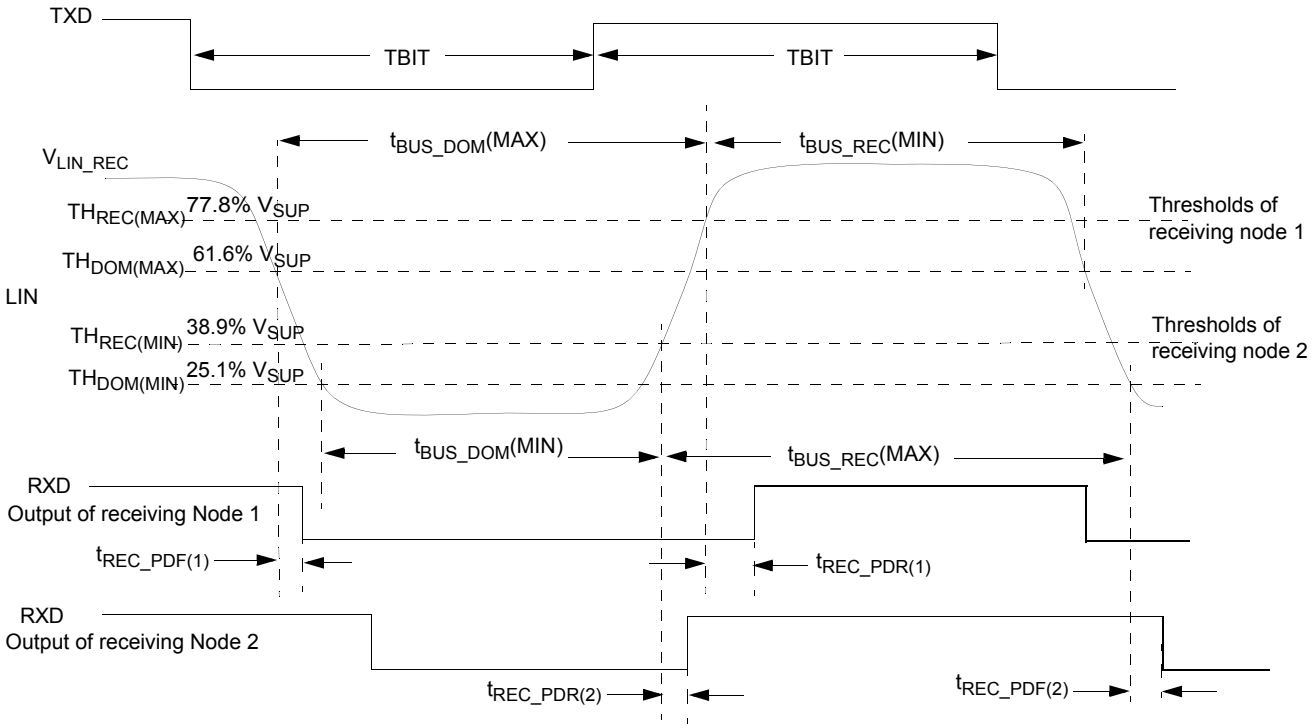


Figure 11. LIN Timing Measurements for Slow Baud Rate

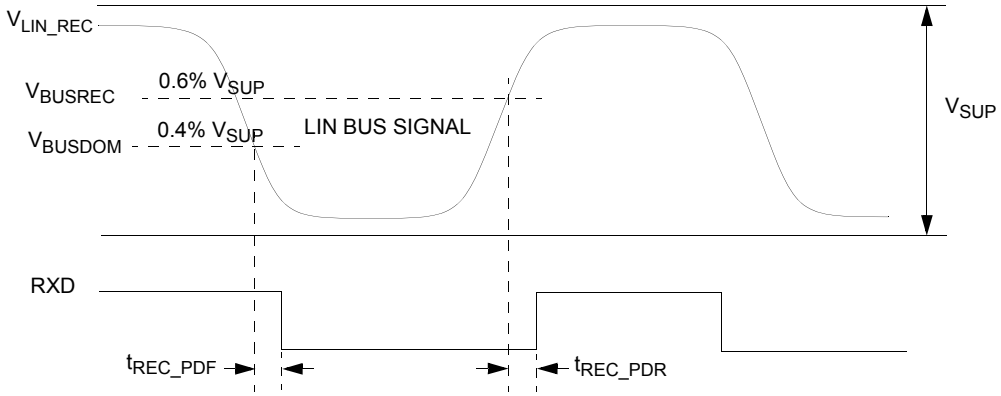


Figure 12. LIN Receiver Timing

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 33789 provides an integrated solution for multiple basic functions in an air bag control module.

As a system basis chip, the 33789 supplies different voltages to a complete airbag system with centralized power management. It controls the wake-up and power down of the system through the Power Mode Control function. It runs the Watchdog State Machine to respond to the MCU refresh and controls all of internal and external resets. It operates in Safing mode to prevent inadvertent deployment of the airbags, and thereby secure the occupants safety. It also operates in Scrap mode, to allow for the disposal of the unused pyrotechnic devices (squibs) at the end of vehicle life. For different voltage applications, it uses internal switches to boost battery voltage up to 33 V to supply external squib drivers and to charge the energy reserve. It then combines internal buck switches and the charge pump to create bus and sync supplies for satellite sensors, and uses an external bipolar transistor to supply V_{CC} for all on-board IC cores.

Safing is another key function of the 33789. There are four SPI5 satellite sensor interfaces, nine DC sensor inputs, and one highly accurate analog input, equipped on the 33789 for the airbag system acquiring different types of safing data. The SPI Monitor in the safing block monitors on-board sensor data and satellite sensor data read by the MCU via the SPI. The on-chip safing logic compares all of the sensor data to the configurable thresholds, and thereby determines whether a safety event (collision) is happening. Whenever a collision is detected, an arm control will be created in which complementary ARM and $\overline{\text{DISARM}}$ logic outputs are activated.

The 33789 can output two PWM signals with high-side/low-side configurable drivers, which can be used to drive alert indicators. The 33789 outputs a multiplexed analog signal to the MCU for diagnostics on all DC sensors, power supplies, and configurable driver outputs.

A LIN / ISO-9141 physical layer interface can be used to communicate with either LIN based Occupant Classification Systems or vehicle diagnostics. Its communication mode can be selected by the MCU through the SPI.

FUNCTIONAL PIN DESCRIPTION

POWER SUPPLY INPUT (VPWR)

VPWR is the system power supply input. It takes a protected 12 V vehicle battery input, which should be protected for load dump and reverse battery. Additional filtering is preferred for better EMC performance.

WAKE-UP INPUT (WAKE)

WAKE is a battery voltage, active high logic input. When activated, it brings the system out of sleep mode by starting the boost and buck converters.

Internally, the WAKE input is implemented with a 200 kΩ pull-down resistance and a 1.0 ms glitch filter.

BOOST SWITCH OUTPUT (BSTSW)

BSTSW is an internal low-side switch output. When the switch is turned on, its voltage will be pulled down close to GND (V_{BSTGND}), thus increasing the current in the boost inductor. When the switch is turned off, the un-interrupted current will charge the boost capacitor.

BOOST SUPPLY INPUT (VBST)

The VBST pin is externally connected to the boost capacitor. It inputs V_{BST} as a regulated higher voltage supply, and distributes it internally for all sub-system applications.

BOOST COMPENSATION CONNECTION (BSTCOMPX)

The two boost compensation pins are used for connecting an external RC filter in the boost converter feedback loop.

ENERGY RESERVE SWITCH OUTPUT (ERSW)

ERSW is an energy reserve control output. It is connected to a charge/discharge switch pair. When the energy reserve voltage across the energy reserve capacitor C_{ER} is lower than the target value, the internal charge switch will be turned on to provide source current from the boost supply to charge C_{ER}. A short discharge pulse can be used for measuring C_{ER} capacitance and ESR.

ENERGY RESERVE MONITOR (VER)

VER is a voltage input for the system, to monitor the voltage across C_{ER}, to maintain enough energy storage.

ENERGY RESERVE DIAGNOSTIC INPUT (VERDIAG)

VER and VERDIAG both monitor the voltage across C_{ER}. However, VERDIAG only takes AC samples coupled by an external capacitor. The VERDIAG sample will be processed with 10-bit ADC and sent to the MCU for C_{ER} diagnostics.

BUCK SWITCH OUTPUT (BUCKSW)

BUCKSW is a synchronous half-bridge switch output for the buck converter, to create V_{BUCK} on C_{BUCK}. When V_{BUCK} is below the target threshold, the high-side switch is turned on to charge C_{BUCK}, sourcing current from the internal V_{BST} connection. Once V_{BUCK} has reached the threshold, the high-side switch is turned off and the low-side driver is turned on for the current circulation.

BUCK SUPPLY INPUT (VBUCK, VBUCK_R)

The 33789 uses two pins to input V_{BUCK}. VBUCK provides supply source for the Sync charge pump and other internal applications, while VBUCK_R shares all applications except Sync.

BUCK COMPENSATION CONNECTION (BUCKCOMPX)

The two buck compensation pins are used for connecting an external RC filter in the buck converter feedback loop.

CHARGE PUMP CAPACITOR CONNECTION (CPCX)

A charge pump capacitor is connected between CPC1 and CPC2.

SYNC SUPPLY CONNECTION (VSYNC)

The internal charge pump outputs current to charge C_{SYNC}, which is externally connected on this pin, to achieve V_{SYNC}. The satellite sensor interface block sources V_{SYNC} to create sync pulse internally.

DEDICATED GROUND CONNECTIONS FOR SWITCHING POWER SUPPLIES (BSTGND, BUCKGND, CPGND)

There are three dedicated ground connection pins designed for the boost converter, buck converter, and charge pump ground returns respectively, to shorten their own current loops for the best EMC performance. Eventually, all of ground pins, including GNDA, VSS, GND_LIN, and GND_PSI, must be connected together and terminated on the circuit board ground.

ANALOG GROUND (GNDA)

The ground return terminal or ground source pin for analog circuits.

DIGITAL GROUND (VSS)

The ground return terminal or ground source pin for logic circuits.

5.0 V V_{CC} TRANSISTOR BASE DRIVER OUTPUT (VCCDRI)

The VCCDRI pin is an internal driver output to control the base pin of an external PNP transistor to regulate 5.0 V V_{CC}.

5.0 V V_{CC} INPUT (VCC)

The VCC pin is used to input 5.0 V V_{CC}, which supplies the internal analog circuit and provides feedback for the linear regulator.

2.5 V V_{DD} CONNECTION (VDD)

2.5 V V_{DD} is converted from VPWR and VBUCK, to supply internal logic circuits. The VDD pin is the connection point between the internal VDD regulator driver and its external load capacitor.

RESET ($\overline{\text{RESET}}$)

The $\overline{\text{RESET}}$ pin is the reset driver output to issue global resets to other system ICs.

PRODUCTION PROGRAMMING AND TEST (PPT)

The PPT pin is an active high enable input. It will be only used by manufacturers to program and test the circuit during production. It should not be connected to any application circuit externally. The PPT pin should be grounded to secure airbag system operation.

LIN INTERFACE (LIN)

The LIN pin is a LIN 2.1 compatible physical layer interface to communicate with devices or diagnostic systems external to the airbag ECU.

LIN GROUND (GND_LIN)

The dedicated ground for LIN (or K-line) interface.

UART CONNECTION (TXD, RXD)

The 33789 uses TXD and RXD ports to receive and transmit 5.0 V logic level LIN bus data through the MCU UART interface.

DC SENSOR INPUTS (INX)

There are nine switch mode analog inputs, IN1 through IN9, on the 33789 to monitor the switch mode sensor status of up to 9 independent DC type sensors. The sensors can be Hall-effect sensors, resistive sensors, on/off switches, or any other regular analog sensors. The 33789 supplies one of four selectable bias voltages for each channel, multiplexes the sensor inputs, and outputs them in serial to the MCU through the AOUT pin.

ANALOG DIAGNOSTIC OUTPUT (AOUT)

The AOUT pin outputs multiple scanned, rescaled, and buffered analog signals to the MCU. With the AOUT signal, the MCU can read DC sensor status, and conduct diagnostics on DC sensors, configurable driver outputs, and all power supplies.

CONFIGURABLE DRIVER OUTPUTS (OUTX_D, OUTX_S)

The 33789 provides two general purpose low current drivers. Each one can be independently configured as either a high-side or a low-side driver by a SPI command. Both the drain and the source terminals of each driver have dedicated pins for external connections.

SATELLITE SENSOR INTERFACES (PSI5_X)

The four satellite sensor interface pins, PSI5_1 through PSI5_4, provide four PSI5 V 1.3 physical connections. All four channels can be enabled or disabled via SPI commands. Each channel can be used to connect up to three satellite sensors in PSI5-P10P-500/3L Synchronous TDM mode, or up to two satellite sensors in Synchronous Satsync-steered mode. The MCU can retrieve the current-modulated sensor data and query the channel status via the SPI.

SYNC-PULSE ACTIVATION SIGNAL INPUT (SATSYNC)

The MCU provides a periodic Satsync signal to the 33789 at the SATSYNC pin to activate higher voltage sync pulse generation, The 33789 adds the sync pulses on each satellite channel in sequence, to synchronize the satellite data sampling.

SATELLITE SENSOR INTERFACE CLOCK INPUT (CLK)

The PSI5 interface block receives a 4.0 MHz clock input from the MCU at the CLK pin, and uses it for satellite sensor signal decoding and synchronizing other internal logic processing.

SATELLITE GROUND (GND_PSI)

GND_PSI is a dedicated common ground connection point for all PSI5 satellite sensor channels.

SERIAL PERIPHERAL INTERFACE (SPI) DATA INPUT (SI)

Since the 33789 is configured as a slave device connected on the Master Out Slave In (SI) line of SPI bus, the SI pin is implemented as an SPI data serial input pin.

SPI DATA OUTPUT (SO)

SO is a Slave Data Output pin for the 33789 to send serial data out via the SPI bus.

SPI CLOCK (SCK)

The 33789 uses the SCK pin to receive the SPI clock signal from the MCU. The SPI clock is used to synchronize the data transaction and the logic processing at the SPI interface block.

SPI CHIP SELECTS ($\overline{CS}$)

The MCU selects to communicate with the 33789 by pulling $\overline{CS}$ pin to ground. Once the data transaction is completed, the voltage level on the $\overline{CS}$ pin will return high.

CHIP SELECTS FOR SPI MONITOR ($\overline{CS\_X}$)

When the MCU sends a “sensor request” over the SPI interface, the 33789 SPI Monitor listens to the sensor response and extracts valid sensor data from up to four sources using additional chip select signals on $\overline{CS}\_x$:

- $\overline{CS}$: dedicated for satellite sensors
- $\overline{CS\_A}$: Intended for an on-board accelerometer
- $\overline{CS\_B}$: Intended for an on-board accelerometer or an expansion satellite receiver
- $\overline{CS\_C}$: Intended for an expansion satellite receiver

ANALOG SENSOR INPUT (A_SENSOR)

There is one analog safing sensor input on the 33789. The analog signal input from the A_SENSOR pin is processed by a 10-bit ADC and digital filters. The 10-bit sensor data result will be stored in a holding register for the SPI reading.

ANALOG SENSOR SELF-TEST (ASST)

The MCU can run a self-test on the on-board analog sensor without triggering Arming. The MCU would need to issue a disable signal to the safing block to ignore the analog sensor data during its self-test period. The ASST pin on the 33789 is the digital input to receive this disable signal. Once the ASST pin is pulled high by the MCU, the internal digit filter will not process the analog sensor data, and the analog sensor register will not be loaded for comparison.

ARM OUTPUT (ARM, $\overline{DISARM}$)

The 33789 uses a pair of digit output pins, ARM and $\overline{DISARM}$, with opposite logic, for the Arming output. They can be directly used by squib drivers as a squib firing enable and/or disable inputs.

Both the ARM and $\overline{DISARM}$ pins are set to high-impedance under the following conditions:

- During resets
- Arm Lockout
- While the Safing State Machine is in Start-up mode

SCRAP CONTROL (SCRAP)

The SCRAP pin on the 33789, is also called ACL input, for an Additional Communication Line, per the ISO-26021 standard. It is a digital signal input to receive the ACL signal from either the MCU or an external device. The ACL signal will be used by the 33789 to determine if it should stay in, or enter into Scrap mode from Arming mode during its scrap handshaking with the MCU.

FUNCTIONAL INTERNAL BLOCK DESCRIPTION

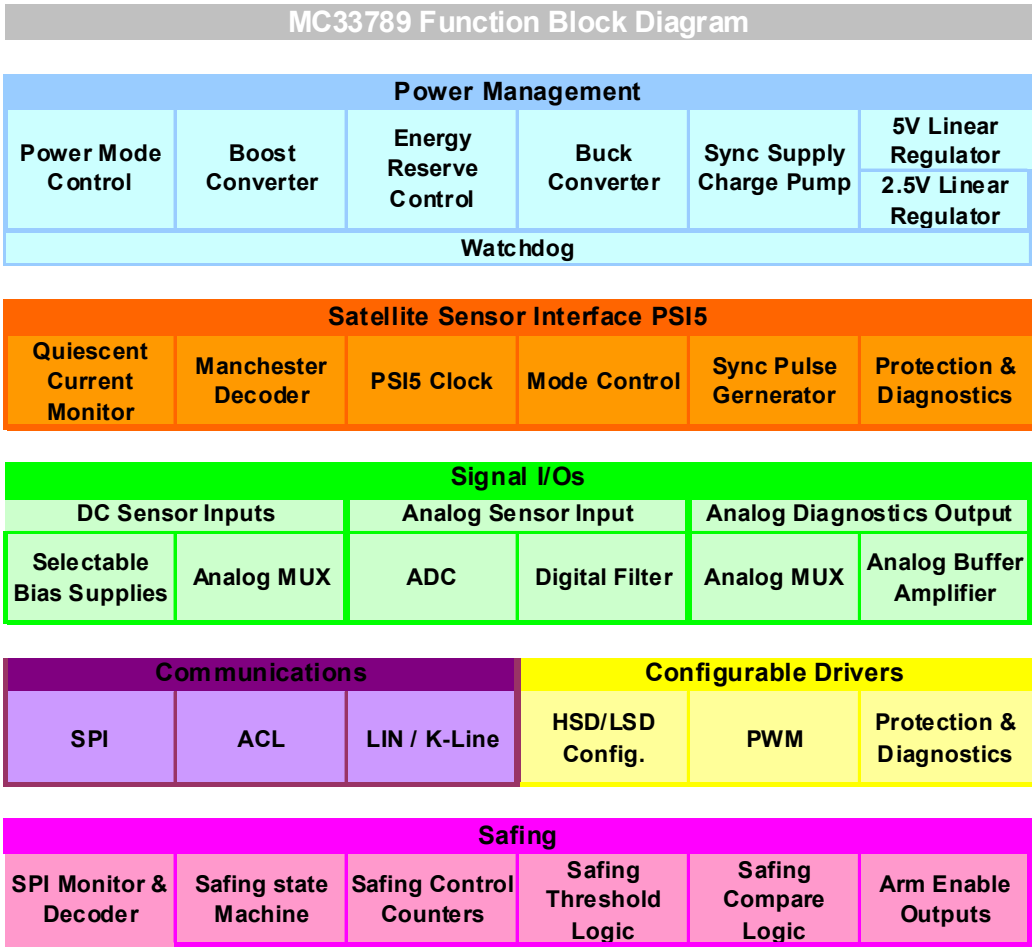


Figure 13. Functional Blocks

BOOST CONVERTER

The boost converter uses an internal power switch combined with external passive components, to create a 33 V boost supply from the 12 V battery input. The 33 V boost output is used for:

- Charging energy reserve capacitor
- Firing squibs when a safing is detected and the battery input is still available
- Power source for all other lower voltage supplies

The boost switch is activated by a wake-up signal, and its operation is controlled by the MCU through the SPI command.

ENERGY RESERVE CONTROL

The energy reserve is a power backup for the air bag system. When a vehicle accident happens and the battery supply is lost, the energy reserve can provide sufficient power to support the system to continuously collect sensor information, process safing messages, and fire squibs, for a time determined by the capacity of the energy reserve.

To secure the energy reserve function, the 33789 has implemented sophisticated controls:

- Monitoring V_{BST} and V_{ER} to determining when the energy reserve capacitor C_{ER} needs to be charged.
- Controlling the turn on time of the high-side charge switch, to keep V_{ER} close to V_{BST}, and limiting the inrush charge current.
- Executing a MCU command to diagnose C_{ER} by momentarily turning on the low-side discharge switch (while turning off the high-side charge switch), and accurately measuring the V_{ER} changes.

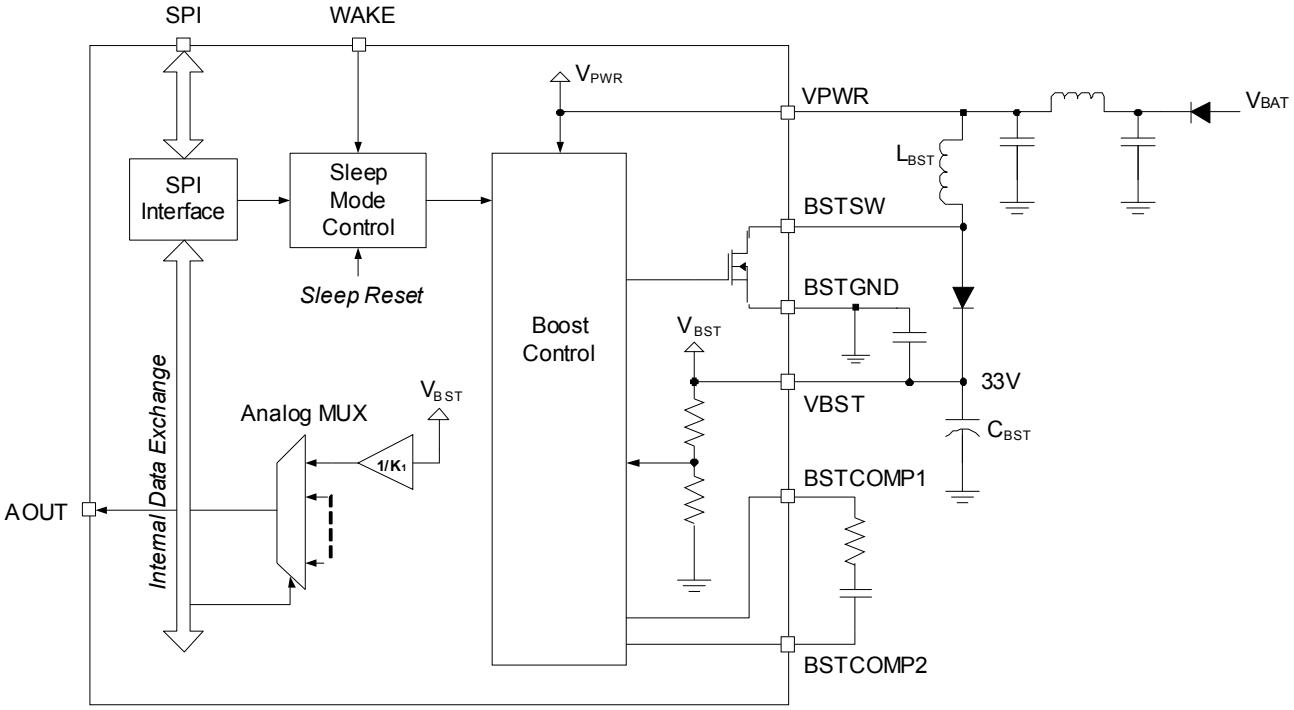


Figure 14. Boost Converter Block Diagram

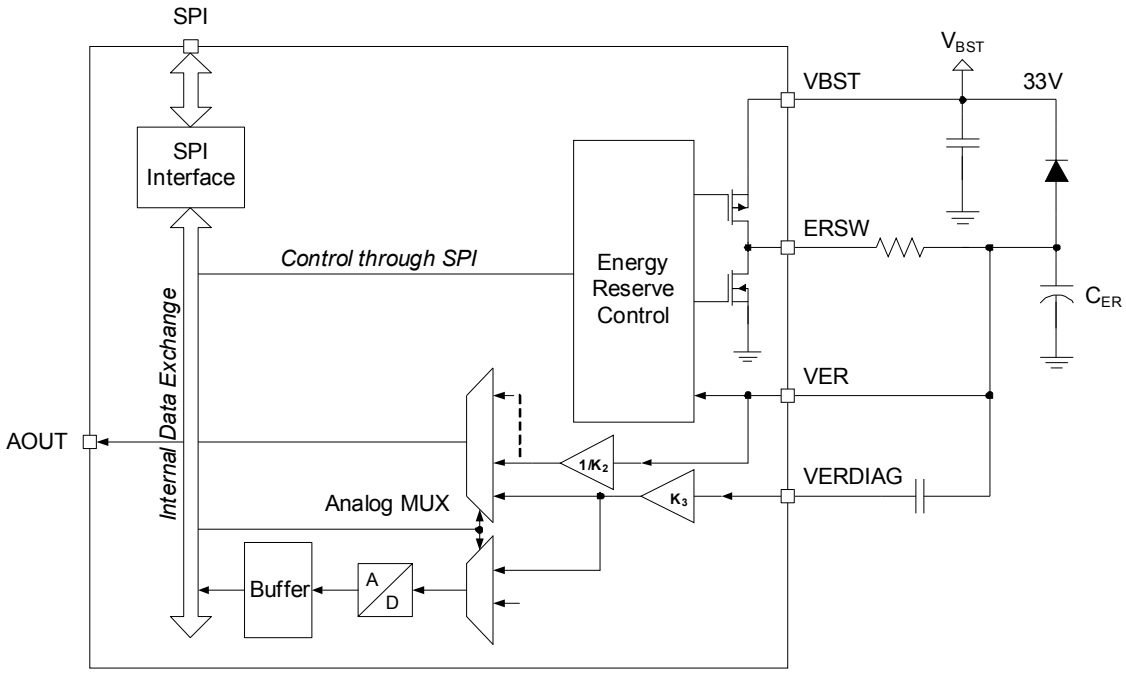


Figure 15. Energy Reserve Control Block Diagram

BUCK CONVERTER

The buck converter creates a step-down intermediate supply voltage, $V_{BUCK} \approx 9.0$ V, from the 33 V V_{BST}. It uses a synchronous buck structure, and controls the internal power switches running at 140 kHz, the same frequency as for the boost switch. The switches are fully protected against overvoltage, overcurrent and overtemperature.

The buck converter operation is under control of the power mode signal and SPI commands from the MCU. The buck converter status can be read via the SPI, and its output voltage, V_{BUCK}, can be monitored via AOUT by the MCU.

The 33789 provides redundant pins to input V_{BUCK} for the voltage regulation and further power conversions.

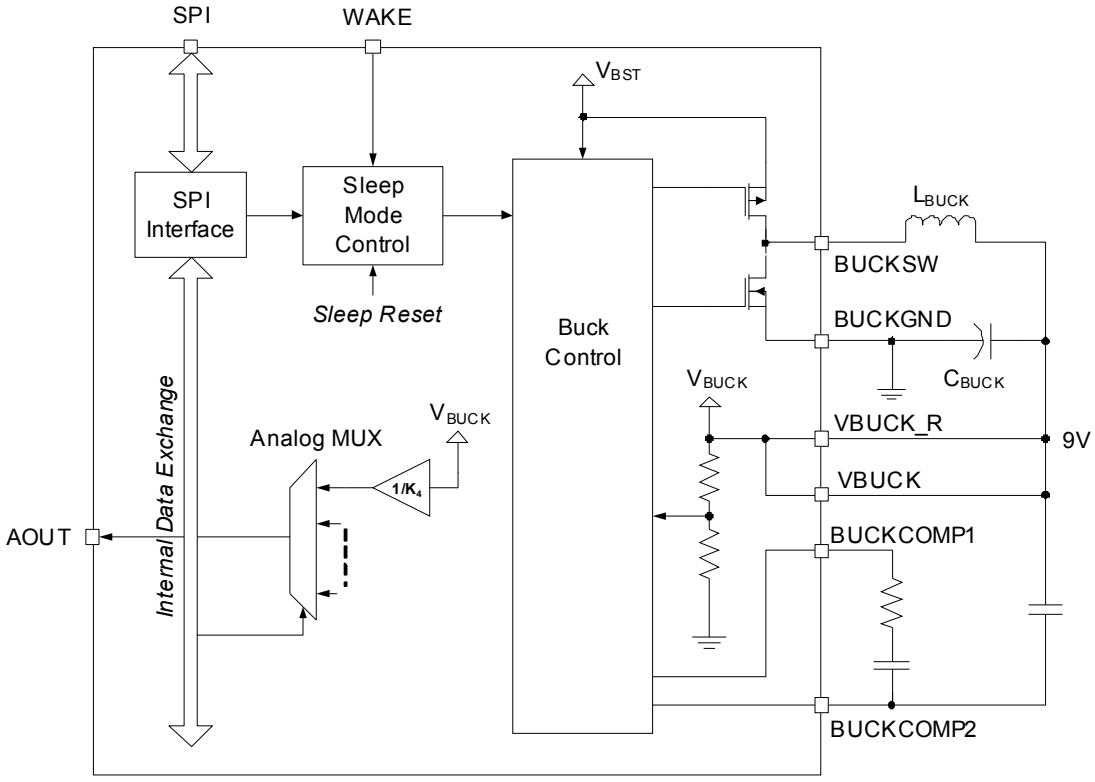


Figure 16. Buck Converter Block Diagram

SYNC SUPPLY FOR PSI5 INTERFACE

To create a regulated sync pulse supply with a voltage at least 5.0 V above the bus voltage for the PSI5 satellite sensor interface, the 33789 uses a charge pump to “double” V_{BUCK}. The charge pump switches are operated at 160 kHz, with output current limitation.

The MCU enables the sync supply and monitors V_{SYNC} via the AOUT for diagnostics.

LINEAR REGULATORS

The 33789 drives an external PNP transistor to provide a 5.0 V V_{CC} output. This design can reduce the IC power dissipation and offers the ECU designer system design flexibility.

As the prime core power supply, V_{CC} can be shared by the 33789 with other on-board ICs.

The 2.5 V V_{DD} used for the 33789 internal circuitry is created by an internal linear regulator, using V_{PWR} (for start-up) and V_{BUCK}. It utilizes an external capacitor through the VDD pin.

WATCHDOG AND $\overline{\text{RESET}}$

The Watchdog State Machine monitors the system clock by reading refresh messages from the MCU via the SPI, and applies state control and power mode control accordingly.

The MCU periodically sends watchdog refresh messages within the watchdog time window. If the refresh to the window watchdog has failed, a system reset will be issued. The $\overline{\text{RESET}}$ pin will be pulled low to drive external reset.

The reset control is also linked to the V_{CC} monitor and the V_{DD} monitor to ensure their output voltages are within the defined tolerances.

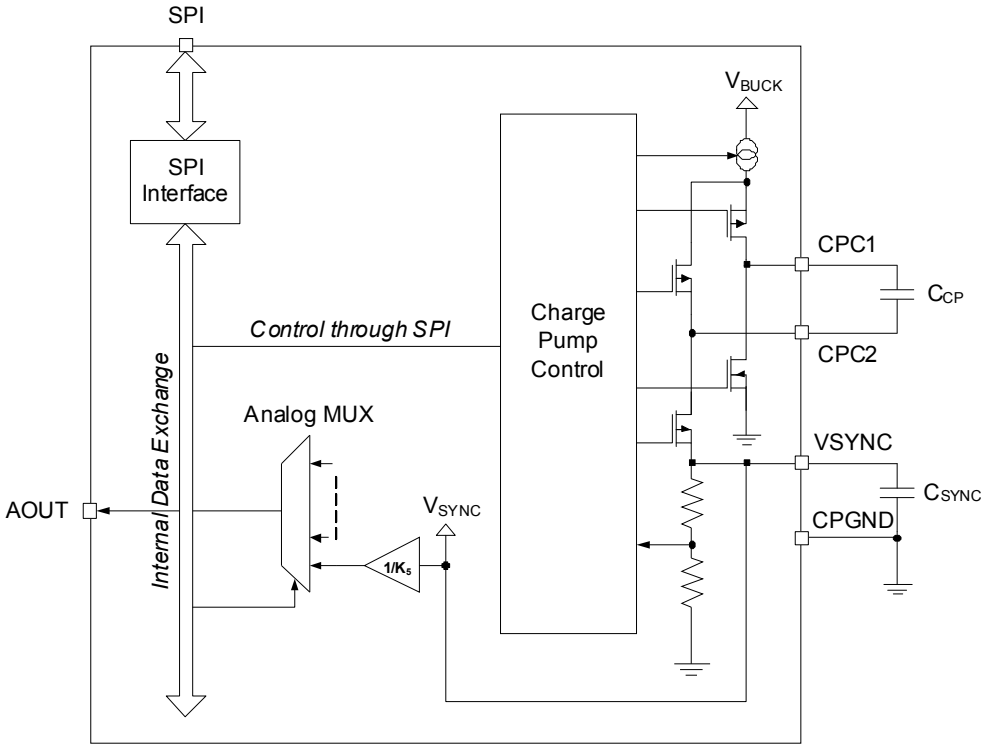


Figure 17. Sync Supply Block Diagram

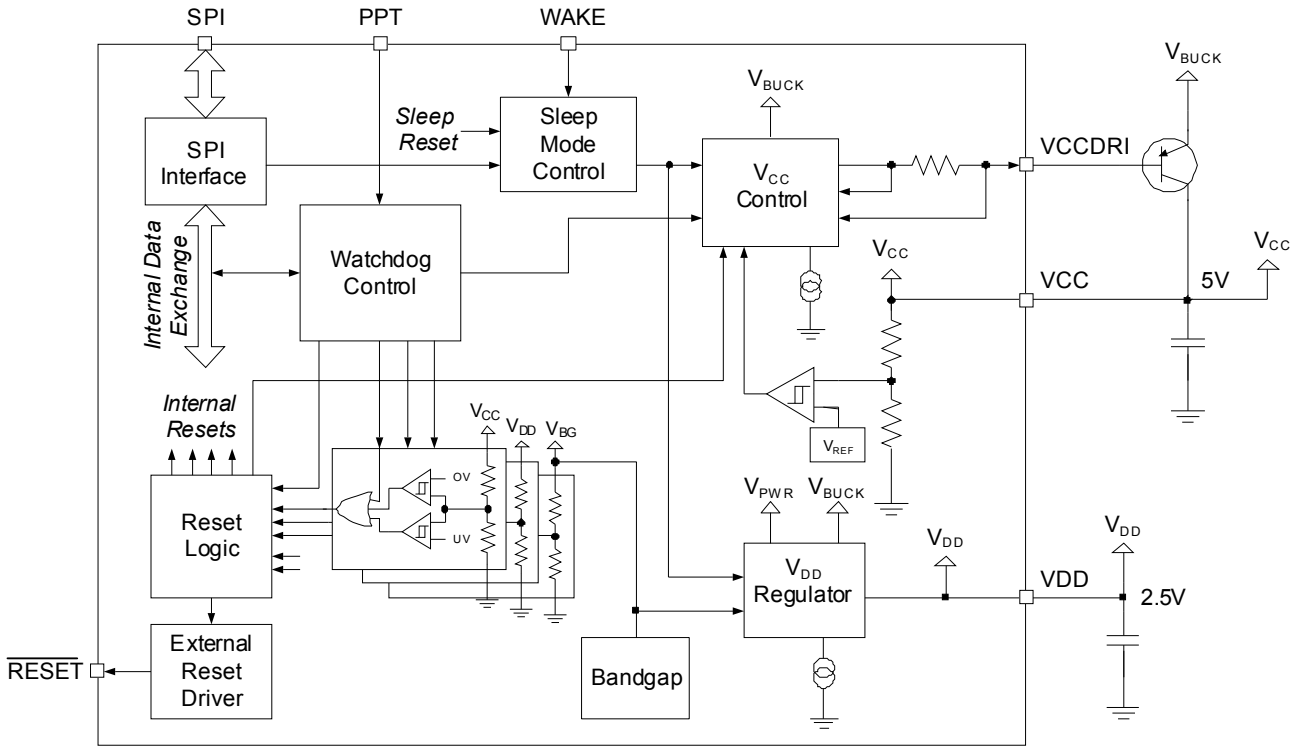


Figure 18. Linear Regulators and Watchdog Block Diagram

SATELLITE SENSOR INTERFACE PSI5

The 33789 provides four satellite sensor interface channels to collect data from up to 12 remote satellite sensors. The physical link is a two-wire pair.

The satellite sensor interface implements the P10P-500/3L mode, as defined in the PSI5 technical specification V1.3 protocol. It also supports 10-bit Synchronous Satsync-Steered mode operation. The interface receives data in synchronous mode only. In addition, a method is provided to allow implementation of the bi-directional communication feature, also defined in PSI5 V1.3, under software control.

All four satellite channels can be independently enabled or disabled via SPI commands. The selection of communication mode and the status acquisition are also controlled by the MCU via the SPI.

The physical layer of the PSI5 interface supplies continuous power and synchronization pulses, created from V_{BUCK} and V_{SYNC} respectively, to the remote satellite sensors. It senses the satellite current draw to receive the Manchester-encoded current modulation signals from the sensors. The interface converts the Satsync signal from the MCU to synchronize the sensor data transmission, and uses the CLK signal from the MCU as a time base for the Manchester decoding.

Each satellite channel has three registers to store decoded messages from up to three satellite sensors. The messages are accessible to the MCU over the SPI. Each channel's fault condition is isolated from the others. All four channels are independently protected from short to GND or battery.

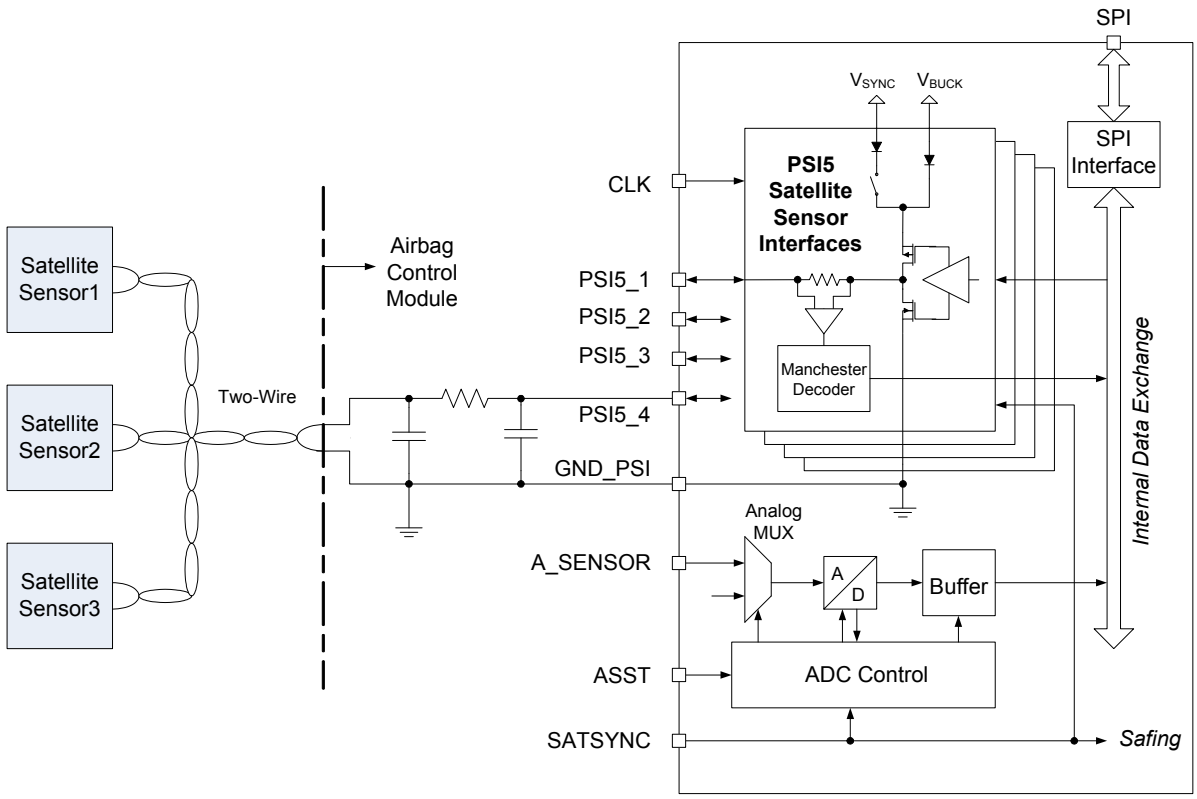


Figure 19. Satellite Sensor Interface and Analog Sensor Input Block Diagram

ANALOG SENSOR INPUT

There is one analog sensor input port provided on the 33789 for a sensitive analog safing sensor signal. The analog input shares a 10-bit A/D converter with the VERDIAG input. The periodic Satsync pulses trigger the A/D conversions.

The digital result of the analog sensor input is saved into a 10-bit analog sensor data register. It can then be read via the SPI and monitored by the safing logic in the same way as the satellite data from the PSI5 interface. The ASST input receives an inhibit signal from the MCU during the analog sensor self-test to stop the buffer register updating, thus avoid the Arming output triggered by an Analog Sensor Self Test fault condition.

DC SENSOR INTERFACE

The DC sensor interface provides 9 channels for Hall-effect sensors, resistive sensors or simple ON/OFF type switching sensors, such as seat belt buckles, seat track position sensors, etc. All nine inputs are multiplexed and buffered before they are output to the MCU through the AOUT pin. The multiplexer is controlled by SPI commands.

The DC sensor interface not only monitors the voltages at each input, but also provides a bias supply with four selectable regulated voltages for each sensor output stage. The supply regulator is capable of measuring and limiting the load current. If the load current exceeds the overcurrent detection threshold, the voltage regulator will enter into a protection mode and become a current source. During the transient period, the regulator output voltage will be increased to maintain the supply current near the current limit level, which is required by the load resistance in the Hall-effect sensor, to establish a sensing signal voltage. The DC sensor load current I_{INx} to the analog output voltage V_{AOUT} conversion curve for the AOUT monotonic operation can be found in Figure 21.

The DC sensor interface allows dual-point measurement that eliminates common-mode ground offset for implementation of sensors without a ground return to the ECU. The DC sensor interface system is capable of diagnosing whether a sensor switch is in a valid position, open circuit, short circuit to other channels, or other vehicle voltage potentials.

There is a low-current active pull-down circuit at each INx input, to discharge the residual voltage after the channel is deselected. The circuit stays activated as long as the DC sensor interface block is enabled and the channel is unselected until the channel is once again selected.

To prevent damage caused by external fault conditions, the interface local temperature is monitored with a safety feature of overtemperature shut down. The bias supply regulator configuration and the current limit functions are controlled by SPI commands, and the fault conditions including the overtemperature error, can be read via the SPI. An internal reset automatically deactivates the bias supply regulator and all of multiplexers and switches.

ANALOG OUTPUT FOR DC SENSOR MONITOR AND ANALOG DIAGNOSTICS

The AOUT pin is for SPI controlled multi-function analog output with an analog buffer amplifier. According to the SPI command, the instant AOUT voltage can be:

- One of the DC sensor inputs with selected bias supply voltage, or the sensor load current
- One of the system power supply voltages (rescaled), including the energy reserve diagnostic measurement
- One of the output pin voltages from the two configurable drivers

The AOUT signal provides a convenient access for the MCU to extract the DC sensor status and conduct diagnostics for all of above sub-systems.

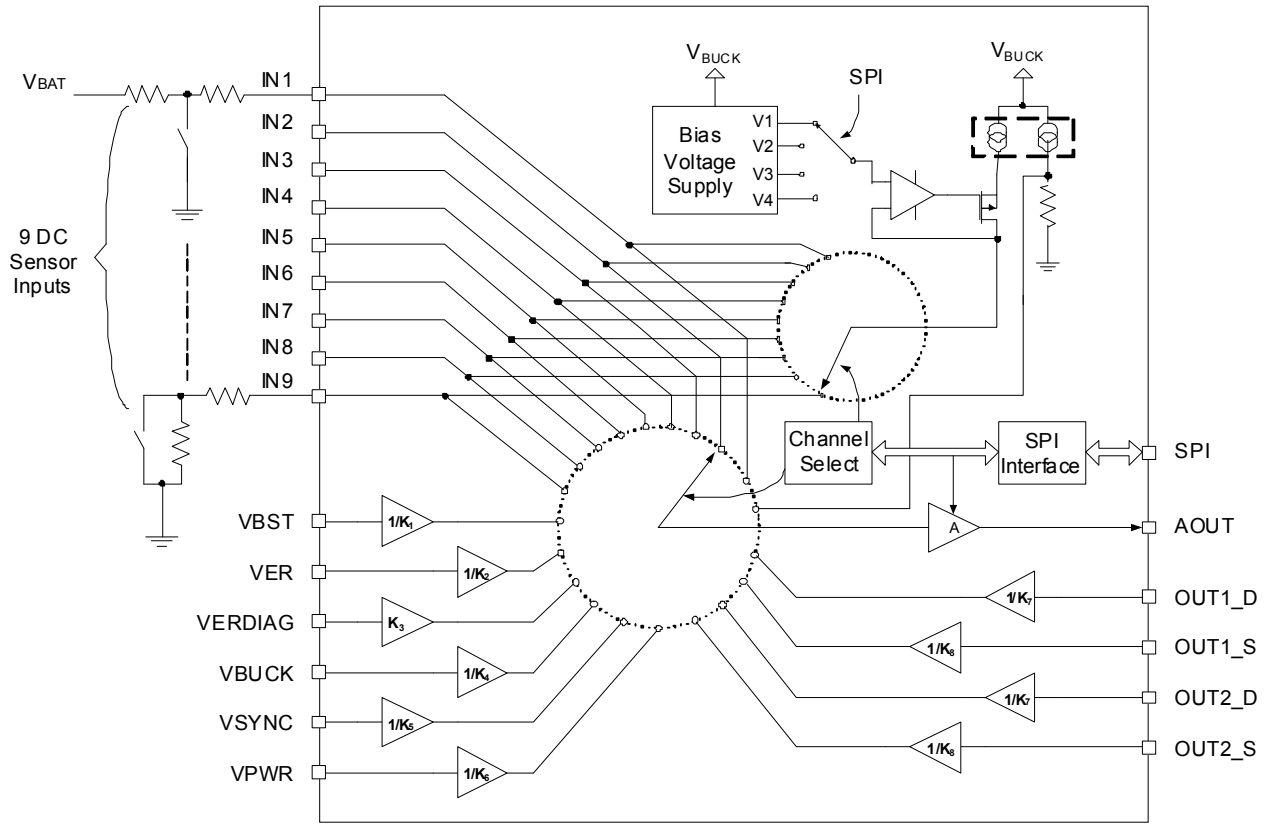


Figure 20. DC Sensor Interface and Analog Output Block Diagram

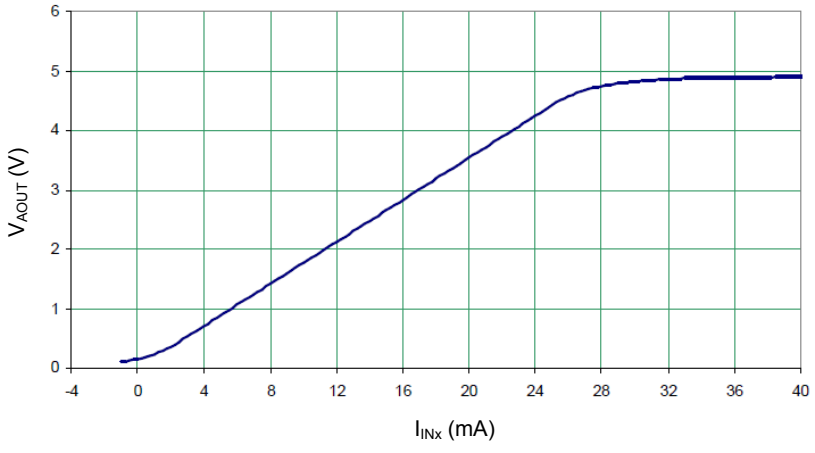


Figure 21. V_{AOUT} vs. I_{INx} Monotonic Operation

SERIAL PERIPHERIAL INTERFACE (SPI)

The 33789 SPI interface uses a slave configuration. It features:

- 16-bit data frame
- Up to 8.0 MHz SPI clock
- 5.0 or 3.3 V compatibility (receives 3.3 V SPI inputs without a level shifter)
- Three extra chip selects $\overline{CS\_A}$, $\overline{CS\_B}$, and $\overline{CS\_C}$ to support SPI monitor extract on-board digital sensor data for up to four sensors.

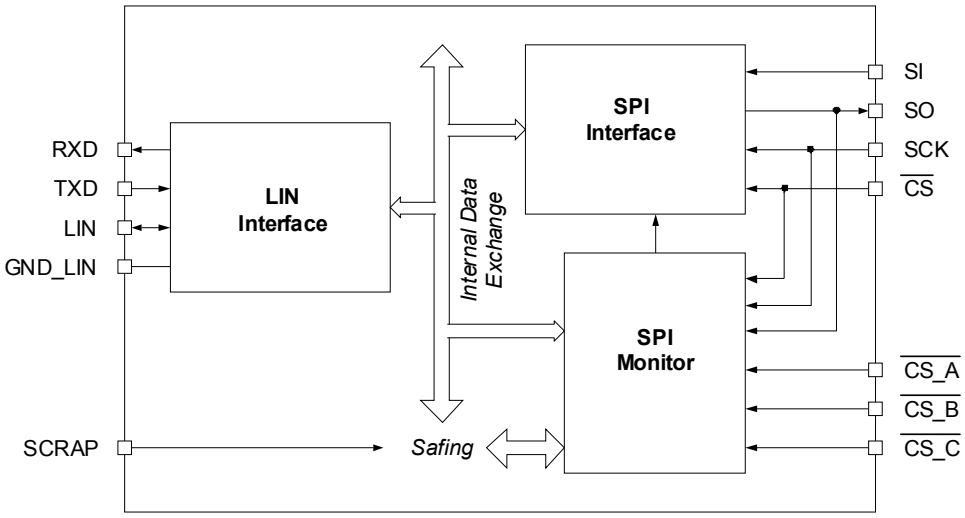


Figure 22. Communication Interfaces Block Diagram

LIN Physical Layer

The LIN physical layer is LIN 2.1 compliant, and supports three communication speeds by changing the output slew rate:

- LIN: up to 10.4 kBaud
- LIN: up to 20 kBaud
- ISO 9141 (K-line): up to 100 kBaud

This external communication interface can also be configured to directly output one of four satellite sensor channel's Manchester code.

SAFING LOGIC

The Safing Logic block utilizes a logic structure, which is independent of the MCU, to monitor both on-board sensors and satellite sensors, to determine the vehicle safety status, and verify the necessity to warrant Arming deployment of the airbag system. The functions of each section can be summarized as following:

1. SPI Monitor and Decoder:
- Extracts all of the sensor data transferred on the SPI in responding the MCU requests
- Checks the sensor data whether they are in valid ranges and in the correct sequence requested by the MCU

2. Safing State Machine:
- Applies overall safing control
- Supports 5 exclusive operation modes:
  - Start-up Mode
  - Diagnostic Mode
  - Safing Mode
  - Scrap Mode
  - Arming Mode

3. Safing Control Counters:

Data Valid Counter

- Incremental by each sensor message containing valid data
- Read by the MCU to determine if the safing logic has sufficient sensor data

Sequence Counter

- Incremented by each valid sensor message
- Ensures the sensor data is requested by the MCU in the correct range of values, and aligns the sensor data to the corresponding safing threshold

4. Safing Threshold Logic:

- Ensures the safing threshold values can be reliably written and read through a secure protocol run by the MCU

5. Safing Compare Logic:

- Compares sensor data with configured threshold aligned by the sequence counter
- Increments the incident counter (sample counter) whenever the sampled sensor data value is beyond the thresholds
- Checks the incident counter to determine if Arming should be asserted.

6. Arming Enable Output:

- A pair of complementary logical outputs used to enable the external arm circuit and/or squib drivers for deployment.

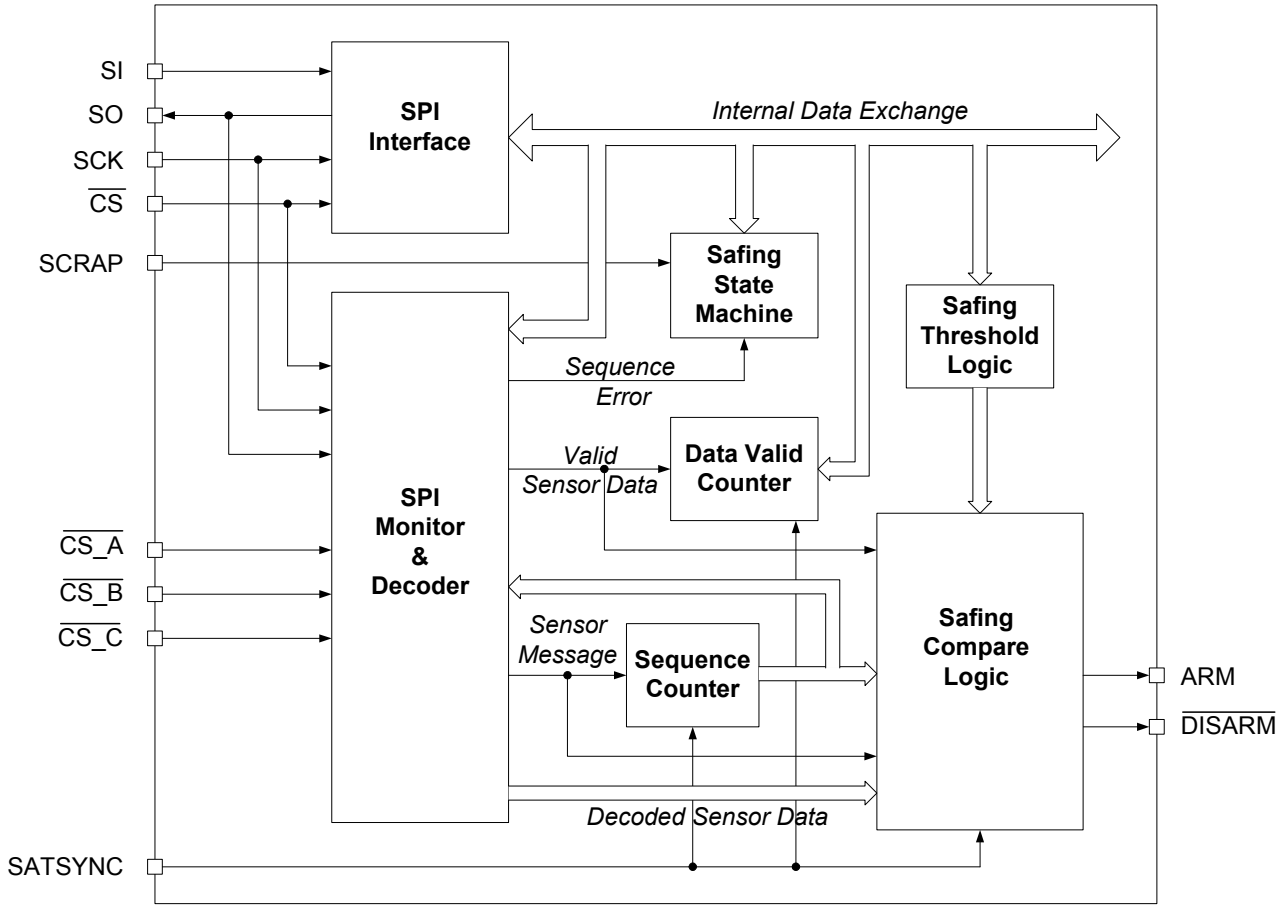


Figure 23. Safing Logic Block Diagram

CONFIGURABLE GENERAL PURPOSE DRIVERS

The 33789 offers two general purpose drivers. Each one can be configured as either a high-side driver or a low-side driver via the SPI. Both drain and source terminals of each driver have connect pins on the package, for external configuration convenience.

The driver output pins can withstand shorts to as low as -1.0 V, as high as V_{PRW} + 1.0 V, and up to 27 V for 5 minutes. They will survive with 40 V load dump. The driver output current capability is 70 mA with current limitation. The driver has integrated diagnostics and short-circuit protection. The output status can be checked by the MCU via the SPI. All output pin voltages can be monitored at the multiplexed analog output pin AOUT.

The driver control block has a built-in 128 Hz 6-bit PWM modulator. Thus, the driver can be used as a dimmable indicator driver (such as an LED). When this option is selected, the activation of both drivers will be logically synchronized, which means both drivers will be turned on simultaneously. This allows an application to combine both drivers in parallel to drive a single load with a doubled drive capability.

The output stage has slew rate control and thermal shut down features to improve performance and reliability.

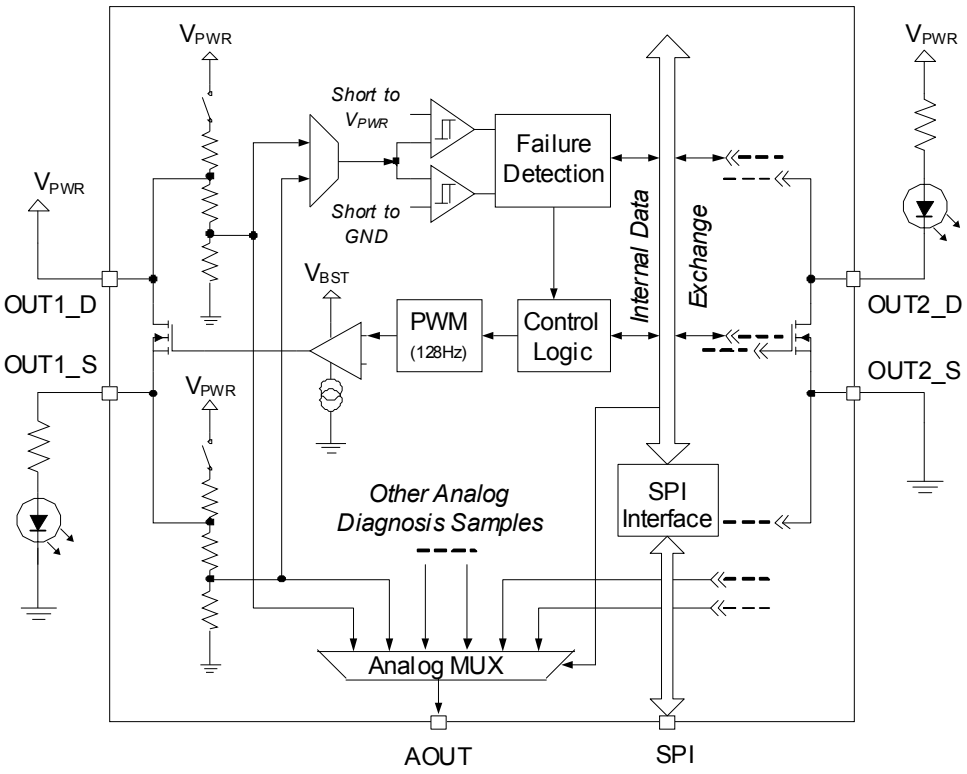


Figure 24. Configurable General Purpose Driver Block Diagram

FUNCTIONAL DEVICE OPERATION

OPERATING MODES

POWER MODE CONTROL

The 33789 Power Mode Control controls the start-up activation of both boost and buck power supplies, based on the voltages on the VPWR and WAKE pins.

The Wake input is a battery voltage, active-high logic input, and the detection threshold is normally $V_{PWR}/2$. When the battery input at the VPWR pin exceeds the low-voltage lockout threshold V_{BST_UV}, and the WAKE state is active (logic high), both the boost and buck converters are started. This low-voltage lockout threshold is also used as the ignition status threshold. The MCU can receive an indication that the threshold has been exceeded, when using the SPI STATUS to read the IGNSTSAT status and receiving the signal IGN=1 (see Table 32).

Hysteresis is applied to prevent inadvertent deactivation of the boost supply. Figure 25 shows the glitch suppression of the Wake-up signal.

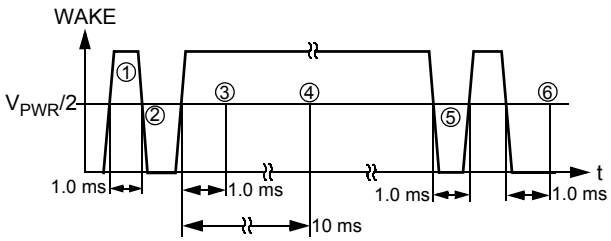


Figure 25. Wake Glitch Suppression

The suppression results of the above six marked scenarios in Figure 25 are:

1. No change of sleep mode state, but current consumption may exceed specification for sleep mode.
2. The Sleep mode current returns to within specified limits.
3. Power supply exits Sleep mode. Switches start operating if applicable voltages exceed the undervoltage lockout threshold, but the Sleep Reset is still active, because of its 10 ms delay in response to the Wake-up signal. The system stays in Sleep mode.
4. Sleep Reset is released and the entire system starts operating. After this point, a SPI command to turn off switches would not be executed, but would be latched and wait for the WAKE signal change to low.
5. The latched SPI command to turn off the switches would not be executed if the Wake signal has turned to a low less than 1.0 ms.
6. After the Wake signal stays low for more than 1.0 ms, the latched SPI command to turn off the switches is executed and the system is turned off.

To simplify the power supply state diagrams, an internal active low signal $\overline{\text{Sleep Mode}}$ needs to be introduced.

Figure 26 shows the logic relation between the $\overline{\text{Sleep Mode}}$ signal and the Wake signal, SPI Buck_off command, and Sleep_Reset status.

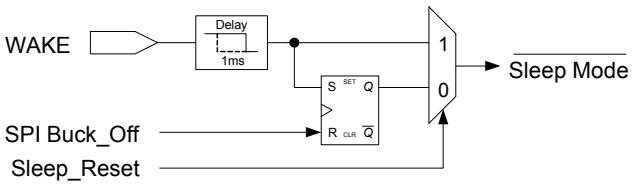


Figure 26. Sleep Mode Control Logic

With the $\overline{\text{Sleep Mode}}$ signal, the 33789 power mode control logic can be illustrated in the following diagrams.

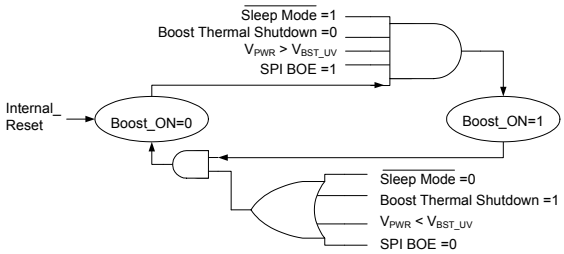


Figure 27. Boost Control Logic Diagram

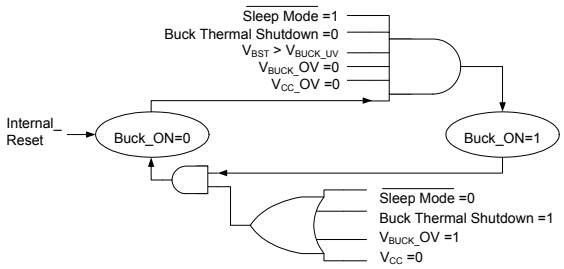


Figure 28. Buck Control Logic Diagram

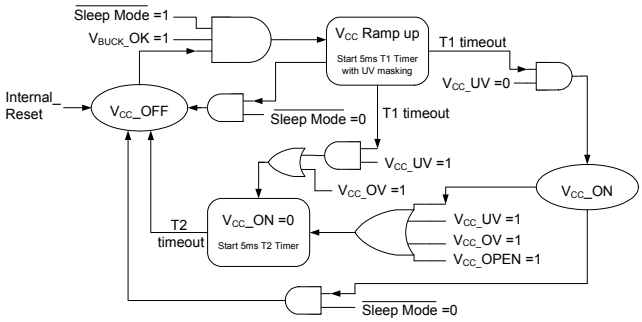


Figure 29. VCC Control Logic Diagram

V_{BUCK} DIAGNOSTIC AND V_{CC} RESTART

Figure 29 indicates "V_{BUCK}_OK = 1" is a necessary condition for V_{CC} start. In a specific case, it can be V_{CC} dependent. The situation could happen during the process of an MCU read of V_{BUCK} from the AOUT pin, via the analog MUX, when V_{CC} is incidentally turned off and attempted to be turned back on.

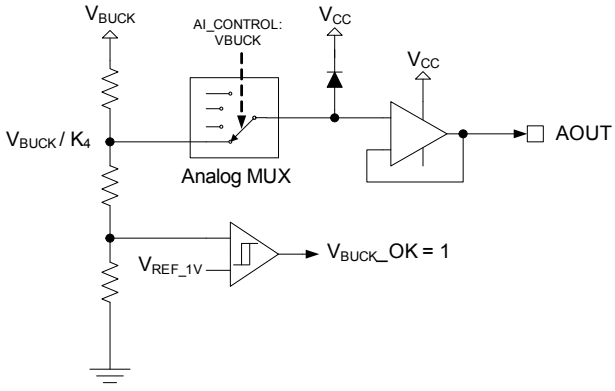


Figure 30. V_{BUCK} Diagnostic and V_{CC} Clamping

In Figure 30, the analog MUX output is clamped to V_{CC}, to protect the 5.0 V buffer amplifier. When V_{CC} is turned off, both the input and output of the MUX are clamped to GND, pulling the V_{BUCK}_OK comparator input below 1.0 V, therefore, "V_{BUCK}_OK = 0". This logic status will lock out V_{CC} from a restart, as long as the MUX is not changed by an internal reset.

In vehicle applications, when the battery voltage drops very low, V_{PWR} will fluctuate near the V_{BST_UV} threshold. This particular operation condition will cause both the boost and buck switches to oscillate, resulting in a V_{CC} on-off restart cycle, as described in Figure 27, Figure 28, and Figure 29 respectively. Other possible conditions causing V_{CC} to turn off, can be found in Figure 29, the VCC Control Logic Diagram.

If the MCU can always read V_{BST} *and* show that V_{BST} is in the specified normal operation voltage range, just before reading V_{BUCK}, the buck capacitor should be able to hold the valid voltage long enough to ensure that V_{CC} will not drop off before the V_{BUCK} diagnostic read is complete. This software implementation can avoid a V_{CC} restart difficulty in the low V_{PWR} fluctuation condition. Users can also find other hardware solutions, with external configurations, to prevent V_{CC} from dropping below its threshold, flipping the V_{BUCK}_OK comparator output.

INTERNAL POWER SUPPLY

The 2.5 V internal supplies are created, based on two voltages: V_{PRE_HIGH} and V_{PRE_LOW}.

V_{PRE_HIGH} Regulator

V_{PRE_HIGH} provides supply for the power switches. The V_{PRE_HIGH} regulator starts operation with the VPWR input. After the VBST output reaches the normal value, it switches the source to VBST.

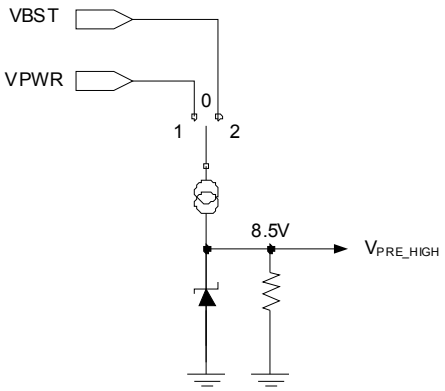


Figure 31. VPRE_HIGH to V_{PRE_HIGH}

The V_{PRE_HIGH} switch control logic can be described with the following truth table in Table 7.

Table 7. V_{PRE_HIGH} Switch Control

Internal Reset	$\overline{\text{Sleep Mode}}$	Boost_OK	Switch Position
1	X	X	0
0	0	X	1
0	1	0	1
0	1	1	2

V_{PRE_LOW} Regulator

V_{PRE_LOW} supplies power for the logic and bandgap circuits. The V_{PRE_LOW} regulator starts operation with the VPWR input. After the VBUCK output reaches the normal value, it switches the source to VBUCK.

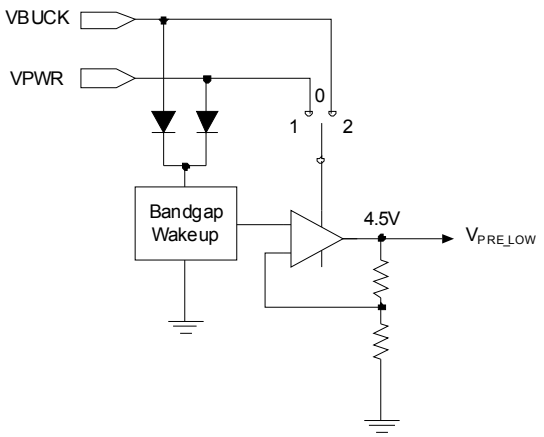


Figure 32. V_{PRE_LOW} Regulator

The V_{PRE_LOW} switch control logic can be described with Table 8.

Table 8. V_{PRE_LOW} Switch Control

$V_{WAKE} > V_{PWR}/2$	$\overline{\text{Sleep Mode}}$	Buck_OK	Switch Position
0	0	X	0
X	1	0	1
X	1	1	2
1	0	X	1

V_{2P5} and V_{DD} Regulators

The 4.5 V V_{PRE_LOW} is used to create a 2.5 V internal supply V_{2P5}, which supplies the analog circuit, and its buffered output V_{DD} supplies digital circuit.

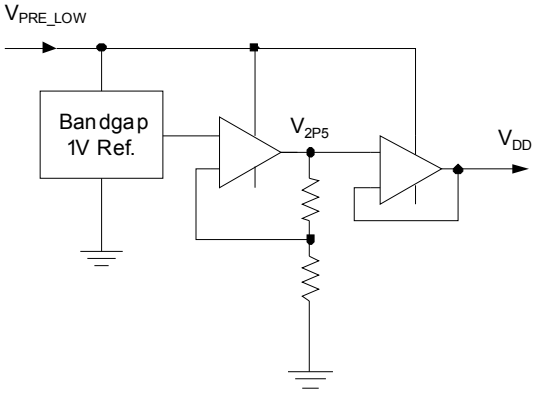


Figure 33. 2.5 V Internal Supply Regulators

V_{DD} Output Capacitor and Diagnostics

The V_{DD} regulator is switched off for about 6.0 µs every 200 ms. Once the capacitor is disconnected or out of tolerance, the output voltage will drop and the V_{DD} undervoltage error can be detected.

WATCHDOG STATES AND RESET

Types of Resets and Reset Sources

The reset functions of the 33789 control both its internal resets and the external resets on all of the devices in the system equipped with a reset input.

The internal reset is triggered by the V_{DD} voltage thresholds and the internal bandgap regulator status.

The external $\overline{\text{RESET}}$ pin is driven by the following reset sources:

- V_{CC} voltage monitor
- Window watchdog
- V_{DD} voltage monitor
- Open ground monitor (for GNDA and VSS)
- Internal bandgap regulator monitor

Figure 34 shows the logic relation between all of the resets and all of the reset sources.

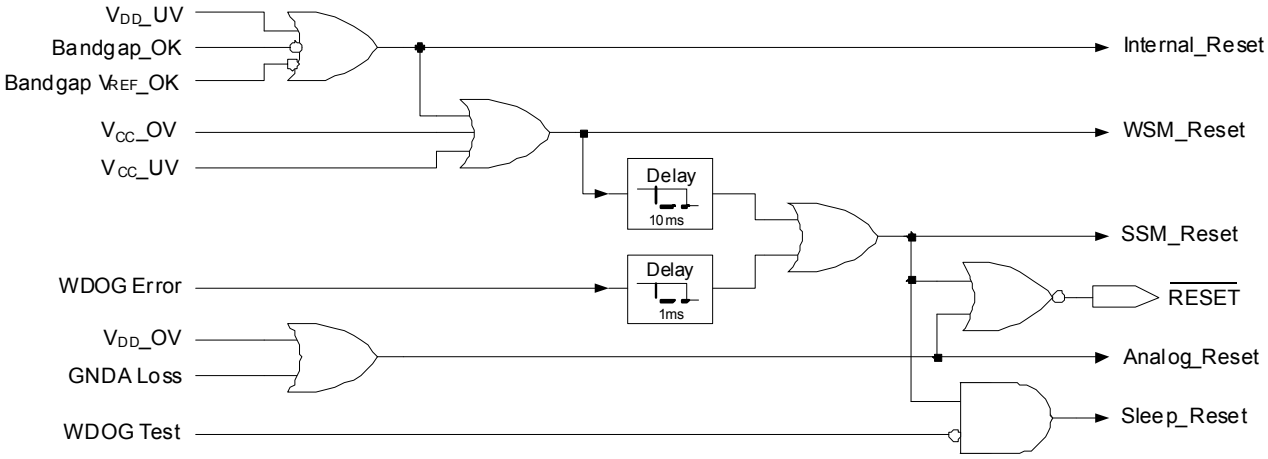


Figure 34. Reset Logic

The functions of the reset signals are:

- Internal_Reset: Resets all internal blocks except Safing and Watchdog
- WSM_Reset: Resets Watchdog State Machine
- SSM_Reset: Resets Safing State Machine
- Analog_Reset: Arm enable for ARM / $\overline{\text{DISARM}}$
- Sleep_Reset: Resets Sleep_Mode Logic

Start-up Behavior

After wake-up, when V_{CC} ramps up, the internal power supply holds the $\overline{\text{RESET}}$ pin low and keeps the watchdog in a “INITIAL” state with the 33789 status register bit WDR = 0, which indicates the reset is not caused by any watchdog error. The register is guaranteed by design to be inactive during the V_{CC} ramp up period.

When the power-on delay has elapsed and V_{CC} has entered into the valid voltage range, the $\overline{\text{RESET}}$ pin is released and the system operation starts.

The Watchdog State machine (WSM) does not start its operation until the first watchdog feed command is received.

Before the first watchdog refresh, the ARM and $\overline{\text{DISARM}}$ outputs are forced to maintain their high-impedance states.

Watchdog Window

A watchdog window is defined as a time window between two adjacent watchdog refreshes. The 33789 uses software watchdog, it periodically receives watchdog refresh signals from the MCU through the SPI interface.

A successful watchdog refresh is a SPI command, WDOG_FEED (high or low), followed by another SPI command, WDOG_FEED (low or high), within a designated watchdog window. (See Figure 35, Watchdog Windows)

Once the 33789 receives the first WDOG_FEED command, the first successful refresh occurs and the watchdog transits from “INITIAL” state to “DRIVE” state. (See Figure 36, Watchdog State Diagram)

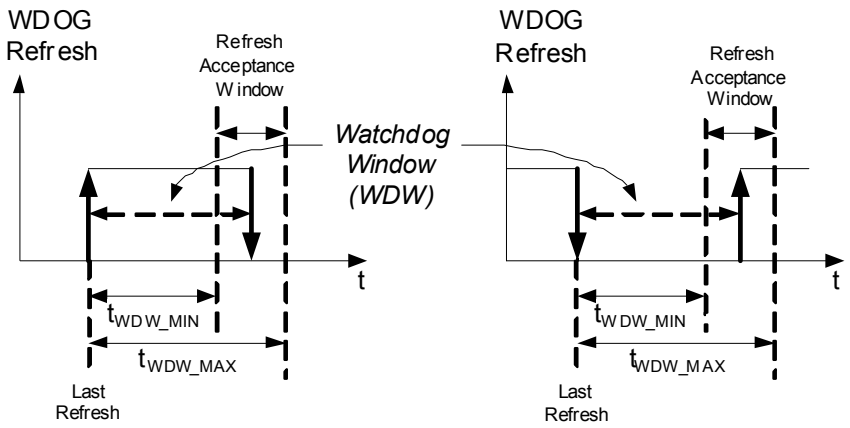


Figure 35. Watchdog Windows

Watchdog Error

WDOG Error is defined as:

NOT [WDOG OVERIDE]

AND

[WDOG_FEED with same polarity as the previous feed

OR

WDOG_FEED before the min. window time to the previous feed

OR

WDOG_FEED after the max. window time to the previous feed]

WDOG Refresh OK is defined as:

WDOG_FEED with opposite polarity to the previous feed

AND

WDOG_FEED after the min. window time to the previous feed

AND

WDOG_FEED before the max. window time to the previous feed

If a window watchdog refresh fails, the $\overline{\text{RESET}}$ pin will be pulled down for 1.0 ms to reset the system, and the 33789 internal status register will set the Watchdog Error Status bit WDR = 1, to indicate a watchdog error is the source of the reset.

The value of the WDR bit is latched and can be read by the MCU via the SPI STATUS request command. The WDR bit is cleared by either a WSM_Reset or a correct WDOG_FEED.

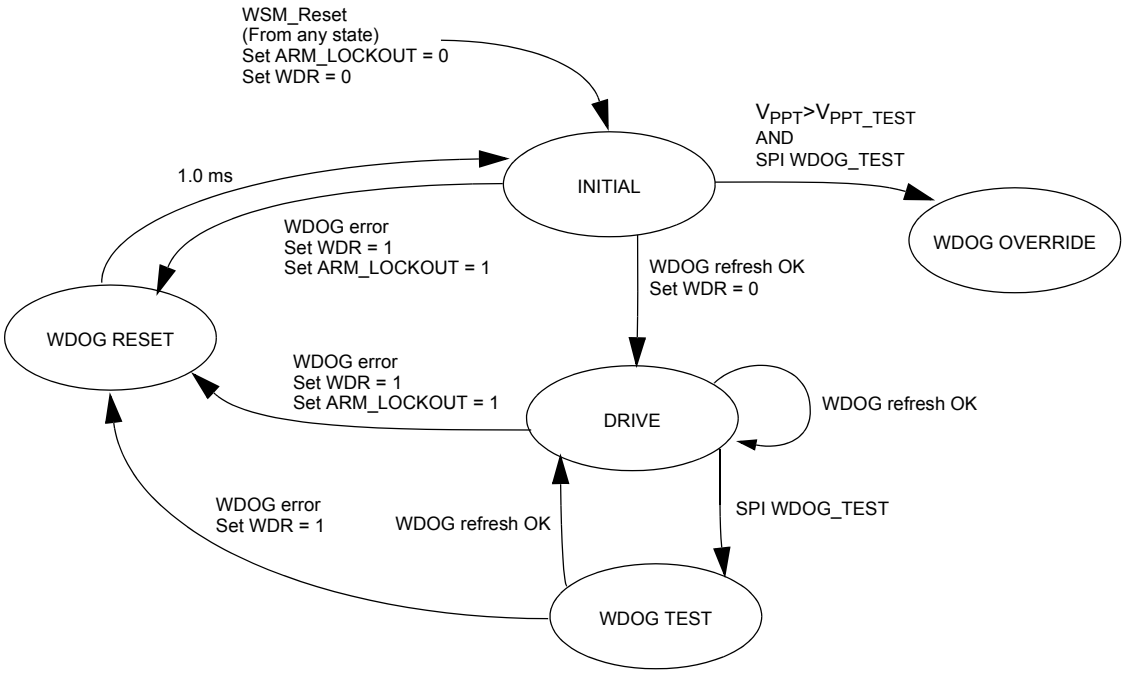


Figure 36. Watchdog State Diagram

Arm Lockout and WDOG_TEST

During a system reset, both the ARM and $\overline{\text{DISARM}}$ pin outputs are forced to the high-impedance state, which is called Arm Lockout. To individually test ARM and $\overline{\text{DISARM}}$ (The tests allow both the ARM and $\overline{\text{DISARM}}$ pins to be set to “1” or “0” at same time) while the WSM is still running in the background, the WSM can be set to the WDOG OVERRIDE state after a WSM reset, or insert the SPI command of WDOG_TEST from the DRIVE state, to avoid setting ARM_LOCKOUT = 1.

Though watchdog error always causes a system reset, which can be measured at the $\overline{\text{RESET}}$ pin and can be checked by using the SPI STATUS command to read the bit WDR = 1, it does not always cause an Arm Lockout, which depends on the WSM running in the DRIVE state, or in the WDOG TEST state before the watchdog error occurs. Regardless whether the watchdog error causes an Arm Lockout, the WSM_Reset always brings the WSM back to the INITIAL state, with the setting of ARM_LOCKOUT = 0 and WDR = 0 at the end of the system reset.

To facilitate testing of the watchdog error function, the SPI command WDOG_TEST can be used to prevent the Arm Lockout caused by a watchdog error. This command is only valid for the next watchdog window: A WDOG_TEST command has to be inserted before a watchdog error (invalid refresh or missing refresh) within the same watchdog window. Thus, once the error occurs, the consequential resets would not cause an Arm Lockout. (See Figure 37 for some typical examples of successful and unsuccessful inserted SPI WDOG_TEST commands)

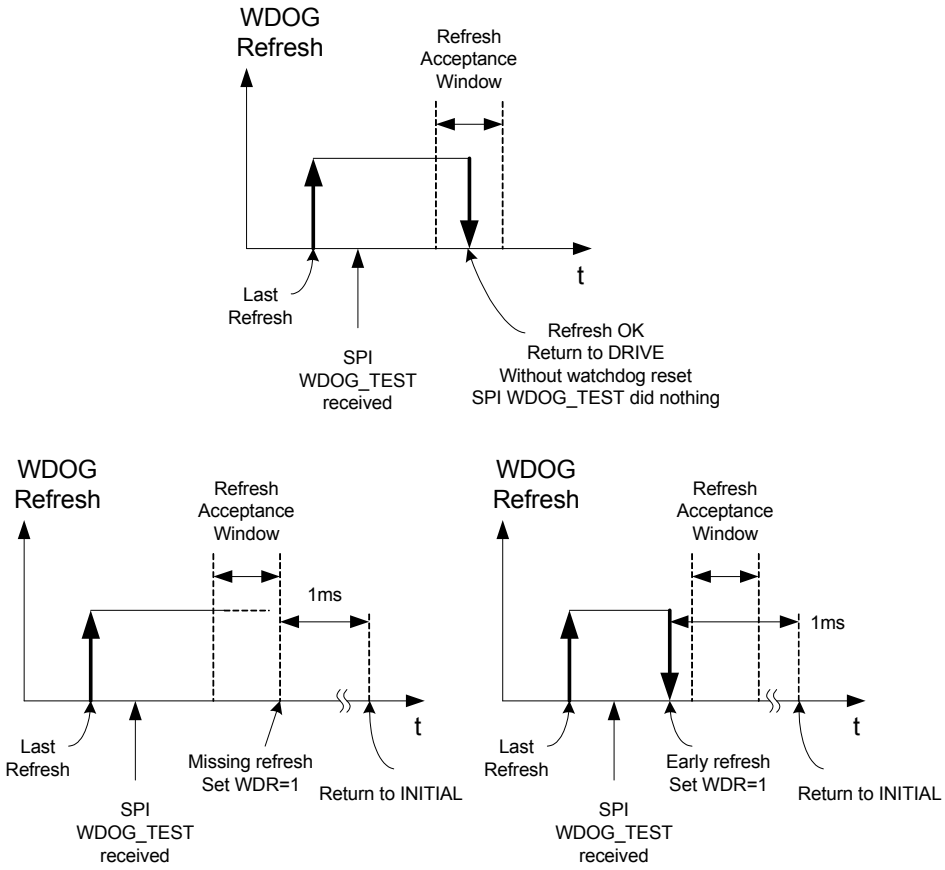


Figure 37. Successful and Unsuccessful WDOG Test Examples

Arming Logic

When an internal Arm signal is created, it shall be output through the ARM and $\overline{\text{DISARM}}$ pins only when the following conditions are satisfied:

While in WDOG_OVERRIDE state

OR

While in DRIVE state with

[SSM_Reset inactive

AND

Arm_Lockout inactive]

In any other conditions, the internal ARM / $\overline{\text{DISARM}}$ control signal shall never be sent to the output, and the output pins ARM and $\overline{\text{DISARM}}$ shall be set to high-impedance.

Whenever an Analog_Reset is created, the ARM and $\overline{\text{DISARM}}$ outputs are set to high-impedance to inhibit outputs by an analog implementation, as a part of failure mode control, the Arming logic result will be ignored.

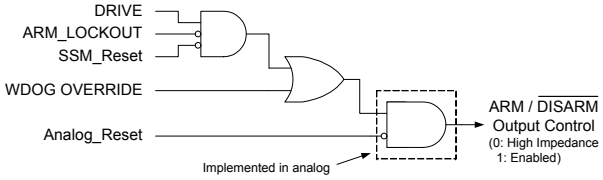


Figure 38. Arming Logic

SATELLITE SENSOR INTERFACE

PSI5 Interface

The satellite sensor interface (see Figure 19) on the 33789 serves as master interface. Each one of its channels independently supplies a regulated DC voltage V_{SAT_OUT} to its satellite devices. At the same time, it monitors the current draw to receive the sensor signals. The output current can be limited for fault protection. The satellite sensors transmit Manchester-encoded data with current modulation. The Manchester coding uses a rising edge to represent logic “0” and a falling edge to represent logic “1”.

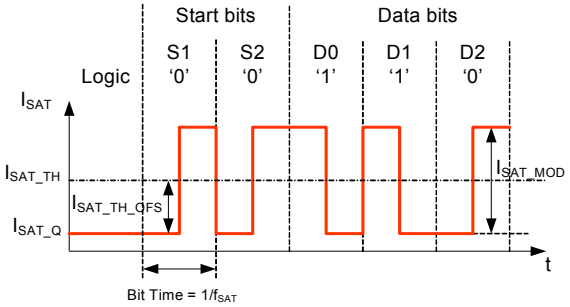


Figure 39. Current Modulation and Manchester Bit Encoding of Satellite Sensor

The PSI5-P 10P -500/3L mode of PSI5 V1.3 protocol has the following features:

- PSI5-P: Peripheral Sensor Interface - Parallel Bus mode
- 10P: 10 data bits + 1 parity bit
- -500: 500 µs nominal synchronization period
- /3: three time slots for sensor data
- L: 125 kbps

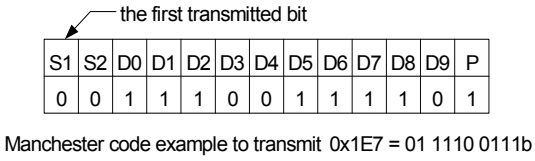


Figure 40. Satellite Data Frame Format

The even parity is checked for the entire data transmission except the start bits. If a parity error is detected, an error message will be sent to the MCU.

The 33789 automatically calibrates the sensor clock, to align the sampling timing of the receiver for the Manchester decoding.

Each channel has implemented an input data filter to remove the glitch from the input signal and recover data from waveform distortion, to reduce the decoding error. The input data filter includes sampling / holding circuit, shift register, and majority detector.

If one or more of following statements are true, a Manchester Error will be directed to the MCU:

- Two valid start bits are detected, and at least one of the expected 13 mid-bit transitions are not detected.
- Two valid start bits are detected, and more than 13 mid-bit transitions are detected.
- Two valid start bits are detected, and the sampled logic levels before and after any of the 13 expected mid-bit transitions are the same.

Synchronous Operation Modes

To synchronize the sampling of satellite sensor data, the master interface circuitry on the 33789 creates a sync pulse with increased voltage added on the top of sensor supply voltage V_{SAT_OUT}, to signal the initiation of sampling to the satellites. The MCU periodically sends a satellite synchronization signal (Satsync) to the 33789, to activate the sync pulses and controls the timing of the satellite data acquisition.

When the rising edge of the Satsync signal is detected, the master interface outputs four Sync pulses, one for each channel, on channels PSI5_1 through PSI5_4, in sequence. A 4.0 µs stagger time is inserted from channel to channel, to avoid high peak current. Figure 41 illustrates the sync signals’ voltage and timing relations.

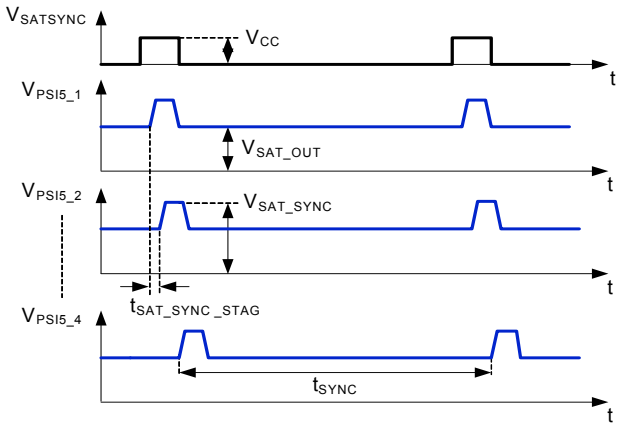


Figure 41. Satellite Synchronization Pulses

The sync pulse driver can either source or sink bus current. It outputs higher charge current to increase the bus voltage V_{PSI5_X} from V_{SAT_OUT} to V_{SAT_SYNC}, at the beginning of Sync pulse, and discharges the bus capacitance at the end of sync pulse, to return the bus voltage back to V_{SAT_OUT}.

The pull-down device to sink the bus current is current limited. The sync pulse output from the interface is wave-shaped to limit the slew rate for EMC improvement. In the synchronous mode operation, satellite sensors transmit data in response to Sync pulse. Each satellite has its own assigned time slot for sending data. All of the satellites need to be pre-programmed for timing order, to realize different communication start times.

The 33789 PSI5 interface supports two types of synchronous operation modes for scheduling satellite data transfer. The operation mode can be selected channel-by-channel per MCU SPI commands.

1. Synchronous Time-division Multiplexed (TDM) Mode

The PSI5-P 10P -500/3L mode is a synchronous TDM mode of the PSI5 protocol, which supports one to three satellites per channel.

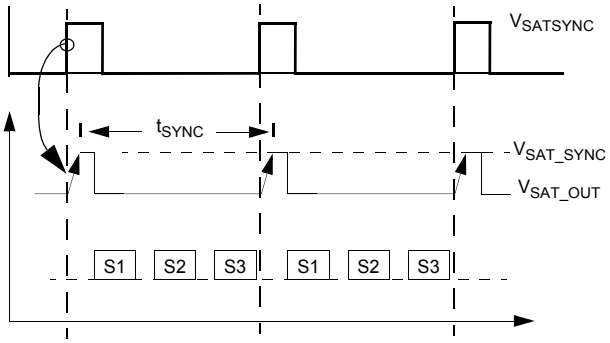


Figure 42. Synchronous TDM Mode

The rising edge of the Satsync signal triggers the generation of the sync pulse, the falling edge of Satsync is ignored.

The time window between two Sync pulses is divided into three time slots, each slot for one of the three satellite sensor's data. Once the three Manchester data are received and decoded in sequence at the 33789, they are stored in order into three internal registers A, B, and C.

All bits of these registers are simultaneously updated upon reception of the satellite message to prevent partial frame data from being checked out via the SPI interface. A fixed blanking interval, which is triggered by the rising edge of the Satsync signal, is inserted at the receiver to avoid false triggering of the Manchester decoder.

The PSI5 Sync pulse can also be used for bidirectional communication. This feature allows the 33789 to send commands to satellites, which is useful to pre-program or re-program the satellite sensors in the system. Once the PSI5 bus is set to bidirectional communication mode by the MCU via the SPI, in every fixed Satsync period, the appearance of the sync pulse represents a logic "1", and the missing pulse represents a logic "0".

The communications between an airbag ECU (master terminal) and the PSI5 satellite sensors (slave terminals), use two different modulations:

Sensors → ECU: current modulation

ECU → Sensors: voltage modulation

2. Satsync-steered Mode

The Satsync-steered mode is another type of TDM operation. It supports up to two satellites per channel.

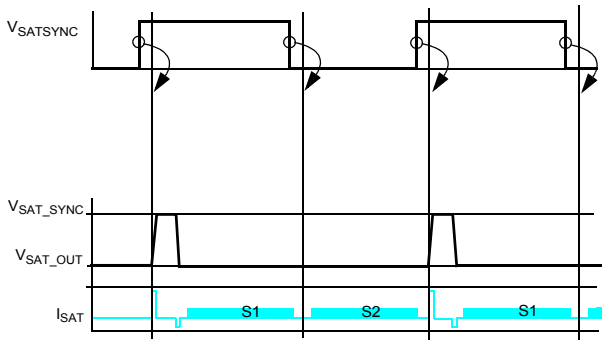


Figure 43. Satsync-steered Mode

The data from two parallel connected satellite sensors are transferred in serial, and they are time-divided with alignment to the Satsync edges.

At the 33789, the logic level of the Satsync signal steers the incoming sensor data into two input data registers:

- When the Satsync input is high, the received data is stored in register A
- When the Satsync input is low, the received data is stored in register B.

Quiescent Current Monitoring

The quiescent current on the PSI5 bus has a wide tolerance range. It varies from sensor to sensor, and depends on the number of the sensors on the bus. Supply voltage and ambient temperature also have an influence on the satellite sensor quiescent current. The 33789 automatically calibrates the interface quiescent current, and resets the adaptive current detection threshold, to achieve the demodulation accuracy.

The 33789 uses three different timing strategies to monitor quiescent current in different communication states:

1) During Startup

The PSI5 standard V1.3 allows the sensor quiescent current settling time t_{SET}, up to 10 ms.

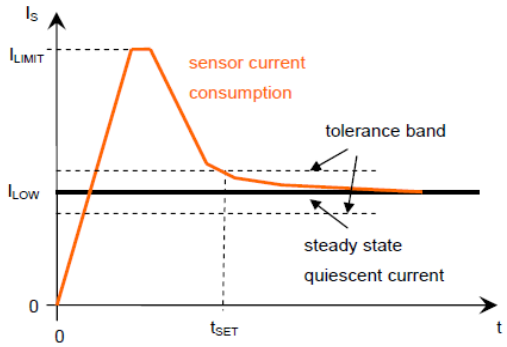


Figure 44. Sensor Current Consumption During Startup

To ensure a proper measurement, the 33789 starts to measure the bus quiescent current 10 ms after a channel is activated, and inhibits the Sync pulse generation until the first measurement is completed. The first measurement takes 35 ms.

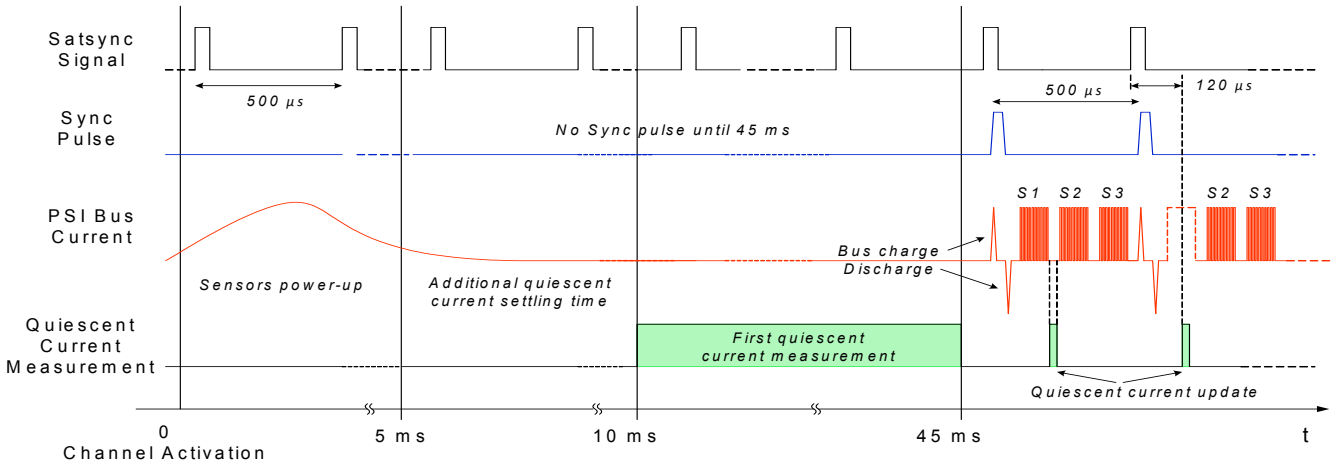


Figure 45. Quiescent Current Measurement Timing

2) During Run-time with First Data Frame

In every Sync cycle, if there is a data transfer activity during the first time slot, and the parity bit of the first data frame is checked as correct, the receiver updates the quiescent current 2.0 µs after the end of the parity bit.

3) During Run-time without First Data Frame

If there is no data transfer activity detected in the first time slot, the receiver updates quiescent current 120 µs after the rising edge of the Satsync signal. The receiver would stop the updating if there is any data bit detected during the update process.

ANALOG / DIGITAL CONVERTER

The 33789 uses a single analog to digital converter, ADC, to measure the two analog input signals:

- A_SENSOR: On-board analog safing sensor input
- VERDIAG: The voltage change across the energy reserve capacitor C_{ER} for diagnosis

When the 33789 receives the falling edge of Satsync signal, the ADC Control Logic asserts Start Of Conversion (SOC) signal, which is synchronized with the analog multiplexer (MUX) input select timing, to trigger the 10-bit A/D conversions for the two input signals in sequence. When each of conversions is completed, the ADC sends an End Of Conversion (EOC) signal back to the Control Logic, to set Sensor_val or ER_Val, depending on which input is processed.

Analog Sensor Data

After the A_SENSOR signal conversion, the Control Logic sets Sensor_val to load the data from the ADC into a high-pass digital filter, HPF, to reduce slow offset drifts caused by aging and environment. This offset remove process is also called Zero Adjust. The output of HPF is then latched into a 10-bit holding register, ASENSOR_RG.

The MCU can use Sensor Request SPI command to access the 10-bit data from ASENSOR_RG. This allows the SPI Monitor in the 33789 safing block to treat A_SENSOR data exactly same as satellite sensor data. Similar to the satellite sensor data, subsequent SPI requests of A_SENSOR data before the next Satsync falling edge will result in an error response, with the ND (No Data) bit set for Exception status.

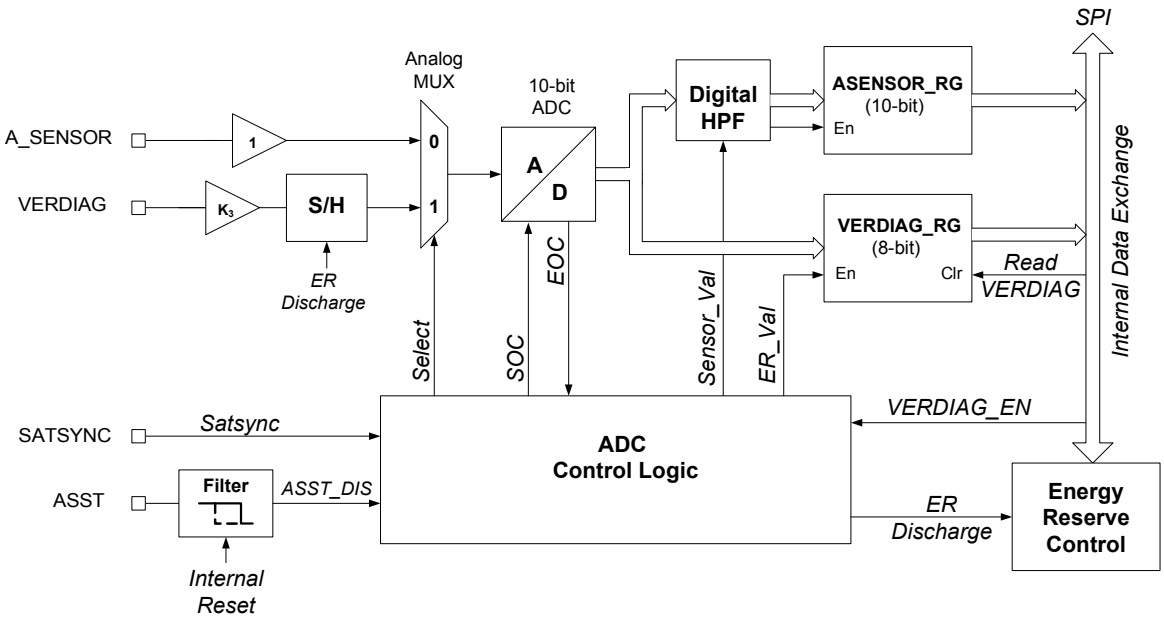


Figure 46. The 33789 ADC Process Diagram

VERDIAG Signal Conversion

To convert the VERDIAG signal, VERDIAG _EN shall be active in advance. At the next Satsync falling edge, the ADC Control Logic asserts the ER Discharge signal to turn the ER charge switch (the high-side driver) off and the ER discharge switch (the low-side driver) on, discharging the energy reserve capacitor (see Figure 15, Energy Reserve Control Block Diagram). A sampling and holding circuit catches the initial VERDIAG voltage drop to have the ER diagnostic signal ready.

When the MUX Select is switched from “0” to “1” (after the A_SENSOR signal conversion), the acquired initial VERDIAG voltage drop value is passed through and loaded into the ADC. Then the Control Logic set SOC to trigger the conversion.

At the end of conversion, if the VERDIAG_EN signal is still active, following EOC, the ER Discharge signal will be de-asserted to turn off the ER discharge switch and turn the ER charge switch back on. At the same time, upon receiving EOC, the Control Logic sets ER_Val to latch the 8 most significant bits (MSB) of the 10-bit ADC output into a holding register VERDIAG_RG. This register will be cleared after a SPI read.

The internal VERDAIG_EN signal is activated by ESR_DIAG SPI command from the MCU with the EN bit set (EN = ’1’), and it remains set until a subsequent ESR_DIAG SPI command with EN = ’0’. With this design, the 33789 can automatically repeat the ESR test on the ER capacitor in every Satsync cycle, using only one SPI command.

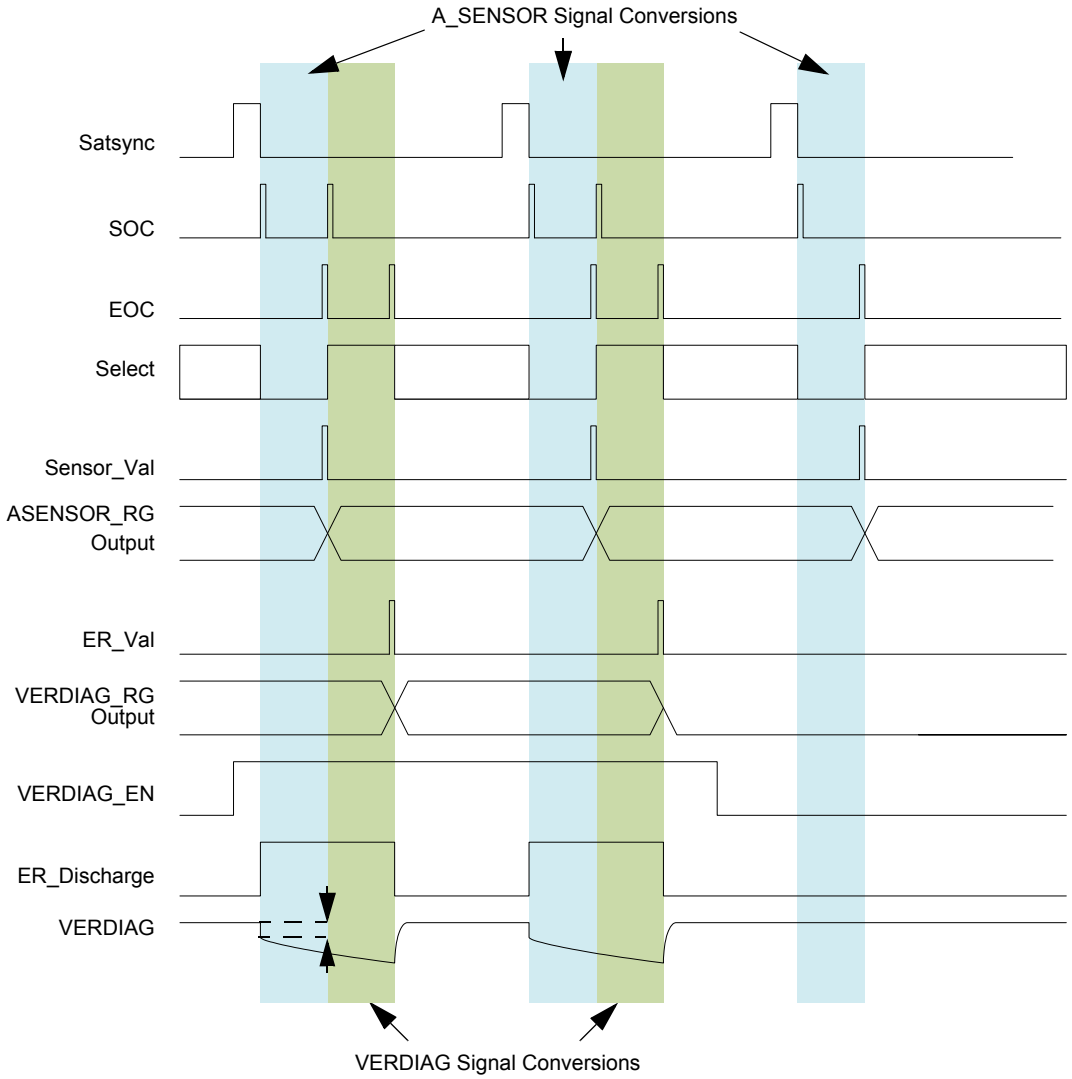


Figure 47. ADC Logic Sequence

Analog Sensor Self Test

On-board analog sensor self-test is often used to verify the functionalities and the connection between the sensor and the MCU. To facilitate the test without activation of the Arming outputs due to a fault possibility, the 33789 monitors the Analog Sensor Self Test control signal ASST from the MCU. An internal Analog Sensor Self Test Disable signal ASST_DIS is generated when the ASST pin is read logic high. The ASST_DIS signal is used to block the setting of Sensor_Val, thus inhibit triggering of the HPF and updating of the ASENSOR_RG, as the result, it suspends safing. The ASST input is filtered to prevent either inadvertent disabling of the safing during periodic self-test, or inadvertent arming, due to the slow response of the sensor output after the self-test signal deasserted. The filter is implemented with the following features:

- ASST_DIS is cleared upon an internal reset.
- ASST_DIS is set only after the ASST input is set for 3 consecutive Satsync falling edges.
- Once set, ASST_DIS will be cleared only after the ASST input is cleared for 6 consecutive Satsync falling edges.

SENSOR MESSAGE, OPERATION COMMAND AND SPI

The 33789 communicates with the MCU via the SPI bus.

SI and SO are in parallel, to transmit serial data as a bidirectional communication interface when the chip select $\overline{CS}$ is active (pulled low), and each bit of both signals is synchronized by the SPI clock SCK. SI data is clocked into the 33789 at the rising edge of SCK, and SO data is clocked out at the falling edge of SCK.

Following a SI data request from the MCU, the 33789 transmits a SO response in single stage pipeline fashion. The request/response pattern can be seen in Figure 48.

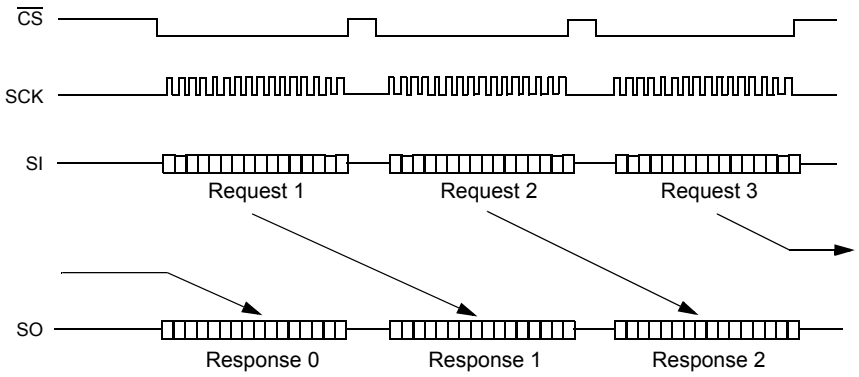


Figure 48. SPI Data Frame Latency

MESSAGE FORMATS OF SPI DATA

There are two types of messages communicated on the 33789 SPI bus: a sensor request/response message and a non-sensor request/response message. After an internal reset, the response on SO to the first SPI command is a non-sensor data error response (with RE=1, see Table 9). There is a single bit (SEN, bit 13) in the request frame which defines the message type.

Sensor Message Format

The MCU uses the sensor request/response to retrieve sensor data from:

- The 33789 satellite interface block
- On-board digital sensors with SPI interface

These types of messages, as well as the analog sensor data, are also monitored by the Safing Logic block of the 33789.

Table 9. SPI Sensor Data, - Message Format

	MSB															LSB	
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
SI	SQ1	SQ0	SEN	SQ2	0	0	0	0	0	0	0	0	LC3	LC2	LC1	LC0	Sensor Data Request
	x	x	1	x	0	0	0	0	0	0	0	0	a	a	a	a	Digital Sensor Data for Logical Channel ‘aaaa’b

	MSB															LSB	
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
SO	SQ2	SQ1	SQ0	P	ST1	ST0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Sensor Data Response
					⇓	⇓											**Status Decode:**
					0	0	Unused										Unused
					0	1	Sensor Data from Satellite and On-board Sensors										Sensor Data
					1	0	Self-test Data										On-board Sensor Self-test
					1	1	ES1	ES0									Exception Status
							⇓	⇓									**Exception Status Decode:**
							0	0	0	0	OE	ND	CNC	HE	ME	DE	Slave (Receiver/on-board sensor) Error Status

Table 9. SPI Sensor Data, - Message Format (continued)

MSB									LSB	
0	1	x	x	x	x	x	x	x	x	Reserved
1	0	x	x	x	x	x	x	x		Used for Non-sensor Data Responses
1	1	x	x	x	x	x	x	x	x	Reserved

Table 10. SPI Sensor Data, - Message Bit Definition

SENSOR DATA REQUEST SI BIT DEFINITION

Name	Bit Position	Definition
SQ2:SQ0	15, 14, 12	Sequence identifier - used for synchronizing samples
SEN	13	Sensor bit - Defines the request as a sensor data request or a non-sensor data request (1 = sensor data, 0 = non-sensor data)
LC3:LC0	3:0	Logical channel select

SENSOR DATA RESPONSE SO BIT DEFINITION

Name	Bit Position	Definition
SQ2:SQ0	15:13	Sequence identifier - used for synchronizing sensor samples
P	12	Parity - Ensures odd parity for bits 15:0 of SO
ST1:ST0	11:10	Status - Identifies the contents in D9:D0 of SO (sensor data, self-test data, error, etc.)
ES1:ES0	9:8	Exception Status - Identifies the contents of exception data (Receiver/On-board Sensor Error Status, or Satellite Error)
OE	5	Overcurrent Error - Overcurrent of the low-side driver (short to battery)
ND	4	No data (channel specific) - Sensor data not available
CNC	3	Conditions Not Correct for operation (channel specific) as defined elsewhere - Request cannot be fulfilled because the channel is off, or in the wrong mode, etc.
HE	2	Hardware Error in slave (channel/channel pair specific) - caused by hardware errors defined elsewhere, such as overtemperature overcurrent of the high-side driver (short to GND), reference out of range, etc.
ME	1	Manchester error (channel specific) - incorrect number of bits, timing violation, etc. in Manchester bit-stream
DE	0	Data error (channel specific) - Parity or CRC error in Manchester data
D9:D0	9:0	Sensor Data - For ST1:ST0 = 01

The Logic Channel Field (LC3:LC0) is used for the address of each of all 12 possible satellite sensors and one analog sensor. Each sensor address along with its channel and time slot on the bus, is assigned in Table 11.

Table 11. Logic Channel Assignment

Logic Channel (LC3: LC0)	Physic Channel	Time Slot	Data Register
0000	PSI5_1	1	PSI5_1 RG_A
0001	PSI5_1	2	PSI5_1 RG_B
0010	PSI5_1	3	PSI5_1 RG_C
0011	PSI5_1	-	N/A
0100	PSI5_2	1	PSI5_2 RG_A
0101	PSI5_2	2	PSI5_2 RG_B
0110	PSI5_2	3	PSI5_2 RG_C
0111	PSI5_2	-	N/A
1000	PSI5_3	1	PSI5_3 RG_A
1001	PSI5_3	2	PSI5_3 RG_B
1010	PSI5_3	3	PSI5_3 RG_C
1011	PSI5_3	-	N/A
1100	PSI5_4	1	PSI5_4 RG_A
1101	PSI5_4	2	PSI5_4 RG_B
1110	PSI5_4	3	PSI5_4 RG_C
1111	A_SENSOR	N/A	ASENSOR_RG

After the data from a given logic channel is read via the SPI interface, subsequent requests for the data from the same logic channel will result in an ERROR response with the No Data bit set (ND = '1').

The conditions for setting and clearing of status bits in the Sensor Data Request messages are defined in Table 12.

Table 12. SPI Sensor Data Request, - Error and Status Bit Setting

Bit	Description	Setting Condition	Clearing Condition	Channel Behavior
OE	Overcurrent Error	Satellite channel low-side overcurrent (short to V+ condition) and no hardware error (HE) detected	Internal reset or LINE_ENABLED command with xLE = 0 (OFF) for the affected channel	Channel is deactivated
ND	No Data	Channel is ON, no Manchester error, data error or overcurrent error is detected and a valid satellite frame has not been received	Cleared after a valid satellite data frame is received	None
CNC	Conditions Not Correct	Request for undefined channel or request for a channel not turned ON	Internal reset, or upon requesting a valid channel after it has been turned ON	None
HE	Hardware Error	Any of the following: 1. Satellite channel high-side overcurrent (short to GND condition) 2. Satellite average I_Q is out of range 3. Channel overtemperature conditions	Internal reset, or LINE_ENABLE command with xLE = 0 (OFF) for the affected channel	Channel is deactivated
ME	Manchester Error	Improper Manchester data - incorrect number of data bits, incorrect data edge timing, with no overcurrent or hardware errors detected	Internal reset, or cleared when read	None
DE	Data Error	Satellite data parity error, with no overcurrent error or hardware error detected	Internal reset, or cleared when read	None

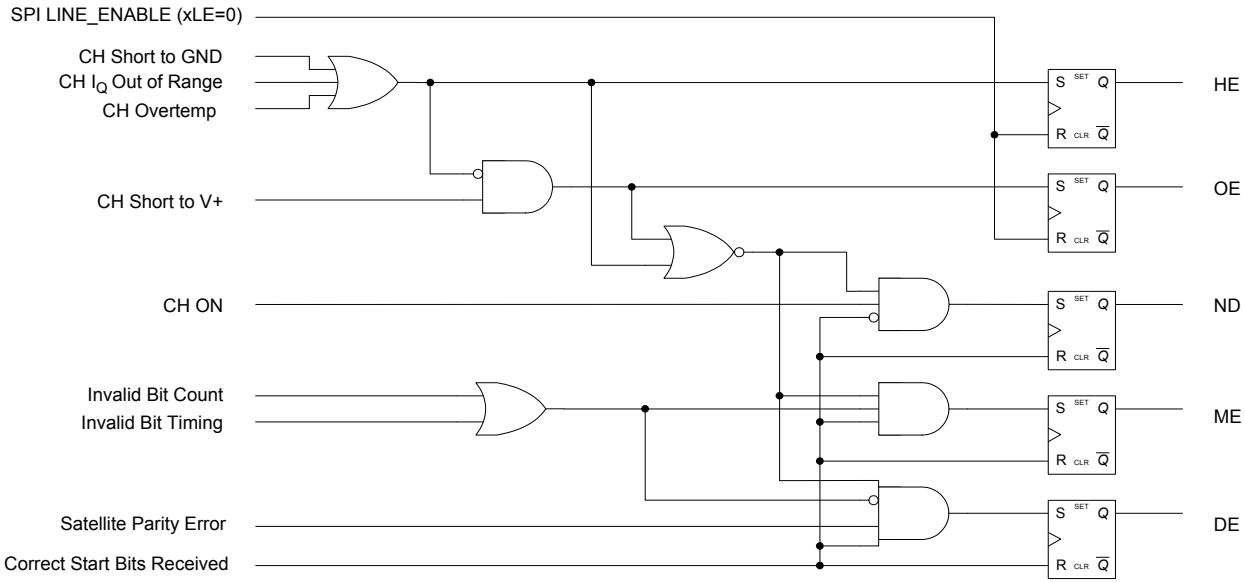


Figure 49. SPI Sensor Data Response, - Error Bit Logic

Non-sensor Message Format

Non-sensor messages are used for all of configurations, diagnostics, controls, etc. data traffic. Their message formats and bit definitions are listed in Table 13 and Table 14.

Table 13. SPI Non-sensor Data, - Message Format

	MSB															LSB	
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
SI	OP1	OP0	SEN	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	Slave Data Request
	⇓	⇓															**Operand Decode:**
	0	0	0	x	x	x	x	x	x	x	x	x	x	x	x	x	Reserved
	0	1	0	Write Address					Write Data								Write
	1	0	0	Read Address					x	x	x	x	x	x	x	x	Read
	1	1	0	x	x	x	x	x	x	x	x	x	x	x	x	x	Test

	MSB															LSB	
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
SO	0	OP1	OP0	P	ST1	ST0	ES1	ES0	D7	D6	D5	D4	D3	D2	D1	D0	Slave Data Response
		⇓	⇓														
		0	0	P	1	1	1	0	0	0	0	0	0	SE	RE	0	Error Response
		0	1	P	1	1	1	0	Slave Status								Write Response
		1	0	P	1	1	1	0	Read Data								Read Response
		1	1	P	1	1	1	0	x	x	x	x	x	x	x	x	Test Response

Table 14. SPI Non-sensor Data, Message Bit Definition

SLAVE COMMAND SI BIT DEFINITION

Name	Bit Position	Definition
OP1:OP0	15:14	Opcode - Defines operation (Read, Write)
SEN	13	Sensor bit - Defines the request as a sensor data request or non-sensor data request (1 = sensor data, 0 = non-sensor data)
A4:A0	12:8	Address - For read or write operation
D7:D0	7:0	Data - For write operation

SLAVE RESPONSE SO BIT DEFINITION

Name	Bit Position	Definition
OP1:OP0	14:13	Opcode - Identifies the contents of Read or Write data in D9:D0 - copied from SI if the request is granted
p	12	Parity - Ensures odd parity for bits 15:0 of SO
ST1:ST0	11:10	Status - Always ‘11’ for non-sensor response
ES1:ES0	9:8	Exception Status - Always ‘10’ for non-sensor response
D7:D0	7:0	Read Data/ Error Data/ Status
SE	2	SPI Error - set to ‘1’ for request (SI) frame violations (incorrect number of SCK pulses, etc.)
RE	1	Request Error - set to ‘1’ for illegal, or unknown requests

OPERATIONAL-MODE SPI COMMANDS

PSI5 Interface SPI commands

SENSOR_DATA

The SENSOR_DATA command is used to sample sensor data from the PSI5 interface and the analog sensor input. This is the only command that uses the sensor data request/response format. The details of this command are defined in Table 9, Table 10, Table 11 and Table 12.

LINE_MODE (0x4F, 0x8F)

The LINE_MODE command is used to configure the PSI5 receiver channels individually, for either Synchronous TDM Mode or Satsync-Steered. The command is latched until a subsequent SPI update or internal reset. The response indicates the current state of the line mode for each channel.

Table 15. SPI Command, - LINE_MODE

LINE_MODE (0x4F, 0x8F)

		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	**SI**	0	1	0	0	1	1	1	1	x	x	x	x	LM4	LM3	LM2	LM1
	SO	0	0	1	P	1	1	1	0	0	0	0	0	LM4	LM3	LM2	LM1
Read	**SI**	1	0	0	0	1	1	1	1	x	x	x	x	x	x	x	x
	SO	0	1	0	P	1	1	1	0	0	0	0	0	LM4	LM3	LM2	LM1

Default →

LM	Line Mode
0	Channel PSI5_x protocol = Synchronous TDM Mode
1	Channel PSI5_x protocol = Satsync-Steered Mode

LINE_ENABLE (0x43, 0x83)

The LINE_ENABLE command is used to activate or deactivate the PSI5 channels individually. The command is latched until a subsequent SPI update or internal reset. Some incident conditions, such as a thermal or overcurrent shutdown could deactivate the channel as well. The response indicates the current state of the line activation and the overtemperature status for each channel.

Table 16. SPI Command, - LINE_ENABLE

LINE_ENABLE (0x43, 0x83)

		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	**SI**	0	1	0	0	0	0	1	1	x	x	x	x	4LE	3LE	2LE	1LE
	SO	0	0	1	P	1	1	1	0	OT4	OT3	OT2	OT1	4LE	3LE	2LE	1LE
Read	**SI**	1	0	0	0	0	0	1	1	x	x	x	x	x	x	x	x
	SO	0	1	0	P	1	1	1	0	OT4	OT3	OT2	OT1	4LE	3LE	2LE	1LE

Default →

OTx	Overtemperature Shutdown Indicator
0	No overtemperature shutdown on channel PSI5_x
1	Overtemperature shutdown on channel PSI5_x

Default →

xLE	Line Enable
0	Channel PSI5_x OFF
1	Channel PSI5_x ON

SYNC_ENABLE (0x44, 0x84)

The SYNC_ENABLE command is used to individually enable or disable the Sync pulse generation for the PSI5 channels while in Synchronous TDM Mode. It can be used to support bidirectional communication between the 33789 and the satellites. The state of the xSE bits is checked at the rising edge of the Satsync signal for each Satsync period.

In Satsync-steered mode, the SYNC_ENABLE command is latched until subsequent SPI update or reset, but it has no effect on the Sync pulse output, because the communication back to the satellite via the Sync pulse modulation is disabled.

The internal reset sets xSE = 1 for default.

The response indicates the current state of the Sync pulse enable register for each channel.

Table 17. SPI Command, - SYNC_ENABLE

SYNC_ENABLE (0x44, 0x84)

		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	SI	0	1	0	0	0	1	0	0	x	x	x	x	4SE	3SE	2SE	1SE
	SO	0	0	1	P	1	1	1	0	0	0	0	0	4SE	3SE	2SE	1SE
Read	SI	1	0	0	0	0	1	0	0	x	x	x	x	x	x	x	x
	SO	0	1	0	P	1	1	1	0	0	0	0	0	4SE	3SE	2SE	1SE

	xSE	Sync Pulse Enable
	0	Channel PSI5_x sync pulse disabled
Default →	1	Channel PSI5_x sync pulse enabled

LIN Interface Control SPI Commands

LIN_CONFIG (0x50, 0x90)

The LIN_CONFIG command is used to control the LIN physical interface configuration. It supports two functions:

1) LIN signal wave-shaping:

There are three different slew rates that can be selected along with the LIN speed selection for the best EMC performance.

•>20 kBaud: Wave-shaping disabled. For test and production configuration use only

•20 kBaud: For LIN compliant 20 kBaud communications

•10.4 kBaud: For 10.4 kBaud LIN communications. It also can be used for ISO-9141communication.

2) Output Manchester Code at the RXD Pin:

This Manchester code output feature allows one of four PSI5 current/voltage converters to output the voltage modulated Manchester signal through the RXD pin. The logic level changes of the output voltage represent the detection threshold triggering status of the selected PSI5_x channel current drawn. This feature provides a convenient access for using test and development tools to acquire satellite sensor data.

The LIN_CONFIG command is latched until a subsequent SPI update or internal reset. The response indicates the current state of the LIN_CONFIG bits.

Table 18. SPI Command, - LIN_CONFIG

LIN_CONFIG (0x50, 0x90)

		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	**SI**	0	1	0	1	0	0	0	0	x	x	REN	RXO1	RXO0	FSEL	LSR1	LSR0
	SO	x	0	1	P	1	1	1	0	x	x	REN	RXO1	RXO0	0	LSR1	LSR0
Read	**SI**	1	0	0	1	0	0	0	0	x	x	x	x	x	x	x	x
	SO	x	1	0	P	1	1	1	0	x	x	REN	RXO1	RXO0	0	LSR1	LSR0

	LIN Slew Rate Select		
	LSR1	**LSR0**	**Function**
Default →	0	0	20 kBaud communications
	0	1	10.4 kBaud communications
	1	0	> 20 kBaud communications (no pulse shaping)
	1	1	> 20 kBaud communications (no pulse shaping)

	Boost/Buck Frequency Selection	
	FSEL	**Function**
Default →	0	Low speed switching (140 kHz)
	1	High speed switching (245 kHz)

Table 18. SPI Command, - LIN_CONFIG (continued)

	RX Output Select (for REN = 1)		
	RXO1	RXO0	Function
Default →	0	0	Satellite Channel 1
	0	1	Satellite Channel 2
	1	0	Satellite Channel 3
	1	1	Satellite Channel 4

	RXD Output Enable	
	REN	Function
Default →	0	Normal function (RX outputs LIN signal)
	1	Satellite monitor (RX outputs satellite Manchester signal)

Power Supply Control SPI Commands

PS_CONTROL (0x51, 0x91)

The PS_CONTROL command is used for the system power management, including controls of boost supply, buck supply, sync supply, energy reserve, and V_{CC}, as shown in Table 19.

The command is latched until a subsequent SPI update or internal reset occurs. Some incident conditions, such as a thermal or overcurrent shutdown, could also deactivate the function. The response indicates the current state of system power management.

The charge / discharge fault (CDF) bit is cleared by an internal reset, or by a SPI command attempting to deactivate both switches, by setting ERC[1:0] to '00'. Unlike other registers that are only set to their default state by an internal reset, the ERC bits are set to their default state by a Sleep Reset.

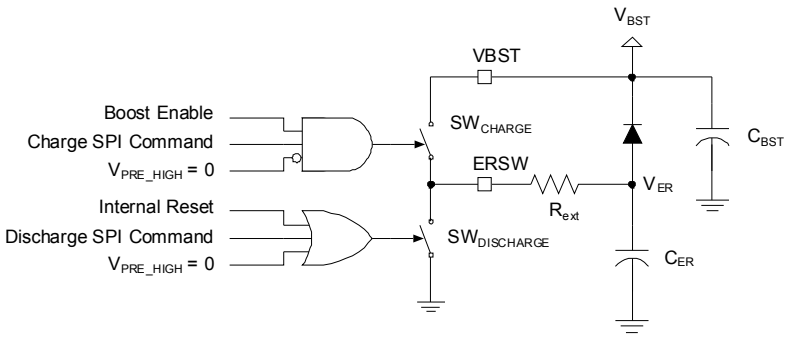


Figure 50. Energy Reserve Charge and Discharge Logic

Table 19. SPI Command, - PS_CONTROL

PS_CONTROL (0x51, 0x91)

		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	**SI**	0	1	0	1	0	0	0	1	x	x	SC	BOE	x	BUE	ERC1	ERC0
	SO	0	0	1	P	1	1	1	0	BST	CDF	SC	BOE	0	BUE	ERC1	ERC0
Read	**SI**	1	0	0	1	0	0	0	0	x	x	x	x	x	x	x	x
	SO	x	1	0	P	1	1	1	0	x	x	REN	RXO1	RXO0	x	LSR1	LSR0

	Boost Status	
	BST	**Function**
Default →	0	Boost voltage is less than threshold (~80% of target)
	1	Boost voltage is greater than threshold (~80% of target)

	CER Charge/Discharge Switch Failure Status	
	CDF	**Function**
Default →	0	No overcurrent/temp fault on charge or discharge switches
	1	Overcurrent/temp fault on charge or discharge switches

	Sync Supply Control	
	SC	**Function**
Default →	0	Deactivate sync supply
	1	Activate sync supply

	Boost Enable	
	BOE	**Function**
	0	Deactivate boost
Default →	1	Activate boost

	Buck Enable	
	BUE	**Function**
	0	Deactivate buck request
Default →	1	Activate buck

	Energy Reserve Control			
	ERC1	**ERC0**	**Discharge Switch**	**Charge switch**
	0	0	OFF	OFF
	0	1	OFF	ON
Default →	1	0	ON	OFF
	1	1	OFF	OFF

ESR_DIAG (0x42, 0x82)

The ESR_DIAG command is used to initiate the energy reserve capacitor ESR test and read the VERDIAG voltage for the test.

Writing the enable bit (EN = '1') in the command will open the charge switch and close the discharge switch at the next Satsync falling edge, to allow the measurement of the ESR voltage. The enable state will remain set for repeating ESR test until a subsequent SPI ESR_DIAG command with EN = '0'. The ESR_DIAG command will respond to a read request with the most recent VERDIAG voltage from the A/D converter.

Table 20. SPI Command, - ESR_DIAG

ESR_DIAG (0x42, 0x82)

		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	**SI**	0	1	0	0	0	0	1	0	x	x	x	x	x	x	x	EN
	SO	0	1	0	P	1	1	1	0	x	x	x	x	x	x	x	EN
Read	**SI**	1	0	0	0	0	0	1	0	x	x	x	x	x	x	x	x
	SO	0	1	0	P	1	1	1	0	D7	D6	D5	D4	D3	D2	D1	D0

Default →

Boost Status	
EN	**Function**
0	Disable ESR test (VERDIAG_EN = 0)
1	Enable ESR test (VERDIAG_EN = 1)

D7:D0	Function
Data	VERDIAG voltage (ADC[9:2]) 1.95 mV/count

Analog Interface SPI Commands

AI_CONTROL (0x52, 0x92)

The AI_CONTROL command selects an analog voltage source to be routed to the analog diagnostics output AOUT pin. The lower 5 bits of the command are used for the selection to form the multiplexed analog measurement.

The AI_CONTROL command is latched until a subsequent SPI update, or a DIAG_CLR SPI command, or an internal reset occurs. The response indicates the current state of the analog interface control.

Table 21. SPI Command - AI_CONTROL

AI_CONTROL (0X52, 0X92)

		15	14	13	12	11	10	9	8								
Write	**SI**	0	1	0	1	0	0	1	0	X	X	X	AIC4	AIC3	AIC2	AIC1	AIC0
	SO	0	0	1	P	1	1	1	0	0	0	0	AIC4	AIC3	AIC2	AIC1	AIC0
Read	**SI**	1	0	0	1	0	0	1	0	X	X	X	X	X	X	X	X
	SO	0	1	0	P	1	1	1	0	0	0	0	AIC4	AIC3	AIC2	AIC1	AIC0

Analog Interface Request Bits							
AIC4	**AIC3**	**AIC2**	**ACIC1**	**AIC0**	**HEX**	**Function**	**Multiplier**
0	0	0	0	0	$00	RSENSE	÷1
0	0	0	0	1	$01	VERDIAG	x 5
0	0	0	1	0	$02	VPWR	÷ 5.6
0	0	0	1	1	$03	VBST	÷ 8.5
0	0	1	0	0	$04	VER	÷ 8.5
0	0	1	0	1	$05	VBUCK	÷ 2.8
0	0	1	1	0	$06	VSYNC	÷ 5
0	0	1	1	1	$07	IN1	÷ 2
0	1	0	0	0	$08	IN2	÷ 2
0	1	0	0	1	$09	IN3	÷ 2
0	1	0	1	0	$0A	IN4	÷ 2
0	1	0	1	1	$0B	IN5	÷ 2
0	1	1	0	0	$0C	IN6	÷ 2
0	1	1	0	1	$0D	IN7	÷ 2

Analog Interface Request Bits							
0	1	1	1	0	$0E	IN8	÷ 2
0	1	1	1	1	$0F	IN9	÷ 2
1	0	0	0	0	$10	Unused (High-Z-output)	
1	0	0	0	1	$11	OUT1-D	÷ 5.6
1	0	0	1	0	$12	OUT1-S	÷ 5.6
1	0	0	1	1	$13	OUT2-D	÷ 5.6
1	0	1	0	0	$14	OUT2-S	÷ 5.6
1	0	1	0	1	$15	Unused (High-Z-output)	
1	0	1	1	0	$16	Unused (High-Z-output)	
1	0	1	1	1	$17	Unused (High-Z-output)	
1	1	0	0	0	$18	Unused (High-Z-output)	
1	1	0	0	1	$19	Unused (High-Z-output)	
1	1	0	1	0	$1A	Unused (High-Z-output)	
1	1	0	1	1	$1B	Unused (High-Z-output)	
1	1	1	0	0	$1C	Unused (High-Z-output)	
1	1	1	0	1	$1D	Unused (High-Z-output)	
1	1	1	1	0	$1E	Unused (High-Z-output)	
Default → 1	1	1	1	1	$1F	Unused (High-Z-output)	

DC Sensor Interface SPI Commands

DCS_CONTROL (0x53, 0x93)

The DCS_CONTROL command is used to control two internal analog multiplexers for the DC sensor input interface activation, which include:

- Sensor Channel Selection (SS): Determines which DC sensor input shall be connected to the internal regulated bias voltage supply for the analog diagnostic output AOUT.
- Bias Voltage Selection (VS): Determines which one of four predefined voltages shall be used for the bias supply applied on the selected DC sensor output stage.

The DCS_CONTROL command is latched until a subsequent SPI update, or a DIAG_CLR SPI command, or an internal reset occurs. Some incident conditions, such as thermal or overcurrent shutdown could deactivate the selections. The response of the command indicates the current state of the DC sensor interface control.

Table 22. SPI Command - DCS_CONTROL

DCS_CONTROL (0X53, 0X93)

		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	**SI**	0	1	0	1	0	0	1	1	SS3	SS2	SS1	SS0	VS1	VS0	x	x
	SO	0	0	1	P	1	1	1	0	SS3	SS2	SS1	SS0	VS1	VS0	0	0
Read	**SI**	1	0	0	1	0	0	1	1	X	X	X	X	X	X	X	X
	SO	0	1	0	P	1	1	1	0	SS3	SS2	SS1	SS0	VS1	VS0	0	0

SS3	SS2	SS1	SS0	Input Sensor Select
Default → 0	0	0	0	Voltage Supply not connected to any INx
0	0	0	1	Voltage Supply connected to IN1
0	0	1	0	Voltage Supply connected to IN2
0	0	1	1	Voltage Supply connected to IN3
0	1	0	0	Voltage Supply connected to IN4
0	1	0	1	Voltage Supply connected to IN5
0	1	1	0	Voltage Supply connected to IN6
0	1	1	1	Voltage Supply connected to IN7

SS3	SS2	SS1	SS0	Input Sensor Select
1	0	0	0	Voltage Supply connected to IN8
1	0	0	1	Voltage Supply connected to IN9
1	0	1	0	Voltage Supply not connected to any INx (reserved)
1	0	1	1	Voltage Supply not connected to any INx (reserved)
1	1	0	0	Voltage Supply not connected to any INx (reserved)
1	1	0	1	Voltage Supply not connected to any INx (reserved)
1	1	1	0	Voltage Supply not connected to any INx (reserved)
1	1	1	1	Voltage Supply not connected to any INx (reserved)

	VS1	VS0	Supply Voltage Select
Default →	0	0	Supply Voltage = 1.5 V
	0	1	Supply Voltage = 2.5 V
	1	0	Supply Voltage = 5.0 V
	1	1	Supply Voltage = 6.5 V

Safing Logic SPI Commands

SAFE_CONTROL (0x58, 0x98)

The SAFE_CONTROL command is used for the following safing logic features:

•Safing State Machine (SSM) operation mode control

•Arming output test mode control, - the Arming outputs (via ARM and $\overline{\text{DISARM}}$ pins) can only be tested while SSM is in Diag mode

•Request of the number of valid data messages received from sensors

•Error status of the safing logic

The Sequence Error (SE) bit is cleared upon the Satsync rising edge.

Once an offset of the digital A_SENSOR data is detected at the HPF, which corresponds to an offset falls outside of ±25% of the expected output, an internal offset error signal will be created and the Offset Error (OE) bit will be set. The HPF will continue process the A_SENSOR data received from the ACD, but ASENSOR_RG will not be updated with the OE bit set. The OE bit is cleared upon the SPI read only if the offset error condition is no longer present, which means the A_SENSOR input has returned to the valid range.

Table 23. SPI Command - SAFE_CONTROL

SAFE_CONTROL (0X58, 0X98)

		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	SI	0	1	0	1	1	0	0	0	X	X	X	X	MR1	MR0	TEN	LEV
	SO	0	0	1	P	1	1	1	0	VD3	VD2	VD1	VD0	MD1	MD0	OE	SE
Read	**SI**	1	0	0	1	1	0	0	0	X	X	X	X	X	X	X	X
	SO	0	1	0	P	1	1	1	0	VD3	VD2	VD1	VD0	MD1	MD0	OE	SE

	MR1	MR0	Mode Request
Default →	0	0	No mode change requested
	0	1	Request change to Safing Mode
	1	0	Request change to Scrap Mode
	1	1	No mode change requested

	TEN	Arming Output Test Enable
Default →	0	ARM/$\overline{\text{DISARM}}$ output Test mode disabled
	1	ARM/$\overline{\text{DISARM}}$ output Test mode enabled

LEV	Arming Output Test Level Select
Default → 0	Set ARM=0, $\overline{\text{DISARM}}$ = 0 if TEN = 1 and in Diag mode
1	Set ARMN=1, $\overline{\text{DISARM}}$ = 1 if TEN = 1 and in Diag mode

VD3:VD0	Valid Data Count
xxxx	Number of digital sensor messages received with valid sensor data

MD1	MD0	Mode Status
Default → 0	0	Startup Mode or Diag mode
0	1	Safing mode
1	0	Scrap mode
1	1	Arming mode

OE	A_SENSOR Data Offset Error
Default → 0	Offset error not detected on analog safing sensor input
1	Offset error detected on analog safing sensor input

SE	Sequence Error
Default → 0	Sequence error not detected
1	Sequence error detected

SCRAP_SEED (0x59, 0x99)

The SCRAP_SEED command is a read-only command used to request an 8-bit seed value for the safing state machine to enter into Arming mode. Upon reception of this command, the 33789 freezes the free-running seed counter, calculates a key value, and populates the frozen value as the response.

A subsequent command that submits the key value (SCRAP_KEY) will allow the entry into Arming mode.

Table 24. SPI Command, - SCRAP_SEED

SCRAP_SEED (0x59, 0x99)

		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write *	**SI**	0	1	0	1	1	0	0	1	x	x	x	x	x	x	x	x
	SO	0	0	0	P	1	1	1	0	0	0	0	0	0	0	1	0
Read	**SI**	1	0	0	1	1	0	0	1	x	x	x	x	x	x	x	x
	SO	0	1	0	P	1	1	1	0	S7	S6	S5	S4	S3	S2	S1	S0

S7:S0	Function
SEED	8-bit seed value for Scrap Mode entry

* The Write response will always be ERROR with the RE bit set to ‘1’

SCRAP_KEY (0x5A, 0x9A)

The SCRAP_KEY command is a write-only command used to request an 8-bit key value for the Safing state machine to enter into Scrap mode. Upon reception of this command, the 33789 checks the submitted key value against the internally calculated key value, if they are equal, enters Arming mode.

Periodic SCRAP_KEY commands are required for the Safing state machine to remain in Arming mode.

Table 25. SPI Command, - SCRAP_KEY

SCRAP_KEY (0x5A, 0x9A)

		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	**SI**	0	1	0	1	1	0	1	0	K7	K6	K5	K4	K3	K2	K1	K0
	SO	0	0	1	P	1	1	1	0	0	0	0	0	0	0	0	0
Read *	**SI**	1	0	0	1	1	0	1	0	x	x	x	x	x	x	x	x
	SO	0	0	0	P	1	1	1	0	0	0	0	0	0	0	1	0

K7:K0	Function
KEY	8-bit key value for Scrap Mode entry

* The READ response will always be ERROR with the RE bit set to ‘1’

T_UNLOCK (0x4D, 0x8D)

The T_UNLOCK command is a write-only command used to submit an unlock code to the Safing state machine to enable updating of the safing thresholds. The response from the 33789 is a fixed write response with all of data bits set to '0'.

This command is only valid while the Safing state machine is in Start-up mode, and attempting T_UNLOCK commands while in other modes will result in an ERROR response with the RE bit set.

Table 26. SPI Command, - T_UNLOCK

T_UNLOCK (0x4D, 0x8D)

		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	**SI**	0	1	0	0	1	1	0	1	U7	U6	U5	U4	U3	U2	U1	U0
	SO	0	0	1	P	1	1	1	0	0	0	0	0	0	0	0	0
	SO **	0	0	0	P	1	1	1	0	0	0	0	0	0	0	1	0
Read *	**SI**	1	0	0	0	1	1	0	1	x	x	x	x	x	x	x	x
	SO	0	0	0	P	1	1	1	0	0	0	0	0	0	0	1	0

U7:U0	Function
UNLOCK	8-bit key value for safing threshold update

* The Read response will always be ERROR with the RE bit set to ‘1’

** The response to a Write while not in Start-up Mode results in ERROR with RE = 1

SAFE_THx (0x45 ~ 0x4C, 0x85 ~ 0x8C)

The SAFE_THx command is a read/write command used for reading and writing the 8 safing threshold values.

Writing of the safing thresholds can be enabled only if the following conditions are all met:

- The previously received message was a T_UNLOCK command
- The Unlock code in the T_UNLOCK command is correct per definition
- The Safing state machine is in Start-up mode

Reading of the safing thresholds is enabled in any state, and requires no prior unlock message.

A total of eight safing thresholds can be read or written using the eight commands as shown in Table 27.

Table 27. SPI Command, - SAFE_THx

SAFE_THx (0x45~0x4C, 0x85~0x8C)

		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	**SI**	0	1	0	0	A3	A2	A1	A0	DE	T6	T5	T4	T3	T2	T1	T0
	SO	0	0	1	P	1	1	1	0	DE	T6	T5	T4	T3	T2	T1	T0
	SO **	0	0	0	P	1	1	1	0	0	0	0	0	0	0	1	0

Table 27. SPI Command, - SAFE_THx

Read *	**SI**	1	0	0	0	A3	A2	A1	A0	x	x	x	x	x	x	x	x
	SO	0	1	0	P	1	1	1	0	DE	T6	T5	T4	T3	T2	T1	T0

Command	A3	A2	A1	A0	Function
0x45,0x85	0	1	0	1	Safing Threshold 0 Command
0x46,0x86	0	1	1	0	Safing Threshold 1 Command
0x47,0x87	0	1	1	1	Safing Threshold 2 Command
0x48,0x88	1	0	0	0	Safing Threshold 3 Command
0x49,0x89	1	0	0	1	Safing Threshold 4 Command
0x4A,0x8A	1	0	1	0	Safing Threshold 5 Command
0x4B,0x8B	1	0	1	1	Safing Threshold 6 Command
0x4C,0x8C	1	1	0	0	Safing Threshold 7 Command

Default →

DE	Dwell Extension
0	Dwell Extension = 255 ms
1	Dwell Extension = 2 s

T6:T0	Safing Threshold
THRESHOLD	7-bit Safing Threshold data

* Response when [T_UNLOCK register value] = [DE, T6:T0]^0xAD
** Response when any of the following conditions exist (ERROR with RE = 1)
1 Previous SPI command was not T_UNLOCK write
2 [T_UNLOCK register value] <> [DE, T6:T0]^0xAD
3 Not in Start-up Mode

Watchdog Control SPI Commands

WDOG_FEED (0x4E, 0x8E)

The WDOG_FEED command is a write-only command used to service the watchdog.
Only watchdog 'high' or watchdog 'low' is accepted, any other values are ignored by the logic.
The 33789 responds to the command is a fixed write response with all data bits set to '0'.
Any attempted read access to WDOG_FEED will result in an ERROR response with the RE bit set to '1'.

Table 28. SPI Command, - WDOG_FEED

WDOG_FEED (0x4E, 0x8E)

		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	**SI**	0	1	0	0	1	1	1	0	D7	D6	D5	D4	D3	D2	D1	D0
	SO	0	0	1	P	1	1	1	0	0	0	0	0	0	0	0	0

Read *	**SI**	1	0	0	0	1	1	1	0	x	x	x	x	x	x	x	x
	SO	0	0	0	P	1	1	1	0	0	0	0	0	0	0	1	0

* The READ response will always be ERROR with the RE bit set to '1'

D7:D0	Function
0x55	Watchdog feed value LOW
0xAA	Watchdog feed value HIGH
Other	No effect

WDOG_TEST (0x55, 0x95)

The WDOG_TEST command is a write-only command used to put the watchdog state machine into the “wait for refresh failure” state. This can be used to test the watchdog error.

The 33789 responds to the command is a fixed write response with all data bits set to '0'.

Any attempted read access to WDOG_TEST will result in an ERROR response with the RE bit set to '1'.

Table 29. SPI Command, - WDOG_TEST

WDOG_TEST (0x55, 0x95)

		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	**SI**	0	1	0	1	0	1	0	1	x	x	x	x	x	x	x	x
	SO	0	0	1	P	1	1	1	0	0	0	0	0	0	0	0	0
Read *	**SI**	1	0	0	1	0	1	0	0	x	x	x	x	x	x	x	x
	SO	0	0	0	P	1	1	1	0	0	0	0	0	0	0	1	0

* The READ response will always be ERROR with the RE bit set to ‘1’

Other SPI Commands

DIAG_CLR (0x54, 0x94)

The DIAG_CLR command is a write-only command used to force all diagnostic controls to their default state. It affects two latched commands: AI_CONTROL and DCS_CONTROL. The response to the command is a fixed write response with all data bits set to '0'.

Any attempted read access to DIAG_CLR will result in an ERROR response with the RE bit set to '1'.

Table 30. SPI Command, - DIAG_CLR

DIAG_CLR (0x54, 0x94)

		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	**SI**	0	1	0	1	0	1	0	0	x	x	x	x	x	x	x	x
	SO	0	0	1	P	1	1	1	0	0	0	0	0	0	0	0	0
Read *	**SI**	1	0	0	1	0	1	0	0	x	x	x	x	x	x	x	x
	SO	0	0	0	P	1	1	1	0	0	0	0	0	0	0	1	0

* The READ response will always be ERROR with the RE bit set to ‘1’

STATUS (0x56, 0x96)

The STATUS command is a read-only command used to retrieve the C33789 status for diagnostic purposes. The response to the command is a read response containing the current 33789 status.

Attempted write access to STATUS will result in an ERROR response with the RE bit set to '1'.

There are two status bits latched in the 33789 after they are set to their 'active' states. Once the bits are read via a STATUS command, they are set to their 'inactive' states. Only an internal reset and the STATUS read command can set these bits to their 'inactive' states, and immediately after either of them occur, the states are updated to reflect their true status. This is designed to ensure intermittent error conditions can be detected by the system.

The following table defines these bits and their 'active' and 'inactive' states:

Table 31. Two Latched Status

Bit Name	Function	Active State	Inactive State
BOT	Boost Supply Overtemperature	1	0
IGN	IGNSTAT state	0	1

The WDR bit is set whenever the 33789 detects an incorrect watchdog refresh, and can be cleared by a WSM Reset or by a correct watchdog feed.

Table 32. SPI Command - STATUS

STATUS(0x56, 0x96)

		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write *	**SI**	0	1	0	1	0	1	1	0	X	X	X	X	X	X	X	X
	SO	0	0	0	P	1	1	1	0	0	0	0	0	0	0	1	0
Read	**SI**	1	0	0	1	0	1	1	0	X	X	X	X	X	X	X	X
	SO	0	1	0	P	1	1	1	0	SOT	DCOT	BOT	IGN	WU	WS1	WS0	WDR

	SOT	Sync Supply Overtemperature Error
Default →	0	Sync supply overtemperature error not detected
	1	Sync supply overtemperature error detected

	DCOT	DC Sensor Regulator Overtemperature Error
Default →	0	DC sensor regulator overtemperature error not detected
	1	DC sensor regulator overtemperature error detected

	BOT	Boost Supply Overtemperature Error
Default →	0	Boost supply overtemperature error not detected
	1	Boost supply overtemperature error detected

	IGN	IGNSTAT State
	0	V_{PWR} < IGNSTAT threshold V_{BST_UV}
Default →	1	$V_{PWR} \geq$ IGNSTAT threshold V_{BST_UV}

	WU	Wake Pin State
	0	WAKE Pin = 0
Default →	1	WAKE Pin = 1

	Watchdog State		
	WS1	WS0	Function
Default →	**0**	**0**	Watchdog State = “INITIAL”
	0	**1**	Watchdog State = “DRIVE” and ARM_LOCKOUT = 0
	1	**0**	Watchdog State = “DRIVE” and ARM_LOCKOUT = 1
	1	**1**	Watchdog State = “WDOG_TEST” or “WDOG_OVERRIDE”

	WDR	Watchdog Error Status
Default →	0	Previous reset was not caused by watchdog error
	1	Previous reset was caused by watchdog error

* The Write response will always be ERROR with RE bit set to “1”

OUT1_CTL (0x5B, 0x9B) and OUT2_CTL (0x5C, 0x9C)

The OUTx_CTL commands are used to activate/deactivate the general purpose drivers. OUT1_CTL is for driver1 (OUT1_D, OUT1_S), and OUT2_CTL is for driver 2 (OUT2_D, OUT2_S).

They are also used to configure the PWM duty cycle. Setting the duty cycle to 111111b will turn the driver ON without PWM, i.e. 100% duty cycle. Setting the duty cycle to 000000b will deactivate the driver, i.e. 0% duty cycle, thus it is considered as an “OFF” command.

The OUTx_CTL commands also configure the drivers as a Highside Driver or Low-side Driver.

The response from the command indicates the echo of the driver designation, comparator diagnostics information, and shows if a thermal shutdown occurred.

Table 33. SPI Command, - OUT1_CTL

OUT1_CTL (0x5B, 0x9B)

		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	**SI**	0	1	0	1	1	0	1	1	DC5	DC4	DC3	DC2	DC1	DC0	HS	x
	SO	0	0	1	P	1	1	1	0	TS	0	OFF23	OFF13	ON23	ON13	HS	0
Read *	**SI**	1	0	0	1	1	0	1	1	x	x	x	x	x	x	x	x
	SO	0	1	0	P	1	1	1	0	TS	0	OFF23	OFF13	ON23	ON13	HS	0

		DC5:DC0	DC%		DC5:DC0	DC%		DC5:DC0	DC%
Default →	0	000000	OFF	22	010110	34.9	43	101011	68.3
	1	000001	1.6	23	010111	36.5	44	101100	69.8
	2	000010	3.2	24	011000	38.1	45	101101	71.4
	3	000011	4.8	25	011001	39.7	46	101110	73.0
	4	000100	6.3	26	011010	41.3	47	101111	74.6
	5	000101	7.9	27	011011	42.9	48	110000	76.2
	6	000110	9.5	28	011100	44.4	49	110001	77.8
	7	000111	11.1	29	011101	46.0	50	110010	79.4
	8	001000	12.7	30	011110	47.6	51	110011	81.0
	9	001001	14.3	31	011111	49.2	52	110100	82.5
	10	001010	15.9	32	100000	50.8	53	110101	84.1
	11	001011	17.5	33	100001	52.4	54	110110	85.7
	12	001100	19.0	34	100010	54.0	55	110111	87.3
	13	001101	20.6	35	100011	55.6	56	111000	88.9
	14	001110	22.2	36	100100	57.1	57	111001	90.5
	15	001111	23.8	37	100101	58.7	58	111010	92.1
	16	010000	25.4	38	100110	60.3	59	111011	93.7
	17	010001	27.0	39	100111	61.9	60	111100	95.2
	18	010010	28.6	40	101000	63.5	61	111101	96.8
	19	010011	30.2	41	101001	65.1	62	111110	98.4
	20	010100	31.7	42	101010	66.7	63	111111	ON
	21	010101	33.3						

	HS	Driver Configuration Select
Default →	0	LS Driver
	1	HS Driver

	ON13	Driver ON 1/3 V_{PWR} Comparator Result
Default →	0	Diagnosis below threshold
	1	Diagnosis above threshold

	ON23	Driver ON 2/3 V_{PWR} Comparator Result
Default →	0	Diagnosis below threshold
	1	Diagnosis above threshold

	OFF13	Driver OFF 1/3 V_{PWR} Comparator Result
Default →	0	Diagnosis below threshold
	1	Diagnosis above threshold

	OFF23	Driver OFF 2/3 V_{PWR} Comparator Result
Default →	0	Diagnosis below threshold
	1	Diagnosis above threshold

	TS	Thermal Shutdown Indicator
Default →	0	No shutdown has occurred
	1	Thermal shutdown has occurred*

* Status is cleared after OFF command is sent

Table 34. SPI Command, - OUT2_CTL

OUT2_CTL (0x5C, 0x9C)

		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	**SI**	0	1	0	1	1	1	0	0	DC5	DC4	DC3	DC2	DC1	DC0	HS	x
	SO	0	0	1	P	1	1	1	0	TS	0	OFF23	OFF13	ON23	ON13	HS	0
Read *	**SI**	1	0	0	1	1	1	0	0	x	x	x	x	x	x	x	x
	SO	0	1	0	P	1	1	1	0	TS	0	OFF23	OFF13	ON23	ON13	HS	0

		DC5:DC0	DC%		DC5:DC0	DC%		DC5:DC0	DC%
Default →	0	000000	OFF	22	010110	34.9	43	101011	68.3
	1	000001	1.6	23	010111	36.5	44	101100	69.8
	2	000010	3.2	24	011000	38.1	45	101101	71.4
	3	000011	4.8	25	011001	39.7	46	101110	73.0
	4	000100	6.3	26	011010	41.3	47	101111	74.6
	5	000101	7.9	27	011011	42.9	48	110000	76.2
	6	000110	9.5	28	011100	44.4	49	110001	77.8
	7	000111	11.1	29	011101	46.0	50	110010	79.4
	8	001000	12.7	30	011110	47.6	51	110011	81.0
	9	001001	14.3	31	011111	49.2	52	110100	82.5
	10	001010	15.9	32	100000	50.8	53	110101	84.1
	11	001011	17.5	33	100001	52.4	54	110110	85.7
	12	001100	19.0	34	100010	54.0	55	110111	87.3
	13	001101	20.6	35	100011	55.6	56	111000	88.9
	14	001110	22.2	36	100100	57.1	57	111001	90.5
	15	001111	23.8	37	100101	58.7	58	111010	92.1
	16	010000	25.4	38	100110	60.3	59	111011	93.7
	17	010001	27.0	39	100111	61.9	60	111100	95.2
	18	010010	28.6	40	101000	63.5	61	111101	96.8
	19	010011	30.2	41	101001	65.1	62	111110	98.4
	20	010100	31.7	42	101010	66.7	63	111111	ON
	21	010101	33.3						

	HS	Driver Configuration Select
Default →	0	LS Driver
	1	HS Driver

	ON13	Driver ON 1/3 V_{PWR} Comparator Result
Default →	0	Diagnosis below threshold
	1	Diagnosis above threshold

	ON23	Driver ON 2/3 V_{PWR} Comparator Result
Default →	0	Diagnosis below threshold
	1	Diagnosis above threshold

	OFF13	Driver OFF 1/3 V_{PWR} Comparator Result
Default →	0	Diagnosis below threshold
	1	Diagnosis above threshold

	OFF23	Driver OFF 2/3 V_{PWR} Comparator Result
Default →	0	Diagnosis below threshold
	1	Diagnosis above threshold

	TS	Thermal shutdown indicator
Default →	0	No shutdown has occurred
	1	Thermal shutdown has occurred*

* Status is cleared after OFF command is sent

NOP (0x57, 0x97)

The NOP command is used to retrieve the response from a previous command without altering anything within the 33789.

The response for the command is a fixed write response with all data bits set to '0'. Any attempted read access to NOP will result in an ERROR response with the RE bit set to '1'.

Table 35. SPI Command, - NOP

NOP (0x57, 0x97)

		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	**SI**	0	1	0	1	0	1	1	1	x	x	x	x	x	x	x	x
	SO	0	0	1	P	1	1	1	0	0	0	0	0	0	0	0	0
Read *	**SI**	1	0	0	1	0	1	1	1	x	x	x	x	x	x	x	x
	SO	0	0	0	P	1	1	1	0	0	0	0	0	0	0	1	0

* The READ response will always be ERROR with the RE bit set to '1'

Operational Mode SPI Command Table

All of the 33789 operational mode SPI commands are summarized in Table 36.

Table 36. Operational Mode SPI Command Table

Operational Mode SPI Commands																					
ADDR	Command	Function	R/W	Write Data									Read Data								
				15:08	7	6	5	4	3	2	1	0	15:08	7	6	5	4	3	2	1	0
00				40									80								
01				41									81								
02	ESR_DIAG	Enable ESR Test / Read VER-DIAC	R/W	42	x	x	x	x	x	x	x	EN	82	D7	D6	D5	D4	D3	D2	D1	D0
03	LINE_ENABLE	Satellite Channel Enable	R/W	43	x	x	x	x	4LE	3LE	2LE	1LE	83	OT4	OT3	OT2	OT1	4LE	3LE	2LE	1LE
04	SYNC_ENABLE	Satellite Channel Sync Pulse Enable	R/W	44	x	x	x	x	4SE	3SE	2SE	1SE	84	0	0	0	0	4SE	3SE	2SE	1SE
05	SAFE_TH_0	Safing Threshold 0 Value	R/W	45	T7	T6	T5	T4	T3	T2	T1	T0	85	T7	T6	T5	T4	T3	T2	T1	T0
06	SAFE_TH_1	Safing Threshold 1 Value	R/W	46	T7	T6	T5	T4	T3	T2	T1	T0	86	T7	T6	T5	T4	T3	T2	T1	T0
07	SAFE_TH_2	Safing Threshold 2 Value	R/W	47	T7	T6	T5	T4	T3	T2	T1	T0	87	T7	T6	T5	T4	T3	T2	T1	T0
08	SAFE_TH_3	Safing Threshold 3 Value	R/W	48	T7	T6	T5	T4	T3	T2	T1	T0	88	T7	T6	T5	T4	T3	T2	T1	T0
09	SAFE_TH_4	Safing Threshold 4 Value	R/W	49	T7	T6	T5	T4	T3	T2	T1	T0	89	T7	T6	T5	T4	T3	T2	T1	T0
0A	SAFE_TH_5	Safing Threshold 5 Value	R/W	4A	T7	T6	T5	T4	T3	T2	T1	T0	8A	T7	T6	T5	T4	T3	T2	T1	T0
0B	SAFE_TH_6	Safing Threshold 6 Value	R/W	4B	T7	T6	T5	T4	T3	T2	T1	T0	8B	T7	T6	T5	T4	T3	T2	T1	T0
0C	SAFE_TH_7	Safing Threshold 7 Value	R/W	4C	T7	T6	T5	T4	T3	T2	T1	T0	8C	T7	T6	T5	T4	T3	T2	T1	T0
0D	T_UNLOCK	Safing Threshold Unlock	W	4D	U7	U6	U5	U4	U3	U2	U1	U0	8D	0	0	0	0	0	0	1	0
0E	WDOG_FEED	Watchdog Pet Command	W	4E	D7	D6	D5	D4	D3	D2	D1	D0	8E	0	0	0	0	0	0	1	0
0F	LINE_MODE	Satellite Synchronization Select	R/W	4F	x	x	x	x	LM4	LM3	LM2	LM1	8F	0	0	0	0	ILM4	LM3	LM2	LM1
10	LIN_CONFIG	LIN Configuration	R/W	50	x	x	REN	RX01	RXO 0	x	LSR1	LSR0	90	x	x	REN	RX01	RXO 0	x	LSR1	LSR0
11	PS_CONTROL	Energy Reserve Activation Control	R/W	51	x	x	SC	BOE	x	BUE	ERC 1	ERC 0	91	BST	CDF	SC	BOE	0	BUE	ERC 1	ERC 0
12	AI_CONTROL	Analog Interface Control	R/W	52	x	x	x	AIC4	AIC3	AIC2	AIC1	AIC0	92	0	0	0	AIC4	AIC3	AIC2	AIC1	AIC0
13	DCS_CONTROL	DC Sensor Control	R/W	53	SS3	SS2	SS1	SS0	VS1	VS0	x	x	93	SS3	SS2	SS1	SS0	VS1	VS0	0	0
14	DIAG_CLR	Diagnostic Test Clear	W	54	x	x	x	x	x	x	x	x	94	0	0	0	0	0	0	1	0
15	WDOG_TEST	Watchdog Test	W	55	x	x	x	x	x	x	x	x	95	0	0	0	0	0	0	1	0
16	STATUS	33789 Status	R	56	x	x	x	x	x	x	x	x	96	SOT	DCOT	BOT	IGN	WU	WS1	WS0	WDR
17	NOP	No-Op	W	57	x	x	x	x	x	x	x	x	97	0	0	0	0	0	0	1	0
18	SAFE_CTL	ARM/DISARM Output and Mode Control	R/W	58	X	X	X	X	MR1	MR0	TEN	LEV	98	VD3	VD2	VD1	VD0	MD1	MD0	OE	SE
19	SCRAP_SEED	Scrapping Function Seed Request	R	59	x	x	x	x	x	x	x	x	99	S7	S6	S5	S4	S3	S2	S1	S0
1A	SCRAP_KEY	Scrapping Function Key Submit	W	5A	K7	K6	K5	K4	K3	K2	K1	K0	9A	0	0	0	0	0	0	1	0
1B	OUT1_CTL	General Purpose Driver1 Output Control	R/W	5B	DC5	DC4	DC3	DC2	DC1	DC0	HS	x	9B	TS	0	OFF23	OFF13	ON23	ON13	HS	0
1C	OUT2_CTL	General Purpose Driver2 Output Control	R/W	5C	DC5	DC4	DC3	DC2	DC1	DC0	HS	x	9C	TS	0	OFF23	OFF13	ON23	ON13	HS	0
1D				5D									9D								
1E				5E									9E								
1F				5F									9F								

TEST-MODE SPI COMMANDS

The 33789 enters Test mode when the PPT pin is driven high, i.e. 5.0 V, and the test-mode entry command is received.

Table 37. SPI Command, - Test Mode Entry

TESTMODE (ADDR=0xD5, DATA=0x52)

		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEST	SI	1	1	0	1	0	1	0	1	0	1	0	1	0	0	1	0
	SO	0	1	1	0	1	1	1	0	0	0	0	0	0	0	0	0

FAILURE MODE REQUIREMENTS

SPI Error

SPI Error is defined as a condition where the SPI frame format is incorrect.

When a SPI error is detected, the 33789 will respond with an error response message on SO with the 'SPI Error' (SE) bit set. When a SPI error is detected, the 33789 will immediately set SO to a high-impedance state.

SPI errors could be caused by:

•An incorrect number of SPI SCK cycles (>16, or <16 but >0), while $\overline{CS}$ is active

•Too short of an inter-frame time

SPI Request Error

A SPI Request Error is defined as a condition, where the content of a SPI request message is incorrect.

When a SPI Request Error is detected, the 33789 will respond with an error response message on SO with the 'Request Error' (RE) bit set.

SPI request errors could be caused by:

•An undefined command (e.g. incorrect address in bits [12:8])

•An illegal operation for a defined command (e.g. attempting to write when receiving a read-only command)

•An attempted command request while in the incorrect state for the command (e.g. T_UNLOCK command while not in Start-up mode)

SAFING

SAFING CONCEPT

The safing concept involves the utilization of logic independence of the MCU to monitor both on-board and remote satellite sensors, to determine if a sufficient inertial activity is present to warrant deployment Arming of the system.

While in the Safing state, on the rising edge of the SATSYNC input, the MCU will request samples from all digital sensing sources, in a predetermined sequence with SPI commands. If sensor data in response is valid, the safing logic will compare it to the appropriate safing threshold. The threshold was arranged based on the expected sequence of sampling. The safing thresholds of the 33789 have been assigned to pairs of sequence numbers as shown in Table 38.

Table 38. Sequence to Safing Threshold Mapping

Sequence Identifier	Safing Threshold
0000	Threshold 0
0001	
0010	Threshold 1
0011	
0100	Threshold 2
0101	
0110	Threshold 3
0111	
1000	Threshold 4
1001	
1010	Threshold 5
1011	
1100	Threshold 6
1101	
1110	Threshold 7

If three consecutive samples from the same sensor exceed the threshold, an internal safing signal is set. This safing signal activation will assert the Arming outputs (ARM and $\overline{\text{DISARM}}$) for the duration of the signal, plus a Dwell Extension period after it is cleared. The Dwell Extension period is defined either 255 ms or 2.0 seconds depending on the safing condition.

To prevent a loss of synchronization between the sampling order and the desired threshold (e.g. a sensor fails to respond), an internal Sequence Counter is designated to maintain the increments each time a sensor's data response is received, whether it includes valid data or not. This Sequence Counter is reset at each rising edge of Satsync to re-synchronize with the next sampling period. If a sequence ID in the SPI request/response (SQ2:SQ0) does not match the corresponding value in the Sequence Counter, the 33789 will immediately set a Sequence Error bit and disable safing on digital sensors for the rest of the sample period, until the next Satsync rising edge.

Another counter, Valid Data Counter, which is also reset at each rising edge of Satsync, is used to determine how many SPI data frames containing valid sensor data have been received in each sampling period. The Valid Data Counter is readable via the SPI for the MCU.

SAFING STATE MACHINE

The Safing State Machine (SSM) is used to control the safing function and provide diagnostics. The control logic of the 33789 Safing State Machine can be described in Figure 51. This logic provides a high level of robustness to the system architecture by restricting the primary safing function while diagnostics are performed. It facilitates key-on and run-time diagnostic tests. It also provides a means of activating safing for the scrap function, which would be useful to safely activate the Arming outputs for disposal of pyrotechnic devices at the end of vehicle life.

The 33789 Safing State Machine supports five mutually exclusive modes of operation:

Start-up Mode

The Start-up mode is entered upon the release of SSM Reset.

While in Start-up mode, sampling sensor data and activating the ARM/$\overline{\text{DISARM}}$ outputs are inhibited.

Updating the safing thresholds is permitted only while in Start-up mode.

When the watchdog service begins (upon the first successful watchdog feed), the SSM enters the Diagnostic mode.

Diagnostic Mode

When the Diagnostic mode is entered, testing of the ARM and $\overline{\text{DISARM}}$ outputs are enabled, which allows the MCU to activate the signals both high or both low for testing the interface. It is not possible to set both of the outputs in their active states (ARM=1 and $\overline{\text{DISARM}}$=0) in this mode.

The SSM remains in this mode until a SAFE_CTL SPI command is received for either a Safing mode transition or a Scrap mode transition.

Safing Mode

Upon reception of the SAFE_CTL command with the CTL field set to 'Safing' while in Diagnostic mode, the SSM enters Safing mode.

Safing mode is the primary run-time mode for normal operation. The safing logic can perform all of the safing functions, including monitoring sensor data and setting the ARM/$\overline{\text{DISARM}}$ signals for Arming output while in this state.

The only means of exiting Safing mode is the assertion of the SSM Reset signal.

Scrap Mode

If the MCU sends the 33789 a SAFE_CTL command with the CTL field set to 'Scrap', while the SSM is in Diagnostic mode, it will force the SSM enter into Scrap mode.

Once entered into Scrap mode, the SSM stops monitoring the sensor interface, and the safing compare logic is disabled.

From Scrap mode, the SSM can be moved into Arming mode only if the MCU initiates the transition. The only way to move it back from Scrap mode to Start-up mode is through an SSM Reset.

Arming Mode

While in Arming Mode, the safing outputs are asserted (ARM = 1 and $\overline{\text{DISARM}}$ = 0) to enable firing of squibs.

In order to protect from an inadvertent enter into Arming mode, and to prevent undesired activation of the safing signal, a handshake is used to control entering into and exiting out of Arming mode.

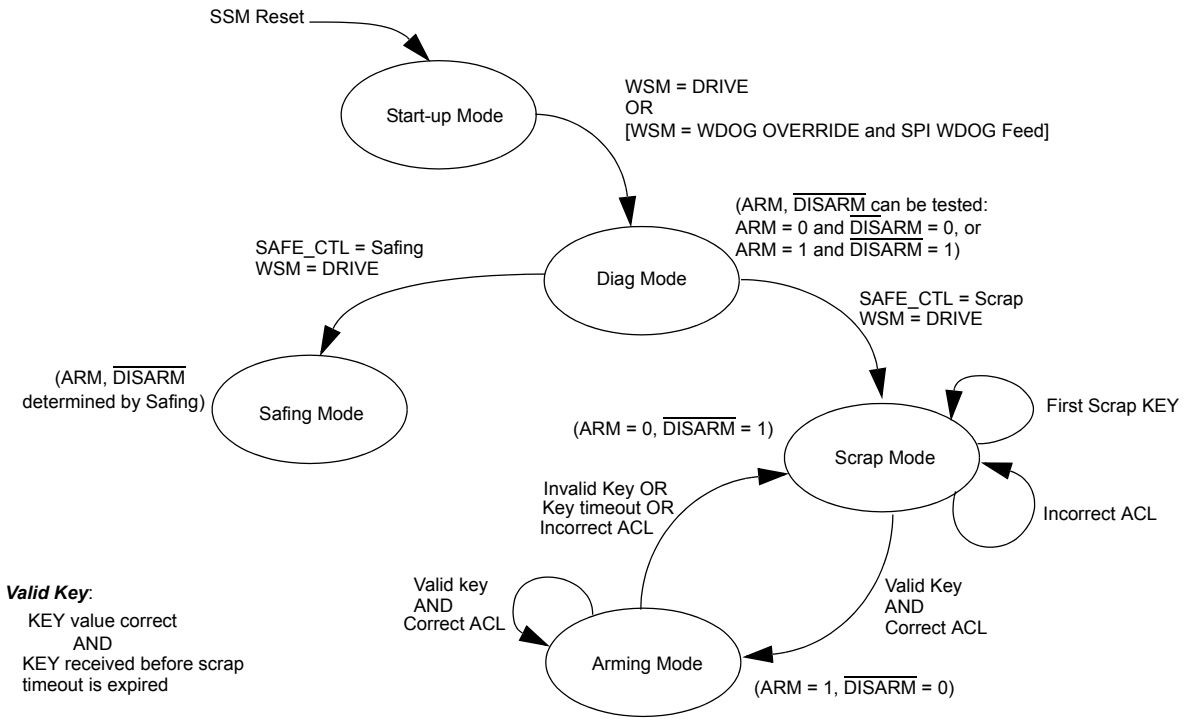


Figure 51. Safing State Diagram

The handshake sequence for activating the Arming outputs is illustrated in Figures 52. The strategy is:

The 33789 uses a free-running 8-bit counter to generate a seed value;

- The MCU read the seed value with the SCRAP_SEED command;
  - The MCU uses the seed value to generate an 8-bit key;
    - The MCU submits the key value with the SCRAP_KEY command;
- The 33789 freezes the seed value read by the MCU and computes its own key;
  - Compares two key values at the 33789;
  - The 33789 receives the ACL signal at the SCRAP pin from the MCU;
    - If two key values match each other,
      AND
      the ACL signal is valid,

Transition into Arming mode

To remain in Arming mode, the MCU must periodically refresh the 33789 with SCRAP_KEY command containing correct key value, and the 33789 must continuously receive a valid ACL signal at the SCRAP pin from either the MCU or another external device, depending on the application. This must occur before the scrap timeout timer expires (in about 600 µs).

If the periodic scrap key is incorrect, or not been received before timeout, or there is no valid ACL signal at the SCRAP pin, the SSM reverts back to the Scrap mode, and the Arming outputs are deactivated.

The scrap key is derived from the seed value using a simple logic inversion on the even-numbered bit (0, 2, 4, 6), - equivalent to a bit-wise XOR of the seed value with 0x55, logically.

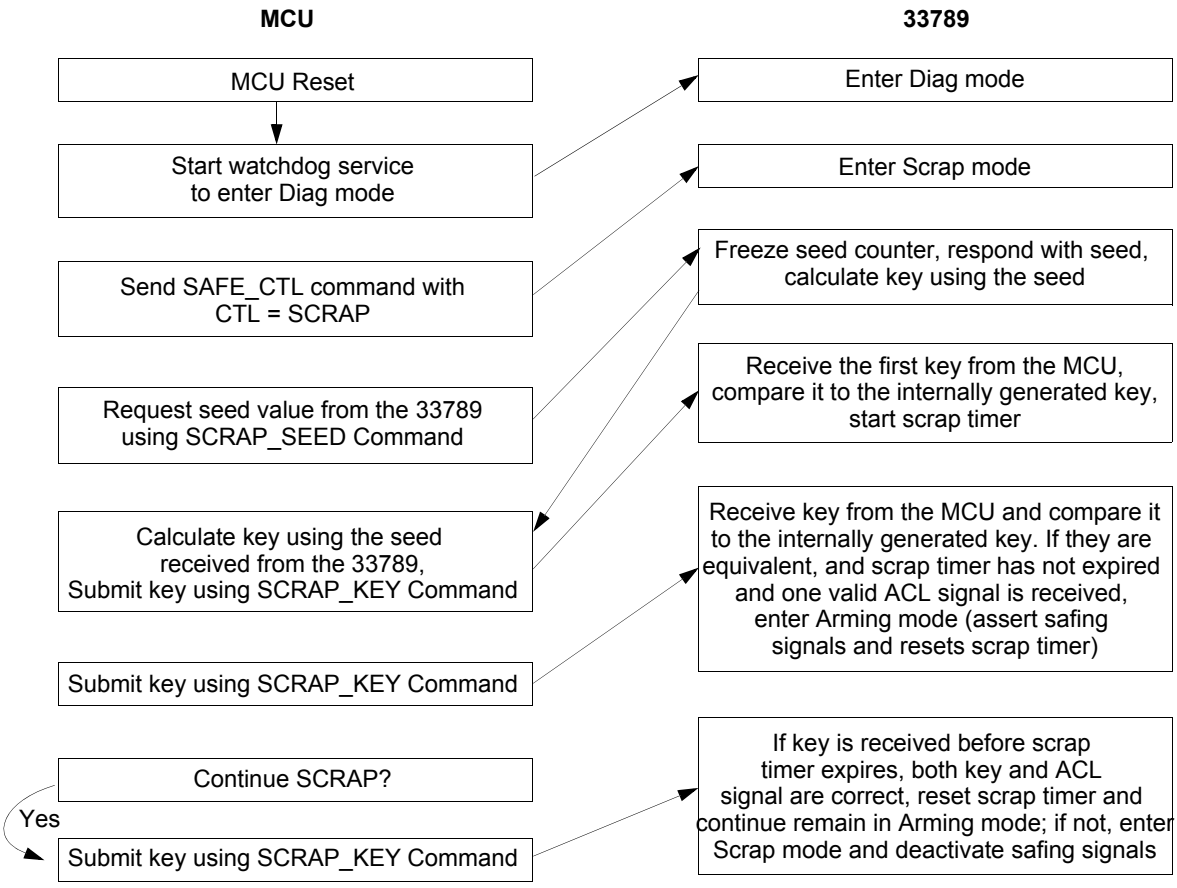


Figure 52. Arming Mode Handshake

SPI MONITOR AND DECODER

The SPI Monitor block extracts valid sensor data from the SPI sensor data messages read by the MCU to be able to determine the safing status. All of the safing related sensor data received by the safing block, including the satellite sensor data from the PSI5 interface, analog sensor data from A_SENSOR input, and other digital sensor data from local ECU sensors, are monitored for correctness of data and sequence by the SPI monitor decoder, and will be further used in the safing logic processing.

The SPI monitor is capable of receiving sensor data through the SPI interface from up to 4 sources with 4 specifically assigned chip select signals:

- $\overline{CS}$: Dedicated to the PSI5 satellite channels
- $\overline{CS\_A}$: Intended for an on-board high-g X, or X/Y accelerometer
- $\overline{CS\_B}$: Intended for an on-board high-g Y, or expansion of satellite receiver
- $\overline{CS\_C}$: Intended for an expansion of satellite receiver

While the Safing State Machine is in Safing mode, the SPI Monitor listens to all of the SPI SO responses from satellite receivers and on-board sensors corresponding to sensor data request from the MCU, and uses predefined sensor message format and data validation criteria to check the messages. Functions of the SPI Monitor results in generation of three important internal signals within the safing block:

Sensor Message Detection: - generate SENS_MSG

When the SENS_MSG signal is activated, it indicates a valid sensor message is received and the Sequence Counter is not frozen (when frozen, the counter value equal to '1110').

The SPI Monitor needs to qualify the SPI message frame first by “Frame Check”:

1. SPI data is captured when the chip select is low;
2. The first 16 bits of SO data are captured regardless of the total number of SCK edges detected;
3. A valid frame is detected when the chip select goes high and at least 16 SCK edges have been detected;
4. Frames fewer than 16 SCK edges are ignored;

5. If more than one chip select is active at any time during an SPI frame, the SPI frame shall not be validated.

All of the necessary conditions to generate SENS_MSG can be found in Figure 53.

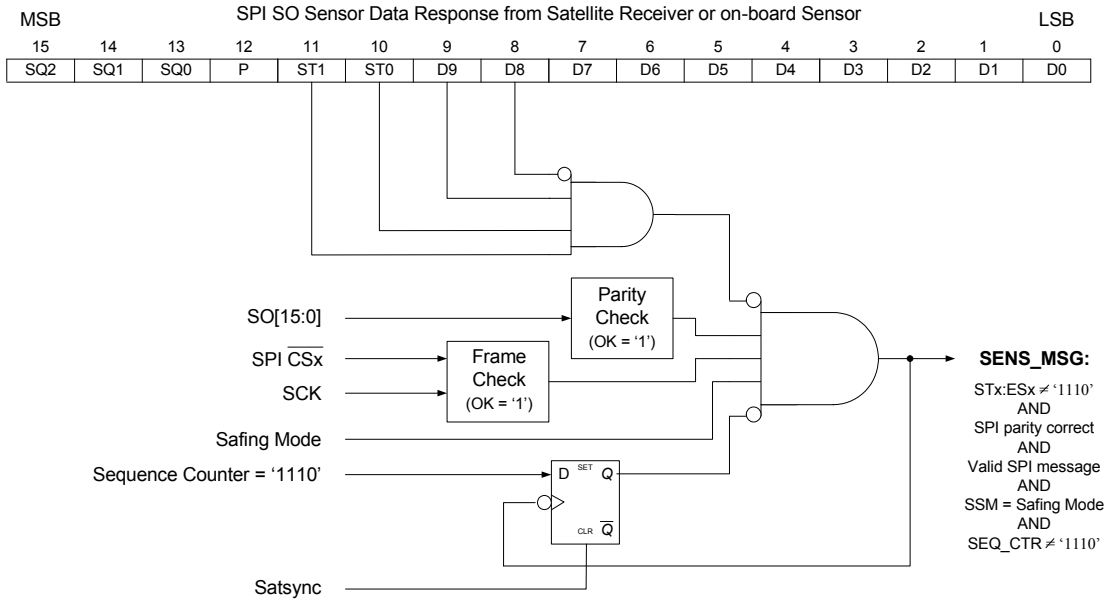


Figure 53. SPI Decode Logic for SENS_MSG Signal

Sequence Error Detection: - Generate SEQ_ERROR

When a valid sensor message is detected (SENS_MSG = 1), the SPI Monitor compares the SQ2:SQ0 field (sequence number) of the SPI response message with the expected sequence number determined by the Sequence Counter. If there is a mismatch, the SEQ_ERROR signal is asserted, as shown in Figure 54.

Activation of SEQ_ERROR will set the Sequence Error bit of the SPI SAFE_CTL command register (SE = 1), and disable the safing comparison for the affected sensor and all subsequent sensors for the rest of the current sampling period, until the next Satsync rising edge.

While in Safing mode, the MCU must ensure that the sampling sequence is maintained for every sampling period, regardless of the state of sensors, to prevent a sequence error from disabling safing on the remaining channels in the sequence. Therefore, if there is a sensor disabled, the MCU must continue requesting data from the sensor to maintain the sampling sequence. However, it may load a "dummy" request to fill the SQ2:SQ0 field of the response message.

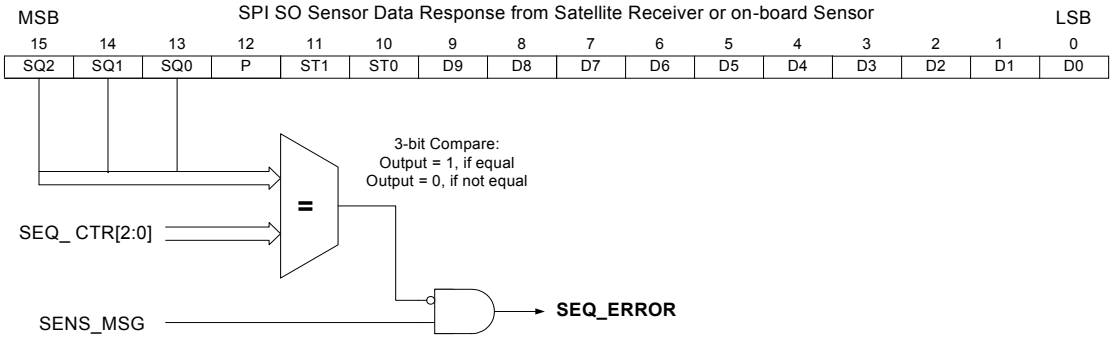


Figure 54. Sequence Error Detection Logic

Sensor Data Validation: - generate DAT_VALID

The DAT_VAL signal is activated whenever a SPI sensor data response message containing valid sensor data is received while in Safing mode.

All of following conditions must be met to validate the sensor data:

1. ST1:ST0 field of the SO response must be '01', - to confirm this is a sensor data;
2. The SENS_MSG signal must be active, - to confirm it has a qualified message frame;

3. The data must be in the valid value range:
   - Data (D9:D0) within -480_{DEC} ~ $+480_{DEC}$ inclusive if the sequence counter value >2
   - Data (D9:D0) within -512_{DEC} ~ $+511_{DEC}$ inclusive if the sequence counter value <3
4. The Sequence Error (SE) bit is clear.

The SPI decode logic to validate sensor data can be illustrated in Figure 55.

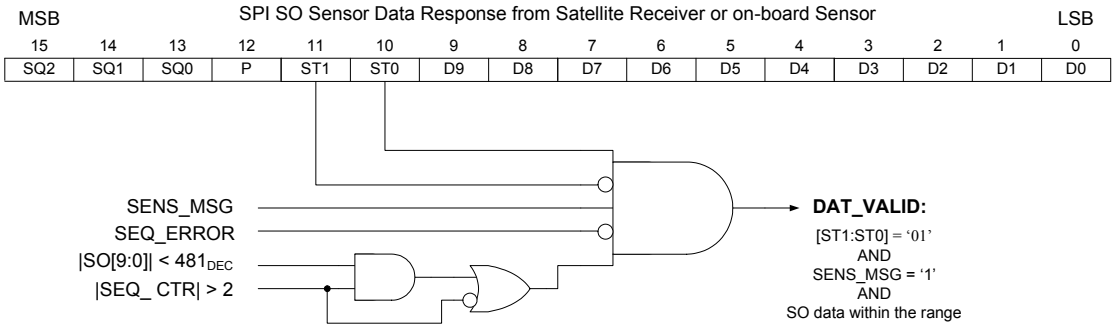


Figure 55. SPI Decode Logic for DAT_VAL Signal

SAFING CONTROL COUNTERS

There are two 4-bit Safing control counters in the Safing logic block.

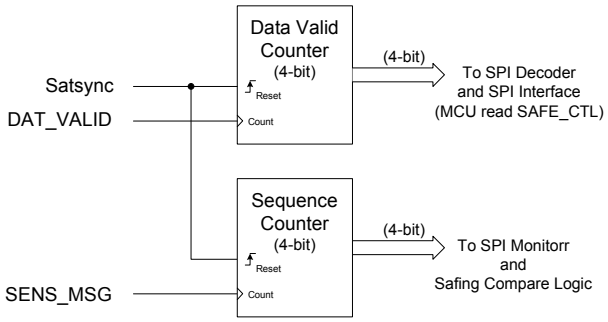


Figure 56. Safing Control Counters

Sequence Counter

The Sequence Counter increments each time a valid sensor SPI message is received, regardless of whether it contains valid data, an error message, or self-test data. It is incrementally based on the SENS_MSG signal from the SPI Monitor block, and it resets on each Satsync rising edge.

Due to the control of SENS_MSG, the Sequence Counter will never advance beyond '1110'. In order to correlate correctly with the received SPI messages, the Sequence Counter is reset to a value of '1111', so the first sample received causes it to increment to '0000'.

This counter is not read nor write accessible via the SPI interface. The counter contents are used by the SPI Monitor logic to detect sequence errors, and by the Safing Compare Logic, to correlate sensor samples to the appropriate safing threshold for comparison.

Data Valid Counter

The Data Valid Counter increments each time a sensor SPI message is received that contains valid sensor data (ST1:ST0 = '01'). It is incrementally based on the DAT_VALID signal from the SPI Monitor block, and resets on each Satsync rising edge.

Due to the control of SENS_MSG, the Data Valid Counter will freeze once the Sequence Counter reaches a value of '1110'. The Data Valid Counter is reset to a value of '0000' on each Satsync rising edge to accurately reflect the number of samples received.

The count value can be read by the MCU using the SPI SAFE_CTL command to determine whether all digital sensor samples have been received by safing logic.

SAFING THRESHOLD LOGIC

The Safing Threshold logic ensures the safing comparison threshold value can be reliably written and read by the MCU.

The 33789 is capable of storing eight 8-bit safing thresholds. The MSB of threshold data is used to indicate the Dwell Extension pulse width (either 255 ms or 2.0 s).

The thresholds are correlated to the sampling sequence number pair, as shown in Figure 57.

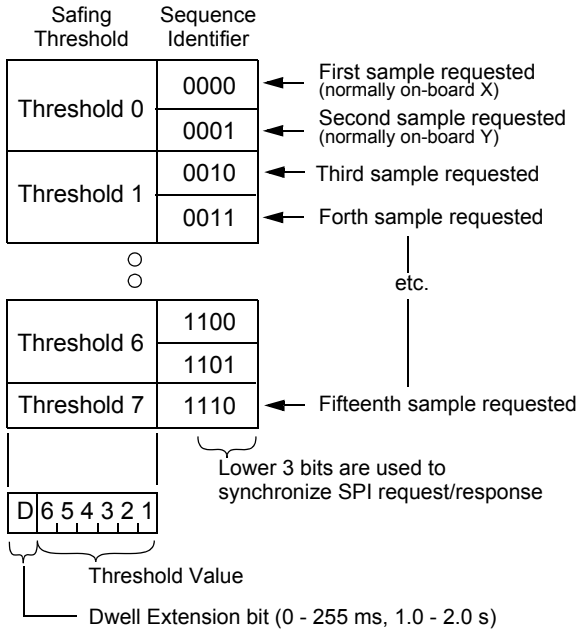


Figure 57. Safing Threshold Storage

Upon the Safing state machine reset, all of the threshold values are rest to default values. Applications may choose to use these default values or reprogram them.

The default safing thresholds are listed in Table 39:

Table 39. Default Safing Thresholds

Sequence # (Sampling Order)	Sequence ID	Desired 10-bit Threshold Value (dec)	Desired 10-bit Threshold Value (hex)	Dwell Extension	Targeted Sensor Type	Targeted Sensor Threshold	Encoded 8-bit Threshold (hex)
0	0000	27	1B	255 ms	On-board 50 g X	2.8 g	0D
1	0001				On-board 50 g Y		
2	0010	42	2A	2.0 s	Digital ARS	30°/s	95
3	0011				Analog ARS		
4	0100	16	10	255 ms	Satellite 240 g	10 g	08
5	0101						
6	0110	16	10	255 ms	Satellite 240 g	10 g	08
7	0111						
8	1000	16	10	255 ms	Satellite pressure	7.8%o	08
9	1001						
10	1010	16	10	255 ms	Satellite 240 g	10 g	08
11	1011						
12	1100	8	8	255 ms	Satellite 480 g	10 g	04
13	1101						
14	1110	8	8	255 ms	Satellite 480 g	10 g	04

SPI Read / Write Access to Safing Thresholds

The MCU has read and write access to the safing thresholds via the SPI interface, using eight SPI SAFE_THx commands.

The application specific safing thresholds are allowed to be written to the safing logic only when the 33789 in Start-up mode, to ensure the Arming outputs are disabled during the threshold updates and to prevent inadvertent modification of the thresholds during Safing or Scrap mode.

As additional protection against an undesired safing threshold update, writing an “unlock key” into the T_UNLOCK register prior to writing thresholds value through the SAFE_THx command is required. The T_UNLOCK command must immediately precede the SAFE_THx command to correctly update the threshold values.

The unlock key value is calculated by bit-wise XORing the threshold value with the value '0xAD'.

To successfully update the safing threshold registers, all of the following conditions must be met:

•The 33789 is in Start-up mode

•The previous SPI command must be a T_UNLOCK write command

•The SAFE_THx command data field must be equal to the unlock code from the T_UNLOCK command XORed with 0xAD:

•SAFE_THx(data) = [T_UNLOCK(data)] ^ 0xAD

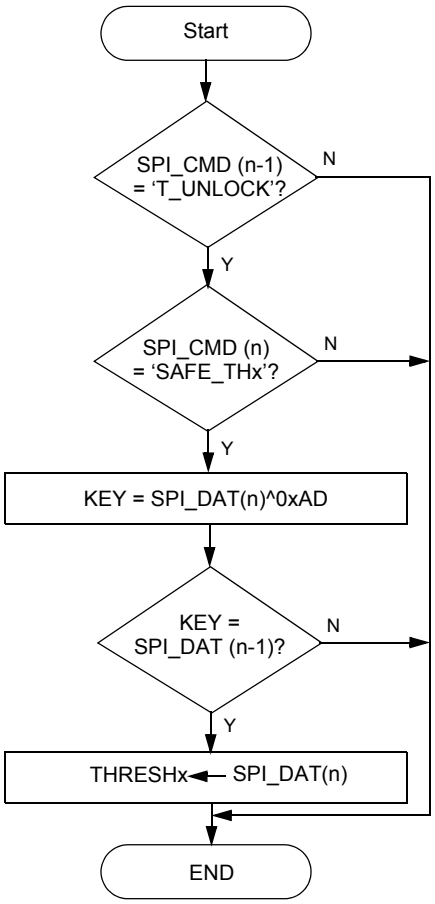


Figure 58. Safing Threshold Write Flowchart

Safing Threshold Encoding

Since the safing comparison involves the 8-bit threshold and a 9-bit magnitude, the desired threshold value must be divided by two (shift right by one bit) before being stored in the 33789. An additional MS '0 ' bit is then appended to the threshold value used for comparison.

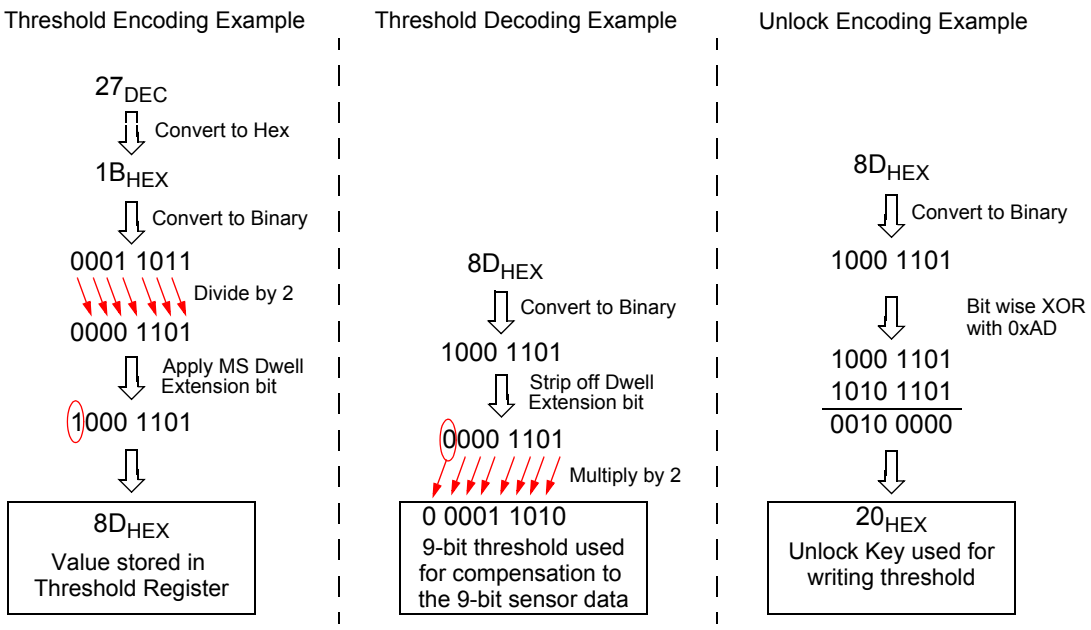


Figure 59. Safing Threshold and Unlock Key Encoding

SAFING COMPARISON LOGIC

Safing Comparison Enable

The sensor data comparison is conducted under conditions of:

- The SPI message frames are received
- The sensor data is valid
- There is no Sequence Error

Figure 60. Safing Comparison Enable Logic

Safing Magnitude Comparison

All sensor data fed into the Safing Comparison logic is 9-bit, zero-adjusted, positive data, therefore the comparison involves a simple digital magnitude comparison between two 9-bit data.

The sensor data in the SPI response message frame uses a 10-bit sensor data format. It must be converted into 9-bit magnitude data for the comparison with the safing threshold.

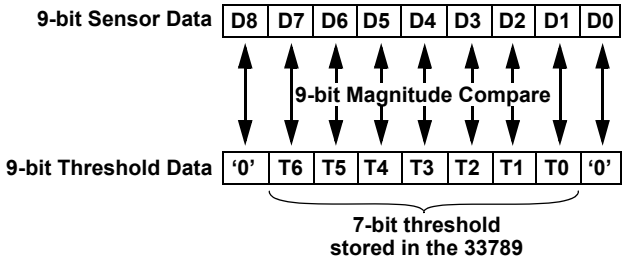


Figure 61. Magnitude Comparison

Sample Counters

The sensor logic block consists of 16 2-bit Sample Counters to facilitate multi-sample evaluation of sensor data for safing.

Each counter corresponds to a specific Sequence ID in the 33789, and is incremented each time when the received sample exceeds its associated safing threshold. If there are three consecutive samples from a same sensor exceed the threshold (Sample Counter = '11'b), the Arming outputs are asserted (ARM = 1, $\overline{\text{DISARM}}$ = 0).

Once the counters reach their maximum value, they are not incremented further. The sample counters are reset upon Safing State Machine Reset, or whenever the corresponding data falls bellow its threshold.

DWELL EXTENSION

While in Safing mode, whenever the Arming signals is activated, Dwell Extension is used to extend the assertion time.

The Dwell Extension is disabled while in Diagnostic mode, - the Arming outputs could be activated for test.

While in Safing mode, If any of the 16 Sample Counters reach to their maximum value('11'b), the Arming outputs are asserted. They will be continuously asserted as long as any of the Sample Counters contain '11'b. and additionally, plus the established Dwell Extension time, after all Sample Counters contain values less than '11'b.

The Dwell Extension time is determined by the MSB (bit 7) of the safing threshold in which safing was met (i.e. the data exceeded the threshold for three consecutive samples). The Dwell Extension time can be either 255 ms or 2.0 s, based on this bit assigned with the safing threshold setting.

If safing is met on more than one Sequence ID with threshold(s) containing both 255 ms and 2.0 s Dwell Extension time choices, the longer (2.0 s) Dwell Extension is used for the safing outputs, which means the longer Dwell Extension time will override the shorter one.

An example of Sample Counter, Dwell Extension time and Arming output is shown in Figure 62.

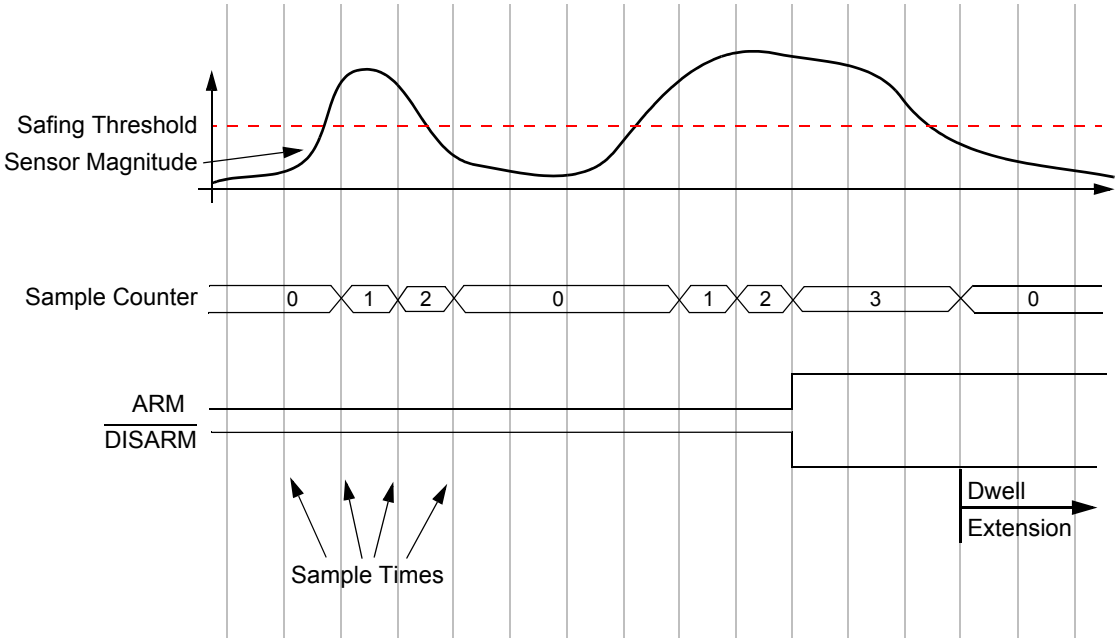


Figure 62. Example of Safing Dwell Extension

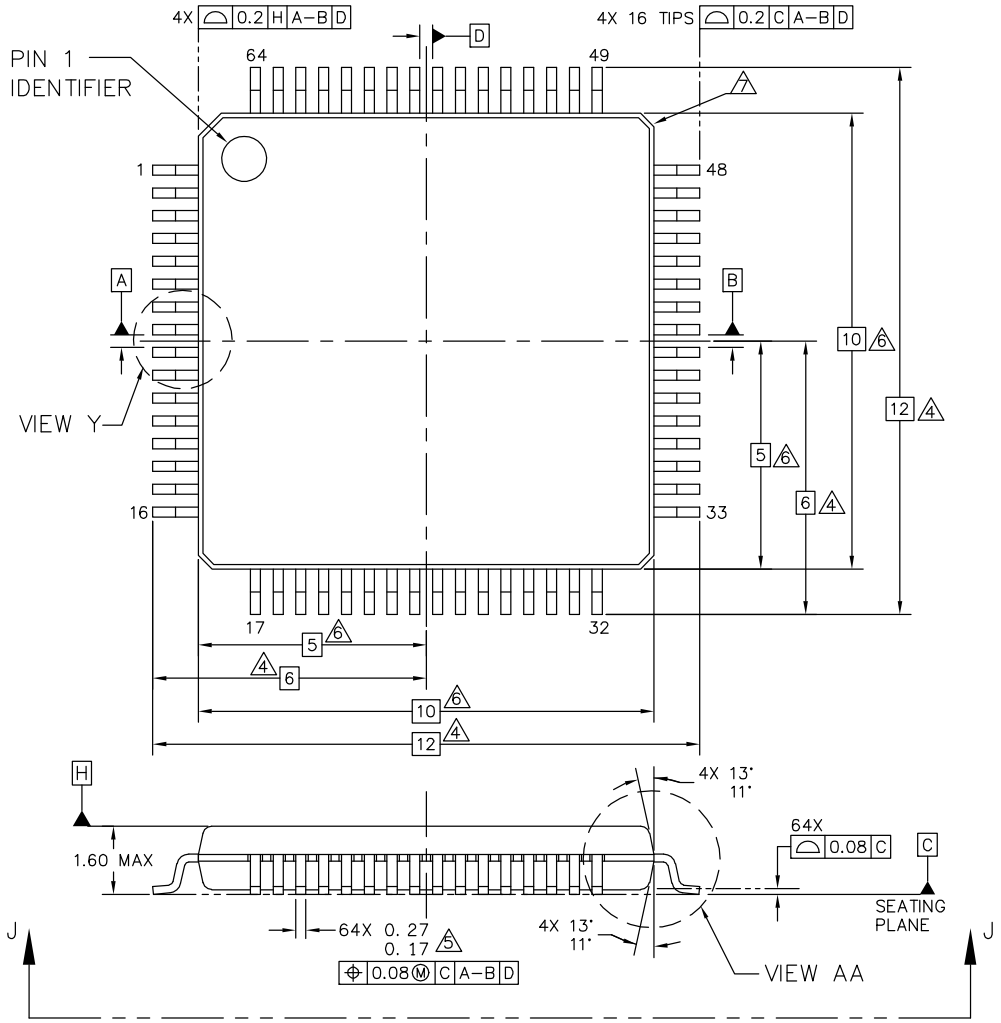
PACKAGING

PACKAGE MECHANICAL DIMENSIONS

Package dimensions are provided in package drawings. To find the most current package outline drawing, go to www.freescale.com and perform a keyword search for the drawing's document number.

Table 40. Packaging Information

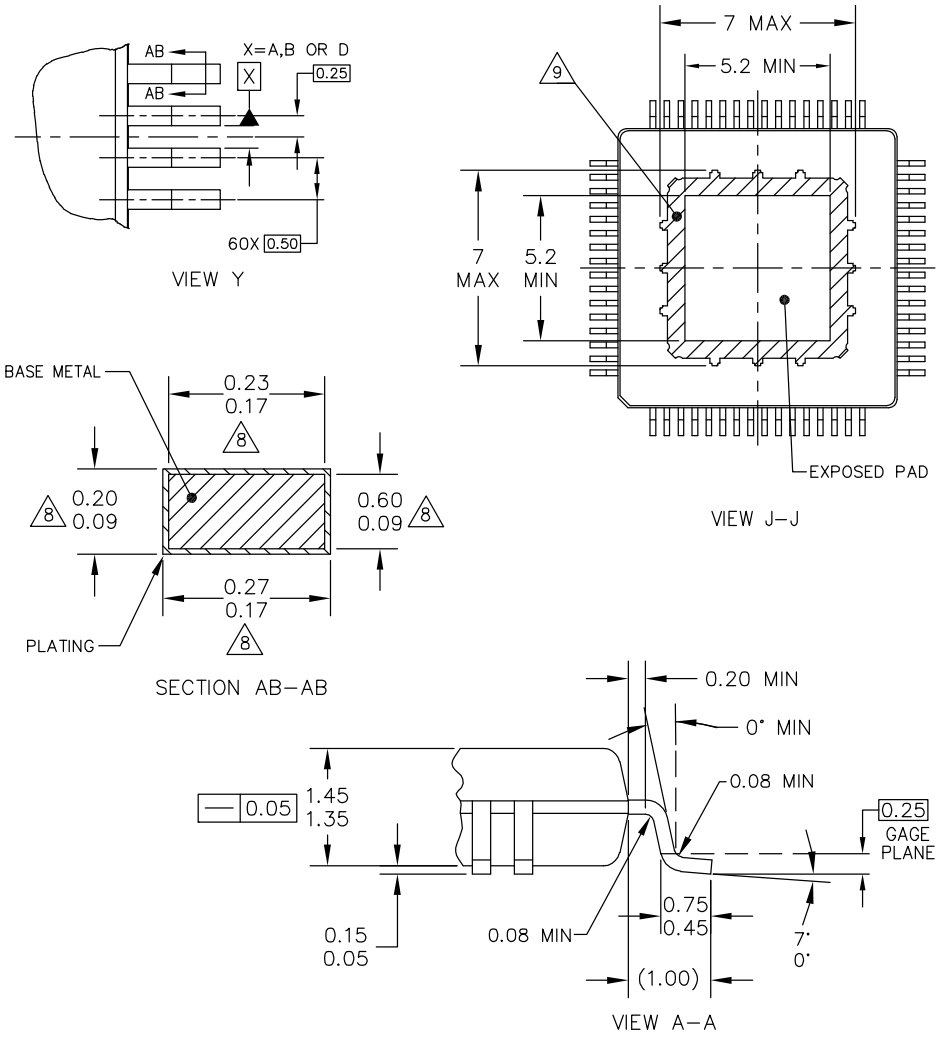
Package	Suffix	Package Outline Drawing Number
64-Pin LQFP-EP	AFE	98ASA10763D



MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASA10763D	REV: A
64 LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, 6.1 x 6.1 EXPOSED PAD	CASE NUMBER: 1899–02	14 DEC 2006
	STANDARD: JEDEC MS–026 BCD	

33789



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TITLE: 64 LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, 6.1 x 6.1 EXPOSED PAD	DOCUMENT NO: 98ASA10763D	REV: A
	CASE NUMBER: 1899-02	14 DEC 2006
	STANDARD: JEDEC MS-026 BCD	

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM DIMENSION BY MORE THAN 0.08 MM. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 MM.
6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE. DIMENSIONS ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 MM AND 0.25 MM FROM THE LEAD TIP.
9. HATCHED AREA TO BE KEEP OUT ZONE FOR PCB ROUTING.
10. LEADFRAME PART NUMBER APPLIED IS 17ASS23232W610.

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASA10763D	REV: A
64 LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, 6.1 x 6.1 EXPOSED PAD	CASE NUMBER: 1899-02	14 DEC 2006
	STANDARD: JEDEC MS-026 BCD	

REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
1.0	2/2011	• Initial Release
2.0	12/2011	• Revised ESD Capability. Took Human Body Model - JESD22/A114(3) from 6.0 kV to 2.0 kV • Redefined INx Active Pull-down Current. Changed Max. from -50 to -30 µA • Added First Dominant bit Delay
3.0	4/2012	• Updated datasheet to include SafeAssure branding and technology identification.
4.0	9/2014	• Removed MCZ33789AE from the ordering information • Added MCZ33789BAE to the ordering information • Updated IERSW_LEAK parameter in Table 5 • Deleted IVDD parameter in Table 5 • Updated VCC_UV parameter in Table 5 • Updated ISAT_TH_OFS parameter Table 5 • Updated ISAT_TH_HYST parameter Table 5 • Corrected the parameter label for $f_{BST/BUCK}$ in Table 5 • Added Note 16 • Added FSEL bit in LIN_CONFIG register in Table 17 • Added new table to explain FSEL bit function in Table 17 • Corrected Figure 37 • Corrected Table 18 • Updated format and back page.

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