

NP90N04VLK

40 V – 90 A – N-channel Power MOS FET Application: Automotive

Data Sheet

Description

The NP90N04VLK is N-channel MOS Field Effect Transistors designed for high current switching applications.

Features

• Super low on-state resistance

 $R_{DS(on)} = 2.8 \text{ m}\Omega \text{ MAX.} (V_{GS} = 10 \text{ V}, I_D = 45 \text{ A})$

- Low C_{iss} : $C_{iss} = 3800 \text{ pF TYP}$. ($V_{DS} = 25 \text{ V}$)
- Logic level drive type
- Designed for automotive application and AEC-Q101 qualified

Ordering Information

Part No.	Lead Plating	Pac	Package	
NP90N04VLK-E1-AY *1	Pure Sn (Tin)	Tape 2500 p/reel	Taping (E1 type)	TO-252 (MP-3ZP)
NP90N04VLK-E2-AY *1			Taping (E2 type)	

Note: *1 Pb-free (This product does not contain Pb in the external electrode)

Absolute Maximum Ratings $(T_A = 25^{\circ}C)$

Item	Symbol	Ratings	Unit
Drain to Source Voltage (V _{GS} = 0 V)	VDSS	40	V
Gate to Source Voltage (V _{DS} = 0 V)	V _{GSS}	±20	V
Drain Current (DC) ($T_C = 25^{\circ}C$)	ID(DC)	±90	A
Drain Current (pulse) *1*3	I _{D(pulse)}	±360	A
Total Power Dissipation (Tc = 25°C)	P _{T1}	147	W
Total Power Dissipation (T _A = 25°C)	P _{T2}	1.2	W
Channel Temperature	T _{ch}	175	°C
Storage Temperature	T _{stg}	–55 to +175	°C
Repetitive Avalanche Current *2*3	I _{AR}	37	A
Repetitive Avalanche Energy *2*3	Ear	136	mJ

Thermal Resistance

Channel to Case Thermal Resistance	$R_{th(ch-C)}$ *3	1.02	°C/W
Channel to Ambient Thermal Resistance	Rth(ch-A) *3	125	°C/W

Notes: *1 T_C = 25°C, $P_W \leq$ 10 $\mu s, \, Duty \, Cycle \leq$ 1%

- *2 R_{G} = 25 $\Omega,\,V_{GS}$ = 20 V \rightarrow 0 V
- *3. Not subject of production test. Verified by design/characterization.



Item	Symbol	MIN.	TYP.	MAX.	Unit	Test Conditions	
Zero Gate Voltage Drain Current	I _{DSS}	_		1	μA	$V_{DS} = 40 \ V, \ V_{GS} = 0 \ V$	
Gate Leakage Current	I _{GSS}	—	_	±10	μA	$V_{GS}=\pm 20~V,~V_{DS}=0~V$	
Gate to Source Threshold Voltage	V _{GS(th)}	1.5	1.8	2.5	V	$V_{DS}=V_{GS},\ I_{D}=250\ \mu A$	
Forward Transfer Admittance *1	y fs	39	78	_	S	$V_{DS} = 5 V, I_D = 45 A$	
Drain to Source On-state Resistance *1	R _{DS(on)1}	—	2.35	2.80	mΩ	$V_{GS} = 10 \text{ V}, \text{ I}_{D} = 45 \text{ A}$	
	R _{DS(on)2}	—	3.00	6.00	mΩ	$V_{GS} = 4.5 \text{ V}, I_D = 23 \text{ A}$	
Input Capacitance *2	Ciss	_	3800	5700	pF	V _{DS} = 25 V	
Output Capacitance *2	Coss	_	530	800	pF	$V_{GS} = 0 V$	
Reverse Transfer Capacitance *2	Crss	_	200	360	pF	f = 1 MHz	
Turn-on Delay Time *2	t _{d(on)}	_	18	40	ns	$V_{DD} = 20 V, I_D = 45 A$	
Rise Time *2	tr	_	8	20	ns	$V_{GS} = 10 V$	
Turn-off Delay Time *2	t _{d(off)}	_	71	142	ns	$R_G = 0 \Omega$	
Fall Time *2	tr	_	9	23	ns		
Total Gate Charge *2	Q _G	_	68	102	nC	V _{DD} = 32 V	
Gate to Source Charge	Q _{GS}	_	17	_	nC	$V_{GS} = 10 V$	
Gate to Drain Charge	Q _{GD}		11		nC	I _D = 90 A	
Body Diode Forward Voltage *1	VF(S-D)	—	0.9	1.5	V	$I_F = 90 \text{ A}, V_{GS} = 0 \text{ V}$	
Reverse Recovery Time	t _{rr}	_	43		ns	$I_F = 90 \text{ A}, V_{GS} = 0 \text{ V}$	
Reverse Recovery Charge	Qrr		59	_	nC	di/dt = 100 A/µs	

Electrical Characteristics (T_A = 25°C)

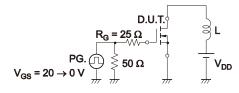
Note: *1 Pulsed test

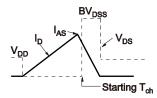
Note: *2 Not subject of production test. Verified by design/characterization.

TEST CIRCUIT 1 AVALANCHE CAPABILITY

TEST CIRCUIT 2 SWITCHING TIME

D.U.T.

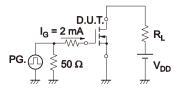


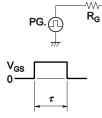


TEST CIRCUIT 3 GATE CHARGE

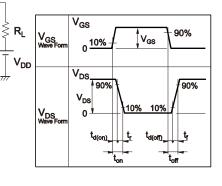
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May 24, 2018



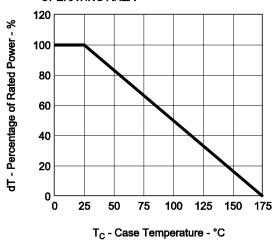


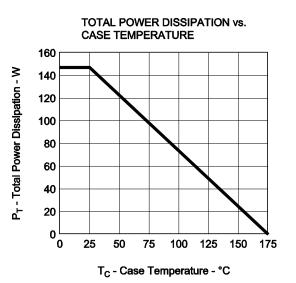




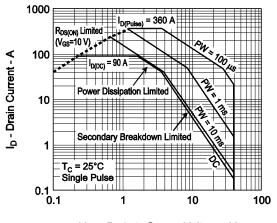
Typical Characteristics $(T_A = 25^{\circ}C)$

DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



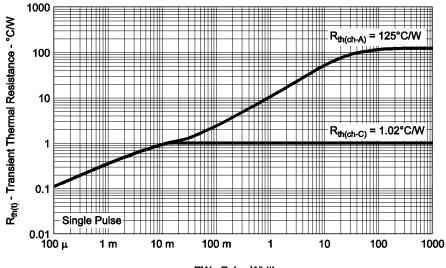




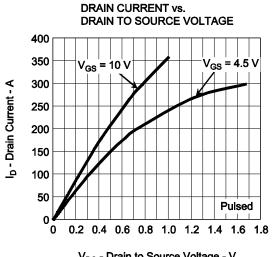




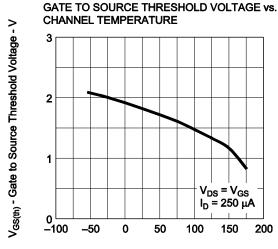
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



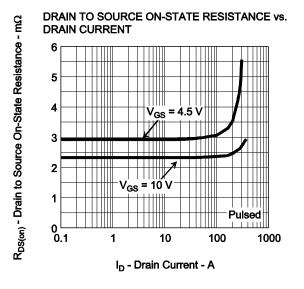




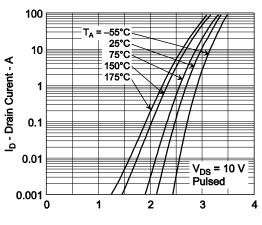
V_{DS} - Drain to Source Voltage - V



T_{ch} - Channel Temperature - °C

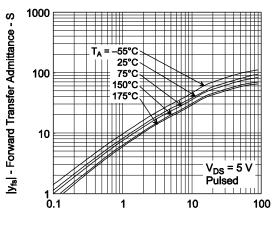


FORWARD TRANSFER CHARACTERISTICS



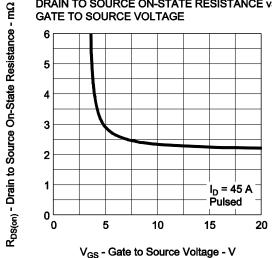


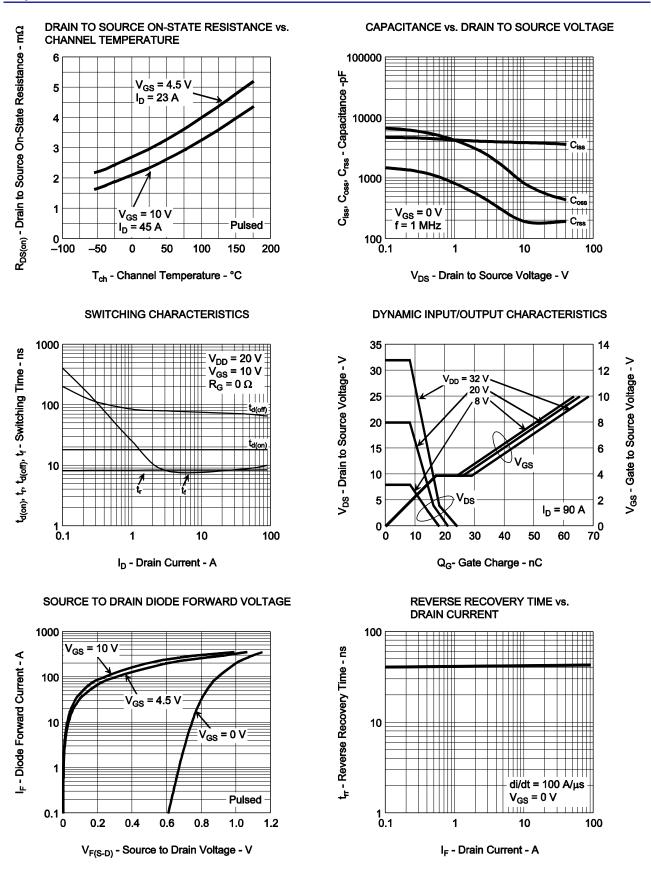
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



I_D - Drain Current - A

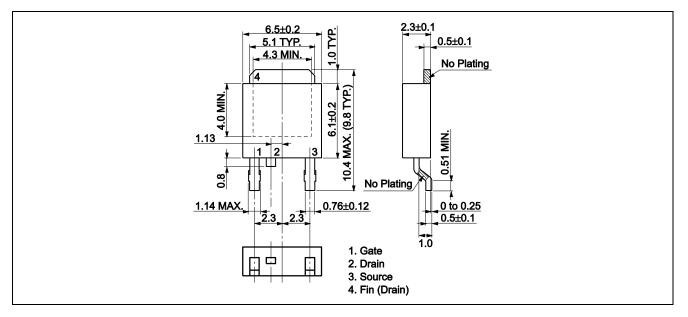




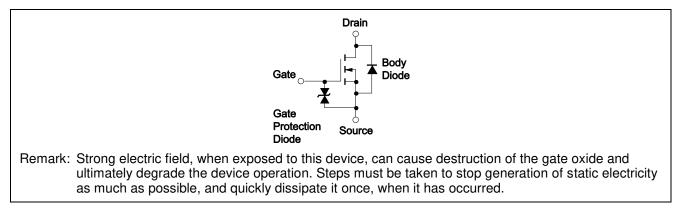


Package Drawing (Unit: mm)

TO-252 (MP-3ZP) (Mass: 0.3g TYP.)



Equivalent Circuit





Revision History

NP90N04VLK Data Sheet

		Description		
Rev.	Date	Page	Summary	
1.00	Nov 10, 2014	—	First Edition Issued	
2.00	May 24,2018	1	Note 3 was added	
		2	Note 2 was added	

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