CY62177DV30
MoBL®

32-Mbit (2M x 16) Static RAM

Features

- **Very high speed: 55 ns and 70 ns**
- **Wide voltage range: 2.20V–3.60V**
- **Ultra-low active power**
  - **Typical active current: 2 mA @ f = 1 MHz**
  - **Typical active current: 15 mA @ f = f_{max}**
- **Ultra low standby power**
- **Easy memory expansion with $\overline{CE}_1$, CE_2 and $\overline{OE}$ features**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Packages offered in a 48-ball FBGA**

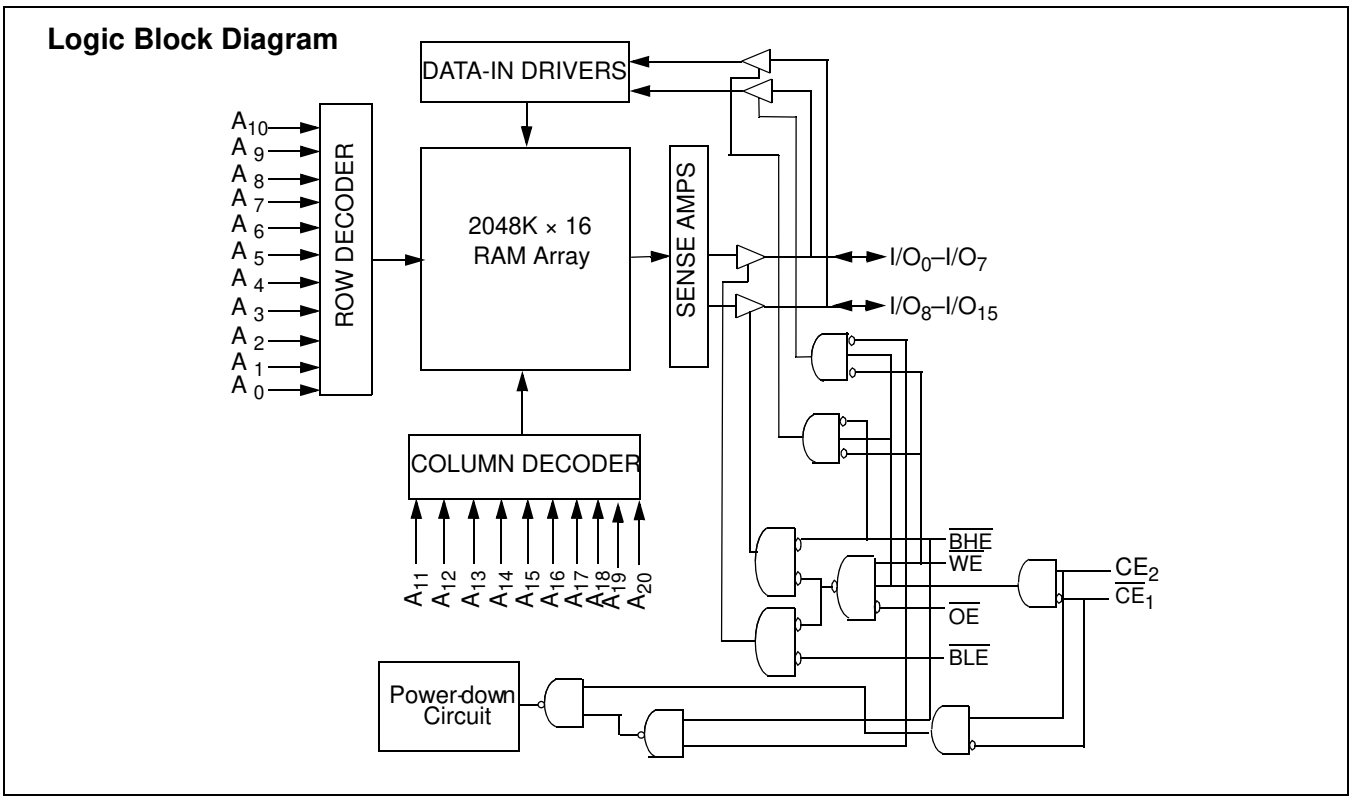
Functional Description[1]

The CY62177DV30 is a high-performance CMOS static RAM organized as 2M words by 16 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones.The device also has an automatic power-down feature that significantly reduces power consumption. The device can also be put into standby mode when deselected ($\overline{CE}_1$ HIGH or CE_2 LOW or both $\overline{BHE}$ and $\overline{BLE}$ are HIGH). The input/output pins (I/O_0 through I/O_{15}) are placed in a high-impedance state when: deselected ($\overline{CE}_1$HIGH or CE_2 LOW), outputs are disabled ($\overline{OE}$ HIGH), both Byte High Enable and Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a write operation ($\overline{CE}_1$ LOW, CE_2 HIGH and $\overline{WE}$ LOW).

Writing to the device is accomplished by taking Chip Enables ($\overline{CE}_1$ LOW and CE_2 HIGH) and Write Enable ($\overline{WE}$) input LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{20}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{20}).

Reading from the device is accomplished by taking Chip Enables ($\overline{CE}_1$ LOW and CE_2 HIGH) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins will appear on I/O_0 to I/O_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory will appear on I/O_8 to I/O_{15}. See the truth table for a complete description of read and write modes.

Logic Block Diagram

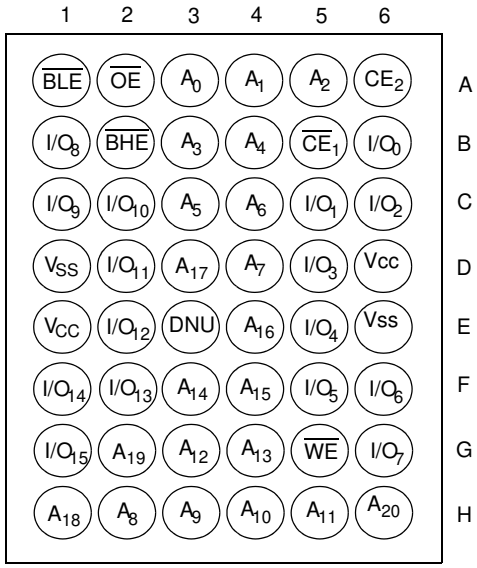


Note:
1. For best practice recommendations, please refer to the Cypress application note “System Design Guidelines” on http://www.cypress.com.

Pin Configuration[2]

FBGA

Top View



Product Portfolio

Product	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
					Operating I_{CC}(mA)				Standby I_{SB2}(µA)	
					f = 1 MHz		f = f_{max}			
	Min.	Typ.[3]	Max.		Typ.[3]	Max.	Typ.[3]	Max.	Typ.[3]	Max.
CY62177DV30L	2.20	3.0	3.60	55	2	4	15	30	5	60
				70			12	25		
CY62177DV30LL				55	2	4	15	30	5	50
				70			12	25		

Notes:
2. DNU pins have to be left floating or tied to Vss to ensure proper application.
3. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ.)}$, $T_A = 25°C$.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to + 150°C

Ambient Temperature with Power Applied.....–55°C to + 125°C

Supply Voltage to Ground Potential .....–0.3V to V_{CC} + 0.3V

DC Voltage Applied to Outputs in High Z State[4, 5].....–0.3V to V_{CC} + 0.3V

DC Input Voltage[4, 5] .....–0.3V to V_{CC} + 0.3V

Output Current into Outputs (LOW).....20 mA

Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current .....>200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC}[6]
CY62177DV30L	Industrial	–40°C to +85°C	2.20V to 3.60V
CY62177DV30LL			

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions			CY62177DV30-55			CY62177DV30-70			Unit
					Min.	Typ.[3]	Max.	Min.	Typ.[3]	Max.	
V_{OH}	Output HIGH Voltage	I_{OH} = –0.1 mA	V_{CC} = 2.20V		2.0			2.0			V
		I_{OH} = –1.0 mA	V_{CC} = 2.70V		2.4			2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 0.1 mA	V_{CC} = 2.20V				0.4			0.4	V
		I_{OL} = 2.1mA	V_{CC} = 2.70V				0.4			0.4	V
V_{IH}	Input HIGH Voltage	V_{CC} = 2.2V to 2.7V			1.8		V_{CC} +0.3V	1.8		V_{CC} +0.3V	V
		V_{CC}= 2.7V to 3.6V			2.2		V_{CC} +0.3V	2.2		V_{CC} +0.3V	V
V_{IL}	Input LOW Voltage	V_{CC} = 2.2V to 2.7V			–0.3		0.6	–0.3		0.6	V
		V_{CC}= 2.7V to 3.6V			-0.3		0.8	-0.3		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}			–1		+1	–1		+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled			–1		+1	–1		+1	µA
I_{CC}	V_{CC} Operating Supply Current	f = f_{MAX} = $1/t_{RC}$	V_{CC} = V_{CCmax} I_{OUT} = 0 mA CMOS levels			15	30		12	25	mA
		f = 1 MHz				2	4		2	4	mA
I_{SB1}	Automatic CE Power-Down Current—CMOS Inputs	$\overline{CE_1}$ ≥ V_{CC}–0.2V, CE_2 < 0.2V, V_{IN} ≥ V_{CC}–0.2V, V_{IN} ≤ 0.2V) f = f_{MAX} (Address and Data Only), f = 0 (OE, WE, BHE and BLE), V_{CC}=3.60V		L		5	100		5	100	µA
				LL		5	100		5	100	
I_{SB2}	Automatic CE Power-Down Current—CMOS Inputs	$\overline{CE_1}$ ≥ V_{CC} – 0.2V, CE_2 < 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, f = 0, V_{CC} = 3.60V		L		5	60		5	60	µA
				LL		5	50		5	50	

Notes:
4. $V_{IL(min.)}$ = –2.0V for pulse durations less than 20 ns.
5. $V_{IH(Max)}$ = V_{CC} + 0.75V for pulse durations less than 20 ns.
6. Full Device AC operation requires linear V_{CC} ramp from 0 to $V_{CC(min)}$ ≥ 500 µs.

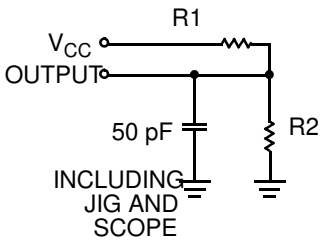
Capacitance[7, 8]

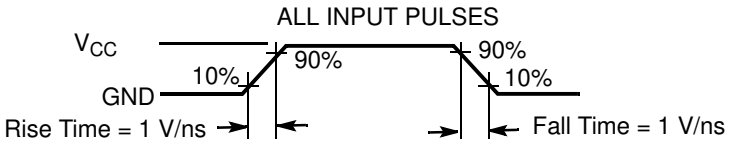
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = $V_{CC(typ)}$	12	pF
C_{OUT}	Output Capacitance		12	pF

Thermal Resistance[7]

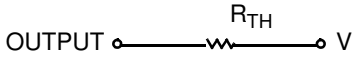
Parameter	Description	Test Conditions	BGA	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	55	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		16	°C/W

AC Test Loads and Waveforms





Equivalent to: THÉVENIN EQUIVALENT



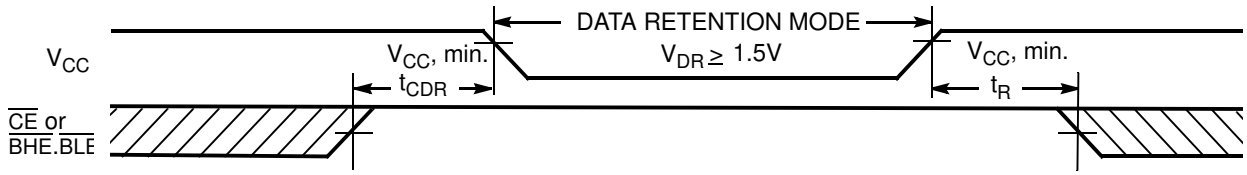
Parameters	2.5V (2.2V to 2.7V)	3.0V (2.7V to 3.6V)	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R_{TH}	8000	645	Ω
V_{TH}	1.20	1.75	V

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions		Min.	Typ.[3]	Max.	Unit
V_{DR}	V_{CC} for Data Retention			1.5			V
I_{CCDR}	Data Retention Current	V_{CC}= 1.5V $\overline{CE_1} \geq V_{CC}$–0.2V, CE_2 < 0.2V, $V_{IN} \geq V_{CC}$ – 0.2V or $V_{IN} \leq$ 0.2V	L			30	µA
			LL			25	
t_{CDR}[7]	Chip Deselect to Data Retention Time			0			ns
t_R[9]	Operation Recovery Time			t_{RC}			ns

Notes:
7. Tested initially and after any design or process changes that may affect these parameters.
8. This applies for all packages.
9. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq$ 100 µs or stable at $V_{CC(min.)} \geq$ 100 µs.

Data Retention Waveform[10, 11]



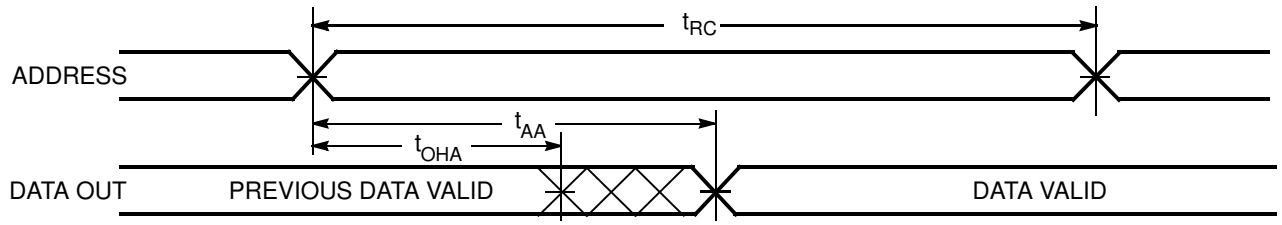
Switching Characteristics Over the Operating Range[11, 12]

Parameter	Description	55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE						
t_{RC}	Read Cycle Time	55		70		ns
t_{AA}	Address to Data Valid		55		70	ns
t_{OHA}	Data Hold from Address Change	10		10		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		55		70	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		25		35	ns
t_{LZOE}	$\overline{OE}$ LOW to LOW Z[13]	5		5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[13, 14]		20		25	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[13]	10		10		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[13, 14]		20		25	ns
t_{PU}	$\overline{CE}$ LOW HIGH to Power-Up	0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		55		70	ns
t_{DBE}	BLE/BHE LOW to Data Valid		55		70	ns
t_{LZBE}	$\overline{BLE}$/$\overline{BHE}$ LOW to Low Z[13]	10		5		ns
t_{HZBE}	$\overline{BLE}$/$\overline{BHE}$ HIGH to HIGH Z[13, 14]		20		25	ns
WRITE CYCLE[15]						
t_{WC}	Write Cycle Time	55		70		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	40		60		ns
t_{AW}	Address Set-Up to Write End	40		60		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	40		45		ns
t_{BW}	$\overline{BLE}$/$\overline{BHE}$ LOW to Write End	40		60		ns
t_{SD}	Data Set-Up to Write End	25		30		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z[13, 14]		20		25	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z[13]	10		10		ns

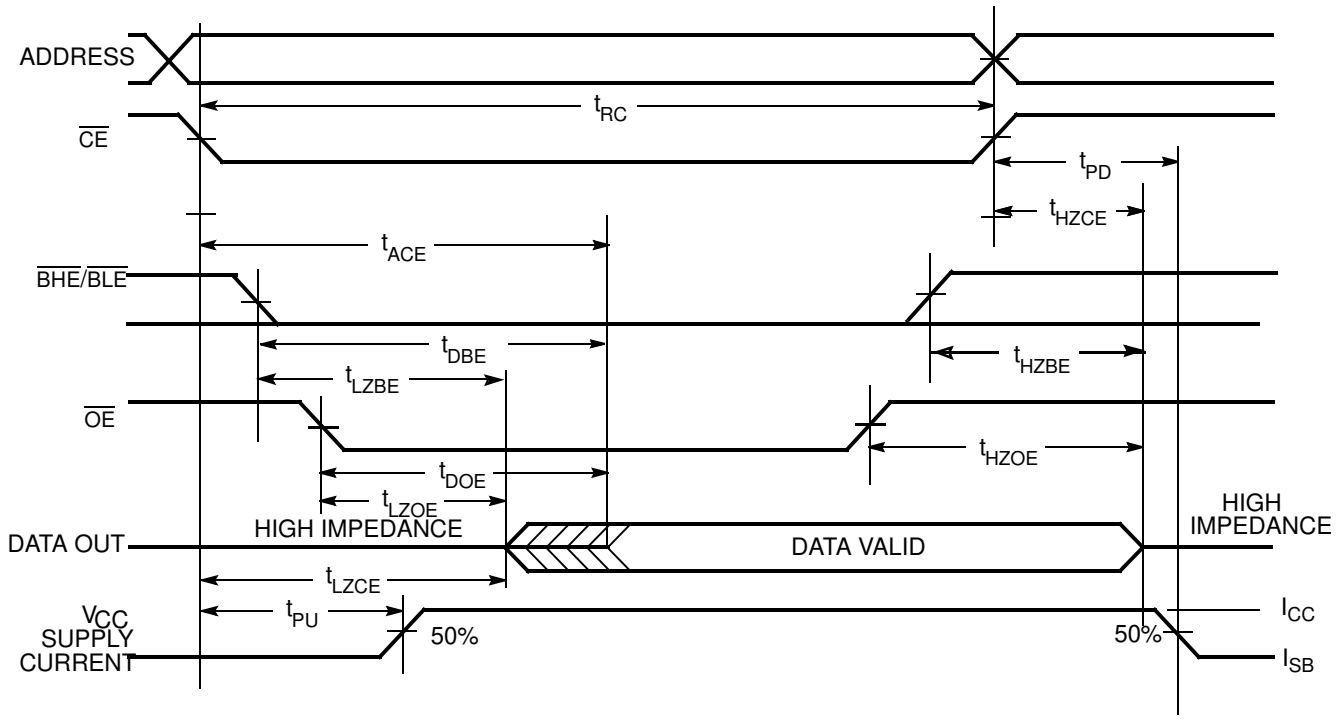
Notes:
10. $\overline{BHE}.\overline{BLE}$ is the AND of both $\overline{BHE}$ and $\overline{BLE}$. Chip can be deselected by either disabling the chip enable signals or by disabling both $\overline{BHE}$ and $\overline{BLE}$.
11. $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
12. Test conditions for all parameters other than tri-state parameters assume signal transition time of 1 ns/V, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ.)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the "AC Test Loads and Waveforms" section.
13. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
14. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
15. The internal Write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IL}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.

Switching Waveforms

Read Cycle 1 (Address Transition Controlled)[16, 17]



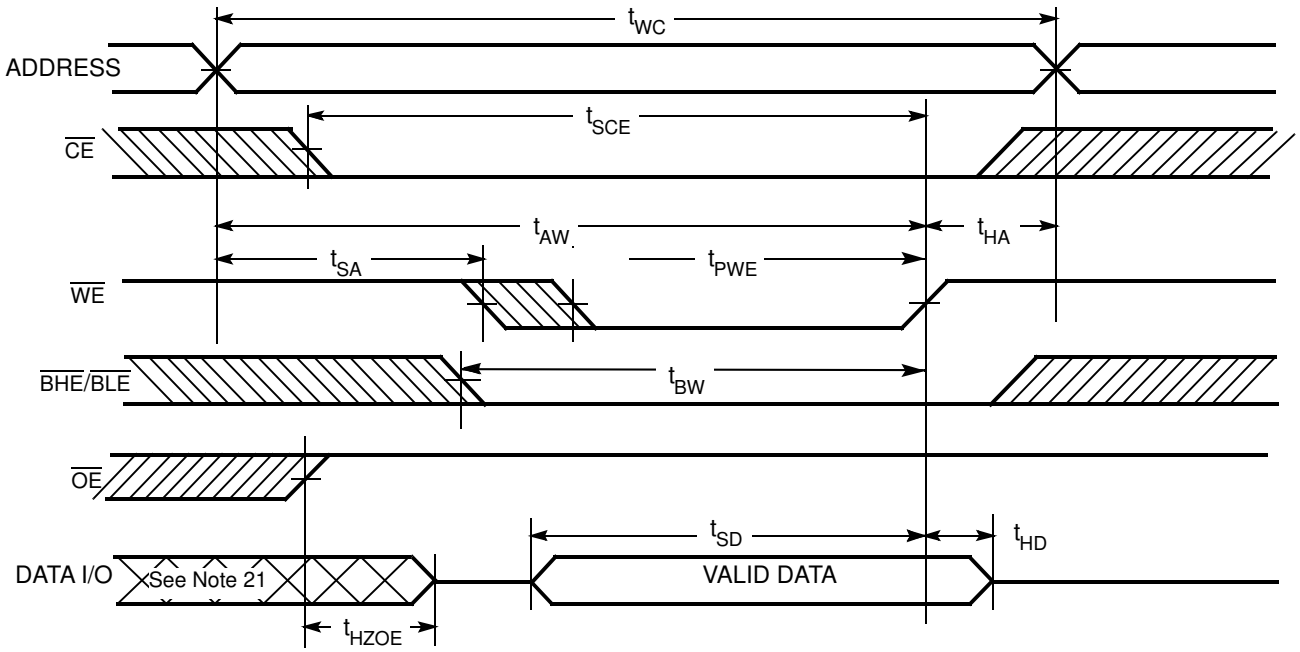
Read Cycle 2 ($\overline{OE}$ Controlled)[11, 17, 18]



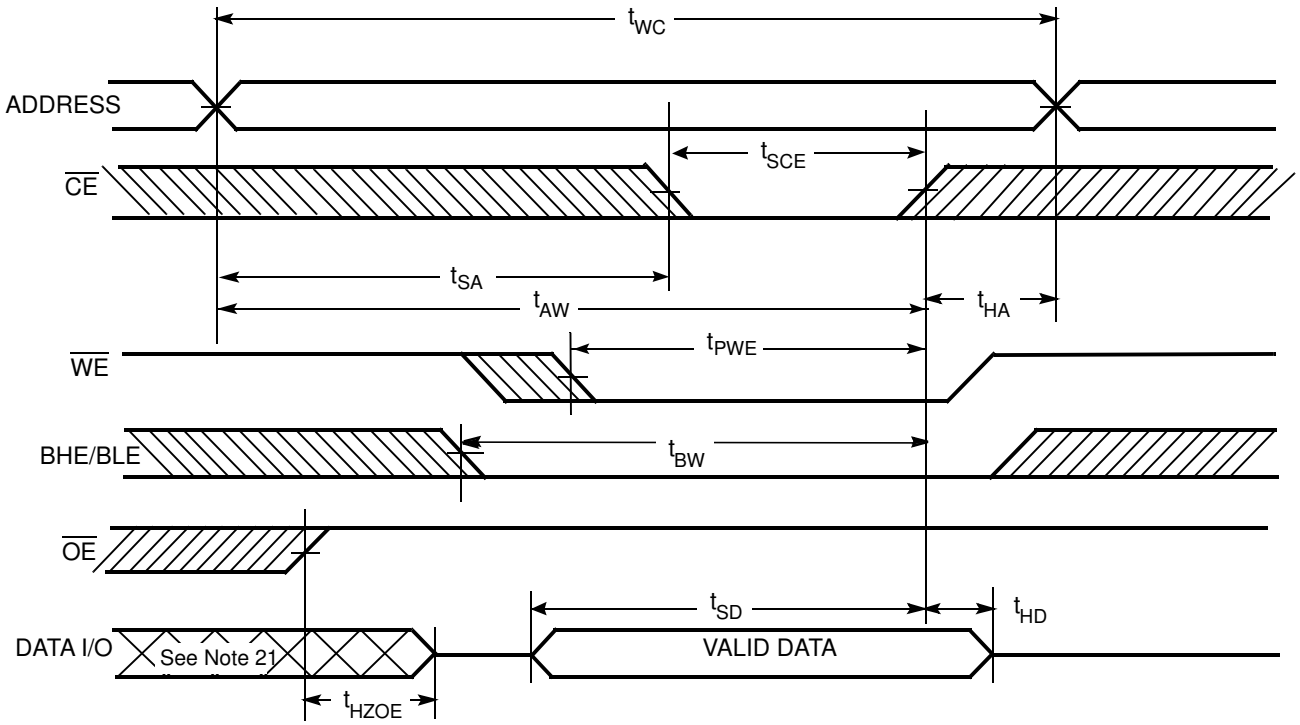
Notes:
16. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IL}.
17. $\overline{WE}$ is HIGH for read cycle.
18. Address valid prior to or coincident with $\overline{CE}$, $\overline{BHE}$, $\overline{BLE}$ transition LOW.

Switching Waveforms (continued)

Write Cycle 1 (WE Controlled)[11, 15, 19, 20, 21]



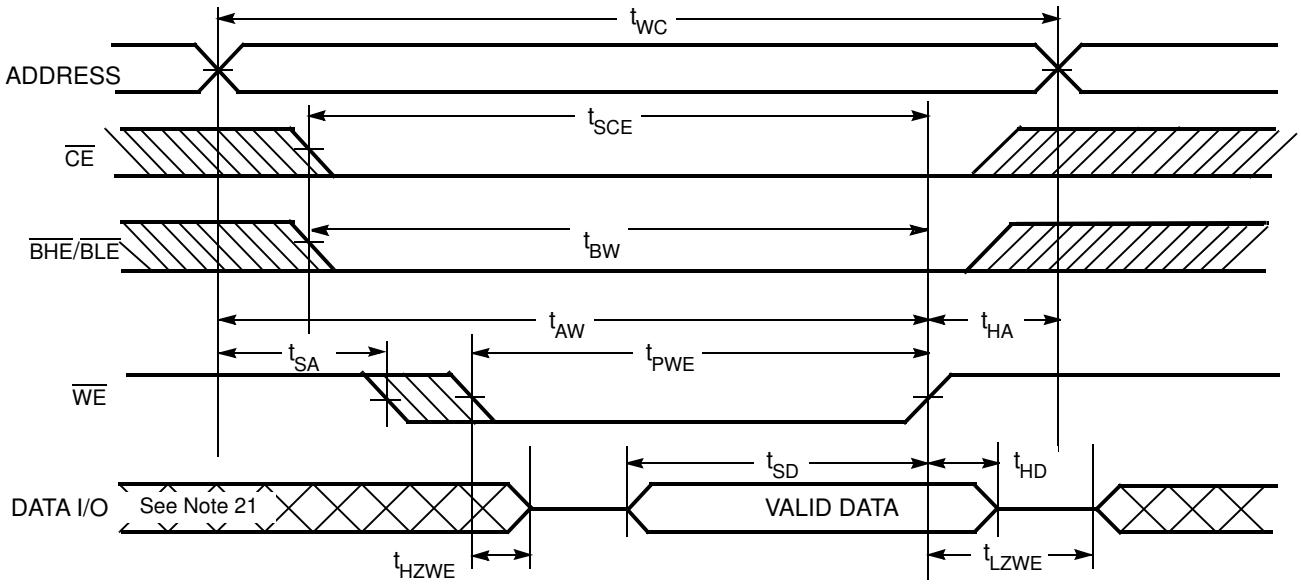
Write Cycle 2 (CE Controlled)[11, 15, 19, 20, 21]



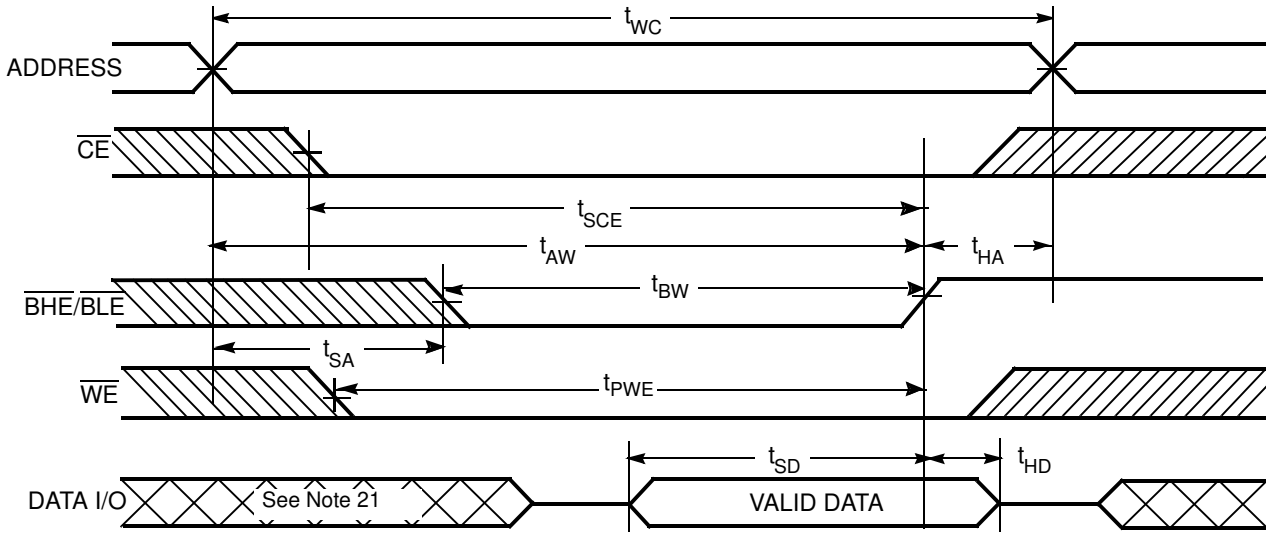
Notes:
19. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
20. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high-impedance state.
21. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle 3 (WE Controlled, OE LOW)[11, 20, 21]



Write Cycle 4 (BHE/BLE Controlled, OE LOW)[11, 20, 21]



Truth Table

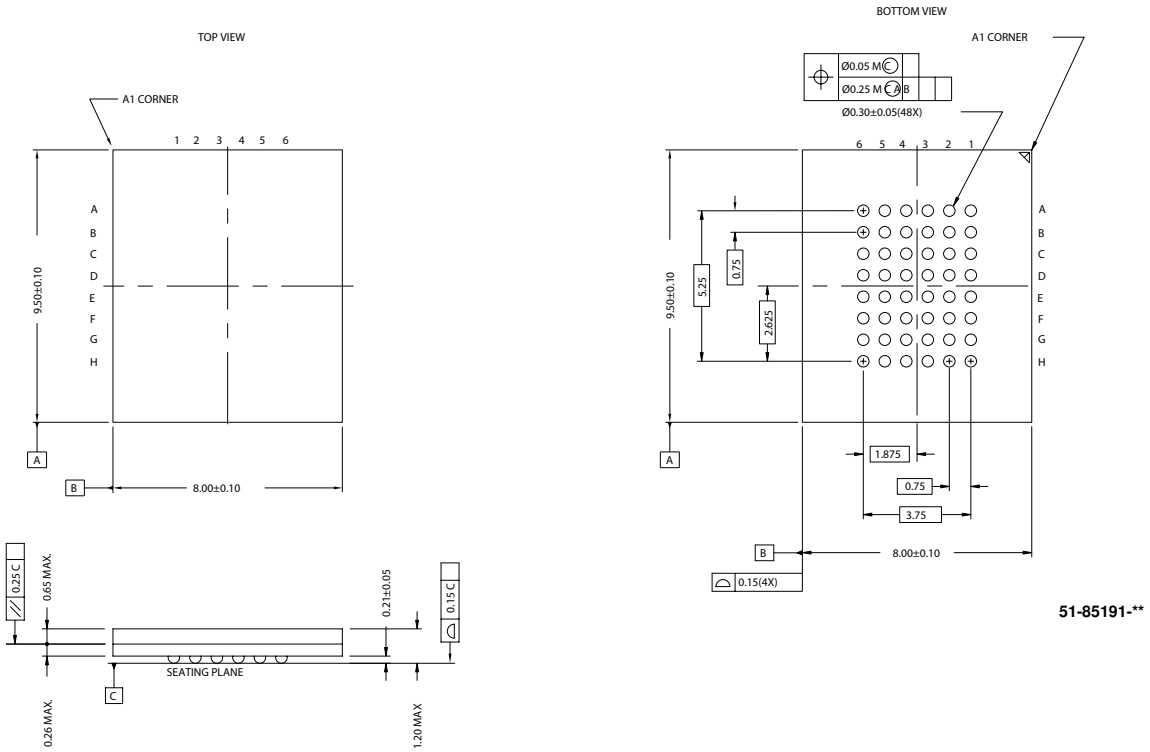
$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
X	L	X	X	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
X	X	X	X	H	H	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	H	L	L	L	Data Out (I/O_0–I/O_{15})	Read	Active (I_{CC})
L	H	H	L	H	L	Data Out (I/O_0–I/O_7); High Z (I/O_8–I/O_{15})	Read	Active (I_{CC})
L	H	H	L	L	H	High Z (I/O_0–I/O_7); Data Out (I/O_8–I/O_{15})	Read	Active (I_{CC})
L	H	H	H	L	H	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	H	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	L	L	High Z	Output Disabled	Active (I_{CC})
L	H	L	X	L	L	Data In (I/O_0–I/O_{15})	Write	Active (I_{CC})
L	H	L	X	H	L	Data In (I/O_0–I/O_7); High Z (I/O_8–I/O_{15})	Write	Active (I_{CC})
L	H	L	X	L	H	High Z (I/O_0–I/O_7); Data In (I/O_8–I/O_{15})	Write	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
55	CY62177DV30L-55BAI	51-85191	48-ball FBGA (8 mm × 9.5mm × 1.2 mm)	Industrial
	CY62177DV30LL-55BAI			
	CY62177DV30LL-55BAXI		48-ball FBGA (8 mm × 9.5mm × 1.2 mm) (Pb-free)	
70	CY62177DV30L-70BAI	51-85191	48-ball FBGA (8 mm × 9.5mm × 1.2 mm)	Industrial

Package Diagram

48 FBGA (8 x 9.5 x 1.2 MM) (51-85191)



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Document History Page

Document Title:CY62177DV30 MoBL® 32-Mbit (2M x 16) Static RAM Document #: 38-05633				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	251075	See ECN	AJU	New Data Sheet
*A	330363	See ECN	AJU	Changed title of data sheet from CYM62177DV30 to CY62177DV30 Added second chip enable (CE_2) Added footnote #12 on page 5
*B	400960	See ECN	NXR	Changed address of Cypress Semiconductor Corporation on Page# 1 from “3901 North First Street” to “198 Champion Court” Changed I_{SB1} from 60 and 40 μA to 100 μA for the L and LL versions for both the 55 and the 70 ns speed bins respectively.
*C	469187	See ECN	NXR	Converted from Preliminary to Final Changed the $I_{SB2(Max)}$ from 40 μA to 50 μA for LL version of both 45 ns and 55 ns speed bins Changed the $I_{CCDR(Max)}$ from 20 μA to 25 μA for LL version Updated the Ordeing Information table