PC Card and Integrated 1394a-2000 OHCI Two-Port PHY/Link-Layer Controller

FEATURES

- ***PC Card Standard* 8.0 Compliant**
- ***PCI Bus Power Management Interface Specification* 1.1 Compliant**
- ***Advanced Configuration and Power Interface (ACPI) Specification* 2.0 Compliant**
- ***PCI Local Bus Specification* Revision 2.2 Compliant**
- **PC 98/99 and PC2001 Compliant**
- ***PCI Bus Interface Specification for PCI-to-CardBus Bridges***
- **Fully Compliant with Provisions of IEEE Std 1394-1995 for a High-Performance Serial Bus and IEEE Std 1394a-2000**
- **Fully Compliant with *1394 Open Host Controller Interface Specification* 1.1**
- **Compatible with Both TPS2211A and TPS2221 PC Card Power Switches**
- **1.8-V Core Logic and 3.3-V I/O Cells with Internal Voltage Regulator to Generate 1.8-V Core V_{CC}**
- **Universal PCI Interfaces Compatible with 3.3-V and 5-V PCI Signaling Environments**
- **Supports PC Card or CardBus with Hot Insertion and Removal**
- **Supports 132-MBps Burst Transfers to Maximize Data Throughput on Both the PCI Bus and the CardBus**
- **Supports Serialized IRQ with PCI Interrupts**
- **Programmable Multifunction Terminals**
- **Serial ROM Interface for Loading Subsystem ID and Subsystem Vendor ID**
- **ExCA-Compatible Registers Are Mapped in Memory or I/O Space**
- **Intel 82365SL–DF Register Compatible**
- **Supports Ring Indicate, $\overline{\text{SUSPEND}}$, PCI $\overline{\text{CCLKRUN}}$ Protocol, and PCI Bus Lock $\overline{\text{LOCK}}$)**
- **Provides VGA/Palette Memory and I/O, and Subtractive Decoding Options, LED Activity Terminals**
- **Fully Interoperable with FireWire™ and i.LINK™ Implementations of IEEE Std 1394**
- **Compliant with *Intel Mobile Power Guideline 2000***
- **Full IEEE Std 1394a-2000 Support Includes: Connection Debounce, Arbitrated Short Reset, Multispeed Concatenation, Arbitration Acceleration, Fly-By Concatenation, and Port Disable/Suspend/Resume**
- **Power-Down Features to Conserve Energy in Battery-Powered Applications Include: Automatic Device Power Down During Suspend, PCI Power Management for Link-Layer and Inactive Ports Powered Down, Ultralow-Power Sleep Mode**
- **Two IEEE Std 1394a-2000 Fully Compliant Cable Ports at 100M Bits/s, 200M Bits/s, and 400M Bits/s**
- **Cable Ports Monitor Line Conditions for Active Connection to Remote Node**
- **Cable Power Presence Monitoring**
- **Separate Cable Bias (TPBIAS) for Each Port**
- **Physical Write Posting of up to Three Outstanding Transactions**
- **PCI Burst Transfers and Deep FIFOs to Tolerate Large Host Latency**
- **External Cycle Timer Control for Customized Synchronization**
- **Extended Resume Signaling for Compatibility with Legacy DV Components**
- **PHY-Link Logic Performs System Initialization and Arbitration Functions**
- **PHY-Link Encode and Decode Functions Included for Data-Strobe Bit Level Encoding**
- **PHY-Link Incoming Data Resynchronized to Local Clock**
- **Low-Cost 24.576-MHz Crystal Provides Transmit and Receive Data at 100M Bits/s, 200M Bits/s, and 400M Bits/s**
- **Node Power Class Information Signaling for System Power Management**

- **Register Bits Give Software Control of Contender Bit, Power Class Bits, Link Active Control Bit, and IEEE Std 1394a-2000 Features**
- **Isochronous Receive Dual-Buffer Mode**
- **Out-Of-Order Pipelining for Asynchronous Transmit Requests**
- **Register Access Fail Interrupt When the PHY SCLK Is Not Active**
- **PCI Power-Management D0, D1, D2, and D3 Power States**
- **Initial Bandwidth Available and Initial Channels Available Registers**
- **$\overline{\text{PME}}$ Support per *1394 Open Host Controller Interface Specification***
- **Advanced Submicron, Low-Power CMOS Technology**

DESCRIPTION

The Texas Instruments PCI4510R device is an integrated single-socket PC Card controller with an IEEE 1394 open host controller link-layer controller (LLC) and two-port 1394 PHY. This high performance integrated solution provides the latest in both PC Card and IEEE 1394 technology.

The controller is compliant with *PCI Local Bus Specification*. Function 0 provides the independent PC Card socket controller compliant with the latest *PC Card Standards*. The controller provides features that make it the best choice for bridging between the PCI bus and PC Cards, and supports either 16-bit or CardBus PC Cards in the socket, powered at 5 V or 3.3 V, as required.

There are no PCMCIA card and socket service software changes required to move systems from the existing CardBus socket controller to the PCI4510R controller. The PCI4510R controller is register compatible with the Intel 82365SL–DF ExCA controller and implements the host interface defined in the *PC Card Standard*. The internal data path logic allows the host to access 8-, 16-, and 32-bit cards using full 32-bit PCI cycles for maximum performance. Independent buffering and the pipeline architecture provides an unsurpassed performance level with sustained bursting. The controller can be programmed to accept posted writes to improve bus utilization. All card signals are internally buffered to allow hot insertion and removal without external buffering.

Function 1 of the controller is an integrated IEEE 1394a-2000 open host controller interface (OHCI) PHY/link-layer controller (LLC) device that is fully compliant with the *PCI Local Bus Specification*, the *PCI Bus Power Management Interface Specification*, IEEE Std 1394-1995, IEEE Std 1394a-2000, and the *1394 Open Host Controller Interface Specification*. It is capable of transferring data between the 33-MHz PCI bus and the 1394 bus at 100M bits/s, 200M bits/s, and 400M bits/s. The controller provides two 1394 ports that have separate cable bias (TPBIAS). The controller also supports the IEEE Std 1394a-2000 power-down features for battery-operated applications and arbitration enhancements.

As required by the *1394 Open Host Controller Interface Specification* and IEEE Std 1394a-2000, internal control registers are memory-mapped and nonprefetchable. The PCI configuration header is accessed through configuration cycles specified by PCI, and it provides plug-and-play (PnP) compatibility. Furthermore, the controller is compliant with the *PCI Bus Power Management Interface Specification* as specified by the *PC 2001 Design Guide* requirements. The controller supports the D0, D1, D2, and D3 power states.

The controller provides PCI bus master bursting, and it is capable of transferring a cacheline of data at 132M bytes/s after connection to the memory controller. Because PCI latency can be large, deep FIFOs are provided to buffer the IEEE 1394 data.

The controller provides physical write posting buffers and a highly-tuned physical data path for SBP-2 performance. The controller also provides multiple isochronous contexts, multiple cacheline burst transfers, advanced internal arbitration, and bus-holding buffers.

The PHY-layer provides the digital and analog transceiver functions needed to implement a two-port node in a cable-based 1394 network. Each cable port incorporates two differential line transceivers. The transceivers include circuitry to monitor the line conditions as needed for determining connection status, for initialization and arbitration, and for packet reception and transmission.

The PHY-layer requires only an external 24.576-MHz crystal as a reference for the cable ports. An external clock may be provided instead of a crystal. An internal oscillator drives an internal phase-locked loop (PLL), which generates the required 393.216-MHz reference signal. This reference signal is internally divided to provide the clock signals that control transmission of the outbound encoded strobe and data information. A 49.152-MHz clock signal is supplied to the integrated LLC for synchronization and is used for resynchronization of the received data. Data bits to be transmitted through the cable ports are received from the integrated LLC and are latched internally in synchronization with the 49.152-MHz system clock. These bits are combined serially, encoded, and transmitted at 98.304M, 196.608M, or 393.216M bits/s (referred to as S100, S200, or S400 speeds, respectively) as the outbound data-strobe information stream. During transmission, the encoded data information is transmitted differentially on the twisted-pair B (TPB) cable pair(s), and the encoded strobe information is transmitted differentially on the twisted-pair A (TPA) cable pair(s).

Various implementation-specific functions and general-purpose inputs and outputs are provided through several multifunction terminals. These terminals present a system with options, such as PCI $\overline{\text{LOCK}}$ and parallel IRQs. ACPI-complaint general-purpose events may be programmed and controlled through the multifunction terminals, and an ACPI-compliant programming interface is included for the general-purpose inputs and outputs.

The controller is compliant with the latest *PCI Bus Power Management Specification*, and provides several low-power modes, which enable the host power system to further reduce power consumption. The controller also has a four-pin interface compatible with both the TI TPS2211A and TPS2221 power switches.

An advanced CMOS process achieves low power consumption and allows the controller to operate at PCI clock rates up to 33 MHz.

NOTE:

This product is for high-volume PC applications only. For a complete datasheet or more information contact support@ti.com.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
PCI4510RGVF	OBSOLETE	NFBGA	GVF	224		TBD	Call TI	Call TI
PCI4510RZVF	OBSOLETE	NFBGA	ZVF	224		TBD	Call TI	Call TI

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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