TPS2359 Dual-Slot ATCA™ AdvancedMC™ Controller with I²C Evaluation Module

This document describes the features and use of the TPS2359EVM, Dual-Slot ATCA AdvancedMC™ Controller with I²C EVM. It provides a module overview and operating specifications. The document contains set-up and operating instructions, including power supply connections and installation of the Windows-compatible GUI, and use of the various features and test points. The EVM circuit schematic and PCB layer pictorials are also included.

1 Introduction

The Dual-Slot AdvancedMC™ Controller Evaluation Module (EVM) is a PCB platform for users to learn about the features and operation of the TPS2359 integrated circuit from Texas Instruments (TI). The TPS2359 Full Featured Dual-Slot AdvancedMC™ Controller manages two 12-V and two 3.3-V power rails, and features inrush and fault current limiting, FET OR'ing, input UVLO protection, logic-level enable inputs and an I²C interface. Current control on the 12-V rails has a high degree of programmability, including independent current limit and fast trip thresholds. System level timing and other control parameters are accessed via the I²C interface, along with readback of FET and output rail status. In addition, current sense and pass and block FET's for the 3.3-V channels are fully integrated into the device.

Power management applications based on the TPS2359 are easily configured to meet the requirements for 12-V and 3.3-V control of Advanced Mezzanine Card (AdvancedMC™) modules. Each device incorporated onto a Carrier Card provides full control for two AdvancedMC™ slots according to the requirements of the Advanced Telecommunications Computing Architecture (ATCA™) specification, PICMG 3.0. In addition, the input supply FET OR'ing control for the 12-V rails facilitates efficient redundant supply implementations in Micro Telecommunications Computing Architecture (MicroTCA™) systems.

2 Description

2.1 Module Overview

The TPS2359EVM is a single-board evaluation platform consisting of two main sections. When oriented with the board nomenclature in a normal, upright reading position towards the user, the top approximately two-thirds is the TPS2359 IC and related components. The bottom third contains a complete USB-to-I²C Interface Adapter, allowing access to the device's internal I²C registers from the USB port of any Windows-based host PC. Power connectors are organized with inputs along the left edge of the board, outputs along the right.

The main (upper) section of the board is comprised of the featured device, input and output banana jacks for connection of the user's supplies and test loads (if desired), and some on-board load capacitance. Numerous jumpers are provided throughout the circuit for maximum configuration flexibility. Test points are available for voltage and waveform monitoring.

The EVM kit includes a USB cable with the mating connector for the Type B-Mini connector on the EVM. The TPS2359 EVM GUI is available for download from the TI website at http://www.GUIdownloadURL. The GUI enables access to the control and status registers of the TPS2359 for quick set-up and operation of the EVM without having to write any code.

2.2 Typical Applications

The TPS2359EVM was designed with independent input and output banana jacks for up to two each 12-V input and 3.3-V input power supplies, and up to two each 12-V and 3.3-V output power rails. This provides the greatest flexibility for configuring the EVM for either ATCA™ or MicroTCA™ applications.

By connecting the two 12-V inputs and two 3.3-V inputs together, the TPS2359EVM can manage the application of a single 12-V supply and single 3.3-V supply to two AdvancedMC-like loads. This configuration allows users to learn about the device operation in non-redundant applications. Driving the supply inputs independently while ganging together the common potential output nodes demonstrates operation in redundant systems, albeit through a common controller device. In either case, the user GUI provides easy access to the internal control bits to complete device configuration for the target application.

As supplied from the factory, the EVM comes with current limits programmed for the requirements of Management Power and Payload Power control for AdvancedMC™ modules. However, limit thresholds on the 12-V channels are programmable by the user; see the TPS2359 datasheet (TI Literature Number SLUS792) for the procedure to establish different limit thresholds via the programming resistors. This flexibility with the TPS2359 enables use in other, proprietary systems requiring 12-V and 3.3-V supply control.

Lastly, the EVM features two expansion ports and related jumpers needed to parallel multiple devices together to create a true redundant system. Additional EVM modules for this purpose can be ordered directly from the TI website at http://www.productfolderURL, or contact your local TI representative.

2.3 Features

The TPS2359EVM includes the following features:

- One TPS2359 Full Featured Dual-Slot AdvancedMC™ Controller IC
- USB- to-I^2C Interface Adapter
- Programming and sense resistors (12-V)
- Low R_{DS}(ON) pass and block FET's (12-V)
- Input and output power jacks for external supply and optional load connection
- Up to 880 μF (4 × 220 μF) jumpered load capacitors (each channel) for simulated Payload Power output bulk capacitance
- 150 μF jumpered load capacitor for each Management Power channel
- Address-setting DIP switch
- Slide switch actuation of enable inputs
- Expansion port headers
- Windows-compatible EVM GUI

The use of these features is described in greater detail later in this document.

3 Electrical Specifications

3.1 Absolute Maximum Ratings

The absolute maximum ratings for the TPS2359EVM are given below in Table 1.

Table 1. Absolute Maximum Ratings[(1)(2)]

PARAMETER	RATING
Input voltage range, +12-V supply	–0.3 V to 13.8 V
Input voltage range, +3.3-V supply	–0.3 V to 4 V
Applied voltage, pins of J21, J41 SUMx, EN3x	–0.3 V to 5 V
Applied voltage, pins of J21, J41 SCL, SDA, $\overline{\text{IRPT}}$	–0.3 V to 3.5 V
Output current, 12-V outputs	TBD
Output current, 3.3-V outputs	Internally limited by device
Output current, SUMx	–5 mA
Output current, $\overline{\text{IRPT}}$	5 mA
Storage temperature range	–55°C to 150°C

(1) All voltages are with respect to the EVM GND node.
(2) Currents are positive into and negative out of the specified terminal.

3.2 Recommended Operating Conditions

The recommended operating conditions for the TPS2359EVM are given in Table 2.

Table 2. Recommended Operating Conditions, TPS2359EVM[(1)(2)]

PARAMETER	MIN	TYP	MAX	UNITS
Input supply voltage, +12-V	8.8	12	13.2	V
Input supply voltage, +12-V (for specified V_{OUT})	11.3	12	13.2	V
Input supply voltage, +3.3-V	2.85	3.3	3.5	V
Input supply voltage, +3.3-V (for specified V_{OUT})	3.235	3.3	3.465	V
Load current, Payload Power Out (either channel)			–7.4	A
Load current, Mgmt Power Out (either channel)			–165	mA

(1) All voltages are with respect to the EVM GND node.
(2) Currents are positive into and negative out of the specified terminal.

3.3 Electrical Characteristics

The electrical characteristics of the TPS2359EVM are as listed in Table 3.

Table 3. Electrical Characteristics, TPS2359EVM(1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
UNLESS OTHERWISE NOTED: V_{IN}(12VINx) and V_{IN}(3V3INx) per Table 2 under *(for specified V_{OUT})*. T_A = 25°C					
Output Voltage, Payload Power Out (either channel)	ENBx = HI, $I_{LPWR} < I_{LPWR\_MAX}$	10.8		13.2	V
Output Voltage, Mgmt Power Out (either channel)	ENBx = HI, $I_{LMP} < I_{LMP\_MAX}$	3.135		3.465	V
Current limit threshold, Payload Power (either channel)		7.4	8.36	9.1	A
Current limit threshold, Mgmt Power (either channel)		170	195	225	mA
Fast trip threshold, Payload Power (either channel)				24.5	A
Fast trip threshold, Mgmt Power (either channel)				400	mA
Output capacitance, Payload Power (C_{L_PWR}) (each channel)	All 4 load caps connected	704	880	1056	µF
Output capacitance, Mgmt Power (C_{L_MP}) (each channel)	Load cap connected	120	150	180	µF
Output ramp time, Payload Power	V_{IN} = 12V–13.2V, V_O = 0V to 98% × V_{IN}, R_{LOAD} = 1K, C_{LOAD} = C_{L_PWR}		1.31	2.01	mS
Output ramp time, Mgmt Power	V_{IN} = 3.3V–3.465V, V_O = 0 V to 98% V_{IN}, R_{LOAD} = 270, C_{LOAD} = C_{L_MP}		2.57	3.74	mS

(1) All voltages are with respect to the EVM GND node.

4 Schematic Diagram

The schematic diagram for the TPS2359EVM is shown in Figure 1 and Figure 2.

Figure 1 includes the TPS2359 device itself along with directly related circuit components and the available on-board loads. Figure 2 shows the schematic for the USB-to-I^{2}C interface provided on the EVM for easy GUI/PC control. The circuitry on this page is not part of a typical implementation.

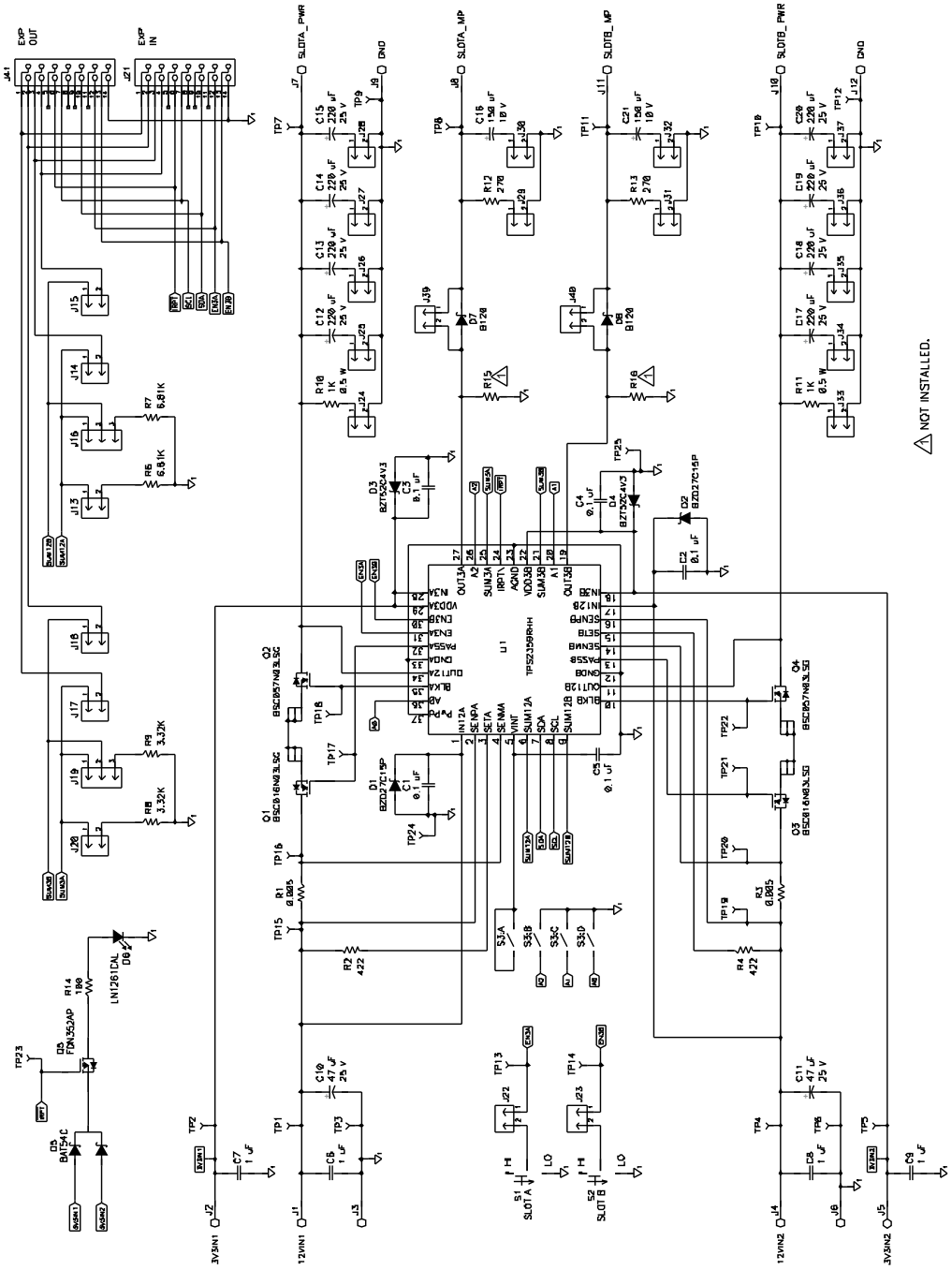


Figure 1. TPS2359 Evaluation Module Schematic Diagram, Sheet 1

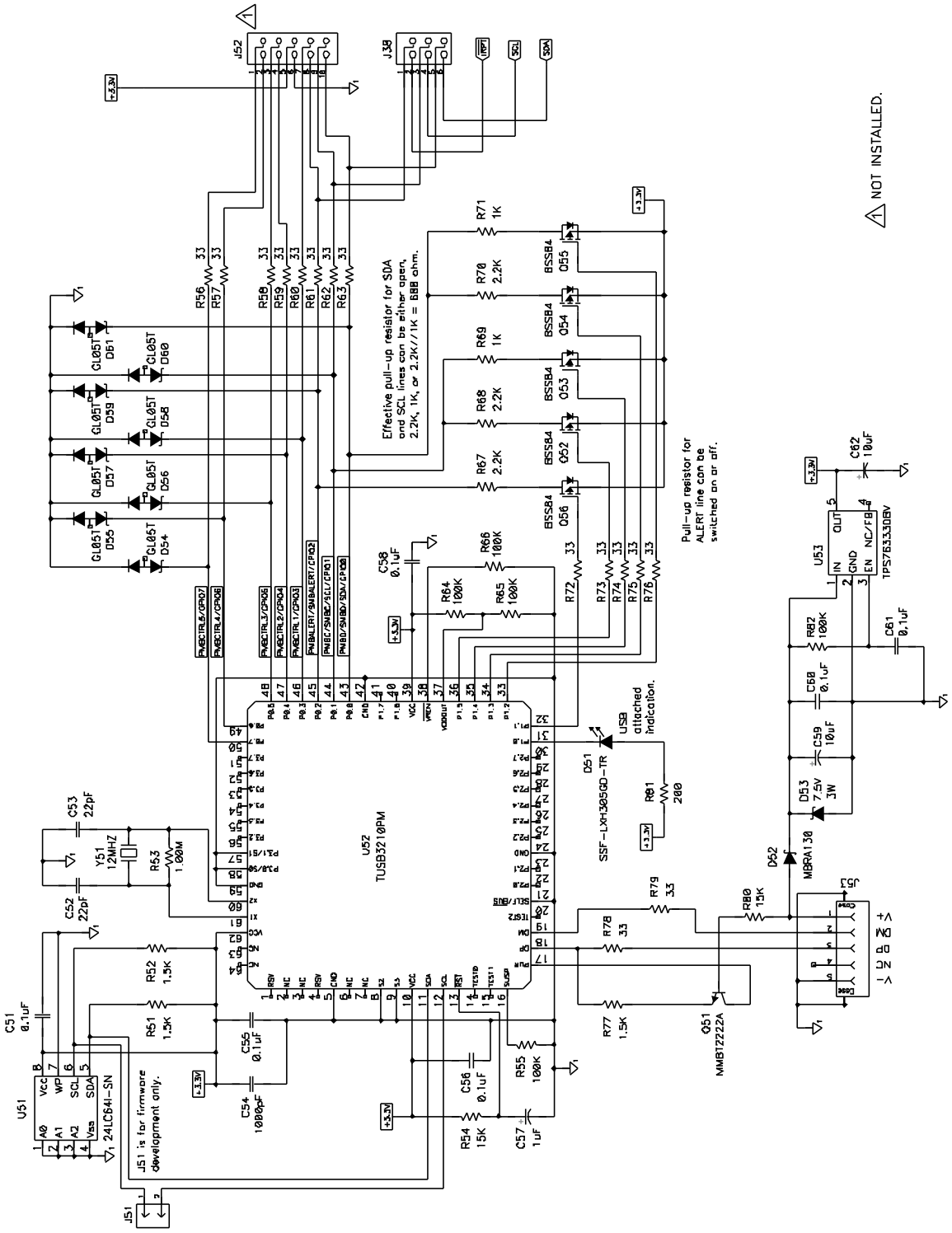


Figure 2. TPS2359 Evaluation Module Schematic Diagram, Sheet 2

5 Test Set-Up

5.1 Equipment Requirements

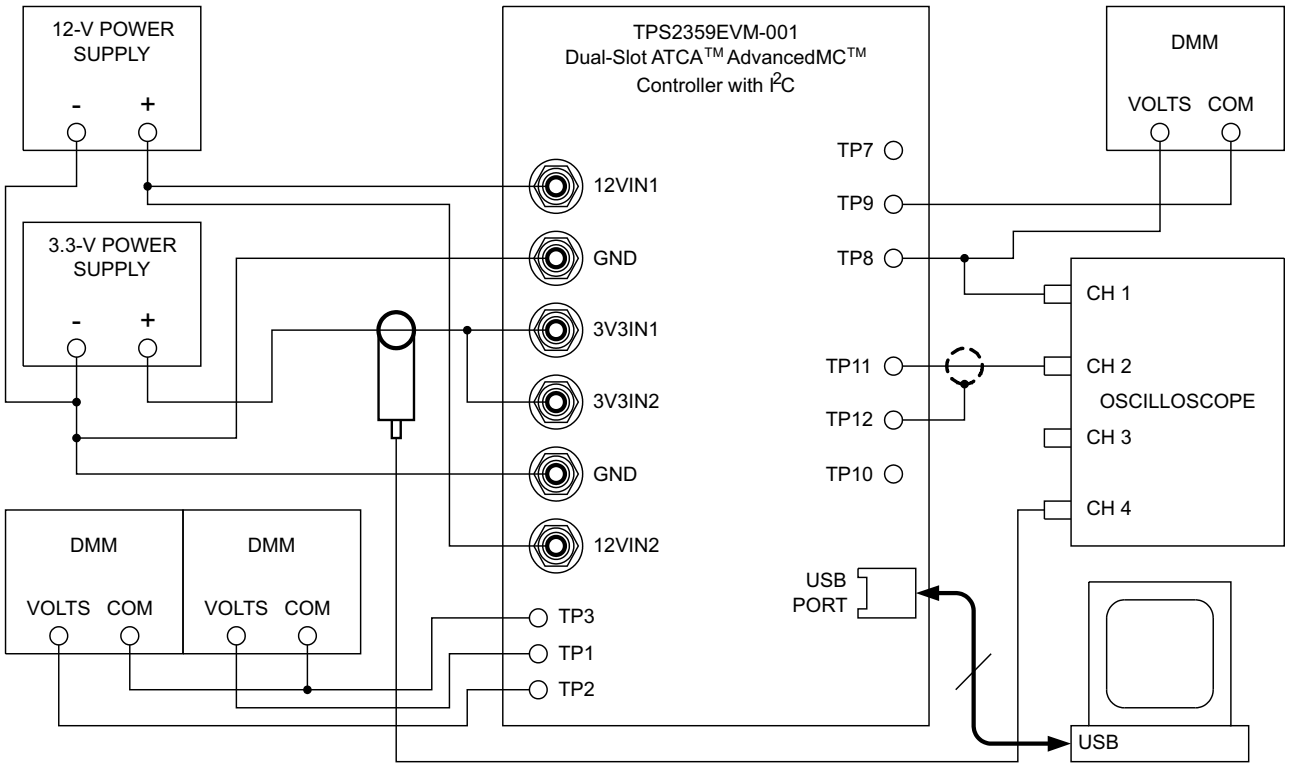
The following test and interface equipment (not supplied) is required to verify EVM module operation, and begin using the EVM.

- Power supply, 3.3 VDC, 500 mA minimum
- Power supply, 15 VDC, 10 A minimum
- Digital multimeters
- Oscilloscope, 4 channel, with current probe
- Personal computer, running Windows OS (95/98/2000/NT/XP), with USB port

Connect the TPS2359EVM and test equipment as shown in Figure 3 for functional check-out of the board and a good starting point for user evaluation of device operation. Screen print labeling on the board employs a naming convention in keeping with the nomenclature of the target ATCA™ and MicroTCA™ applications. Input 3.3-V supplies are connected to the 3V3INx jacks, and 12-V supplies are connected to the 12VINx jacks. A cross-reference of power rail labeling to standards naming is shown in Table 4.

Table 4. TPS2359EVM Output Net and Jack Naming

REF DES	CONNECTOR	LABEL DESCRIPTION
J8	SLOT A MP	AdvancedMC™ Slot A Management Power
J7	SLOT A PWR	AdvancedMC™ Slot A Payload Power
J9	GND	Common load return node for Slot A
J11	SLOT B MP	AdvancedMC™ Slot B Management Power
J10	SLOT B PWR	AdvancedMC™ Slot B Payload Power
J12	GND	Common load return node for Slot B



NOTES:

1. The 3V3INx jacks can be jumpered together with a short test lead at the board, fed from a single lead from the power supply.
2. Run separate leads from the GND jacks back to a common return point made near the power supply output terminals.

Figure 3. TPS2359EVM Set-Up — Non-Redundant System Connection

6 Test Procedure

The following procedure can be used to verify functional operation of the EVM assembly upon receipt.

6.1 GUI Installation

In an ATCA™ or µTCA™ application, the TPS2359 IC may work in conjunction with an Intelligent Platform Management Controller (IPMC) device, which in turn is in communication with shelf management. The Shelf Management Controller (ShMC) configures slot power parameters, and enables and disables rails in response to a dynamically changing system configuration. With the EVM, this control function is realized with the TPS2359 EVM GUI, running on a Windows PC, via the on-board USB-to- I^2C interface.

The GUI is available via download from the TI website (http://www.ti.com). Alternatively, the GUI may be obtained on distribution diskette or by e-mail by contacting your authorized TI representative. To install the GUI on the intended host PC, follow the instructions in this section.

Save the distribution .zip file to the local hard drive of the target PC. Extract the installation executable from the file. The installer filename will be of the form *TPS2359-EVM-GUI-1.0.x.y.exe*, where x and y are minor build revision numbers.

Click on Start → Run …, and navigate to the folder where the executable was extracted to. Click on the installation .exe file. Click on *Open*, then click *OK*. Alternatively, use Windows Explorer to navigate to the GUI folder, then double-click on the.exe file. The TI TPS2359 EVM GUI Setup Wizard welcome screen will appear on the display. Follow the instructions given in the Wizard pop-ups, selecting the desired options, and clicking “Next>” each time to proceed. Note that when the GUI license agreement displays, you must select the *I accept the agreement* radial button in order to proceed.

At the *Ready to install* window, click *Install*, if the settings are O.K. The GUI will be installed to the indicated location, and any selected links created. When the installation complete window of Figure 4 appears, click the *Finish* button to exit the installer.

Note: If the EVM is not yet connected to the power supplies, or the supplies are turned off at this point, it is recommended to uncheck the *Launch Texas Instruments TPS2359 EVM GUI* checkbox before clicking on *Finish*.

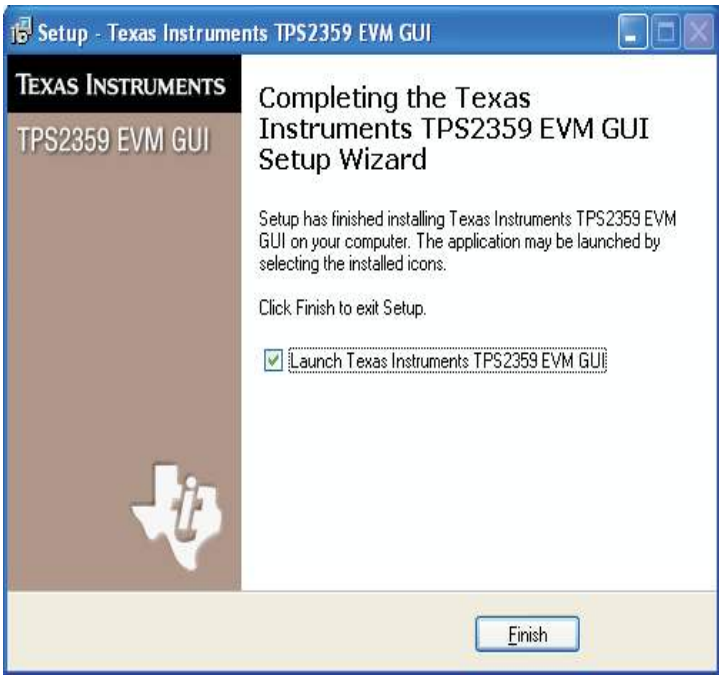


Figure 4. TPS2359 EVM GUI Setup Wizard — Installation Complete

6.2 Jumper Installation

The TPS2359EVM makes use of various jumpers for quick change of functional configurations. Verify the module was supplied with jumpers installed across the following two-pin headers, or reconfigure settings as necessary.

Table 5. Initial Jumper Settings

INSTALLED TWO-PIN JUMPERS
J13, J20
J22, J23
J24 – J28
J29, J30
J31, J32
J33 - J37
J39, J40
J51

In addition, make sure that the indicated pin pairs of the headers listed in Table 6 are connected via shunt jumper.

Table 6. Multi-Pin Jumper Connections

JUMPER	POSITION
J16	Pin 2 – Pin 3
J19	Pin 2 – Pin 3
J38	Pin 1 – Pin 2
J38	Pin 3 – Pin 4
J38	Pin 5 – Pin 6

Set both slot ENABLES switches (bottom left corner of PCB) to the HI position.

6.3 Check-Out Steps

Turn the voltage adjust knobs of both power supplies fully CCW. Adjust the current limit control of the 15-V supply for 10 amps minimum output.

If not already done, connect the EVM and test equipment as shown in Figure 3. Once the EVM USB PORT is connected to the PC, the green LED D51 on the EVM should illuminate.

Turn on the 3.3-V power supply, and adjust the output for 3.3 V ± 5% at test point TP2. Turn on the second supply, and adjust the output for 12 V ± 5% at TP1. Verify the IRPT LED (D6) is off.

On the host PC, launch the EVM GUI from either the Start menu item or desktop icon. The GUI start-up screen of Figure 5 should appear. The TPS2359 EVM GUI auto-detects devices present on the I^2C bus, and then selects the numerically lowest addressed device from the set of discovered devices. The address of the current device for all read and write transactions is displayed in the *Address* field at the top of the GUI screen.

In the GUI window, in both the AMC A and AMC B STATUS panels, verify both the 12A and 12B PASS FET and BLK FET indicators display an OFF status (red background). The two (12A and 12B) OUT>PG Threshold indicators should also be RED. In both (AMC A and AMC B) STATUS panels, verify both the 3.3A and 3.3B PASS/BLK FET indicators display an OFF status (red background). The two VOUT GOOD indicators should also be RED. In the 12A CONTROL panel, click on the FAULT TIME SET up arrow to maximize the displayed value at 15.5 mS. Click on the field with this value displayed (background color turns blue). Repeat this process in the remaining three FAULT TIME fields (12B, 3.3A, 3.3B), being sure to click on the displayed 15.5 mS value each time.

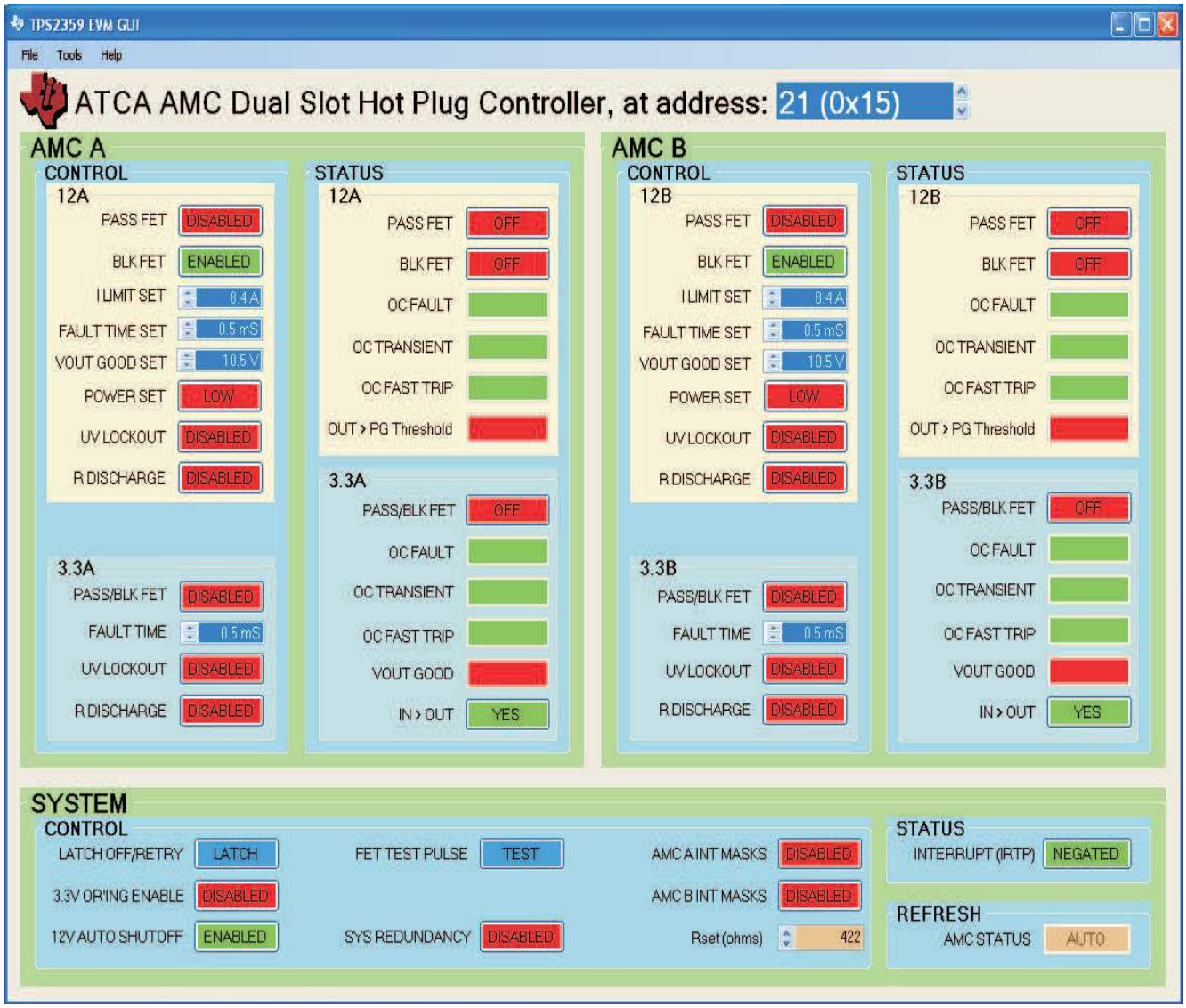


Figure 5. GUI Initial Control and Status Display at Launch.

On the oscilloscope, set the Channel 1 and 2 amplifiers to the 2 V/div scale, and position the traces appropriately in the top half of the display for viewing 3.3-V magnitude waveforms. Set the current pulse amplifier scale to 50 mA/div, and position that trace towards the bottom of the scope screen. Set the scope to trigger on the rising edge of Channel 1, at a threshold of about 1.5 V. Set the time base to 500 µS or 1 mS/div, and set the trigger mode to NORMAL.

In the GUI 3.3A CONTROL panel, click on the PASS/BLK FET button. In the STATUS panel, verify the 3.3A PASS/BLK FET and VOUT GOOD indicator colors change to GREEN. On the oscilloscope, verify a waveform was obtained similar to the one shown in Figure 6. The total ramp time of the Channel 1 waveform, from 0 volts to about 3.2 volts should be 2.6 ± 0.6 mS. The peak amplitude of the current pulse on Channel 4 (I_{PEAK}) should be 195 ± 25 mA. A DVM can be used to verify the voltage at TP8 (with respect to ground at TP9) is within 10 mV of the 3.3-V input supply voltage at 3V3IN1 (TP2).

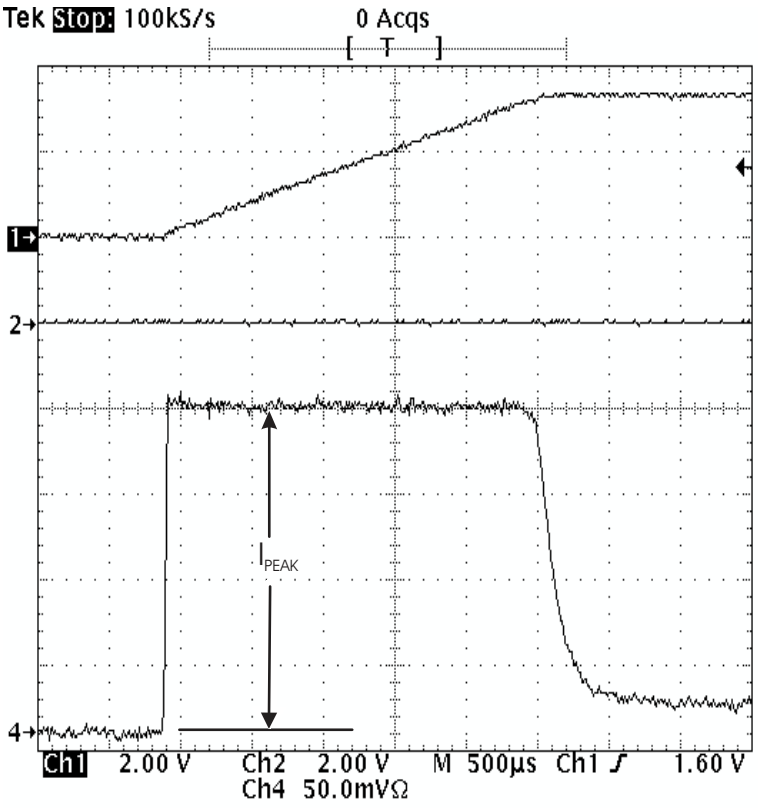


Figure 6. Output Ramp-Up Waveforms – SLOTA_MP Rail

Set the scope to trigger on Channel 2. In the GUI 3.3B CONTROL panel, click on the PASS/BLK FET button. In the STATUS panel, verify the 3.3B PASS/BLK FET and VOUT GOOD indicator colors change to GREEN. On the scope screen, verify a waveform was obtained similar to that shown in Figure 7. The Channel 2 and 4 waveform parameters should be similar to those indicated above for Figure 6. A DVM can be used to verify the output voltage at TP11 (with respect to ground at TP12) is within 10 mV of the 3.3-V input supply setting.

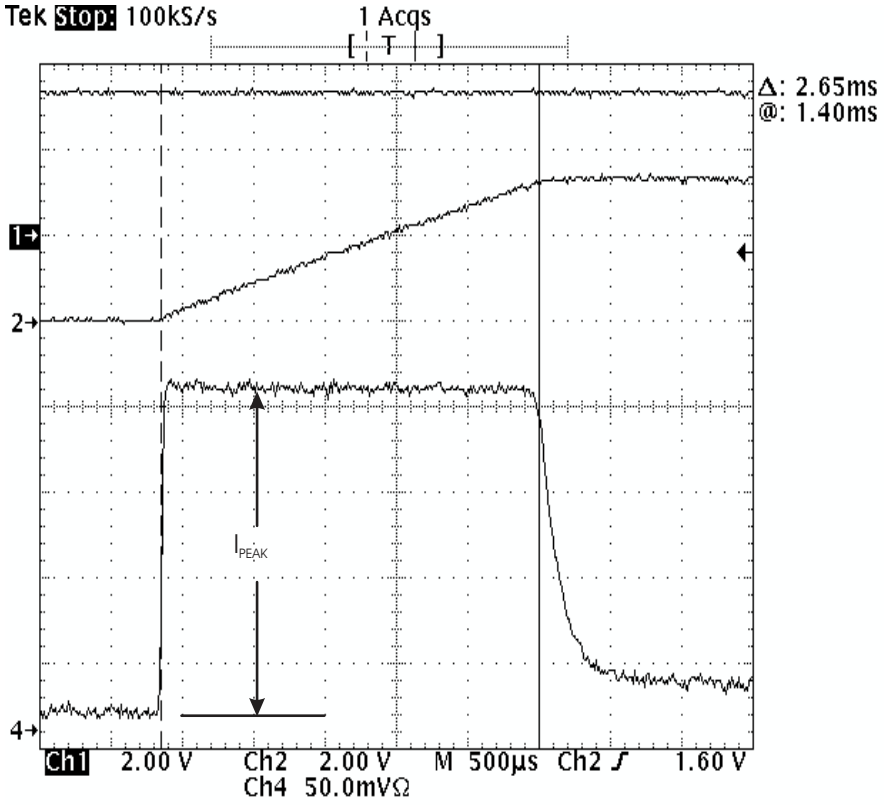


Figure 7. Output Ramp-Up Waveforms – SLOTB_MP Rail

Move the Channel 1 scope probe to TP7, and the Channel 2 probe to TP10. Change the Channel 1 and 2 amplifier scale settings to 5 V/div. Remove the current probe from the 3.3 V supply lead, and clamp it across the 12VIN2 supply lead. Change the Channel 4 amplifier to 2 A/div. Adjust the scope trigger threshold to about 3 volts.

In the GUI 12B CONTROL panel, click on the PASS FET button. In the STATUS panel, verify the 12B PASS FET, BLK FET, and OUT>PG Threshold indicators turn GREEN. On the scope, verify a waveform was obtained similar to that shown in Figure 8. The total ramp time of the Channel 2 trace, from 0 volts to about 11.8 V should be 1.3 ± 0.3 mS. Note that the extent of variance of the 12-V supply setting from a nominal 12.0 V affects this timing result. The average amplitude of the current pulse (i.e., across the flattest part of the peak) on Channel 4 should be 7.9 ± 0.8 A. A DVM can be used to verify the voltage at TP10 (with respect to ground at TP12) is essentially the same as the input supply potential at 12VIN2.

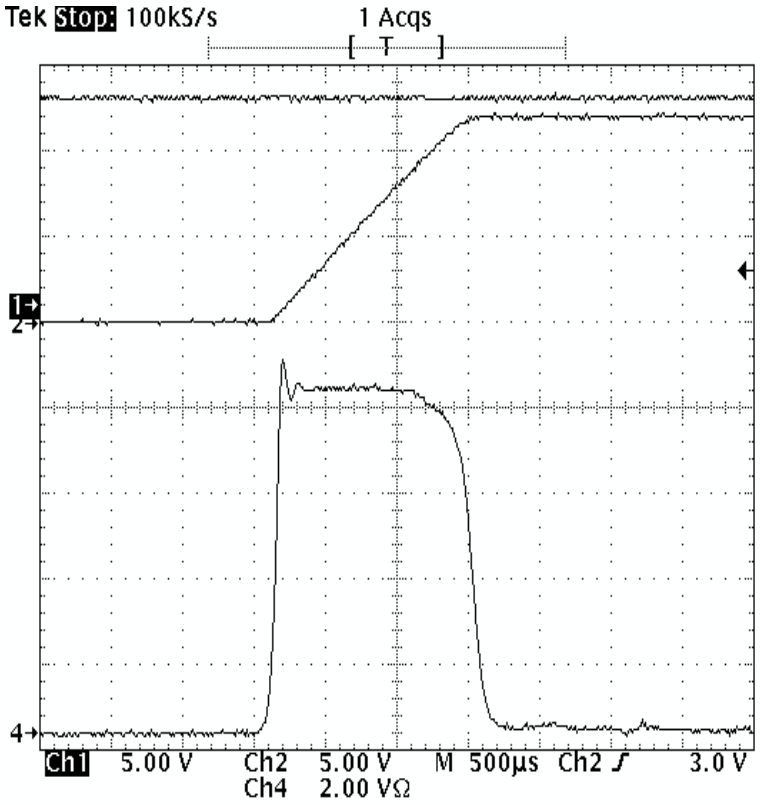


Figure 8. Output Ramp-Up Waveforms — SLOTB_PWR Rail

Set the scope to trigger on Channel 1. Disconnect the current probe and reconnect it across the 12VIN1 supply lead. Move the probe ground lead to test point TP9. In the GUI 12A CONTROL panel, click on the PASS FET button. In the STATUS panel, verify the 12A PASS FET, BLK FET, and OUT>PG Threshold indicators turn GREEN. On the scope, verify a waveform was obtained similar to that shown in Figure 9. The Channel 1 and 4 waveform parameters should be similar to those indicated above for Figure 8. Again, the extent of variance of the 12-V supply setting from a nominal 12.0 V affects the ramp-up timing result. A DVM can be used to verify the voltage at TP7 (with respect to ground at TP9) is essentially the same as the input supply potential at 12VIN1.

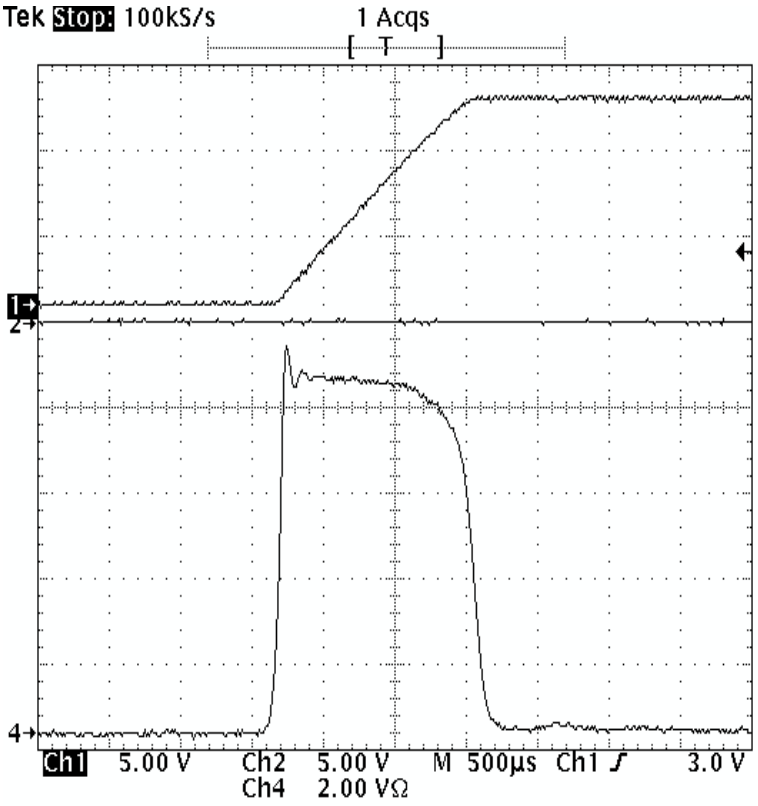


Figure 9. Output Ramp-Up Waveforms — SLOTA_PWR Rail

On the EVM board, set the SLOT B ENABLE slide switch to the LO position. Use a DVM to verify the output voltages at test points TP10 and TP11 (with respect to TP12) decay towards 0 volts. In the AMC B STATUS panel, the 12B PASS FET, BLK FET, and 3.3B PASS/BLK FET indicators should display OFF, with the indicator color changing to red. Both PG indicators (OUT>PG Threshold and VOUT GOOD) should change to RED. On the EVM board, set the SLOT A ENABLE switch to the LO position. The output voltages at test points TP7 and TP8 (with respect to TP9) should now also decay towards 0 volts. Also, the AMC A STATUS FET indicators should display OFF (red background), and the two PG indicators also turn RED.

Module operation as indicated in the above steps, along with obtaining the indicated GUI responses, is a good indication of a fully functional board and correct set-up. This is also a good starting point for further test and user evaluation of the device. Note that the four power channels must be reset by setting each of the PASS FET CONTROL buttons to DISABLED (and returning the ENABLE switches to the HI position), in order to enable subsequent power-up events.

7 EVM Feature Details

7.1 Test Points

The TPS2359EVM contains numerous test points throughout the circuit for user monitoring of waveforms and voltage measurement. Table 7 lists the module test points and the signal available at each one. The EVM PCB layout connects all ground nodes and supply returns to a common GND node, via several power plane areas. However, due to potentially high loading conditions on the two Payload Power outputs, multiple ground test points are provided to mitigate the measurement impact of return current drops. Therefore, where appropriate, certain test points are paired in the table with the pertinent reference point for meter return connections.

Table 7. Module Test Points

TEST POINT	REF. POINT	SIGNAL NAME	DESCRIPTION
TP1	TP3	12VIN1	Input 12 V supply for AdvancedMC™ Slot A
TP2		3V3IN1	Input 3.3 V supply for AdvancedMC™ Slot A
TP4	TP6	12VIN2	Input 12 V supply for AdvancedMC™ Slot B
TP5		3V3IN2	Input 3.3 V supply for AdvancedMC™ Slot B
TP7	TP9	SLOTA_PWR	AdvancedMC™ Slot A Payload Power, 12 V output
TP8		SLOTA_MP	AdvancedMC™ Slot A Management Power, 3.3 V output
TP10	TP12	SLOTB_PWR	AdvancedMC™ Slot B Payload Power, 12 V output
TP11		SLOTB_MP	AdvancedMC™ Slot B Management Power, 3.3 V output
TP13	TP24, TP25	EN3A	Active-high enable input to TPS2359 for the channel A 3.3 V rail
TP14		EN3B	Active-high enable input to TPS2359 for the channel B 3.3 V rail
TP15	TP16		Slot A 12-V load current sense voltage
TP17	TP24	PASSA	TPS2359 channel A pass FET gate drive output
TP18		BLKA	TPS2359 channel A block/OR'ing FET gate drive output
TP19	TP20		Slot B 12-V load current sense voltage
TP21	TP25	PASSB	TPS2359 channel B pass FET gate drive output
TP22		BLKB	TPS2359 channel B block/OR'ing FET gate drive output
TP23	TP24, TP25	/IRPT	Open-drain, active-low /IRPT (interrupt) output signal from TPS2359

7.2 Connecting Loads to the TPS2359EVM

Each of the four power rails of the TPS2359EVM is supplied with some amount of load capacitance in the form of discrete electrolytics. The capacitors can be connected to or disconnected from their associated output nodes using 100-mil, 2-pin shunt jumpers across the on-board PCB headers. These capacitors are intended to simulate input bulk capacitance which may be encountered at the front ends of AdvancedMC™ modules plugged into the card slots of the target application. The AdvancedMC™ standard specifies the maximum allowable input capacitance on both Management and Payload Power rails. The TPS2359EVM provides up to 150 µF capacitance on each of the two Management Power outputs, according to the AdvancedMC™ maximum limit. The EVM also provides up to 880 µF of capacitance, implemented in increments of 220 µF devices, on each of the Payload Power rails, to approximate the 800 µF limit of the standard. In addition, low-level (mA) load resistors can be jumpered in across each output and return. These limited load resistors are intended primarily as reset devices between output ramp events, particularly when loaded with significant capacitance.

Table 8 lists the EVM module's output voltage nodes, and for each one indicates the associated jumper reference designators, and the resultant load value with jumper installed.

Table 8. EVM On-Board Loads

OUTPUT RAIL	JUMPER	DEVICE	VALUE
SLOTA_MP	J30	C16	150 µF
	J29	R12	270 Ω
SLOTB_MP	J32	C21	150 µF
	J31	R13	270 Ω
SLOTA_PWR	J25	C12	220 µF
	J26	C13	220 µF
	J27	C14	220 µF
	J28	C15	220 µF
	J24	R10	1 kΩ
SLOTB_PWR	J34	C17	220 µF
	J35	C18	220 µF
	J36	C19	220 µF
	J37	C20	220 µF
	J33	R11	1 kΩ

Banana jacks are provided along the right-hand edge of the board for connection of the user's optional test loads. The output banana jack reference designators are listed in Table 4 along with the voltage rail available at each one. Also, the net names are screen printed on the PCB, adjacent to their respective jacks.

7.3 I²C Address Selection

Three input pins on the TPS2359 are assigned for setting the device I²C address: A2, A1 and A0. These pins are 3-level inputs, allowing the device to be assigned any one of 27 unique address values. These pins can be tied to ground potential to generate a logic low (L), pulled up to the VINT pin to generate a logic high (H), or left open to float to a mid-range, no-connect (NC) level. On the EVM, address selection is performed using switch S3. However, S3 is a common 4-position, 2-throw DIP switch. The switch is wired into the circuit to pull the corresponding input pin to ground (L) when its DIP position is closed. When a DIP position is open (O), the corresponding pin floats. Therefore, the address space for the EVM is limited to an 8-value subset of the addresses recognized by the TPS2359. Table 9 specifies the valid address space of the TPS2359EVM. Note that switch position S3-4 is not used.

Table 9. TPS2359EVM Valid I²C Addresses

S3 POSITION			DEVICE ADDRESS	
A2	A1	A0	TERNARY	DECIMAL
L	L	L	$000_3 + 22_3$	0 + 8 = 8
L	L	O	$001_3 + 22_3$	1 + 8 = 9
L	O	L	$010_3 + 22_3$	3 + 8 = 11
L	O	O	$011_3 + 22_3$	4 + 8 = 12
O	L	L	$100_3 + 22_3$	9 + 8 = 17
O	L	O	$101_3 + 22_3$	10 + 8 = 18
O	O	L	$110_3 + 22_3$	12 + 8 = 20
O	O	O	$111_3 + 22_3$	13 + 8 = 21

8 Assembly Drawing and PCB Layout

The top assembly drawing and individual PCB layers for the TPS2359EVM are shown in the following figures.

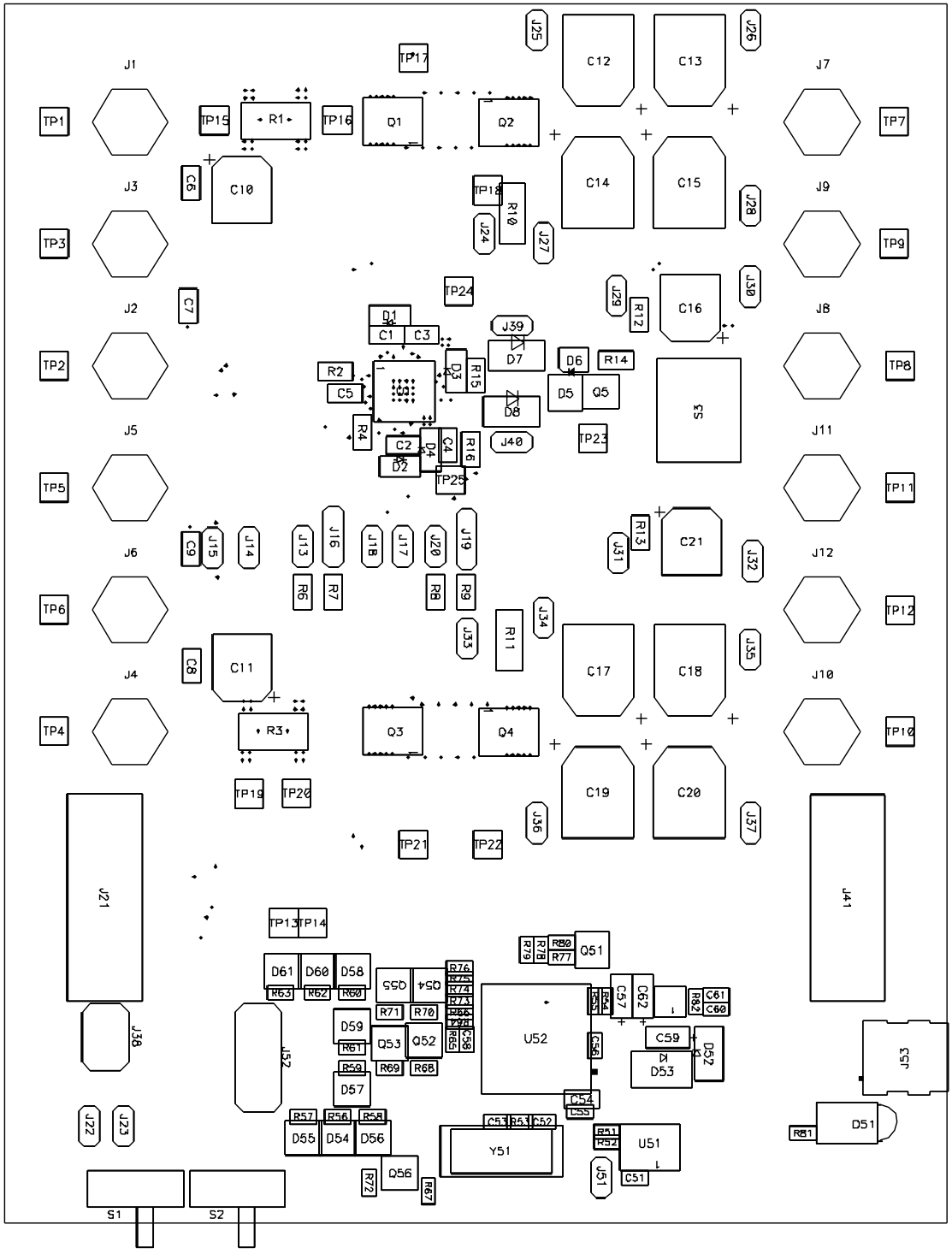


Figure 10. EVM Top Assembly Drawing

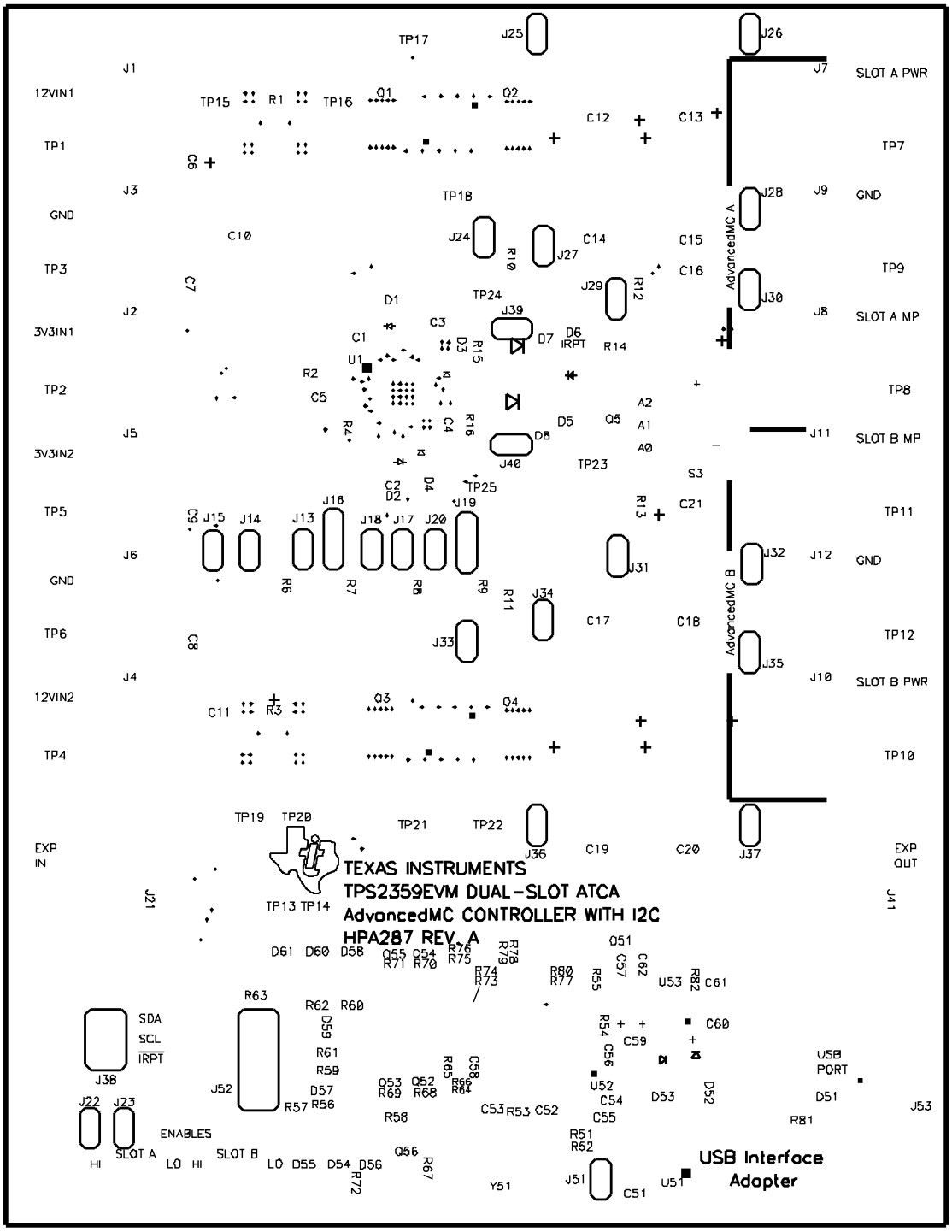


Figure 11. Top Side Silk Screen

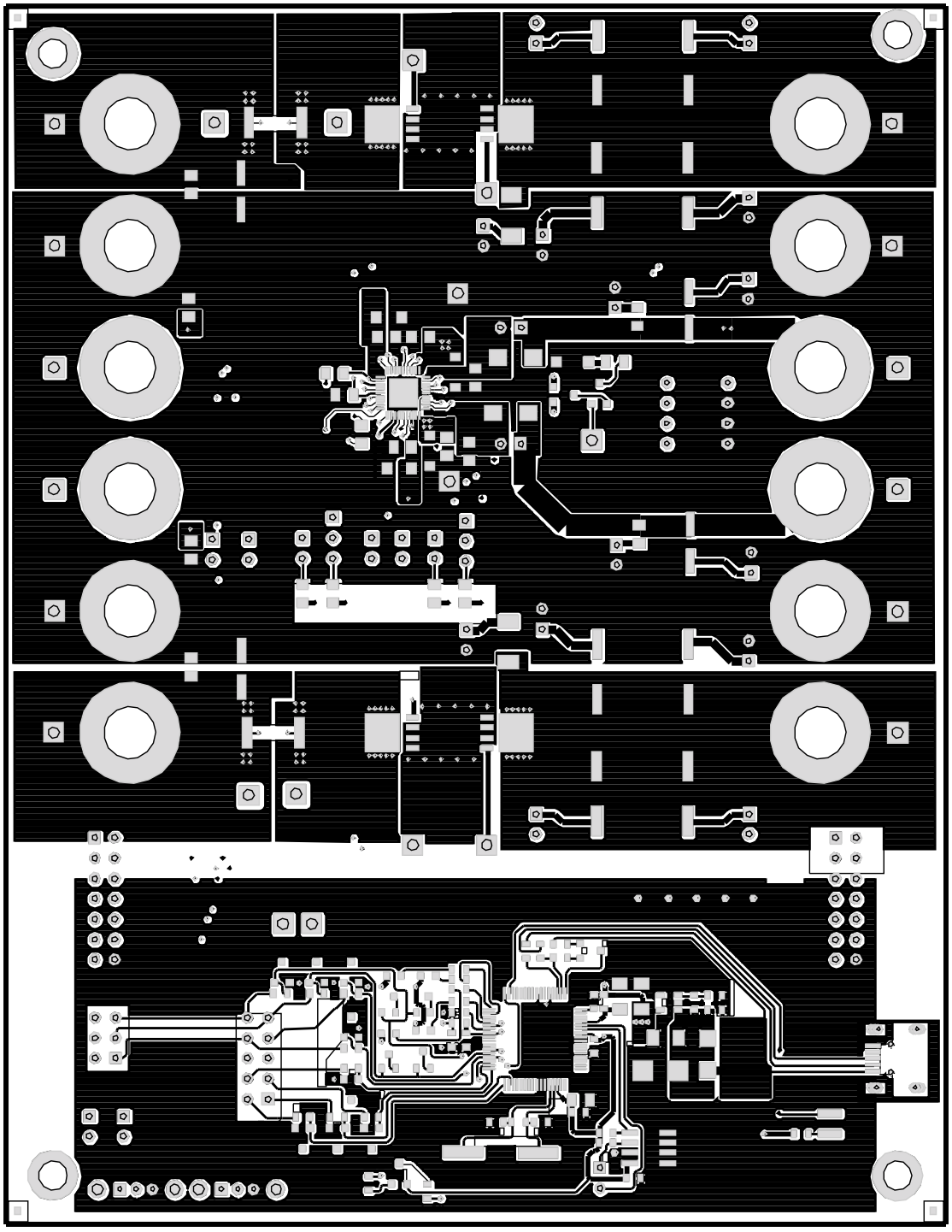


Figure 12. PCB Top Layer

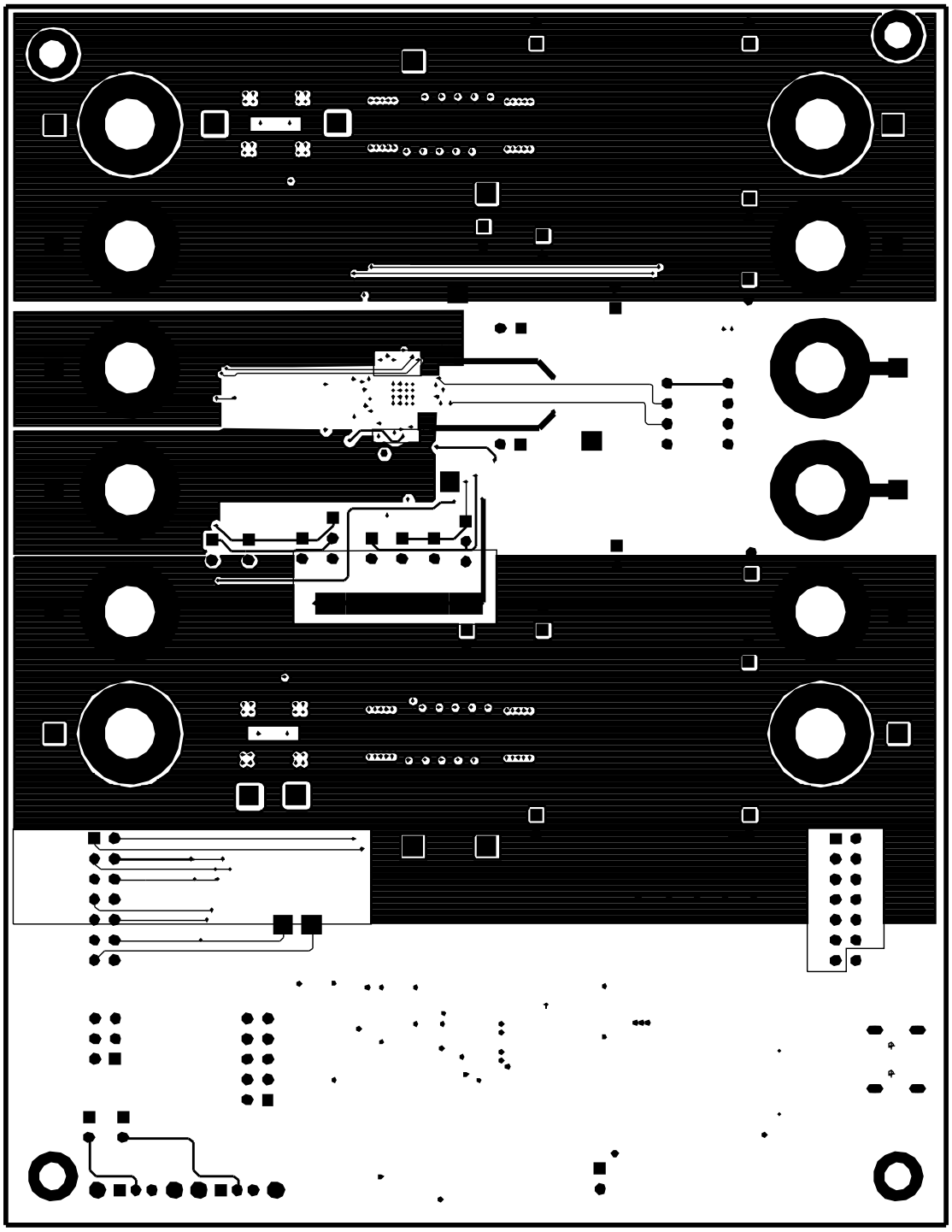


Figure 13. PCB Layer 2

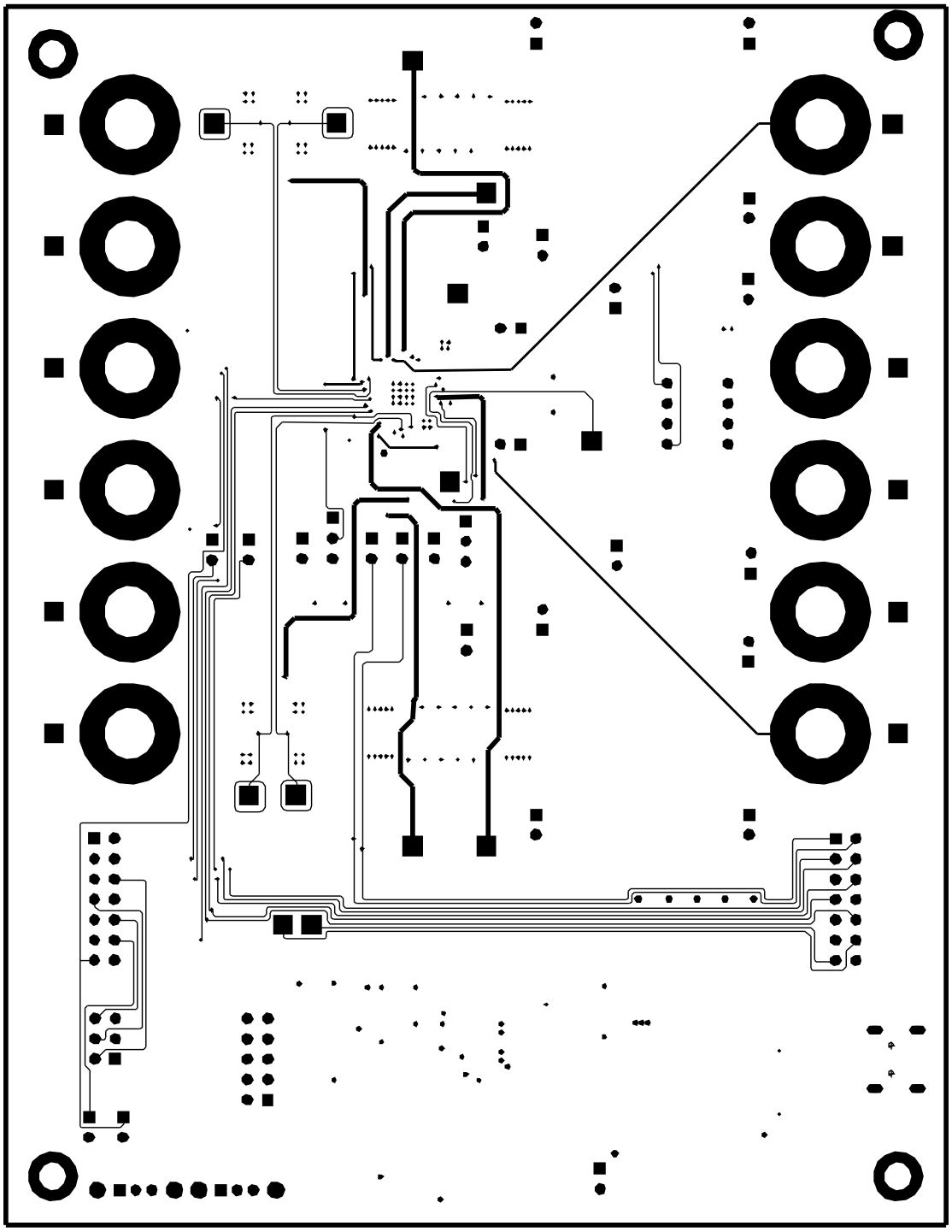


Figure 14. PCB Layer 3

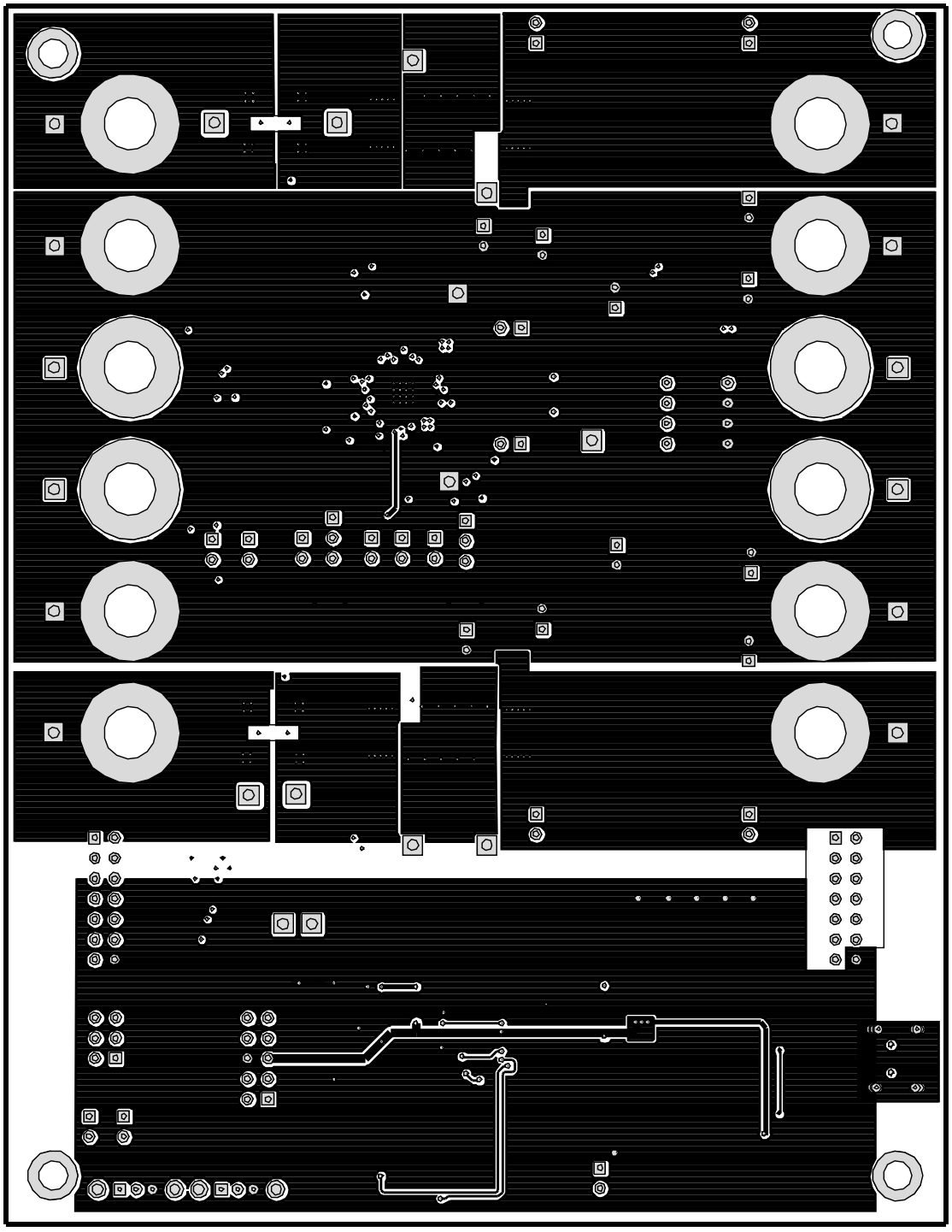


Figure 15. PCB Bottom Layer

9 List of Materials

Table 10. List of Materials[1][2][3]

REF DES	COUNT	DESCRIPTION	PART NUMBER	MFR
C1, C2, C3, C4, C5	5	Capacitor, ceramic, 0.1 µF, 25 V, X7R, 20%, 0805	Std	Std.
C10, C11	2	Capacitor, aluminum, SM, 47 µF, 25 V, 20%, Case D	EEV-FK1E470P	Panasonic
C12, C13, C14, C15, C17, C18, C19, C20	8	Capacitor, aluminum, SM, 220 µF, 25 V, 20%, Case F	EEV-FK1E221P	Panasonic
C16, C21	2	Capacitor, aluminum, SM, 150 µF, 10 V, 20%, Case D	EEV-FK1A151P	Panasonic
C51, C55, C56, C58, C60, C61	6	Capacitor, ceramic, 0.1 µF, 25 V, X7R, 20%, 0603	Std	Std
C52, C53	2	Capacitor, ceramic, 22 pF, 50 V, C0G, 10%, 0603	Std	Std
C54	1	Capacitor, ceramic, 1000 pF, 100 V, C0G, 5%, 0805	Std	Std
C57	1	Capacitor, tantalum, 1 µF, 16 V, 20%, 3216	293D105X0016A2T	Vishay
C59, C62	2	Capacitor, tantalum, 10 µF, 10 V, 20%, 3216	293D106X0010A2T	Vishay
C6, C7, C8, C9	4	Capacitor, ceramic, 1 µF, 25 V, X7R, 20%, 0805	Std	Std
D1, D2	2	Diode, zener, 15 V at 50 mA, 800 mW max., Pzsm = 300 W, D0-219AB	BZD27C15P	Vishay
D3, D4	2	Diode, zener, 4.3 V, 500 mW max., SOD-123	BZT52C4V3	Diodes
D5	1	Diode, dual Schottky, com. cathode, 30 V, 200 mA, SOT-23	BAT54C	Diodes
D51	1	Diode, LED, green, 20 mA, 30 mcd, SMD	SSF-LXH305GD-TR	Lumex
D52	1	Diode, Schottky, 1 A, 30 V, SMA	MBRA130	IR
D53	1	Diode, zener, 7.5 V, 3 W, SMB	1SMB5922BT3	On Semi
D54, D55, D56, D57, D58, D59, D60, D61	8	Diode, TVS, low cap., V(RM) = 5 V, 300 W Pk., SOT-23	GL05T	Vishay
D6	1	Diode, LED, red, GW type, 20 mA, GW	LN1261CAL	Panasonic
D7, D8	2	Diode, Schottky, 1 A, 20 V, SMA	B120	Diodes

(1) "TH" package designation indicates "thru-hole" (leaded) component.
(2) Part number information is for reference only to further illustrate component characteristics; substitution of other mfgrs' part of equal or better specification is permissible. Substitution NOT allowed on part numbers marked with double asterisk (**).
(3) Double pound sign ('##') after part number indicates preferred device. Acceptable substitutes are listed afterwards, in decreasing order of preference.

Table 10. List of Materials (continued)

REF DES	COUNT	DESCRIPTION	PART NUMBER	MFR
J1, J2, J3, J4, J5, J6, J7, J8, J9, J10, J11, J12	12	Jack, banana, non-ins., PC mount, TH	3267	Pomona
J13, J14, J15, J17, J18, J20, J22, J23, J24, J25, J26, J27, J28, J29, J30, J31, J32, J33, J34, J35, J36, J37, J39, J40, J51	25	Header, 2 pin, 100-mil spacing, 0.100 in. x 2	PEC36SAAN	Sullins
J16, J19	2	Header, 3 pin, 100-mil spacing, 0.100 in. x 3	PEC36SAAN	Sullins
J21, J41	2	Header, PCB mnt., vert., 2 x 7, 100 mil spacing	2514-6002UB	3M
J38	1	Header, 2 x 3-pin, 100-mil spacing, 0.100 in. x 2 x 3	PEC36DAAN	Sullins
J52	0	Header, 2 x 5-pin, 100-mil spacing, 0.100 in. x 2 x 5	PEC36DAAN	Sullins
J53	1	Connector, recpt, USB-B, mini, 5-pins, SMT, 0.354 in. x 0.303 in.	UX60-MB-5S8	Hirose
Q1, Q3	2	Transistor, NFET, 30 V, 100A, $R_{DS(on)}$ < 5 mΩ, TDSON-8	BSC016N03LSG## or BSC022N03SG	Infineon
Q2, Q4	2	Transistor, NFET, 30 V, $R_{DS(on)}$ < 20 mΩ, TDSON-8	BSC057N03LSG## or BSC050N03LSG or BSC042N03LSG or BSC022N03SG or BSC016NO3LSG	Infineon
Q5	1	Transistor, PFET, -30 V, 1 A, SOT-23	FDN352AP**	Fairchild
Q51	1	Transistor, NPN, 40 V, 500 mA, SOT-23	MMBT2222A	Fairchild
Q52, Q53, Q54, Q55, Q56	5	Transistor, PFET, -50 V, 130 mA, $R_{DS(on)}$ < 10 Ω at V_{GS} = 5 V, SOT-23	BSS84	Fairchild
R1, R3	2	Resistor, metal strip, 1 W, 1%, 2512	WSL2512-5L000FEA	Vishay-Dale
R10, R11	2	Resistor, chip, 1 kΩ, 1/2 W, 5%, 2010	Std	Std
R12, R13	2	Resistor, chip, 270 Ω, 1/10 W, 5%, 0805	Std	Std
R14	1	Resistor, chip, 100 Ω, 1/10 W, 5%, 0805	Std	Std
R15, R16	0	Resistor, chip, 1/10 W, 5%, 0805	Std	Std
R2, R4	2	Resistor, chip, 422 Ω, 1/10 W, 1%, 0805	Std	Std
R51, R52, R77	3	Resistor, chip, 1.5 kΩ, 1/16 W, 5%, 0603	Std	Std
R53	1	Resistor, chip, 1.00 M, 1/16 W, 1%, 0603	Std	Std
R54, R80	2	Resistor, chip, 15 kΩ, 1/16 W, 5%, 0603	Std	Std
R55, R64, R65, R66, R82	5	Resistor, chip, 100 kΩ, 1/16 W, 5%, 0603	Std	Std
R56, R57, R58, R59, R60, R61, R62, R63, R72, R73, R74, R75, R76, R78, R79	15	Resistor, chip, 33 Ω, 1/16 W, 5%, 0603	Std	Std
R6, R7	2	Resistor, chip, 6.81 kΩ, 1/10 W, 1%, 0805	Std	Std
R67, R68, R70	3	Resistor, chip, 2.2 kΩ, 1/16 W, 5%, 0603	Std	Std
R69, R71	2	Resistor, chip, 1 kΩ, 1/16 W, 5%, 0603	Std	Std
R8, R9	2	Resistor, chip, 3.32 kΩ, 1/10 W, 1%, 0805	Std	Std
R81	1	Resistor, chip, 200 Ω, 1/16 W, 5%, 0603	Std	Std
S1, S2	2	Switch, slide, SPDT, Rt. angle, 200 mA, TH	EG1213**	E-Switch
S3	1	Switch, DIP, 4 pos., raised rocker, 0.38 x 0.48 inch	76SB04S(T) or BD04	Grayhill or C&K Switch

Table 10. List of Materials (continued)

REF DES	COUNT	DESCRIPTION	PART NUMBER	MFR
TP1, TP2, TP4, TP5, TP7, TP8, TP10, TP11, TP13, TP14, TP15, TP16, TP17, TP18, TP19, TP20, TP21, TP22, TP23	19	Test point, white, 0.062 in. hole, TH	5012	Keystone
TP3, TP6, TP9, TP12, TP24, TP25	6	Test point, black, 0.062 in. hole, TH	5011	Keystone
U1	1	Full-Featured Dual-Slot AdvancedMC Controller, QFN-36	TPS2359RHH**	Texas Instruments
U51	1	Serial EEPROM, 64K, 2.5-5.5V, 400 kHz Max., SO-8	24LC64I-SN	Microchip
U52	1	USB, General Purpose Device Controller, PQFP-64	TUSB3210PM**	Texas Instruments
U53	1	Micro-Power 150 mA LDO Regulator, 3.3 V, SOT-23-5	TPS76333DBV**	Texas Instruments
Y51	1	Crystal, 12-MHz, 20 pF, +/- 50 PPM AT 25°C, 0.185 x 0.532	CY12BPSMD	Crystek
N/A	1	PCB, FR-4, 4-layer, SMOBC, 4.63" x 6.0" x .062"	HPA287A**	Any
N/A	26	Shunt, open-top	151-8000	Kobiconn
N/A	4	Spacer, nylon, hex, #6-32, 0.625"	14HTSP020	Eagle
N/A	4	Screw, nylon, rnd Hd, #6-32, 0.25"	010632R025	Eagle
N/A	1	USB cable, 5-pin, B-Mini male to type A male, 2m	AK672M/2-2	Assman

EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 0 V to 13.8 V and the output voltage range of 0 V and 13.8 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than xxx°C. The EVM is designed to operate properly with certain components above xxx°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

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