## Features

- ESD Protect for 4 high-speed I/O channels
- Provide ESD protection for each channel to
  **IEC 61000-4-2 (ESD) ±30kV (air / contact)**
  **IEC 61000-4-4 (EFT) ±70A (5/50ns)**
  **IEC 61000-4-5 (Lightning) ±10A (8/20μs) for any I/O-to-GND**
  **IEC 61000-4-5 (Lightning) ±16A (8/20μs) for VDD-to-GND**
- For low operating voltage applications: 5V, maximum
- Low capacitance : 1.8pF typical
- Fast turn-on and Low clamping voltage
- Array of surge rated diodes with internal equivalent TVS diode
- Small package saves board space
- Solid-state silicon-avalanche and active circuit triggering technology
- ***Green Part***

## Applications

- LAN applications
- Notebook and PC Computers
- Handheld electronics
- Monitors and Flat Panel Displays
- USB 2.0 data lines protection
- Video lines protection

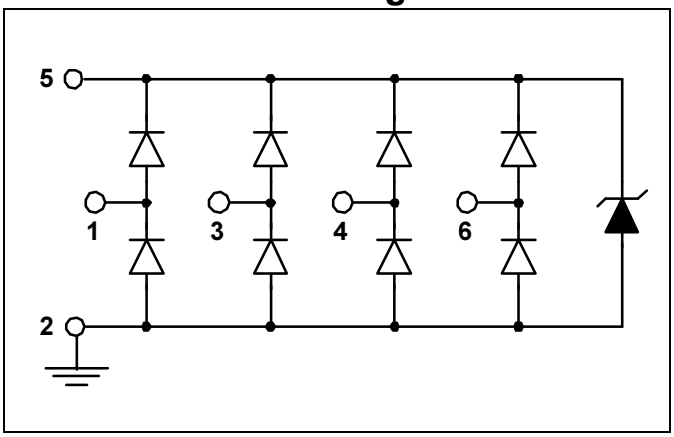
## Description

AZC615-04S is a high performance design which includes surge rated diode arrays to protect high speed data interfaces. The AZC615-04S has been specifically designed to protect sensitive components, which are connected to data and transmission lines, from over-voltage caused by Electrostatic Discharging (ESD), Electrical Fast Transients (EFT), and Lightning.

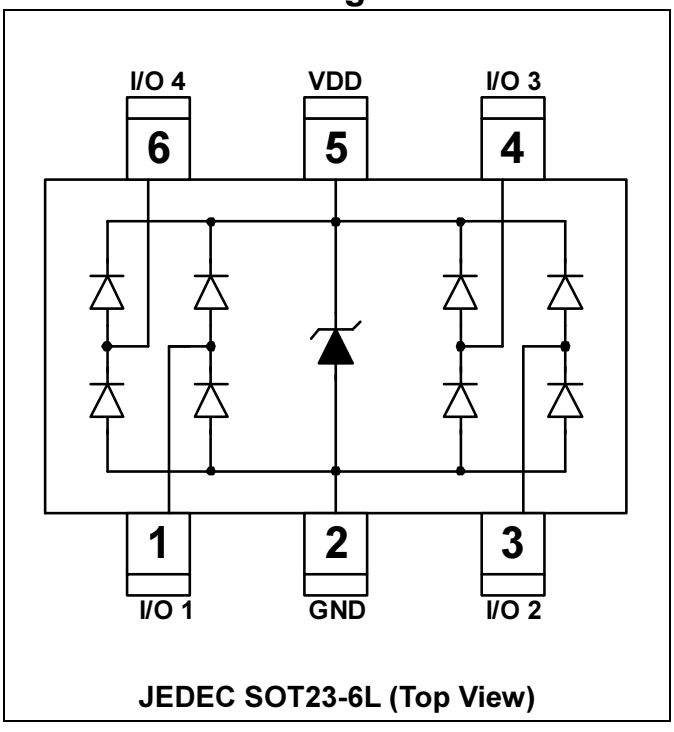
AZC615-04S is a unique design which includes surge rated, low capacitance steering diodes and a unique design of clamping cell which is an equivalent TVS diode in a single package. During transient conditions, the steering diodes direct the transient to either the internal ESD line or to the ground line. The internal unique design of clamping cell prevents over-voltage on the internal ESD line and I/O lines, which is protecting any downstream components.

AZC615-04S may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (± 15kV air, ±8kV contact discharge).

## Circuit Diagram




## Pin Configuration




**JEDEC SOT23-6L (Top View)**

## SPECIFICATIONS

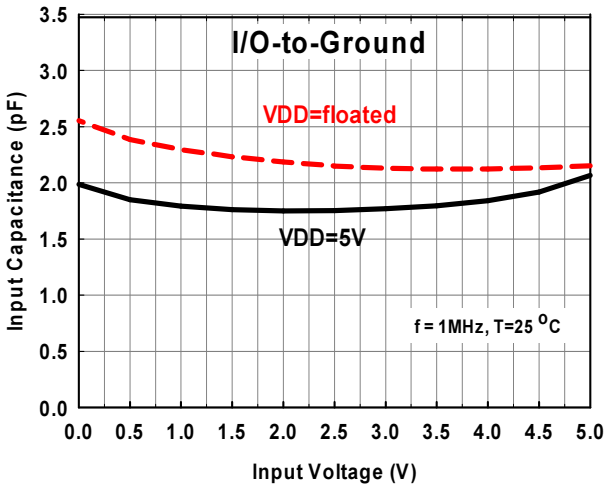
| **ABSOLUTE MAXIMUM RATINGS** ($T_A$= 25°C, unless otherwise specified) | | | |
|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **RATING** | **UNITS** |
| Peak Pulse Current (tp =8/20μs, I/O-to-GND)<br>Peak Pulse Current (tp =8/20μs, VDD-to-GND) | $I_{PP}$ | ±10<br>±16 | **A** |
| Operating Supply Voltage (VDD-to-GND) | $V_{DC}$ | 5.5 | **V** |
| ESD per IEC 61000-4-2 (Air / Contact) | $V_{ESD}$ | ±30 | **kV** |
| Lead Soldering Temperature | $T_{SOL}$ | 260 (10 sec.) | **°C** |
| Operating Temperature | $T_{OP}$ | -55 to +125 | **°C** |
| Storage Temperature | $T_{STO}$ | -55 to +150 | **°C** |

| **ELECTRICAL CHARACTERISTICS** | | | | | | |
|---|---|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **CONDITIONS** | **MIN** | **TYP** | **MAX** | **UNITS** |
| Reverse Stand-Off Voltage | $V_{RWM}$ | Pin 5 to Pin 2, T=25 °C | | | 5 | **V** |
| Reverse Leakage Current | $I_{Leak}$ | $V_{RWM}$ = 5V, T=25 °C, Pin 5 to Pin 2 | | | 1 | **μA** |
| Channel Leakage Current | $I_{CH-Leak}$ | $V_{pin5}$ = 5V, $V_{pin2}$ = 0V, T=25 °C | | | 1 | **μA** |
| Reverse Breakdown Voltage | $V_{BV}$ | $I_{BV}$ = 1mA, T=25 °C, Pin 5 to Pin 2 | 6 | | 9 | **V** |
| Forward Voltage | $V_F$ | $I_F$ = 15mA, T=25 °C, Pin 2 to Pin 5 | | 0.8 | 1.2 | **V** |
| ESD Clamping Voltage – I/O (Note 1) | $V_{clamp\_io}$ | IEC 61000-4-2 +8kV ($I_{TLP}$ = 16A), T=25 °C, contact mode, any I/O-to-GND | | 10.5 | | **V** |
| ESD Clamping Voltage – VDD (Note 1) | $V_{clamp\_VDD}$ | IEC 61000-4-2 +8kV ($I_{TLP}$ = 16A), T=25 °C, contact mode, VDD pin to GND | | 8 | | **V** |
| ESD Dynamic Turn on Resistance – I/O | $R_{dynamic\_io}$ | IEC 61000-4-2, 0~+8kV, T=25 °C, contact mode, any I/O-to-GND | | 0.22 | | Ω |
| ESD Dynamic Turn on Resistance – VDD | $R_{dynamic\_VDD}$ | IEC 61000-4-2, 0~+8kV, T=25 °C, contact mode, VDD pin to GND | | 0.12 | | Ω |
| Lightning Clamping Voltage | $V_{lightning}$ | $I_{PP}$=5A, tp=8/20μs, T=25 °C, any I/O-to-GND | | 7 | | **V** |
| | | $I_{PP}$=10A, tp=8/20μs, T=25 °C, any I/O-to-GND | | 8.5 | | |
| Channel Input Capacitance – 1 | $C_{IN-1}$ | $V_{pin5}$ =5V, $V_{pin2}$ =0V, $V_{IN}$ =2.5V, f =1MHz, T=25 °C, any I/O-to-GND | | 1.8 | 2.5 | **pF** |
| Channel Input Capacitance – 2 | $C_{IN-2}$ | $V_{pin5}$ =floated, $V_{pin2}$ =0V, $V_{IN}$ =2.5V, f=1MHz, T=25 °C, any I/O-to-GND | | 2.2 | 2.8 | **pF** |
| Channel to Channel Input Capacitance | $C_{CROSS}$ | $V_{pin5}$ = $V_{pin2}$=floated, $V_{IN}$ =2.5V, f =1MHz, T=25 °C, between I/O pins | | 1.2 | 1.5 | **pF** |

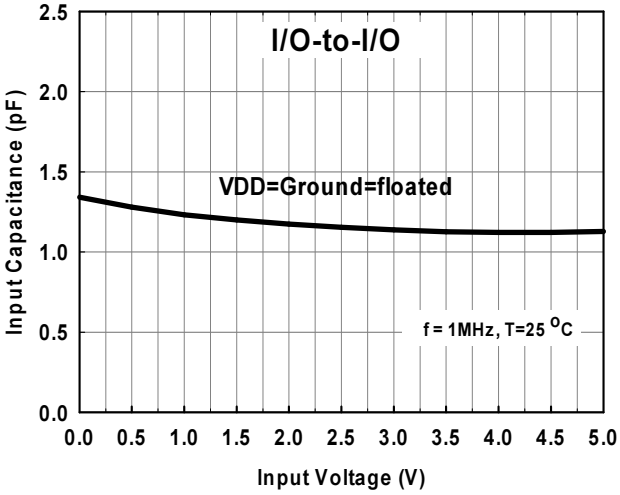
Note 1: ESD Clamping Voltage was measured by Transmission Line Pulsing (TLP) System.
TLP conditions: $Z_0$= 50Ω, $t_p$= 100ns, $t_r$= 1ns.

## Typical Characteristics

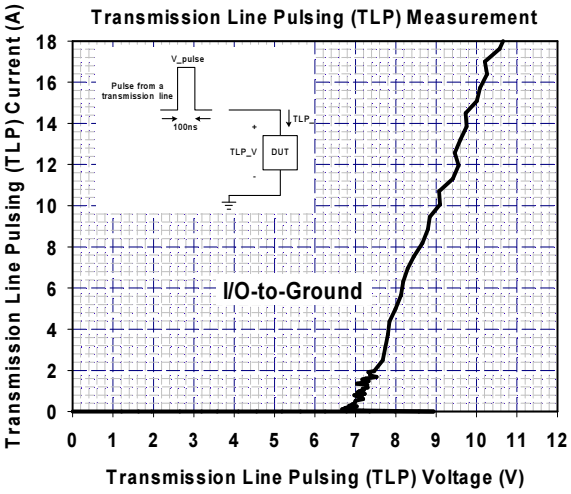
Typical Variation of $C_{IN}$ vs. $V_{IN}$



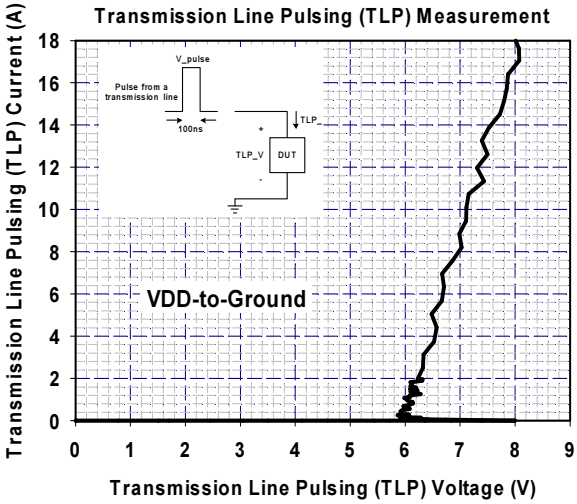

Typical Variation of $C_{I/O\text{-}to\text{-}I/O}$ vs. $V_{IN}$



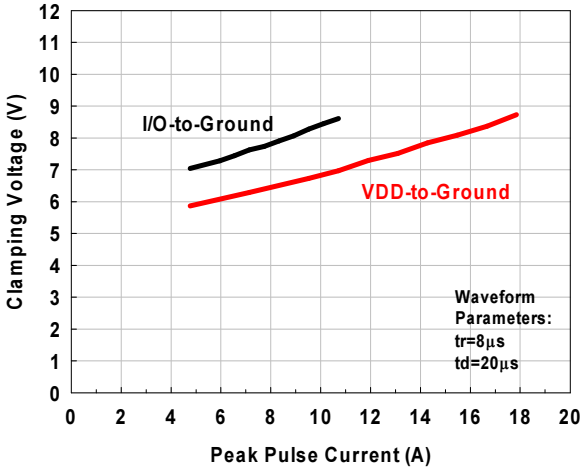

Transmission Line Pulsing (TLP) Measurement




Transmission Line Pulsing (TLP) Measurement




Clamping Voltage vs. Peak Pulse Current



## Applications Information

The AZC615-04S is designed to protect four data lines and power rails from transient over-voltage (such as ESD stress pulse). The device connection of AZC615-04S is shown in the Fig. 1. In Fig. 1, the four protected data lines are connected to the ESD protection pins (pin1, pin3, pin4, and pin6) of AZC615-04S. The ground pin (pin2) of AZC615-04S is a negative reference pin. To get minimum parasitic inductance, the path length should keep as short as possible. In addition, the power pin (pin 5) of AZC615-04S is a positive reference pin. The VDD rail also can be protected by the power-rail ESD clamped circuit (not shown) of AZC615-04S.

AZC615-04S can provide protection for 4 I/O signal lines simultaneously. If the number of I/O signal lines is less than 4, the unused I/O pins can be simply left as NC pins.

In some cases, systems are not allowed to be reset or restart after the ESD stress directly applying at the I/O-port connector. Under this situation, in order to enhance the sustainable ESD Level, a 0.1μF chip capacitor can be added between the VDD and GND rails. The place of this chip capacitor should be as close as possible to the AZC615-04S.

In some cases, there isn't power rail presented on the PCB. Under this situation, the power pin (pin 5) of AZC615-04S can be left as floated. The protection will not be affected, only the load capacitance of I/O pins will be slightly increased. Fig. 2 shows the detailed connection.

In some cases, there aren't VDD and GND rails presented on the PCB. Under this situation, the ground pin (pin 2) of AZC615-04S can also be left as floated. The I/O to I/O protection will not be affected. Fig. 3 shows the detailed connection.

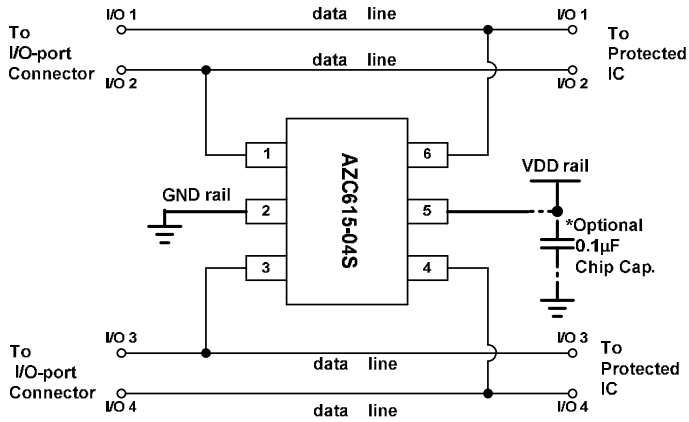



**Fig. 1 Data lines and power rails connection of AZC615-04S.**

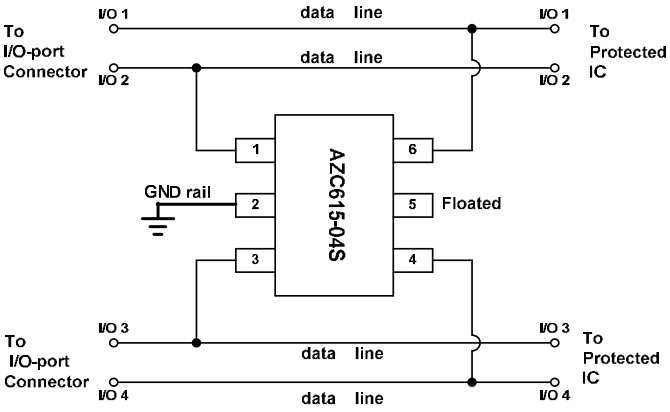



**Fig. 2 Data lines and power rail connection of AZC615-04S. Pin5 is left as floating.**

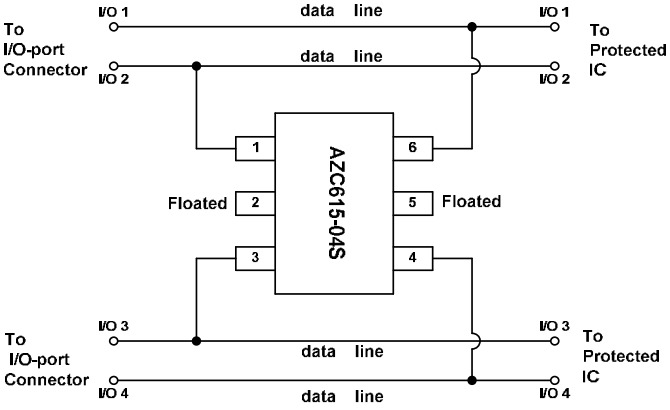


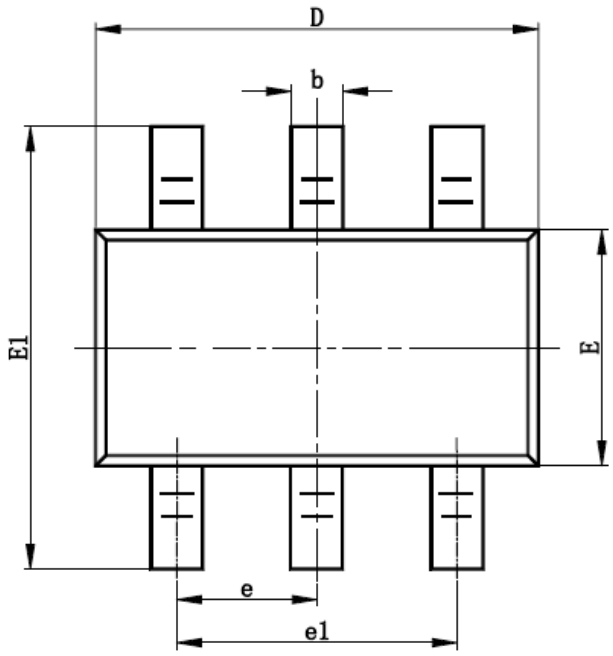

**Fig. 3 Data lines connection of AZC615-04S. Pin2 and Pin5 are left as floating when AZC615-04S provides protection of I/O-to-I/O.**

## Mechanical Details

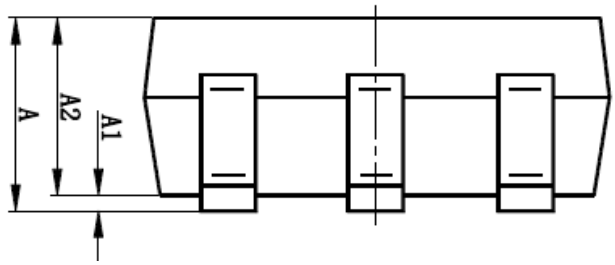
**SOT23-6L**

PACKAGE DIAGRAMS

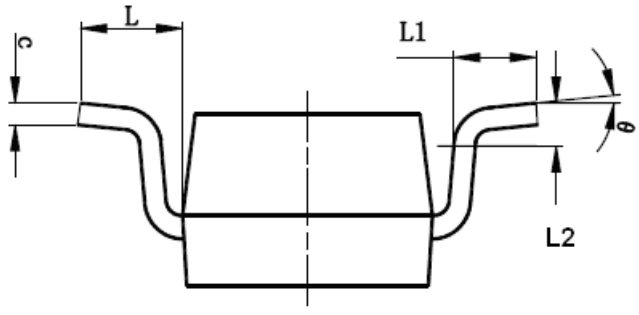
TOP VIEW




SIDE VIEW




END VIEW



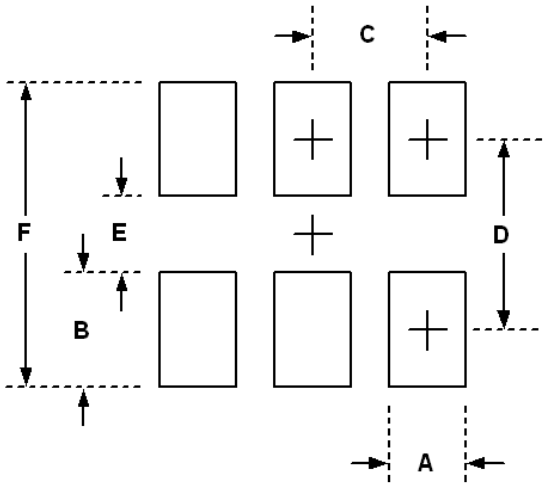

PACKAGE DIMENSIONS

| Symbol | Millimeters | | Inches | |
|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. |
| A | | 1.25 | | 0.049 |
| A1 | 0 | 0.15 | 0.000 | 0.006 |
| A2 | 0.9 | 1.3 | 0.035 | 0.051 |
| b | 0.3 | 0.5 | 0.012 | 0.020 |
| c | 0.08 | 0.21 | 0.003 | 0.008 |
| D | 2.72 | 3.12 | 0.107 | 0.123 |
| E | 1.4 | 1.8 | 0.055 | 0.071 |
| E1 | 2.6 | 3 | 0.102 | 0.118 |
| e | 0.95BSC | | 0.037BSC | |
| e1 | 1.9BSC | | 0.075BSC | |
| L1 | 0.3 | 0.6 | 0.012 | 0.024 |
| L | 0.7REF | | 0.028REF | |
| L2 | 0.25BSC | | 0.010BSC | |
| θ | 0 | 8 | 0 | 8 |

Notes:

- This dimension complies with JEDEC outline standard MO-178 Variation AB.
- Dimensioning and tolerancing per ASME Y14.5M-1994.
- All dimensions are in millimeters, and the dimensions in inches are for reference only.
- 1mm = 40 mils = 0.04 inches.

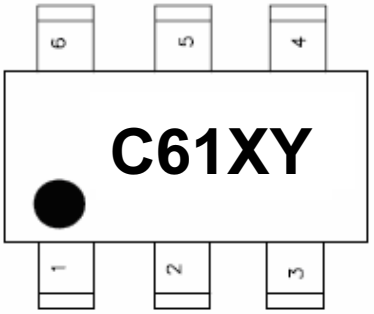
## LAND LAYOUT




| Dimensions | | |
|---|---|---|
| **Index** | **Millimeter** | **Inches** |
| **A** | 0.60 | 0.024 |
| **B** | 1.10 | 0.043 |
| **C** | 0.95 | 0.037 |
| **D** | 2.50 | 0.098 |
| **E** | 1.40 | 0.055 |
| **F** | 3.60 | 0.141 |

Notes:
This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

## MARKING CODE




| Part Number | Marking Code |
|---|---|
| AZC615-04S.R7G (Green Part) | C61XY |

Green means Pb-free, RoHS, and Halogen free compliant.

C61 = Device Code
X = Date Code
Y = Control Code

## Ordering Information

| PN# | Material | Type | Reel size | MOQ | MOQ/internal box | MOQ/carton |
|---|---|---|---|---|---|---|
| AZC615-04S.R7G | Green | T/R | 7 inch | 3,000/reel | 4 reels=12,000/box | 6 boxes=72,000/carton |

## Revision History

| Revision | Modification Description |
|---|---|
| Revision 2017/04/27 | Formal Release. |
| | |
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