NOT RECOMMENDED FOR NEW DESIGNS
RECOMMENDED REPLACEMENT PART
ISL97672B

DATASHEET

ISL97672A

6-Channel LED Driver with Ultra Low Dimming Capability

FN7710
Rev.4.00
Sep 14, 2017

The ISL97672A is an integrated 6-channel power LED driver for LCD backlight applications. The ISL97672A is capable of driving LEDs with input from 4.5V to 26.5V and maximum output up to 45V.

The ISL97672A employs an adaptive boost switching architecture that allows Direct PWM dimming with dimming duty cycle as low as 0.007% at 200Hz or 0.8% at 20kHz. PWM Dimming frequency can be as high as 30kHz.

The ISL97672A employs the dynamic headroom control that monitors the highest LED forward voltage string for output regulation to minimize headroom voltage and power loss in a typical multi-string operation. Typical current matching between channels is ±0.7%.

The ISL97672A incorporates extensive protection functions that flag whenever a fault occurs. The protections include string-open and short-circuit detections, OVP, OTP, and an optional output short-circuit protection with external fault disconnect switch.

The ISL97672A is offered in a compact 20 Ld QFN 3x4 package and can operate in ambient temperatures of -40°C to +85°C.

Related Literature

- For a full list of related documents, visit our website
  - ISL97672A product page

Features

- 6 x 50mA Channels
- 4.5V to 26.5V Input
- 45V Output Max
- Adaptive Boost Switching Architecture
- Direct PWM Dimming with Dimming Linearity of 0.007%~100% at 200Hz or 0.8%~100% <20kHz
- Adjustable 200kHz to 1.4MHz Switching Frequency
- Dynamic Headroom Control
- Fault Protections with Latched Flag Indication
  - String Open/Short Circuit
  - OVP
  - OTP
  - Optional Output Short-Circuit Fault Protection Switch
- Current Matching ±0.7%
- 20 Ld 3x4 QFN Package

Applications

- Notebook Displays LED Backlighting
- LCD Monitor LED Backlighting
- Multi-Function Printer Scanning Light Source

Typical Application Circuit

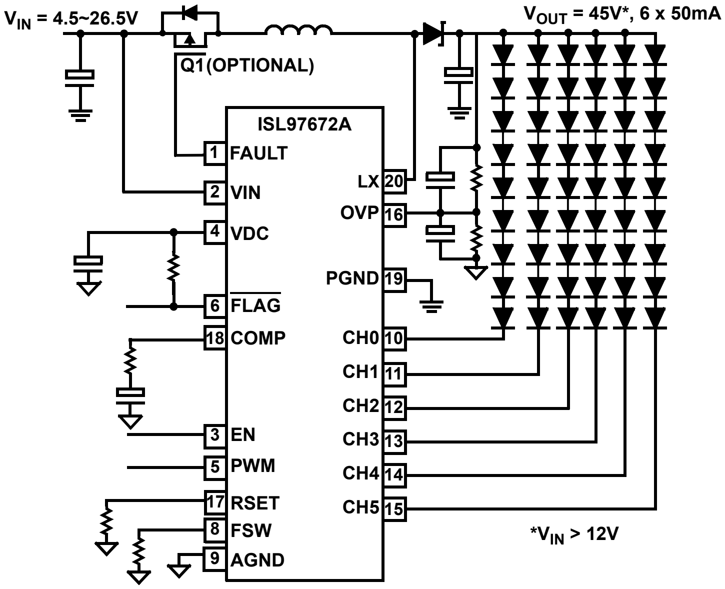


FIGURE 1. ISL97672A TYPICAL APPLICATION DIAGRAM

Block Diagram

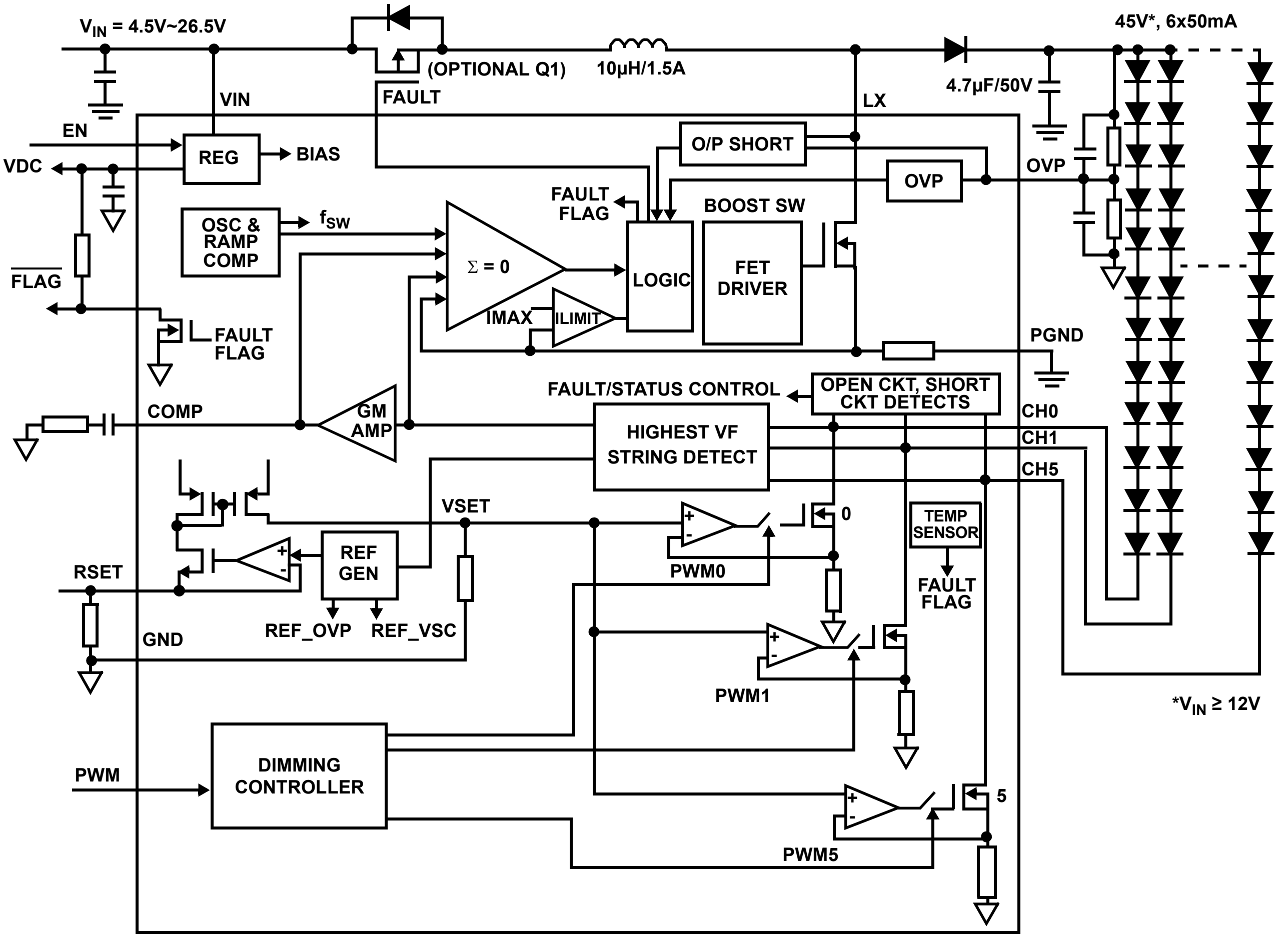


FIGURE 2. ISL97672A BLOCK DIAGRAM

Ordering Information

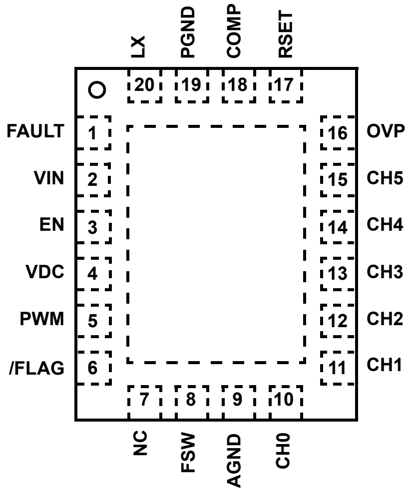
PART NUMBER (Notes 1, 2, 3)	PART MARKING	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL97672AIRZ	672A	20 Ld 3x4 QFN	L20.3x4
ISL97672AIRZ-EVALZ	Evaluation Board		

NOTES:

1. Add "-T" suffix for 6k unit or "-TK" for 1k unit tape and reel options. Refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL97672A. For more information on MSL, see Tech Brief TB363.

Pin Configuration

ISL97672A
(20 LD 3x4 QFN)
TOP VIEW



Pin Descriptions (I = Input, O = Output, S = Supply)

PIN NAME	PIN #	TYPE	DESCRIPTION
FAULT	1	O	A pull-down current output for external P-channel fault disconnect switch.
VIN	2	S	Input supply voltage for IC. Connect a 0.1µF decoupling capacitor close to this pin.
EN	3	I	IC enable pin. Pull high to enable the IC. If EN is low for longer than 30.5ms, IC will be disabled.
VDC	4	S	Internal 5V regulator. Connect a 1µF decoupling capacitor on VDC.
PWM	5	I	PWM input pin for direct PWM dimming control.
/FLAG	6	O	/FLAG is latched low under any fault condition and resets after input power is recycled or part is re-enabled. This pin is an open drain that needs pull-up.
NC	7	I	No Connect.
FSW	8	I	Boost switching frequency set pin. Connect a resistor between this pin and ground to set up desired boost switching frequency. See "Switching Frequency" on page 9 for resistance calculation.
AGND	9	S	Analog Ground for precision circuits.
CH0, CH1 CH2, CH3 CH4, CH5	10, 11, 12, 13, 14, 15	I	Current source and channel monitoring input for channel 0, 1, 2 3, 4, 5.
OVP	16	I	Overvoltage protection input. See "OVP and V_{OUT}" on page 10.
RSET	17	I	LED DC current set pin. Connect a resistor between this pin and ground to set up maximum LED DC current. See "Maximum DC Current Setting" on page 9 for resistance calculation.
COMP	18	O	Boost compensation pin. Connect an RC compensation network between this pin and GND to optimize boost stability and transient response.
PGND	19	S	Power ground.
LX	20	O	Boost converter switching node.

Absolute Maximum Ratings (T_A = +25°C)

VIN, EN	-0.3V to 28V
FAULT	VIN - 8.5V to VIN + 0.3V
VDC, COMP, RSET, PWM, OVP, FSW	-0.3V to 5.5V
CH0 - CH5, LX	-0.3V to 45V
PGND, AGND	-0.3V to 0.3V

NOTE: Voltage ratings are with respect to AGND pin.

ESD Rating

Human Body Model (Tested per JESD22-A114E)	3kV
Machine Model (Tested per JESD22-A115-A)	300V
Charged Device Model	1kV

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
20 Ld QFN Package (Notes 4, 5, 7)	40	2.5
Thermal Characterization (Typical)		PSI_{JT} (°C/W)
20 Ld QFN Package (Note 6)		1
Maximum Continuous Junction Temperature		+125°C
Storage Temperature		-65°C to +150°C

Operating Conditions

Temperature Range	-40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See TB379.
5. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.
6. PSI_{JT} is the junction-to-top thermal resistance. If the package top temperature can be measured, with this rating then the die junction temperature can be estimated more accurately than the θ_{JA} and θ_{JC} thermal resistance ratings.
7. Refer to JESD51-7 high effective thermal conductivity board layout for proper via and plane designs.

Electrical Specifications

All specifications are tested at T_A = +25°C, V_{IN} = 12V, EN = 5V, R_{SET} = 20.5kΩ, unless otherwise noted. **Boldface limits apply over the operating junction temperature range, -40°C to +85°C.**

PARAMETER	DESCRIPTION	CONDITION	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
GENERAL						
V_{IN} (Note 10)	VIN Supply Voltage	T_C = <+60°C T_A = +25°C	4.5		26.5	V
IVIN	VIN Current	EN = 5V		5		mA
IVIN_STBY	VIN Shutdown Current	T_A = +25°C			5	µA
V_{OUT}	Output Voltage	4.5V < V_{IN} ≤ 26V, F_{SW} = 600kHz			**45**	V
		8.55V < V_{IN} ≤ 26V, F_{SW} = 1.2MHz			**45**	V
		4.5V < V_{IN} ≤ 8.55V, F_{SW} = 1.2MHz			**V_{IN}/0.19**	V
V_{UVLO}	Undervoltage Lock-out Threshold		**2.1**		**2.6**	V
V_{UVLO_HYS}	Undervoltage Lock-out Hysteresis			200		mV
ENABLE AND PWM GENERATOR						
V_{IL}	Guaranteed Range for PWM Input Low Voltage				**0.8**	V
V_{IH}	Guaranteed Range for PWM Input High Voltage		**1.5**		**VDD**	V
FPWM	PWM Input Frequency Range		**200**		**30,000**	Hz
t_{ON}	Minimum On Time		**250**		**350**	ns
REGULATOR						
VDC	LDO Output Voltage	V_{IN} > 6V	**4.55**	4.8	**5**	V
IVDC_STBY	Standby Current	EN = 0V			**5**	µA
VLDO	VDC LDO Droop Voltage	V_{IN} > 5.5V, 20mA		20	**200**	mV
EN_{Low}	Guaranteed Range for EN Input Low Voltage				**0.5**	V
EN_{Hi}	Guaranteed Range for EN Input High Voltage		**1.8**			V

Electrical Specifications

All specifications are tested at T_A = +25°C, V_{IN} = 12V, EN = 5V, R_{SET} = 20.5kΩ, unless otherwise noted. **Boldface limits apply over the operating junction temperature range, -40°C to +85°C.**

PARAMETER	DESCRIPTION	CONDITION	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
t_{ENLow}	EN Low Time Before Shut-down			30.5		ms
BOOST						
SW_{ILimit}	Boost FET Current Limit		**1.5**	2.0	**2.7**	A
$r_{DS(ON)}$	Internal Boost Switch ON-Resistance	T_A = +25°C		235	300	mΩ
SS	Boost Soft-start Time	100% LED Duty Cycle		7		ms
Eff_peak	Peak Efficiency	V_{IN} = 12V, 72 LEDs, 20mA each, L = 10µH with DCR 101mΩ, T_A = +25°C		92.9		%
		V_{IN} = 12V, 60 LEDs, 20mA each, L = 10µH with DCR 101mΩ, T_A = +25°C		90.8		%
$\Delta I_{OUT}/\Delta V_{IN}$	Line Regulation			0.1		%
D_{max}	Boost Maximum Duty Cycle	F_{SW} = 600kHz	**90**			%
		F_{SW} = 1.2MHz	**81**			%
D_{min}	Boost Minimum Duty Cycle	F_{SW} = 600kHz			**9.5**	%
		F_{SW} = 1.2MHz			**17**	%
f_S	Minimum Switching Frequency	R_{FSW} = 200kΩ	**175**	200	**235**	kHz
f_S	Maximum Switching Frequency	R_{FSW} = 33kΩ	**1.312**	1.50	**1.69**	MHz
$I_{LX\_leakage}$	LX Leakage Current	LX = 45V, EN = 0			**10**	µA
CURRENT SOURCES						
I_{MATCH}	Channel-to-Channel Current Matching	R_{SET} =20.5kΩ (I_{OUT} = 20mA)		±0.7	**±1.0**	%
I_{ACC}	Current Accuracy		**-1.5**		**+1.5**	%
$V_{headroom20}$	Dominant Channel Current Source Headroom at CHx Pin measured with I_{LED}= 20mA	I_{LED} = 20mA T_A = +25°C		500 (Notes 9, 11)		mV
$V_{headroom33}$	Dominant Channel Current Source Headroom at CHx Pin measured with I_{LED}= 33mA	I_{LED} = 33mA T_A = +25°C	560 (Note 9)	710 (Note 11)	860 (Note 9)	mV
$V_{HEADROOM\_RANGE}$	Dominant Channel Current Sink Headroom Range at CHx Pin	I_{LED} = 20mA, T_A = +25°C		90		mV
V_{RSET}	Voltage at RSET Pin	R_{SET} = 20.5kΩ	**1.2**	1.22	**1.24**	V
I_{LEDmax}	Maximum LED Current per Channel	V_{IN} = 12V, V_{OUT} = 45V, F_{SW} = 1.2MHz, T_A = +25°C		50		mA
FAULT DETECTION						
VSC	Channel Short Circuit Threshold	PWM Dimming = 100%	**7.5**	8.2		V
Temp_shtdwn	Over-Temperature Shutdown Threshold			150		°C
Temp_Hyst	Over-Temperature Shutdown Hysteresis			23		°C
VOVPlo	Overvoltage Limit on OVP Pin		**1.199**		**1.24**	V
FLAG_ON	Flag Voltage when Fault Occurs	When Fault Occurs, I_{PULLUP}= 4mA		0.04	**0.12**	V
FAULT PIN						
I_{FAULT}	Fault Pull-down Current	V_{IN} = 12V	**12**	21	**30**	µA
V_{FAULT}	Fault Clamp Voltage with Respect to V_{IN}	V_{IN} = 12, V_{IN} - V_{FAULT}	**6**	7	**8.3**	V

Electrical Specifications

All specifications are tested at T_A = +25°C, V_{IN} = 12V, EN = 5V, R_{SET} = 20.5kΩ, unless otherwise noted. **Boldface limits apply over the operating junction temperature range, -40°C to +85°C.**

PARAMETER	DESCRIPTION	CONDITION	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
LXstart_thres	LX Start-up Threshold		**0.9**		**1.2**	V
$ILX_{Startup}$	LX Start-up Current	VDC = 5.0V	**1**	3.5	**5**	mA

NOTES:

8. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
9. Compliance to limits is assured by characterization and design.
10. At maximum V_{IN} of 26.5V, minimum V_{OUT} is 28V. Minimum V_{OUT} can be lower at lower V_{IN}.
11. Varies within range specified by $V_{HEADROOM\_RANGE}$.

Typical Performance Curves

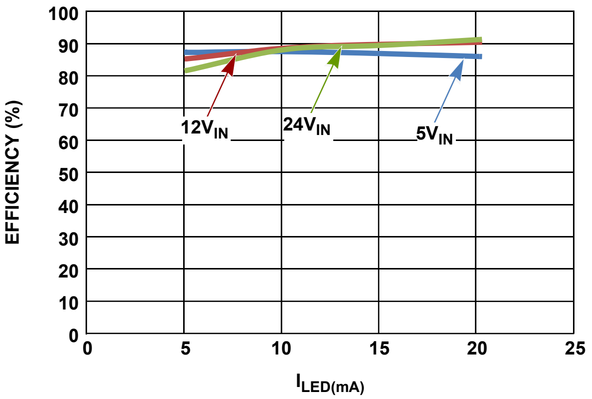


FIGURE 3. EFFICIENCY vs UP TO 20mA LED CURRENT (100% LED DUTY CYCLE) vs V_{IN}

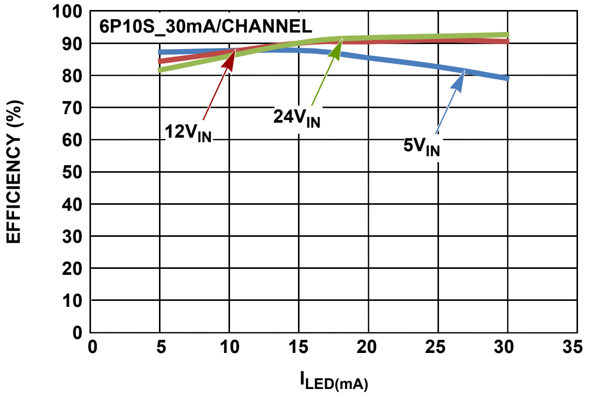


FIGURE 4. EFFICIENCY vs UP TO 30mA LED CURRENT (100% LED DUTY CYCLE) vs V_{IN}

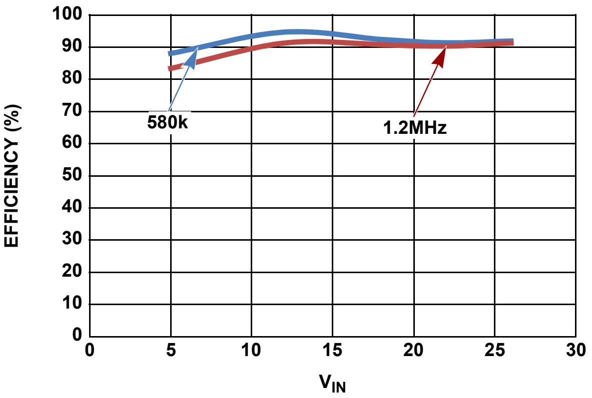


FIGURE 5. EFFICIENCY vs V_{IN} vs SWITCHING FREQUENCY AT 20mA (100% LED DUTY CYCLE)

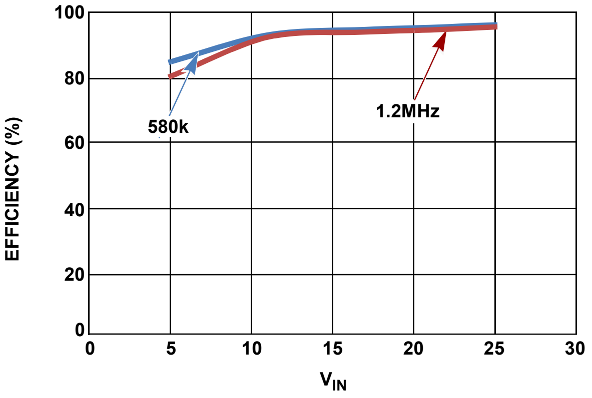


FIGURE 6. EFFICIENCY vs V_{IN} vs SWITCHING FREQUENCY AT 30mA (100% LED DUTY CYCLE)

Typical Performance Curves (Continued)

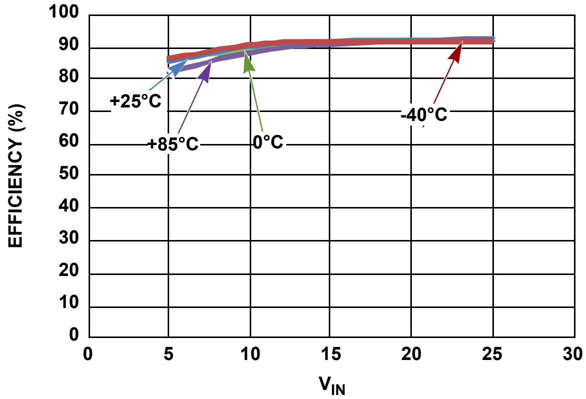


FIGURE 7. EFFICIENCY vs V_{IN} vs TEMPERATURE AT 20mA (100% LED DUTY CYCLE)

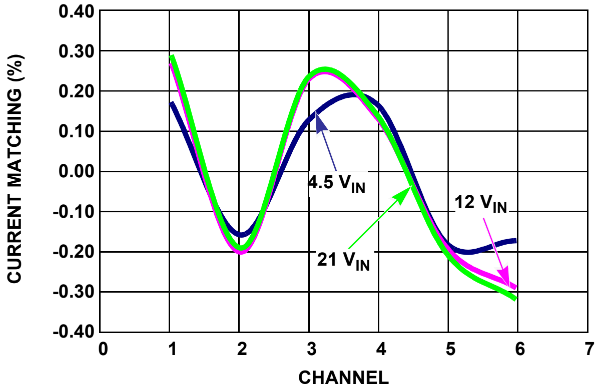


FIGURE 8. CHANNEL-TO-CHANNEL CURRENT MATCHING

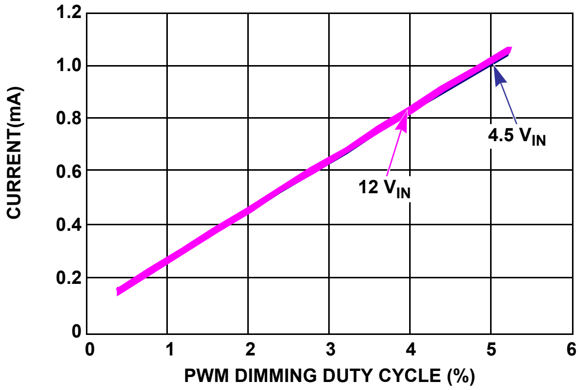


FIGURE 9. CURRENT LINEARITY vs LOW LEVEL PWM DIMMING DUTY CYCLE vs V_{IN}

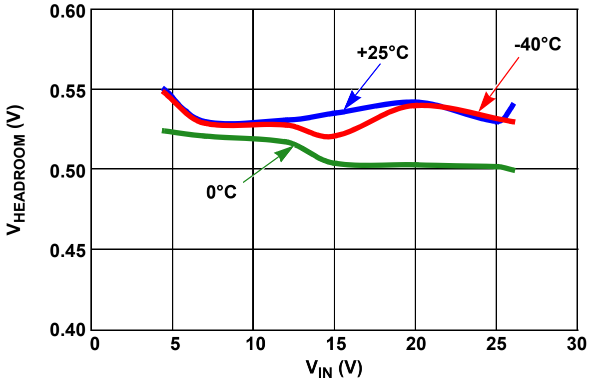


FIGURE 10. $V_{HEADROOM}$ vs V_{IN} vs TEMPERATURE AT 20mA

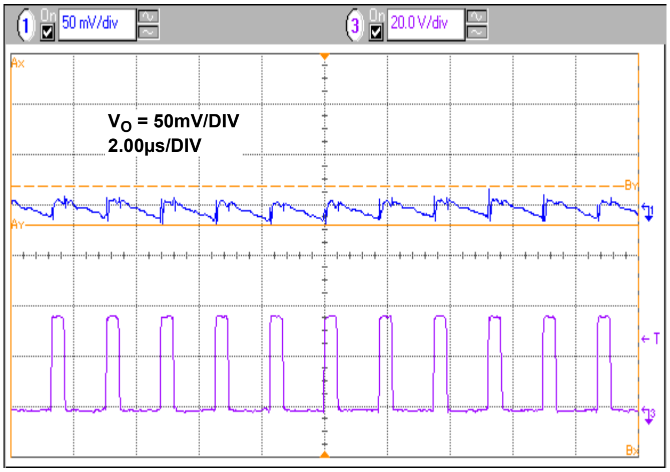


FIGURE 11. V_{OUT} RIPPLE VOLTAGE, V_{IN} = 12V, 6P12S AT 20mA/CHANNEL

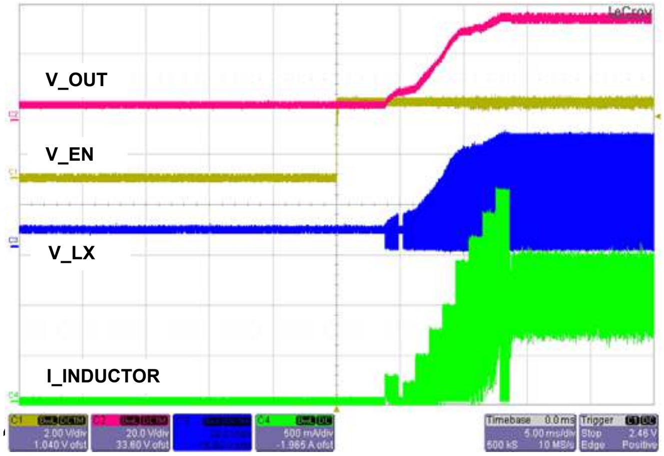


FIGURE 12. START UP WAVEFORMS AT V_{IN} = 6V FOR 6P12S AT 20mA/CHANNEL

Typical Performance Curves (Continued)

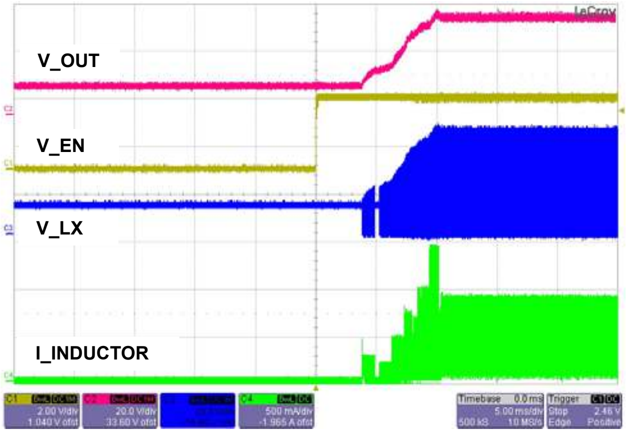


FIGURE 13. STARTUP WAVEFORMS AT V_{IN} = 12V FOR 6P12S AT 20mA/CHANNEL

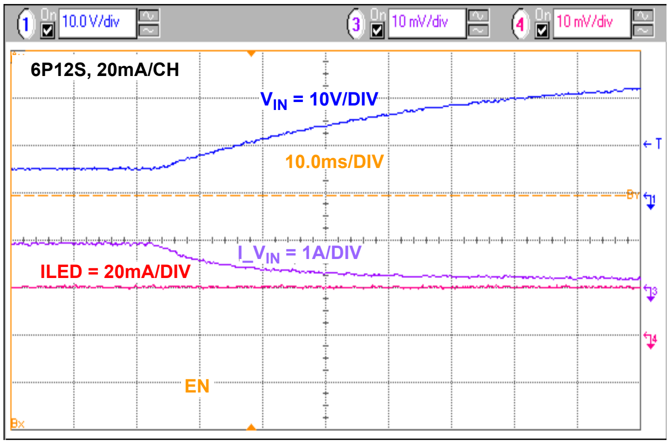


FIGURE 14. LINE REGULATION WITH V_{IN} CHANGE FROM 6V TO 26V, 6P12S AT 20mA/CHANNEL

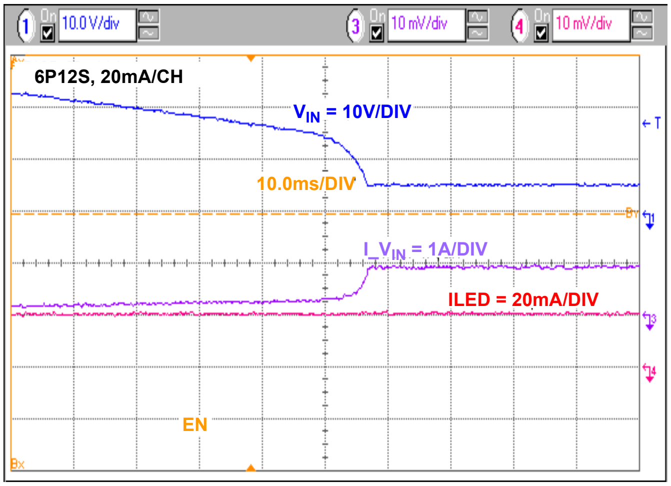


FIGURE 15. LINE REGULATION WITH V_{IN} CHANGE FROM 26V TO 6V FOR 6P12S AT 20mA/CHANNEL

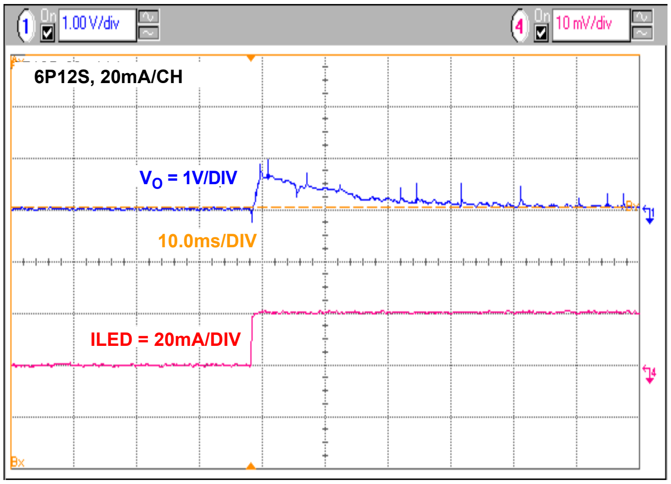


FIGURE 16. BOOST OUTPUT VOLTAGE WITH BRIGHTNESS CHANGE FROM 0% TO 100%, V_{IN} = 12V, 6P12S AT 20mA/CHANNEL

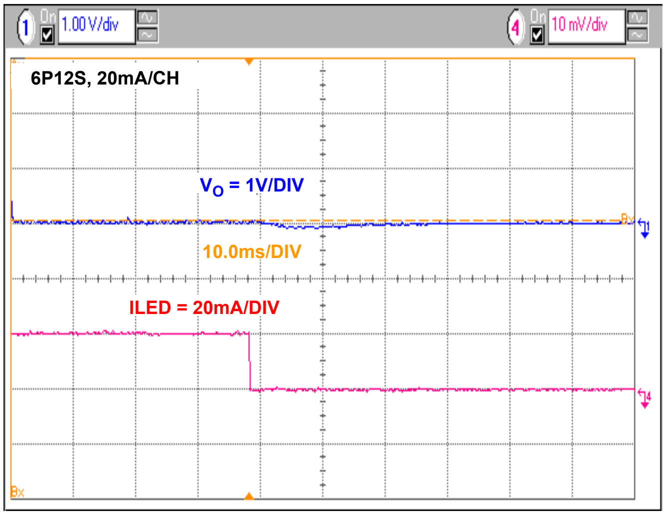


FIGURE 17. BOOST OUTPUT VOLTAGE WITH BRIGHTNESS CHANGE FROM 100% TO 0%, V_{IN} = 12V, 6P12S AT 20mA/CHANNEL

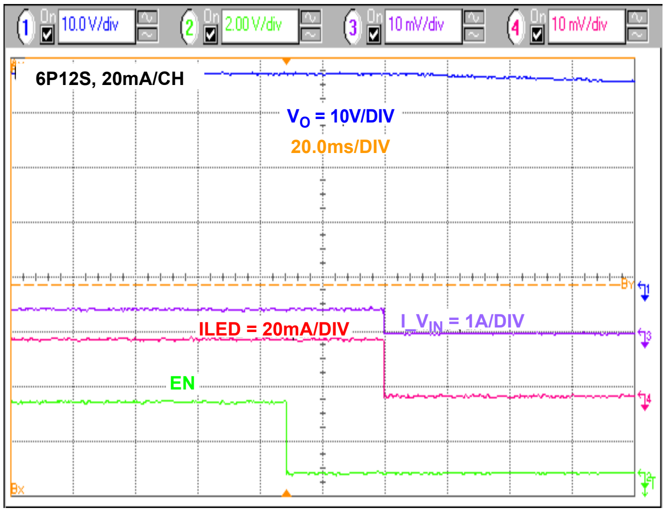


FIGURE 18. ISL97672A SHUTS DOWN AND STOPS SWITCHING ~30ms AFTER EN GOES LOW

Theory of Operation

PWM Boost Converter

The current mode PWM boost converter produces the minimal voltage needed to enable the LED stack with the highest forward voltage drop to run at the programmed current. The ISL97672A employs current mode control boost architecture that has a fast current sense loop and a slow voltage feedback loop. Such architecture achieves a fast transient response that is essential for notebook backlight applications in which drained batteries can be instantly changed to an AC/DC adapter without noticeable visual disturbance. The number of LEDs that can be driven by ISL97672A depends on the type of LED chosen in the application. The ISL97672A is capable of boosting up to 45V and typically driving 13 LEDs in series for each of the 6 channels, enabling a total of 78 pieces of the 3.2V/20mA type of LEDs.

Enable

Device is enabled if the Enable pin voltage is high. If EN is pulled low for longer than 30.5ms, the device will be shutdown. The Enable pin should not float, a 10k or higher pull-down resistor should be connected between EN and GND.

Current Matching and Current Accuracy

Each channel of the LED current is regulated by the current source circuit, as shown in Figure 19.

The LED DC current is set by translating the R_{SET} current to the output, with a scaling factor of $410.5/R_{SET}$. The source terminals of the current source MOSFETs are designed to operate within a range at about 500mV to optimize power loss versus accuracy requirements. The sources of errors of the channel-to-channel current matching come from the op amp's offset, internal layout, reference and current source resistors. These parameters are optimized for current matching and absolute current accuracy. The absolute accuracy is also affected by the external R_{SET}. A 1% tolerance resistor should be used.

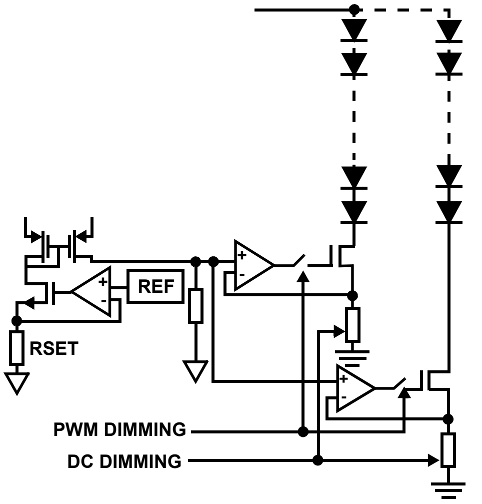


FIGURE 19. SIMPLIFIED CURRENT SOURCE CIRCUIT

Dynamic Headroom Control

The ISL97672A features a proprietary Dynamic Headroom Control circuit that detects the highest forward voltage string or effectively the lowest voltage from any of the CH0 through CH5 pins. When this lowest channel voltage is lower than the short-circuit threshold, V_{SC}, this voltage is used as the feedback signal for the boost regulator. The boost adjusts the output to the correct level such that the lowest channel pin is at the target headroom voltage. Since all LED stacks are connected to the same output voltage, the other channel pins will have a higher voltage, but the regulated current source circuit on each channel ensures that each channel has the same current. The output voltage regulates cycle by cycle, and it is always referenced to the highest forward voltage string in the architecture.

Dimming Controls

The ISL97672A allows two ways of controlling the LED current, and therefore, the brightness. They are:

1. DC current adjustment
2. PWM chopping of the LED current defined in Step 1.

MAXIMUM DC CURRENT SETTING

The LED DC current of each channel can be calculated as shown in Equation 1:

$$I_{LEDmax} = \frac{410.5}{R_{SET}} \qquad \text{(EQ. 1)}$$

For example, if the maximum required LED current ($I_{LED(max)}$) is 20mA, rearranging Equation 1 yields Equation 2:

$$R_{SET} = 410.5/0.02 = 20.52\text{k}\Omega \qquad \text{(EQ. 2)}$$

PWM CURRENT CONTROL

The ISL97672A employs direct PWM dimming such that the output PWM dimming follows directly with the input PWM signal without modifying the input frequency. The average LED current of each channel can be calculated as shown in Equation 3:

$$I_{LED(ave)} = I_{LED} \times PWM \qquad \text{(EQ. 3)}$$

Switching Frequency

The boost switching frequency can be adjusted by connecting a resistor between the FSW pin and GND. The calculation of the resistance is shown in Equation 4:

$$f_{SW} = \frac{(5 \times 10^{10})}{R_{FSW}} \qquad \text{(EQ. 4)}$$

where F_{SW} is the desirable boost switching frequency, and R_{FSW} is the setting resistor.

5V Low Dropout Regulator

There is an internal 5V low dropout (LDO) regulator to develop the necessary low-voltage supply, which is used by the chip's internal control circuitry. VDC is the output of this LDO regulator which requires a bypass capacitor of 1µF or more for the regulation. The VDC pin can be used as a coarse reference as long as it is sourcing only a few milliamps.

IC Protection Features and Fault Management

ISL97672A has several protection and fault management features that improve system reliability. The following sections describe them in more detail.

In-Rush Control and Soft-Start

The ISL97672A has separate, built-in, independent in-rush control and soft-start functions. The in-rush control function is built around an external short-circuit protection P-channel FET in series with VIN. At start-up, the fault protection FET is turned on slowly due to a 21µA pull-down current output from the FAULT pin. This discharges the fault FET's gate-source capacitance, turning on the FET in a controlled fashion. As this happens, the output capacitor is charged slowly through the low-current FET before it becomes fully enhanced. This results in a low in-rush current. This current can be further reduced by adding a capacitor (in the 1nF to 5nF range) across the gate source terminals of the FET.

Once the chip detects that the fault protection FET is turned on fully, it assumes that in-rush is complete. At this point, the boost regulator begins to switch, and the current in the inductor ramps up. The current in the boost power switch is monitored, and switching is terminated in any cycle in which the current exceeds the current limit. The ISL97672A includes a soft-start feature in which this current limit starts at a low value (275mA). This value is stepped up to the final 2.2A current limit in seven additional steps of 275mA each. These steps happen over at least 8ms and are extended at low LED PWM frequencies if the LED duty cycle is low. This extension allows the output capacitor to charge to the required value at a low current limit and prevents high input current for systems that have only a low to medium output current requirement.

For systems with no master fault protection FET, the in-rush current flows towards C_{OUT} when V_{IN} is applied. The in-rush current is determined by the ramp rate of V_{IN} and the values of C_{OUT} and L.

Fault Protection and Monitoring

The ISL97672A features extensive protection functions to cover all perceivable failure conditions. The /FLAG pin is a latched open-drain output that monitors string open, LED short, V_{OUT} short, and overvoltage and over-temperature conditions. This pin resets only when input power is recycled or the part is re-enabled.

The failure mode of an LED can be either an open circuit or a short. The behavior of an open-circuited LED can additionally take the form of either infinite resistance or, for some LEDs, a Zener diode, which is integrated into the device in parallel with the now-opened LED.

For basic LEDs (which do not have built-in Zener diodes), an open-circuit failure of an LED results only in the loss of one channel of LEDs, without affecting other channels. Similarly, a short-circuit condition on a channel that results in that channel being turned off does not affect other channels unless a similar fault is occurring.

Due to the lag in boost response to any load change at its output, certain transient events (such as LED current steps or significant step changes in LED duty cycle) can transiently look like LED fault modes. The ISL97672A uses feedback from the LEDs to determine when it is in a stable operating region and prevents apparent faults during these transient events from allowing any of the LED stacks to fault out. See Table 1 for details.

A fault condition that results in an input current that exceeds the device's electrical limits will result in a shutdown of all output channels.

Short-Circuit Protection (SCP)

The short-circuit detection circuit monitors the voltage on each channel and disables faulty channels that are above approximately 7.5V (this action is described in Table 1 on page 12).

Open-Circuit Protection (OCP)

When one of the LEDs becomes an open circuit, it can behave as either an infinite resistance or as a gradually increasing finite resistance. The ISL97672A monitors the current in each channel such that any string that reaches the intended output current is considered "good." Should the current subsequently fall below the target, the channel is considered an "open circuit." Furthermore, should the boost output of the ISL97672A reach the OVP limit, or should the lower over-temperature threshold be reached, all channels that are not good are immediately considered to be open circuit. Detection of an open circuit channel results in a time-out before the affected channel is disabled. This time-out is sped up when the device is above the lower over-temperature threshold, in an attempt to prevent the upper over-temperature trip point from being reached.

Some users employ special types of LEDs that have a Zener diode structure in parallel with the LED. This configuration provides ESD enhancement and enables open-circuit operation. When this type of LED is open circuited, the effect is as if the LED forward voltage has increased but the lighting level has not increased. Any affected string will not be disabled, unless the failure results in the boost OVP limit being reached, which allows all other LEDs in the string to remain functional. In this case, care should be taken that the boost OVP limit and SCP limit are set properly, to ensure that multiple failures on one string do not cause all other good channels to fault out. This condition could arise if the increased forward voltage of the faulty channel makes all other channels look as if they have LED shorts. See Table 1 for details of responses to fault conditions.

OVP and V_{OUT}

The Overvoltage Protection (OVP) pin has a function of setting the overvoltage trip level as well as limiting the V_{OUT} regulation range.

The ISL97672A OVP threshold is set by R_{UPPER} and R_{LOWER} such that:

$$V_{OUT\_OVP} = 1.22V \times \frac{(R_{UPPER} + R_{LOWER})}{R_{LOWER}} \qquad \text{(EQ. 5)}$$

and output voltage V_{OUT} can regulate between 64% and 100% of the V_{OUT_OVP} such that:‘

Allowable V_{OUT} = 64% to 100% of V_{OUT_OVP}

if, for example, 10 LEDs are used with the worst-case V_{OUT} of 35V.

If R_1 and R_2 are chosen such that the OVP level is set at 40V, then V_{OUT} is allowed to operate between 25.6V and 40V. If the V_{OUT} requirement is changed to an application of six LEDs of 21V, then the OVP level must be reduced. Users should follow the V_{OUT} = (64% ~100%) OVP level requirement; otherwise, the headroom control will be disturbed such that the channel voltage can be much higher than expected. This can sometimes prevent the driver from operating properly.

The resistances should be large, to minimize power loss. For example, a 1MΩ R_{UPPER} and a 30kΩ R_{LOWER} sets OVP to 41.9V. Large OVP resistors also allow C_{OUT} to discharge slowly during the PWM Off time. Parallel capacitors should also be placed across the OVP resistors such that $R_{UPPER}/R_{LOWER} = C_{LOWER}/C_{UPPER}$. Using a C_{UPPER} value of 30pF is recommended. These capacitors reduce the AC impedance of the OVP node, which is important when using high-value resistors. For example, if $R_{UPPER}/R_{LOWER} = 33/1$, then $C_{UPPER}/C_{LOWER} = 1/33$ with C_{UPPER} = 100pF and C_{LOWER} = 3.3nF

Undervoltage Lock-out

If the input voltage falls below the UVLO level, the device stops switching and is reset. Operation restarts only when V_{IN} returns to the normal operating range.

Input Overcurrent Protection

During a normal switching operation, the current through the internal boost power FET is monitored. If the current exceeds the current limit, the internal switch is turned off. Monitoring occurs on a cycle-by-cycle basis in a self-protecting way. Additionally, the ISL97672A monitors the voltage at the LX and OVP pins. At start-up, the LX pins inject a fixed current into the output capacitor. The device does not start unless the voltage at LX exceeds 1.2V. The OVP pin is also monitored such that if it rises above and subsequently falls below 20% of the target OVP level, the input protection FET is also switched off.

Over-Temperature Protection (OTP)

The ISL97672A includes two over-temperature thresholds. The lower threshold is set to +130°C. When this threshold is reached, any channel that is outputting current at a level significantly below the regulation target is treated as “open circuit” and is disabled after a time-out period. This time-out period is 800µs when it is above the lower threshold. The lower threshold isolates and disables bad channels before they cause enough power dissipation (as a result of other channels having large voltages across them) to hit the upper temperature threshold.

The upper threshold is set to +150°C. Each time this threshold is reached, the boost stops switching, and the output current sources switch off. Once the device has cooled to approximately +100°C, the device restarts, with the DC LED current level reduced to 75% of the initial setting. If dissipation persists, subsequent hitting of the limit causes identical behavior, with the current reduced in steps to 50% and finally 25%. Unless disabled via the EN pin, the device stays in an active state throughout.

For complete details of fault protection conditions, see Figure 20 and Table 1.

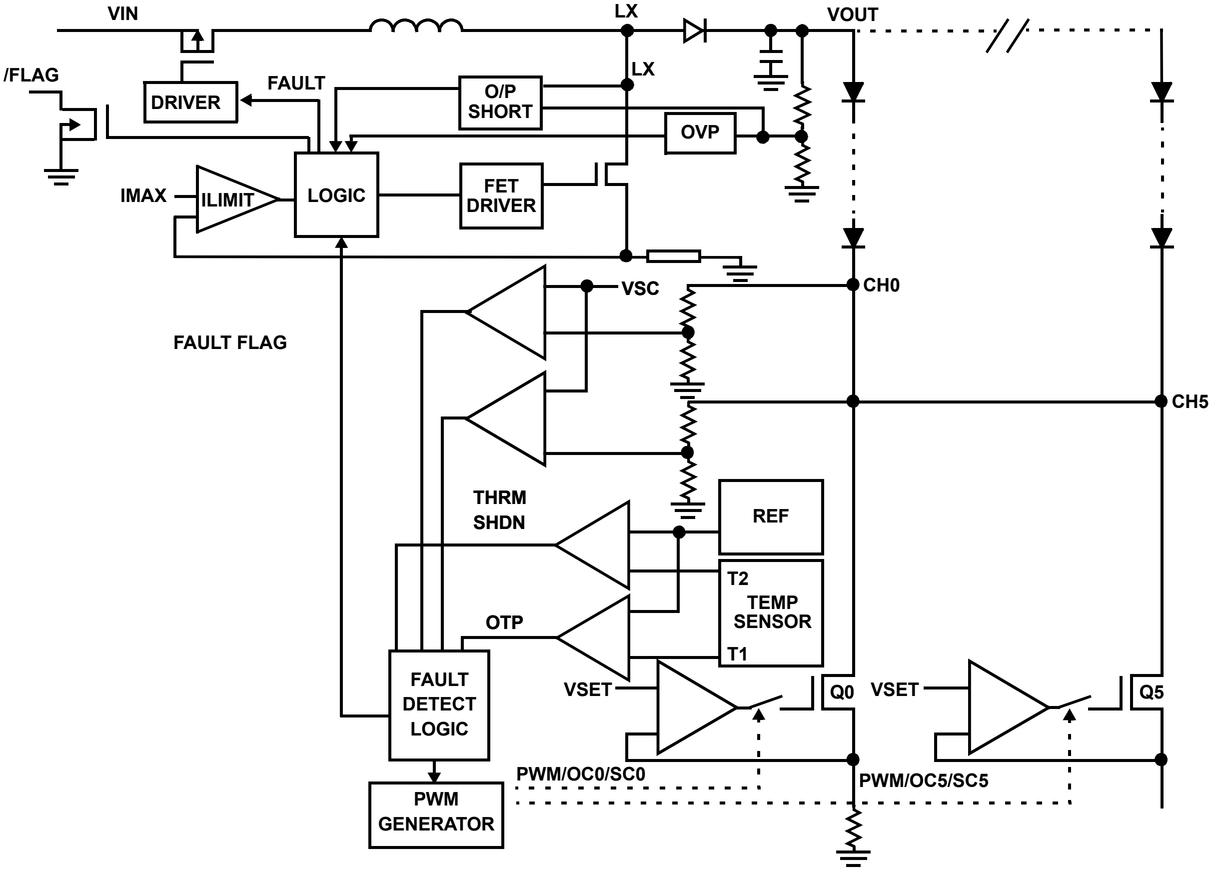


FIGURE 20. SIMPLIFIED FAULT PROTECTIONS

TABLE 1. PROTECTIONS TABLE

CASE	FAILURE MODE	DETECTION MODE	FAILED CHANNEL ACTION	GOOD CHANNEL ACTION	V_{OUT} REGULATED BY
1	CHX short circuit	Upper Over-Temperature Protection limit (OTP) not triggered, and VCHX < 7.5V	CHX ON and burns power.	Remaining channels normal	Highest VF of all channels
2	CHX short circuit	Upper OTP triggered, but VCHX < 7.5V	All channels go off until chip cools, and then come back on with current reduced to 76%. Subsequent OTP triggers further reduce I_{OUT}.	Same as CHX	Highest VF of remaining channels
3	CHX short circuit	Upper OTP not triggered, but CHX > 7.5V	CHX disabled after six PWM cycle time-outs.	Remaining channels normal	Highest VF of remaining channels
4	CHX open circuit with infinite resistance	Upper OTP not triggered, and CHX < 7.5V	V_{OUT} ramps to OVP. CHX times out after six PWM cycles and switches off. V_{OUT} drops to normal level.	Remaining channels normal	Highest VF of remaining channels
5	CHX LED open circuit but has paralleled Zener	Upper OTP not triggered, and CHX < 7.5V	CHX remains ON and has highest VF; thus, V_{OUT} increases.	Remaining channels ON, remaining channel FETs burn power	VF of CHX
6	CHX LED open circuit but has paralleled Zener	Upper OTP triggered, but CHX < 7.5V	All channels go off until chip cools, and then come back on with current reduced to 76%. Subsequent OTP triggers further reduce I_{OUT}.	Same as CHX	VF of CHX
7	CHX LED open circuit but has paralleled Zener	Upper OTP not triggered, but CHX > 7.5V	CHX remains ON and has highest VF; thus, V_{OUT} increases.	V_{OUT} increases, then CHX switches OFF after six PWM cycles. This is an unwanted shut off and can be prevented by setting OVP at an appropriate level.	VF of CHX
8	Channel-to-channel ΔVF too high	Lower OTP triggered, but CHX< 7.5V	Any channel below the target current faults out after six PWM cycles. Remaining channels are driven with normal current.		Highest VF of remaining channels
9	Channel-to-channel ΔVF too high	Upper OTP triggered, but CHX < 7.5V	All channels go off until chip cools and then come back on with current reduced to 75%. Subsequent OTP triggers further reduce I_{OUT}.		Boost switches off
10	Output LED stack voltage too high	V_{OUT} > VOVP	Any channel that is below the target current times out after six PWM cycles, and V_{OUT} returns to normal regulation voltage required for other channels.		Highest VF of remaining channels
11	V_{OUT}/LX shorted to GND at start-up, or V_{OUT} shorted in operation	LX current and timing monitored. OVP pins monitored for excursions below 20% of OVP threshold.	Chip is permanently shut down 31ms after power-up if V_{OUT}/LX is shorted to GND.		

Component Selection

According to the inductor Voltage-Second Balance principle, the change of inductor current during the switching regulator On time is equal to the change of inductor current during the switching regulator Off time. As shown in Equations 6 and 7, since the voltage across an inductor is:

$$\Delta I_L = \frac{V_L}{L} x \Delta t \qquad \text{(EQ. 6)}$$

and ΔI_L @ On = ΔI_L @ Off, therefore:

$$(V_I - 0)/L \times D \times t_S = (V_O - V_D - V_I)/L \times (1 - D) \times t_S \qquad \text{(EQ. 7)}$$

Where D is the switching duty cycle defined by the turn-on time over the switching period. V_D is a Schottky diode forward voltage that can be neglected for approximation.

Rearranging the terms without accounting for V_D gives the boost ratio and duty cycle, respectively, as shown in Equations 8 and 9:

$$V_O / V_I = 1/(1 - D) \qquad \text{(EQ. 8)}$$

$$D = (V_O - V_I)/V_O \qquad \text{(EQ. 9)}$$

Input Capacitor

Switching regulators require input capacitors to deliver peak charging current and to reduce the impedance of the input supply. The capacitors reduce interaction between the regulator and input supply, thus improving system stability. The high switching frequency of the loop causes almost all ripple current to flow into the input capacitor, which must be rated accordingly.

A capacitor with low internal series resistance should be chosen to minimize heating effects and to improve system efficiency. The X5R and X7R ceramic capacitors offer small size and a lower value for temperature and voltage coefficient compared to other ceramic capacitors.

An input capacitor of 10µF is recommended. Ensure that the voltage rating of the input capacitor is able to handle the full supply range.

Inductor

Inductor selection should be based on its maximum current (I_{SAT}) characteristics, power dissipation (DCR), EMI susceptibility (shielded vs unshielded), and size. Inductor type and value influence many key parameters, including ripple current, current limit, efficiency, transient performance, and stability.

Inductor maximum current capability must be adequate to handle the peak current in the worst-case condition. If an inductor core with too low a current rating is chosen, saturation in the core will cause the effective inductor value to fall, leading to an increase in peak-to-average current level, poor efficiency, and overheating in the core. The series resistance, DCR, within the inductor causes conduction loss and heat dissipation. A shielded inductor is usually more suitable for EMI-susceptible applications such as LED backlighting.

The peak current can be derived from the voltage across the inductor during the Off period, as shown in Equation 10:

$$IL_{peak} = (V_O \times I_O)/(85\% \times V_I) + 1/2[V_I \times (V_O - V_I)/(L \times V_O \times f_S)] \tag{EQ. 10}$$

The value of 85% is an average term for the efficiency approximation. The first term is average current that is inversely proportional to the input voltage. The second term is inductor current change that is inversely proportional to L and f_S. As a result, for a given switching frequency and minimum input voltage at which the system operates, the inductor I_{SAT} must be chosen carefully.

Output Capacitors

The output capacitor smooths the output voltage and supplies load current directly during the conduction phase of the power switch. Output ripple voltage consists of discharge and charge of the output capacitor during FET On and OFF time and the voltage drop due to flow through the ESR of the output capacitor. The ripple voltage can be shown as Equation 11:

$$\Delta V_{CO} = (I_O/C_O \times D/f_S) + ((I_O \times ESR) \tag{EQ. 11}$$

The conservation of charge principle shown in Equation 9 also indicates that, during the boost switch Off period, the output capacitor is charged with the inductor ripple current, minus a relatively small output current in boost topology. As a result, the user must select an output capacitor with low ESR and adequate input ripple current capability.

Note: Capacitors have a voltage coefficient that makes their effective capacitance drop as the voltage across them increases. C_{OUT} in Equation 11 assumes the effective value of the capacitor at a particular voltage and not the manufacturer's stated value, measured at 0V.

The value of ΔV_{Co} can be reduced by increasing C_O or f_S, or by using small ESR capacitors. In general, ceramic capacitors are the best choice for output capacitors in small- to medium-sized LCD backlight applications, due to their cost, form factor, and low ESR.

A larger output capacitor also eases driver response during the PWM dimming Off period, due to the longer sample and hold effect of the output drooping. The driver does not need to boost harder in the next On period that minimizes transient current.

The output capacitor is also needed for compensation, and in general, 2x4.7µF/50V ceramic capacitors are suitable for notebook display backlight applications.

Schottky Diode

A high-speed rectifier diode is necessary to prevent excessive voltage overshoot. Schottky diodes are recommended because of their fast recovery time, low forward voltage and reverse leakage current, which minimize losses. The reverse voltage rating of the selected Schottky diode must be higher than the maximum output voltage. Also the average/peak current rating of the Schottky diode must meet the output current and peak inductor current requirements.

Applications

High-Current Applications

Each channel of the ISL97672A can support up to 30mA (50mA @ V_{IN} = 12V). For applications that need higher current, multiple channels can be grouped to achieve the desired current (Figure 21). For example, the cathode of the last LED can be connected to CH0 through CH2; this configuration can be treated as a single string with 90mA current driving capability.

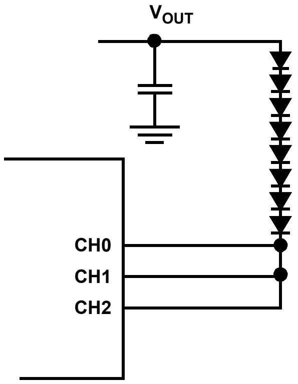


FIGURE 21. GROUPING MULTIPLE CHANNELS FOR HIGH CURRENT APPLICATIONS

Low-Voltage Operations

The ISL97672A VIN pin can be separately biased from the LED power input to allow low-voltage operation. For systems that have only a single supply, V_{OUT} can be tied to the driver VIN pin to allow initial start-up (Figure 22). The circuit works as follows: when the input voltage is available and the device is not enabled, V_{OUT} follows V_{IN} with a Schottky diode voltage drop. The V_{OUT} boot-strapped to the VIN pin allows initial start-up, once the part is enabled. Once the driver starts up with V_{OUT} regulating to the target, the VIN pin voltage also increases. As long as V_{OUT} does not exceed 26.5V and the extra power loss on V_{IN} is acceptable, this configuration can be used for input voltage as low as 3.0V. The Fault Protection FET feature cannot be used in this configuration.

For systems that have dual supplies, the VIN pin can be biased from 5V to 12V, while input voltage can be as low as 2.7V (Figure 23). In this configuration, VBIAS must be greater than or equal to VIN to use the fault FET.

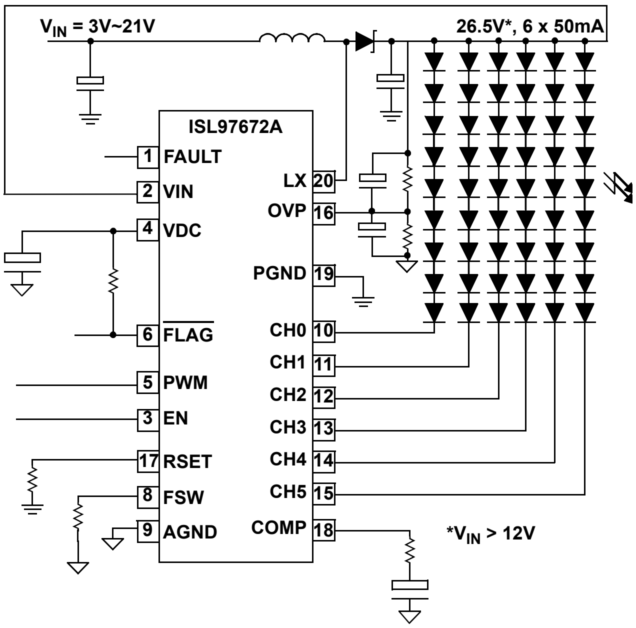


FIGURE 22. SINGLE SUPPLY 3.0V OPERATION

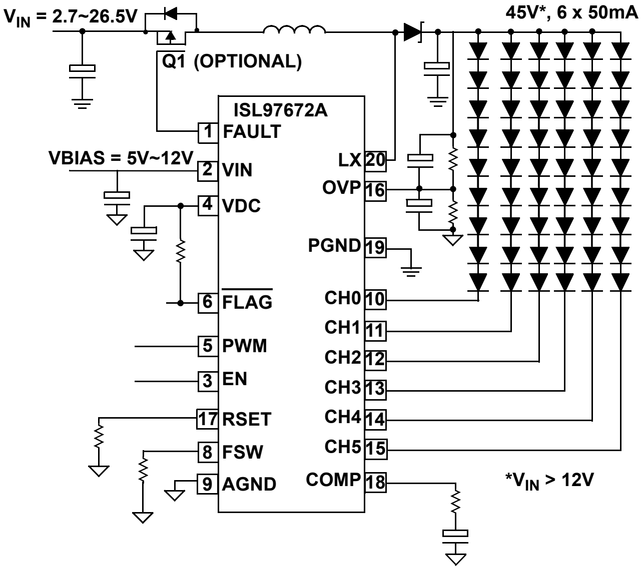


FIGURE 23. DUAL SUPPLY 2.7V OPERATION

Compensation

The ISL97672A incorporates a transconductance amplifier in its feedback path to allow the user to optimize boost stability and transient response. The ISL97672A uses current mode control architecture, which has a fast current sense loop and a slow voltage feedback loop. The fast current feedback loop does not require any compensation, but for stable operation, the slow voltage loop must be compensated. The compensation is a series of Rc, Cc1 network from COMP pin to ground, with an optional Cc2 capacitor connected between the COMP pin and ground. The Rc sets the high-frequency integrator gain for fast transient response, and the Cc1 sets the integrator zero to ensure loop stability. For most applications, the component values in Figure 24 can be used: Rc is 10kΩ and Cc1 is 3.3nF. Depending upon the PCB layout, for stability, a Cc2 of 390pF may be needed to create a pole to cancel the output capacitor ESR's zero effect.

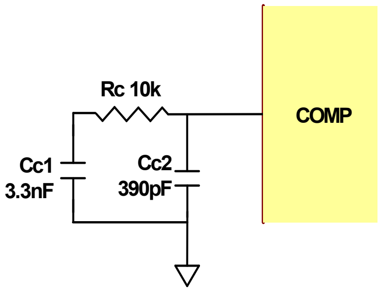


FIGURE 24. COMPENSATION CIRCUIT

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website ensure you have the latest revision.

DATE	REVISION	CHANGE
September 14, 2017	FN7710.4	Added Related Literature. Applied new header/footer. Added $V_{HEADROOM\_RANGE}$ spec to EC table. Added Note 11. In “Current Matching and Current Accuracy” on page 9 updated 2nd sentence in paragraph 2 for clarification.
September 19, 2012	FN7710.3	1. VOVPlo limits changed to [1.199Vmin, 1.24Vmax] in Electrical Specification table. 2. OVP lower limit changed to 64% on page 10. 3. Compensation component values changed to match Figure 24 in “Compensation” on page 14. 4. Description in “PROTECTIONS TABLE” on page 12 changed. 5. Equation 5 on page 10, 1.21 changed to 1.22. 6. 30µA changed to 21µA in “In-Rush Control and Soft-Start” on page 10. 7. 28ms changed to 30.5ms in Pin Descriptions page 3 and “Enable” on page 9. 8. Description of ISL97672A introduction changed on page 1. 9. Pin description changed on page 3. 10. Description for VIN, SS, Temp_shtdwn, Temp_Hyst, FLAG_ON changed in Electrical Specification table 11. 8 channel changed to 6 channel in “PWM Boost Converter” on page 9 12. Description of “Enable” on page 9 changed 13. Description of “Switching Frequency” on page 9 changed. 14. Description of “5V Low Dropout Regulator” on page 9 changed. 15. Description of “In-Rush Control and Soft-Start” on page 10 changed. 16. "Overvoltage Protection (OVP) and Vout" moved to page 11, combined with original "Overvoltage Protection" section. 17. 2.45V deleted from “Undervoltage Lock-out” on page 11. 18. Equation 6 on page 12 changed. 19. “Input Capacitor” on page 13 changed. 20. “Inductor” on page 13 changed 21. Added "Note" in "Output Capacitor" section on page 13 combined "Output Ripple" section with "Output Capacitor" section. 22. Description of “Schottky Diode” on page 13 changed. 23. Description of “Compensation” on page 14 changed. 24. Figure 19, 20 deleted. 25. Stamp on page 1 changed- ISL97671A deleted from Recommended Replacement Part. 26. page 2 Ordering Information table: replaced Retired ISL97672AIRZ-EVAL with ISL97672AIRZ-EVALZ
July 25, 2012		1. Stamped NRND Recommended Replacement Part ISL97672B Updated Figure 12 on page 7 and Figure 13 on page 8. 2. Added “Boldface limits apply over the operating junction temperature range, -40°C to +85°C” to common conditions of “Electrical Specifications” on page 4. 3. Added Note 9 to page 6. Added Note 9 reference to “$V_{headroom20}$” on page 6. 4. Added Vheadroom33 to Electrical Specification table on page 6. 5. Changed “FLAG_ON” on page 6 typ from 0.4 to 0.04. Added max of 0.12. 6. On page 9 in Equations 1 & 2, changed 401.8 to 410.5. 7. On page 13, added "(50mA@VIN=12V)" to “High-Current Applications”. 8. Added Figure 24, “COMPENSATION CIRCUIT,” on page 14.
April 13, 2011	FN7710.2	Changed units from mV to V for “VRSET” on page 5.
March 24, 2011	FN7710.1	Initial Release to web.

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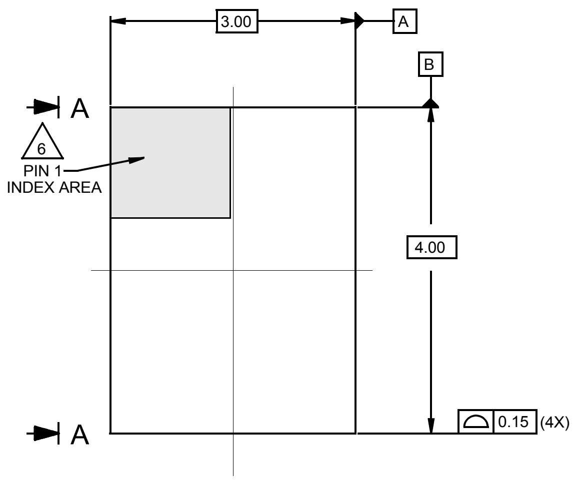
Package Outline Drawing

For the most recent package outline drawing, see L20.3x4.

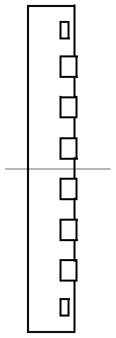
L20.3x4

20 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE

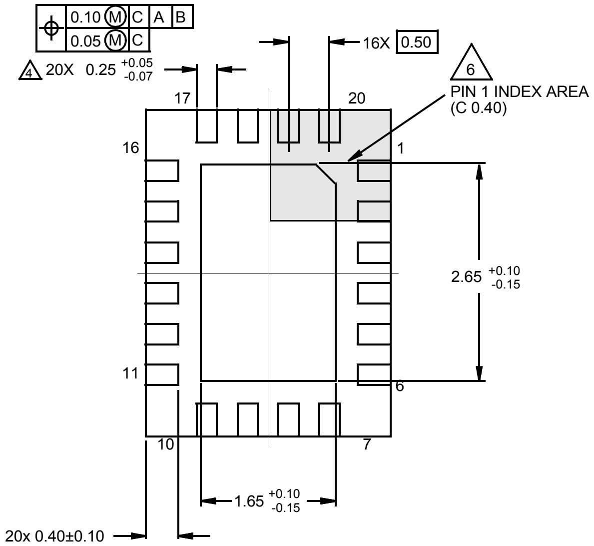
Rev 1, 3/10



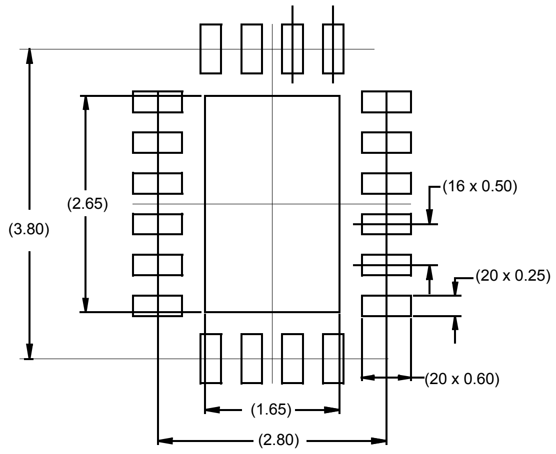
TOP VIEW



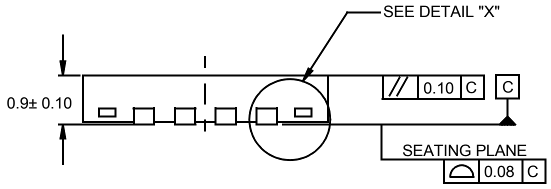
VIEW "A-A"



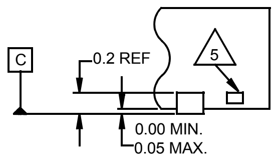
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.