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PTB48520W
SLTS233A–NOVEMBER 2004–REVISED APRIL 2005

# 25-A, 48-V INPUT ISOLATED DC/DC CONVERTER WITH AUTO-TRACK™ SEQUENCING

## FEATURES

- Input Voltage: 36 V to 75 V
- 25-A Total Output Current
- 91% Efficiency
- Wide-Adjust Output Voltage: 1.8 V to 3.6 V
- Overcurrent Protection
- Output Overvoltage Protection
- Overtemperature Shutdown
- Output Enable Control
- Auto-Track Compatible Sequenced Output
- Smart-Sense Remote Sensing
- Undervoltage Lockout
- Industry Standard Size
- Surface Mountable
- 1500-Vdc Isolation
- Agency Approvals (Pending): UL/cUL 60950, EN 60950

## APPLICATIONS

- 3.3-V Intermediate Bus Architectures
- Telecom, High-End Computing Platforms
- Multi-Rail Power Systems with Power-Up Sequencing


## DESCRIPTION

The PTB48520W is a 25-A rated, 48-V input isolated dc/dc converter that incorporates Auto-Track™ power-up sequencing. This allows these modules to simultaneously power up with any other downstream non-isolated, Auto-Track compliant module.

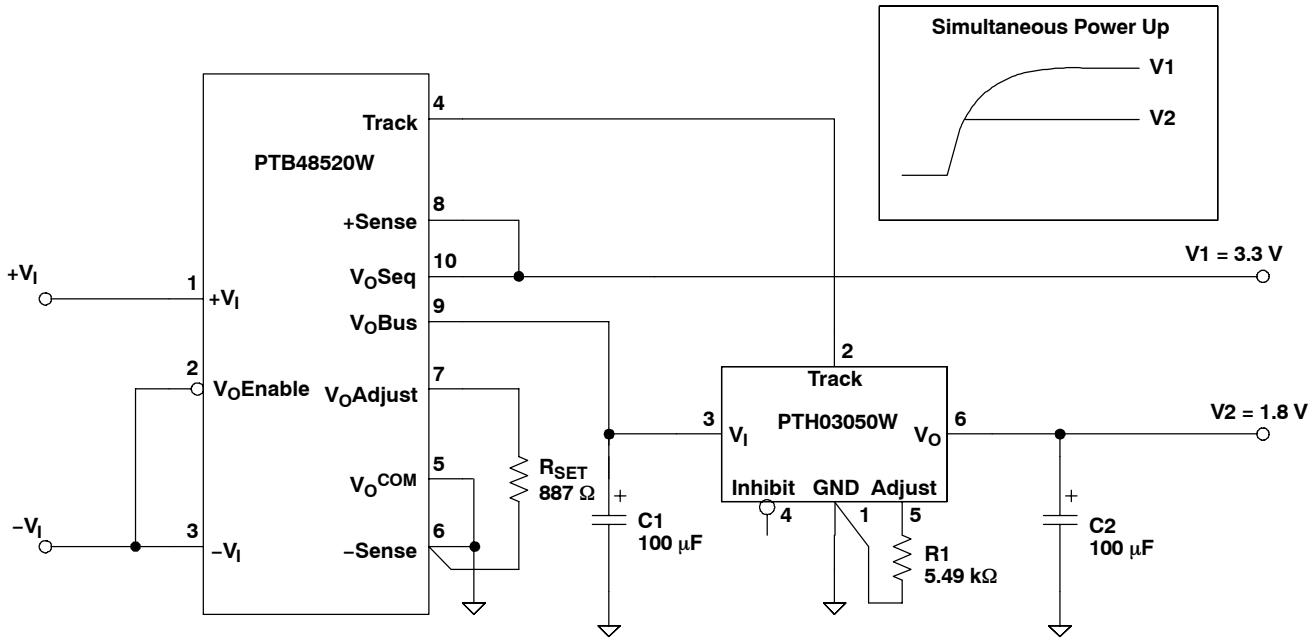
The PTB48520W module provides two outputs, each regulated to the same voltage. During power up, the voltage at $V_o$ *Bus* rises first, allowing this output to provide input power to any downstream non-isolated module. The voltage from $V_o$ *Seq* is then allowed to rise simultaneously, under the control of Auto-Track, along with the outputs from the downstream modules.

Whether used to facilitate power-up sequencing, or operated as a stand-alone module, the PTB48520W includes many features expected of high-performance dc/dc converter modules. The wide output adjust enables the output voltage to be set to to any voltage over the range, 1.8 V to 3.6 V, using a single external resistor. Precise output voltage regulation is ensured with a differential remote sense that intelligently regulates the sequenced output, depending on its sequence status. Other operational features include an input undervoltage lockout (UVLO) and an output enable control. Overcurrent, overvoltage, and overtemperature protection ensures the module ability to survive any load fault.

Typical applications include distributed power architectures in both telecom and computing environments, particularly complex digital systems requiring power sequencing of multiple power supply rails.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## Typical Circuit




## ORDERING INFORMATION

| PTB48520 (Basic Model) | | | |
|---|---|---|---|
| **Output Voltage** | **Part Number** | **DESCRIPTION** | **Package Ref.** (1) |
| 1.8 V to 3.6 V | PTB48520WAH | Horizontal T/H | ERP |
| 1.8 V to 3.6 V | PTB48520WAS | SMD, Standard (2) | ERQ |

(1) See the applicable package reference drawing for the dimensions and PC board layout.
(2) *Standard* option specifies 63/37, Sn/Pb pin solder material.

## ABSOLUTE MAXIMUM RATINGS

| | | | **UNIT** |
|---|---|---|---|
| $V_{(Track)}$ | Track input voltage | | 0 V to $V_O$ Bus + 0.3 V |
| $I_{(Track)}$ max | Track input current | From external source | 10 mA (1) |
| $T_A$ | Operating temperature range | Over $V_I$ range | –40°C to 85°C |
| | Overtemperature protection | PCB temperature (near pin 1) | 115°C |
| $T_{(reflow)}$ | Solder reflow temperature | Surface temperature of module or pins | 235°C (2) |
| $T_{stg}$ | Storage temperature | | –40°C to 125°C |

(1) When the Track input is fed from an external voltage source, the input current must be limited. A 2.74-kΩ value series resistor is recommended.
(2) During solder reflow of SMD package version, do not elevate the module PCB, pins, or internal component temperatures above a peak of 235°C.

## PACKAGE SPECIFICATIONS

| PTB48520W (Suffixes AH and AS) | | | |
|---|---|---|---|
| Weight | | | 28.5 grams |
| Flammability | Meets UL94V-O | | |
| Mechanical shock | Per Mil-STD-883D, Method 2002.3<br>1 msec, 1/2 Sine, mounted | Horizontal T/H (Suffix AH) | 250 Gs (1) |
| | | Horizontal SMD (Suffix AS) | 150 Gs (1) |
| Mechanical vibration | Mil-STD-883D, Method 2007.2<br>20-2000 Hz, PCB mounted | Horizontal T/H (Suffix AH) | 15 Gs (1) |
| | | Horizontal SMD (Suffix AS) | 5 Gs (1) |

(1) Qualification limit.

## ELECTRICAL CHARACTERISTICS

(Unless otherwise stated, $T_A$ = 25°C, $V_I$ = 48 V, $V_O$ = 3.3 V, $C_O$ = 0 µF, and $I_O$ = $I_O$max)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_O$ | Output current | Over $V_I$ range | $I_O$ Bus | 0 | | 25 (1) | A |
| | | | $I_O$ Seq | 0 | | 10 (1) (2) | |
| | | Sum total $I_O$ Bus + $I_O$ Seq | | 0 | | 25 | A |
| $V_I$ | Input voltage range | Over $I_O$ range | | 36 | 48 | 75 | V |
| $V_O$ | Set-point voltage tolerance | | | | ±0.6 (3) | | %$V_o$ |
| | Temperature variation | -40°C ≤ $T_A$ ≤ 85°C | | | ±0.8 | | %$V_o$ |
| | Line regulation | Over $V_I$ range | | | ±1 | | mV |
| | Load regulation | Over $I_O$ range | | | ±1 | | mV |
| | Total output voltage variation | Includes set-point, line, load, –40°C ≤ $T_A$≤ 85°C | | | ±1.5 | ±3 (3) | %$V_o$ |
| | Adjust range | Over $V_I$ range | | 1.8 | | 3.6 | V |
| η | Efficiency | $I_O$ = 15 A | $R_{SET}$ = 887 Ω, $V_O$ = 3.3 V | | 91% | | |
| | | | $R_{SET}$ = 6.98 kΩ, $V_O$ = 2.5 V | | 90% | | |
| | | | $R_{SET}$ = 35.7 kΩ, $V_O$ = 2.0 V | | 89% | | |
| | | | $R_{SET}$ = open cct. $V_O$ = 1.8 V | | 88% | | |
| | $V_O$ Ripple (peak-to-peak) | 20 MHz bandwidth | | | 20 | | $mV_{pp}$ |
| | Transient Response | 1 A/µs load step, 50% to 100% $I_O$max | | | | | |
| | | | Recovery time | | 75 | | µs |
| | | | $V_O$ over/undershoot | | ±3 | | %$V_o$ |
| | Track input (pin 4) | Input current | Pin connected to $V_O$ COM | | | -0.13 | mA |
| | | Open-circuit voltage | | 0 | | $V_o$ Bus | V |
| | | Input slew rate limits | | 0.1 (4) | | 1 | V/ms |
| | Output enable input (pin 2) | Referenced to -$V_I$ (pin 3) | | | | | |
| | | | Input high voltage ($V_{IH}$) | 2 | | Open (5) | V |
| | | | Input low voltage ($V_{IL}$) | -0.2 | | 0.8 | |
| | | | Input low current ($I_{IL}$) | | –480 | | µA |
| | Standby input current | Pin 2 open | | | 2 | | mA |
| | No-load input current | Pins 2 and 3 connected, $I_O$ Tot = 0 | | | 50 | | mA |
| | Overcurrent threshold, $I_O$ (tot) | Shutdown, followed by autorecovery | | | 40 | | A |

(1) See temperature derating curves for safe operating area (SOA), or consult factory for appropriate derating.
(2) When load current is supplied from the $V_O$ Seq output, the module exhibits higher power dissipation and slightly lower operating efficiency.
(3) The set-point voltage tolerance is affected by the tolerance and stability of $R_{SET}$. The stated limit is unconditionally met if $R_{SET}$ has a tolerance of 1%, with 100 ppm/°C temperature stability.
(4) When controlling the Track input from an external source, the slew rate of the applied signal **must** be greater than the minimum limit. Failure to allow the voltage to completely rise to the voltage at the $V_O$ (bus) output, at no less than the minimum specified rate, may thermally overstress the converter.
(5) The $V_O$ Enable input has an internal pull-up, and if left open the converter output isturned off. A discrete MOSFET or bipolar transistor is recommended to control this input. The open-circuit voltage is approximately 20% of the input voltage. If the output enable feature is not used, this pin should be permanently connected to –$V_I$. See the application information for other interface considerations.

## ELECTRICAL CHARACTERISTICS (continued)

(Unless otherwise stated, $T_A$ = 25°C, $V_I$ = 48 V, $V_O$ = 3.3 V, $C_O$ = 0 μF, and $I_O$ = $I_O$max)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| OVP | Output overvoltage protection | Output shutdown and latch off | | 125 | | %$V_o$ |
| UVLO | Undervoltage lockout | | 30 | 34 | 36 | V |
| $f_S$ | Switching frequency | Over $V_I$ range | 225 | 275 | 325 | kHz |
| | Internal input capacitance | | | 3 | | μF |
| | External output capacitance | Between both outputs and $V_O$ COM | 0 | | 5000 | μF |
| | Isolation voltage | Input-output | 1500 | | | Vdc |
| | Isolation capacitance | Input-output | | 1000 | | pF |
| | Isolation resistance | Input-output | 10 | | | MΩ |
| MTBF | Reliability | Telcordia SR-332 50% stress, $T_A$ = 40°C, ground benign | 1.2 | | | $10^6$ Hrs |

## TERMINAL FUNCTIONS

| TERMINAL | | DESCRIPTION |
|---|---|---|
| NAME | NO. | |
| +$V_I$ (1) | 1 | The positive input for the module with respect to –$V_I$. When powering the module from a negative input voltage, this input is connected to the input source ground. |
| –$V_I$ (1) | 3 | The negative input supply for the module, and the 0-V reference for the *$V_O$ Enable* input. When powering the module from a positive source, this input is connected to the input source return. |
| $V_O$ Enable (1) (2) | 2 | An open-collector (open-drain) negative logic input that is referenced to –$V_I$. This input must be pulled to –$V_I$ potential to enable the output voltage. A high impedance connection disables the module output. If the output enable feature is not used, pin 2 should be permanently connected to –$V_I$. The module then produces an output whenever a valid input source is applied. |
| $V_O$ Bus | 9 | Produces a positive power output with respect to *$V_O$ COM*. This is the main output from the converter when operated in a stand-alone configuration. It is dc isolated from the input power pins and is the first output to rise when the converter is either powered or enabled. In power-up sequencing applications, this output can provide a 3.3-V standby source to power the downstream non-isolated modules. |
| $V_O$ Seq | 10 | This is the sequenced output voltage from the converter. This voltage can be directly controlled from the Track pin. During power up, $V_O$ Seq rises with the Track pin voltage, typically 20 ms after the $V_O$ Bus output has reached regulation. |
| $V_O$ COM | 5 | This is the output power return for both the *$V_O$ Bus* and *$V_O$ Seq* output voltages. This node should be connected to the load circuit common. |
| Track | 4 | The voltage at this pin directly controls the voltage *$V_O$ Seq* regulated output. It is primarily used to sequence the voltage *$V_O$ Seq* with the regulated outputs from any downstream non-isolated modules that are powered from the converter *+$V_O$ Bus* output. In these applications, the *Track* pin is simply connected to the track control of each of the non-isolated modules. The *Track* pin has an internal transistor, which holds it at *$V_O$ COM* potential for approximately 20 ms after the *$V_O$ Bus* output is in regulation. Following this delay, the *Track* voltage and *$V_O$ Seq* rises simultaneously with the output voltage of all the non-isolated modules that are under the control of Auto-Track. |
| $V_O$ Adjust | 7 | A resistor must be connected between this pin and *–Sense* to set the converter output voltage. A 0.05-W rated resistor may be used, with tolerance and temperature stability of 1% and 100 ppm/°C, respectively. If this pin is left open, the converter output voltage defaults to its lowest value. The specification table gives the preferred resistor values for the popular bus voltages. |
| +Sense | 8 | The *+Sense* pin can be connected to either the *$V_O$ Bus* or *$V_O$ Seq* outputs. When connected to *$V_O$ Seq*, remote sense compensation will be delayed until the power-up sequence is complete. The voltage at *$V_O$ Bus* is raised slightly. The pin may be left open circuit, but connecting it to one of the output terminals improves load regulation of that output. |
| –Sense | 6 | Provides the converter with a remote sense capability when used with +Sense. For optimum output voltage accuracy, this pin should always be connected to *$V_O$ COM*. This pin is also the reference connection for the output voltage set-point resistor. |

(1) These functions indicate signals electrically common with the input.
(2) Denotes negative logic: Low (–$V_I$) = Normal operation, Open = Output off

## TYPICAL CHARACTERISTICS

### Characteristic Data; $V_I$ = 48 V (1)

EFFICIENCY
vs
OUTPUT CURRENT ($V_O$ Bus)

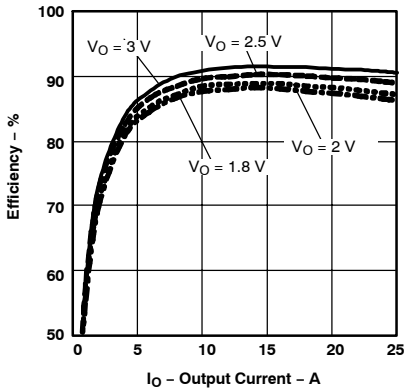



Figure 1.

OUTPUT VOLTAGE RIPPLE
vs
OUTPUT CURRENT ($V_O$ Bus)

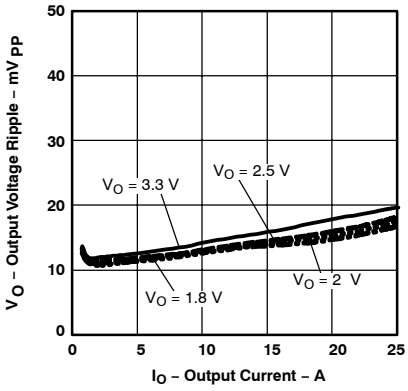



Figure 2.

POWER DISSIPATION
vs
OUTPUT CURRENT ($V_O$ Bus)

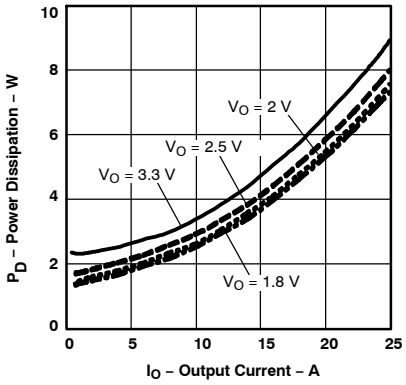



Figure 3.

(1) All data listed in Figure 1, Figure 2, and Figure 3 have been developed from actual products tested at 25°C. This data is considered typical data for the dc-dc converter.

## TYPICAL CHARACTERISTICS (continued)

### Safe Operating Areas; $V_I$ = 48 V(2)

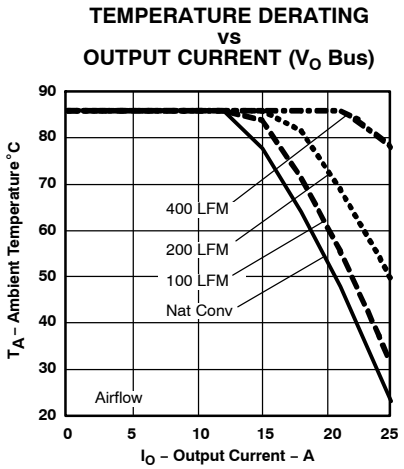



**Figure 4.**

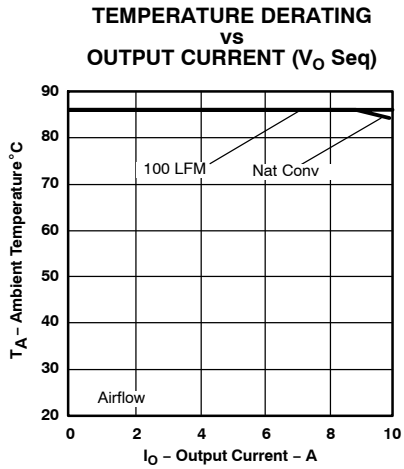



**Figure 5.**

(2) The temperature derating curves represent operating conditions at which internal components are at or below manufacturer's maximum rated operating temperature. See Figure 4 and Figure 5.

## APPLICATION INFORMATION

### Operating Features and System Considerations for the PTB48520W DC/DC Converter

#### Overcurrent Protection

To protect against load faults, these converters incorporate output overcurrent protection. Applying a load to the output that exceeds the converter overcurrent threshold (see applicable specification) causes the output voltage to momentarily fold back, and then shut down. Following shutdown, the module periodically attempts to automatically recover by initiating a soft-start power up. This is often described as a *hiccup* mode of operation, whereby the module continues in the cycle of successive shutdown and power up until the load fault is removed. Once the fault is removed, the converter automatically recovers and returns to normal operation.

#### Output Overvoltage Protection

The converter continually monitors for an output overvoltage (OV) condition, directly across the $+V_O$ *Bus* output. The OV threshold automatically tracks the output voltage set point to a level that is 25% higher than that set by the external $R_{(SET)}$ voltage adjust resistor. If the output voltage exceeds this threshold, the converter is immediately shut down and remains in a latched-off state. To resume normal operation, the converter must be actively reset. This can only be done by momentarily removing the input power to the converter. For fail-safe operation and redundancy, the OV protection uses circuitry that is independent of the converter internal feedback loop.

#### Differential Output Voltage Sense

A differential remote sense allows a converter regulation circuitry to compensate for limited amounts of IR drop, that may be incurred between the converter and load, in either the positive or return PCB traces. Connecting the (+)Sense and (–)Sense pins to the respective positive and ground reference of the load terminals improves the load regulation of the converter output voltage at that connection point. The (–)Sense pin should always be connected to the $V_O$ *COM*. The (+)Sense pin may be connected to either the $+V_O$ *Bus* or $+V_O$ *Seq* outputs.

When the (+)Sense pin is connected to the $V_O$ *Seq* output, the voltage at $V_O$ *Bus* voltage regulates slightly

## APPLICATION INFORMATION (continued)

higher. Depending on the load conditions on the $V_O$ *Seq* output, the voltage at $V_O$ *Bus* may be up to 100 mV higher than the converter set-point voltage. In addition, the Smart-Sense feature (incorporated into the converter) only engages sense compensation to the $V_O$ *Seq* output when that output voltage is close to the set point. During other conditions, such as power-up and power-down sequencing events, the sense circuit automatically defaults to sensing the $V_O$ *Bus* voltage, internal to the converter.

Leaving the (+)Sense and (–)Sense pins open does not damage the converter or load circuitry. The converter includes default circuitry that keeps the output voltage in regulation. If the remote sense feature is not used, the (–)Sense pin should always be connected to $V_O$ *COM*.

***Note:*** The remote sense feature is not designed to compensate for the forward drop of nonlinear or frequency dependent components that may be placed in series with the converter output. Examples include OR-ing diodes, filter inductors, ferrite beads, and fuses. When these components are enclosed by the sense pin connections, they are effectively placed inside the regulation control loop, which can adversely affect the stability of the converter.

### Overtemperature Protection

Overtemperature protection is provided by an internal temperature sensor, which monitors the temperature of the converter PCB (close to pin 1). If the PCB temperature exceeds a nominal 115°C, the converter shuts down. The converter then automatically restarts when the sensed temperature falls to approximately 105°C. When operated outside its recommended thermal derating envelope (see data sheet derating curves), the converter typcially cycles on and off at intervals from a few seconds to one or two minutes. This is to ensure that the internal components are not permanently damaged from excessive thermal stress.

### Undervoltage Lockout

The undervoltage lockout (UVLO) is designed to prevent the operation of the converter until the input voltage is close to the minimum operating voltage. The converter is held off when the input voltage is below the UVLO threshold, and turns on when the input voltage rises above the threshold. This prevents high start-up current during normal power up of the converter, and minimizes the current drain from the input source during low input voltage conditions. The converter meets full specifications when the minimum specified input voltage is reached. The UVLO circuitry also overrides the operation of the $V_O$ *Enable* control. Only when the input voltage is above the UVLO threshold is the $V_O$ *Enable* control functional.

### Primary-Secondary Isolation

These converters incorporate electrical isolation between the input terminals (primary) and the output terminals (secondary). All converters are tested to a withstand voltage of 1500 VDC. This complies with UL/cUL 60950 and EN 60950 and the requirements for operational isolation. It allows the converter to be configured for either a positive or negative input voltage source. The data sheet *Terminal Functions* table provides guidance as to the correct reference that must be used for the external control signals.

### Output Voltage Adjustment

The $V_O$ *Adjust* control sets the output voltages to a value higher than 1.8 V. For output voltages other than 1.8 V a single external resistor, $R_{(set)}$, must be connected directly between $V_O$ *Adjust* (pin 7) and (–)Sense (pin 6) pins. A 0.05-W rated resistor can be used. The tolerance should be 1%, with a temperature stability of 100 ppm/°C (or better). Place the resistor close to the converter and connect it directly between pins 7 and 6 using dedicated PCB traces (see typical application). Table 1 gives the preferred value of the external resistor for a number of standard voltages, along with the actual output voltage that this resistance value provides.

For other output voltages the value of the required adjust resistor may be calculated using Equation 1.

$$R_{set} = 6.49\ k\Omega \times \frac{1.225\ V}{V_{set} - 1.805\ V} - 4.42\ k\Omega \quad (1)$$

**Table 1. Standard Values of $R_{SET}$ for Common Output Voltages**

| $V_O$ (Required) | $R_{SET}$ (Standard Value) | $V_O$ (Actual) |
|---|---|---|
| 3.6 V | 0 Ω | 3.604 V |
| 3.3 V | 887 Ω | 3.303 V |
| 2.5 V | 6.98 kΩ | 2.503 V |
| 2.0 V | 35.7 kΩ | 2.003 V |
| 1.8 V | Open | 1.805 V |

### Input Current Limiting

**The converter is not internally fused.** For safety and overall system protection, the maximum input current to the converter must be limited. Active or passive current limiting can be used. Passive current limiting can be a fast-acting fuse. A 125-V fuse, rated no more than 10 A, is recommended. Active current limiting can be implemented with a current limited *Hot-Swap* controller.

### Thermal Considerations

Airflow may be necessary to ensure that the module can supply the desired load current in environments with elevated ambient temperatures. The required airflow rate is determined from the safe operating area (SOA). The SOA is the area beneath the applicable airflow rate curve on the graph of temperature derating vs output current. (See Typical Characteristics.) Operating the converter within the SOA limits ensures that all the internal components are at or below their stated maximum operating temperatures.

## Using the Output Enable Control on the PTB48520 Auto-Track Compatible DC/DC Converter

The $V_O$ Enable (pin 2) control is an active low input that allows the output voltage from the converter to be turned on and off while it is connected to the input source. The $V_O$ Enable input is referenced to the $-V_I$ (pin 3) (1), on the primary side of the converter isolation, and has its own internal pullup. The open-circuit voltage is approximately 20% of the applied input source voltage.

For the converter to function normally, pin 2 must be pulled low to $-V_I$ potential (2). The converter output then produces a regulated voltage whenever a valid source voltage is applied between $+V_I$ (pin 1) and $-V_I$ (pin 3) (3). If the voltage at pin 2 is allowed to rise above VIH(min), (see specification table), the output from the converter is turned off.

Figure 6 is an application schematic that shows the typical use of the Output Enable function. Note the discrete transistor (Q1). Either a discrete MOSFET or bipolar transistor is recommended to control this input. Table 2 gives the threshold requirements.

When placed in Off state, the output neither sources or sinks output current. The load voltage then decays as the output capacitance is discharged by the load circuit. With the output turned off, the current drawn from the input source is typically reduced to 2 mA.

(1) The *$V_O$ Enable* control uses $-V_I$ (pin 3) as ground reference. All voltages are with respect to $-V_I$.
(2) Use an open-collector (or open-drain) discrete transistor to control the *$V_O$ Enable* input. A pullup resistor is not necessary. To disable the converter, the control pin should be pulled low to less than +0.8 V. If the Output Enable feature is not used, pin 2 should be permanently connected to $-V_I$ (pin 3).
(3) The converter incorporates a UVLO. The UVLO does not allow the converter to power up until the input voltage is close to its minimum specified operating voltage. This is regardless of the state of the *Output Enable* control. Consult the specifications for the UVLO thresholds.

**Table 2. Output Enable Control Requirements (1)**

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| $V_{IH}$ | 2 | | | V |
| $V_{IL}$ | | | 0.8 | V |
| $V_{O/C}$ [Open-Circuit] | | | 15 | V |
| $I_I$ [pin 1 at $-V_{in}$] | | | –0.8 | mA |

(1) The *$V_O$ Enable* control uses $-V_I$ (pin 3) as its ground reference. All voltages are with respect to $-V_I$.

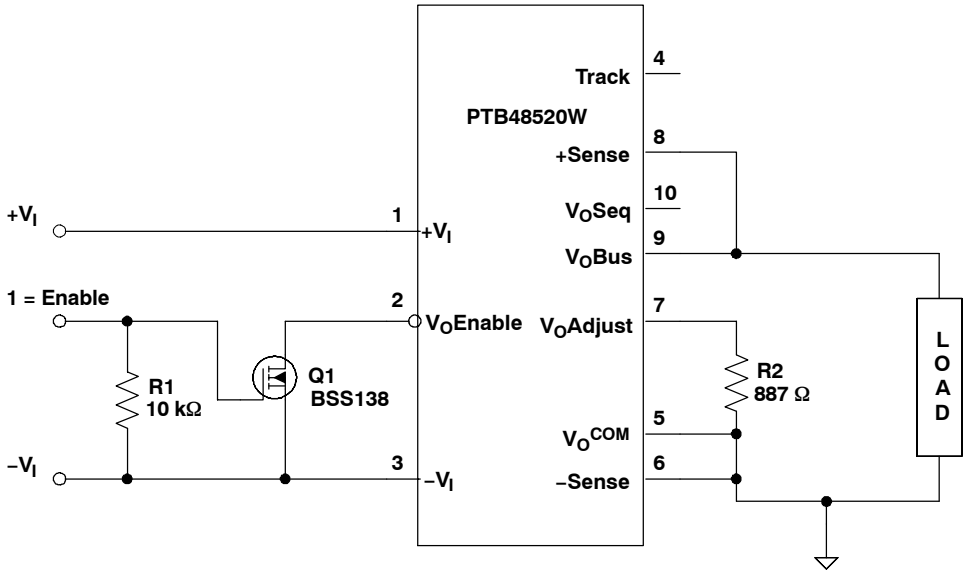



**Figure 6. Output Enable Operation**

**Turn-On Time:** In the circuit of Figure 6, turning Q1 off allows the voltage at pin 2 to rise to its internal pullup voltage. This disables the converter output. When Q1 is then turned on, it applies a low-level voltage to pin 2,

and enables the output of the converter. The converter produces a regulated output voltage within 50 ms. Figure 7 shows the output response of the converter after Q1 is turned on. The turnon of Q1 corresponds to the drop in the Q1 Vds waveform. Although the output voltage rise time is short (<10 ms), the indicated delay time ($t_d$) varies depending on the input voltage and the module's internal timing. The output voltage of the module was set to 3.3 V. The waveforms were measured with 48-Vdc input voltage and a 10-A resistive load.

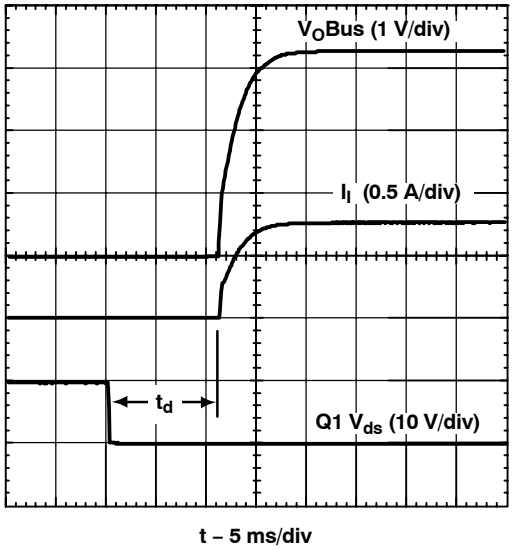



**Figure 7. Output Enable Power-Up Characteristic**

## Sequenced Power Up with POL Modules

### Overview

The dc/dc converter has two outputs, $V_O$ Seq and $V_O$ Bus. $V_O$ Bus is the main output from the converter. $V_O$ Seq is an output that is derived from $V_O$ Bus and can be sequenced with other supply voltages during power up. Both outputs are regulated to the same set-point voltage, except that the rise in the $V_O$ Seq output is controlled by the pin called Track, and delayed during power-up events. The delay allows the converter to both power and sequence with one or more non-isolated, 3.3-V input, Auto-Track compatible modules[1]. The rise of all output voltages is coordinated using a control signal common to the Track inputs of all Auto-Track compliant modules. The hold-off delay built into the PTB48520W holds the track control signal low to comply with the power-up requirements of the downstream non-isolated modules.

### Auto-Track Features

Figure 8 shows a block diagram of the converter Auto-Track features. During power up, $V_O$ Bus (pin 9) rises promptly, whenever the converter is connected to a valid input source and its output is enabled. $V_O$ Seq (pin 10) is the Auto-Track compatible output that is derived from $V_O$ Bus but controlled by the voltage presented at the Track input (pin 4). The control relationship is on a volt-for-volt basis, and is active from 0 V up to a voltage just below the $V_O$ Bus output. Between these two limits, the voltage at $V_O$ Seq follows that at the Track input. Once the Track input is at the $V_O$ Bus voltage, raising it higher has no further effect. The voltage at $V_O$ Seq cannot go higher than $V_O$ Bus, and if connected to +Sense (pin 8), then regulates at the set-point voltage.[2]

The control relationship between $V_O$ Seq and the Track input is the same as other Auto-Track compatible outputs, across all module types. By connecting the Track input of the converter to the Track inputs of other Auto-Track modules, all the associated output voltages can be made to follow the same rising control voltage during power-up transitions.[3] A suitable rising voltage is produced by the Track input internal R-C time constant. An external ramp waveform[4, 5] may also be used.

The Track input of the dc/dc converter includes a pullup resistor ($R_{TRK}$) to $V_O$ Bus, and a 1-$\mu$F capacitor ($C_{TRK}$) to $V_O$ COM. This enables the Track input to rise automatically once the internal MOSFET turns off. In sequencing applications, the non-isolated modules are powered by the $V_O$ Bus output. The internal MOSFET holds the Track voltage at ground for 20 ms after the $V_O$ Bus output is in regulation. This gives the non-isolated modules time to initialize so that their outputs can rise with the $V_O$ Seq output.

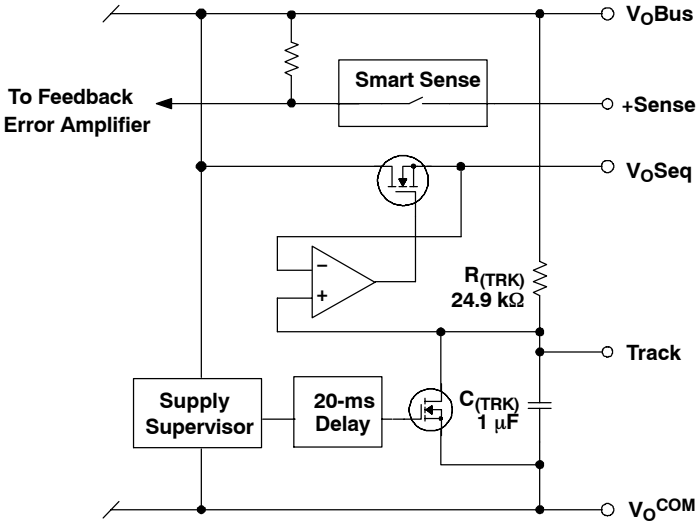



**Figure 8. Block Diagram of Auto-Track Features**

**Notes:**

1. Auto-Track compatible modules incorporate a Track input that can take direct control of the output voltage during power-up transistions. The control relationship is on a volt-for-volt basis and is active between the 0 V and the module's set-point voltage. Once the Track input is above the set-point voltage, the module remains at its set point. Connecting the Track input of a number of such modules together allows their outputs to follow a common control voltage during power up.
2. When +Sense (pin 8) is connected to the $V_o$ Seq output (pin 10), the $V_o$ Seq output is tightly regulated to the set-point voltage. In this configuration, the voltage at the $V_O$ Bus output (pin 9) is up to 100 mV higher.
3. The $V_O$ Seq output cannot sink load current. This constraint does not allow the module to coordinate a sequenced power down.
4. The slew rate for the Track input signal must be between 0.1 V/ms and 1 V/ms. Above this range, the $V_o$ Seq output may no longer accurately follow the Track input voltage. A slew rate below this range may thermally stress the converter. These slew rate limits are met whenever the Track input voltage is controlled by the internal R-C time constant of the modules being sequenced.
5. Whenever an external voltage is used to control the Track input, the source current **must** be limited. A resistance value of 2.74-kΩ is recommended for this purpose. This is necessary to protect the internal transistor to the converter's Track control input. This transistor holds the track control voltage at ground potential for 20 ms after the $V_O$ Bus output is in regulation.

### Typical Power-Up Sequencing Configuration

Figure 10 shows how the converter (U1) can be configured to provide two 3.3-V sources, that allow it to both power and sequence with one or more non-isolated POL modules. The example shows two PTH03050W modules (U2 and U3), each rated for up 6 A of output current. Additional voltages, as well as modules with a higher output current capability can also be specified to meet a specific application. The number of downstream modules, their respective output voltage and load current rating is only limited by the amount of current available at the $V_O$ Bus output. This is 25 A, less the current allocated to the load circuit via the $V_O$ Seq output.

The output voltage adjust range is 1.8 V to 3.6 V, which is compatible with the 3.3-V input non-isolated POL modules. In these applications, the output voltage must always be set to 3.3 V (R1 = 887 Ω). Note that this sets the output voltage of both the $V_O$ Bus and $V_O$ Seq outputs. The 3.3-V input non-isolated modules, U2 and U3, can be set to any voltage over the range, 0.8 V to 2.5 V. In this example, they are set to 2.5 V (R2 = 2.21 kΩ) and 1.8 V (R3 = 5.49 kΩ), respectively. Figure 9 shows the power-up waveforms from Figure 10 when the Track control input to all three modules are simply connected together.

The converter provides input power to the downstream non-isolated modules via the $V_O$ Bus output. This output rises first to allow the downstream modules to complete their power-up initialization. $V_O$ Seq (3.3 V), and the outputs $V_{(POL)}1$ (2.5 V) and $V_{(POL)}2$ (1.8 V), supply the load circuit. These three outputs are controlled by the track control voltage, which the converter holds at ground potential for 20 ms. When the track control voltage is finally allowed to rise, the three outputs rise simultaneously to their respective set-point voltages.

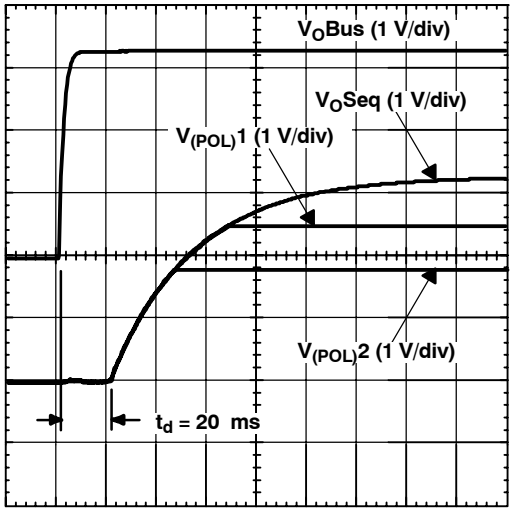



**Figure 9. Power-Up Waveforms with POL Modules**

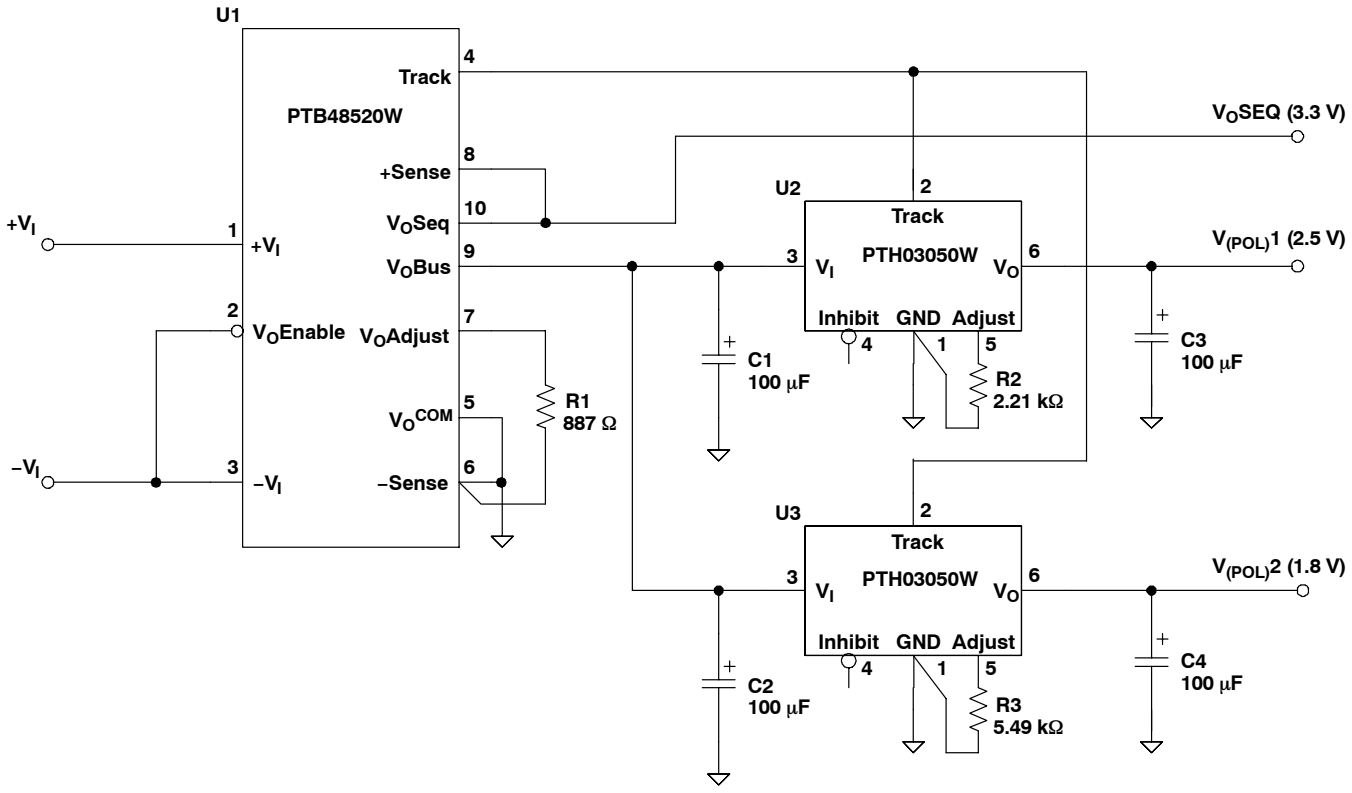



**Figure 10. Power-Up Sequencing With Non-Isolated POL Modules**

### Stand-Alone Operation

The wide output voltage adjust range makes the PTB48520W an attractive product as a stand-alone dc/dc converter. In these applications, it is not required to power up or sequence with any non-isolated POL modules. The output voltage can be adjusted to any value over the range, 1.8 V to 3.6 V, and the Auto-Track features simply disregarded.

Figure 11 shows the recommended configuration when the module is used as a stand-alone converter. In this case, a sequenced output voltage is not required, and the main output ($V_O$ Bus) can be used to supply the load. Both the Track pin and the $V_O$ Seq output are simply left open circuit. The (+)Sense pin is connected to the $V_O$ Bus output for improved load regulation.

When the converter is operated in this mode, the output from $V_O$ Bus rises promptly on power up. The converter also exhibits slightly less power dissipation along with a corresponding improvement in operating efficiency.

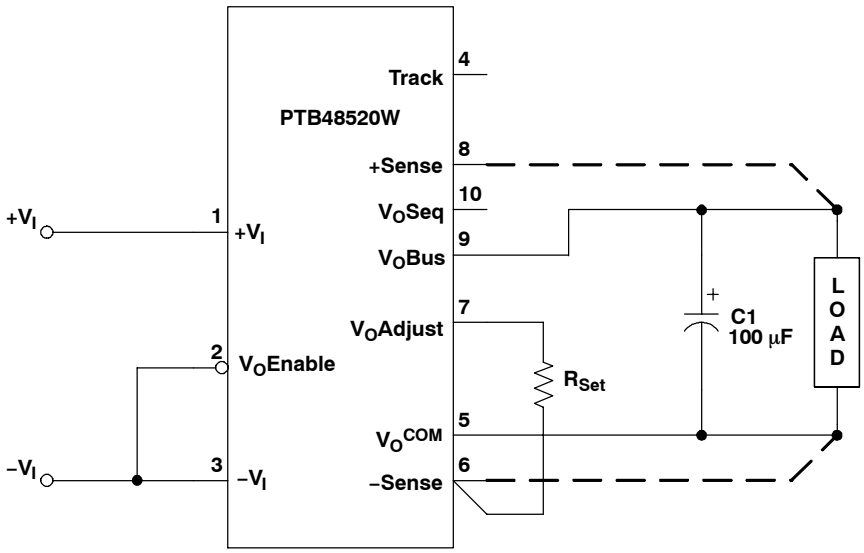



**Figure 11. Stand-Alone Configuration**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PTB48520WAH | NRND | Through-Hole Module | ERP | 10 | 9 | RoHS (In Work) & non-Green | SN | N / A for Pkg Type | -40 to 85 | | |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

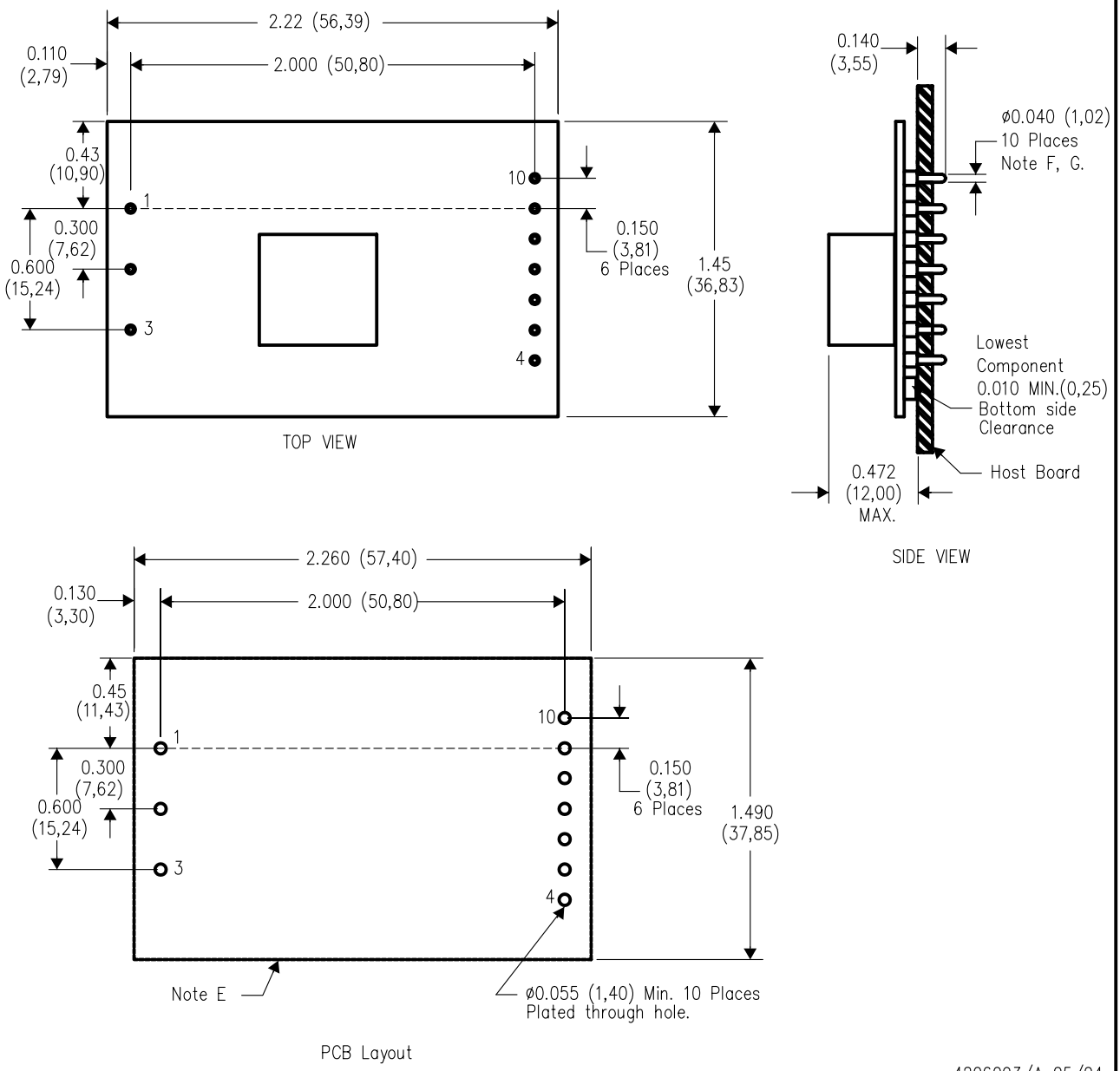
**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

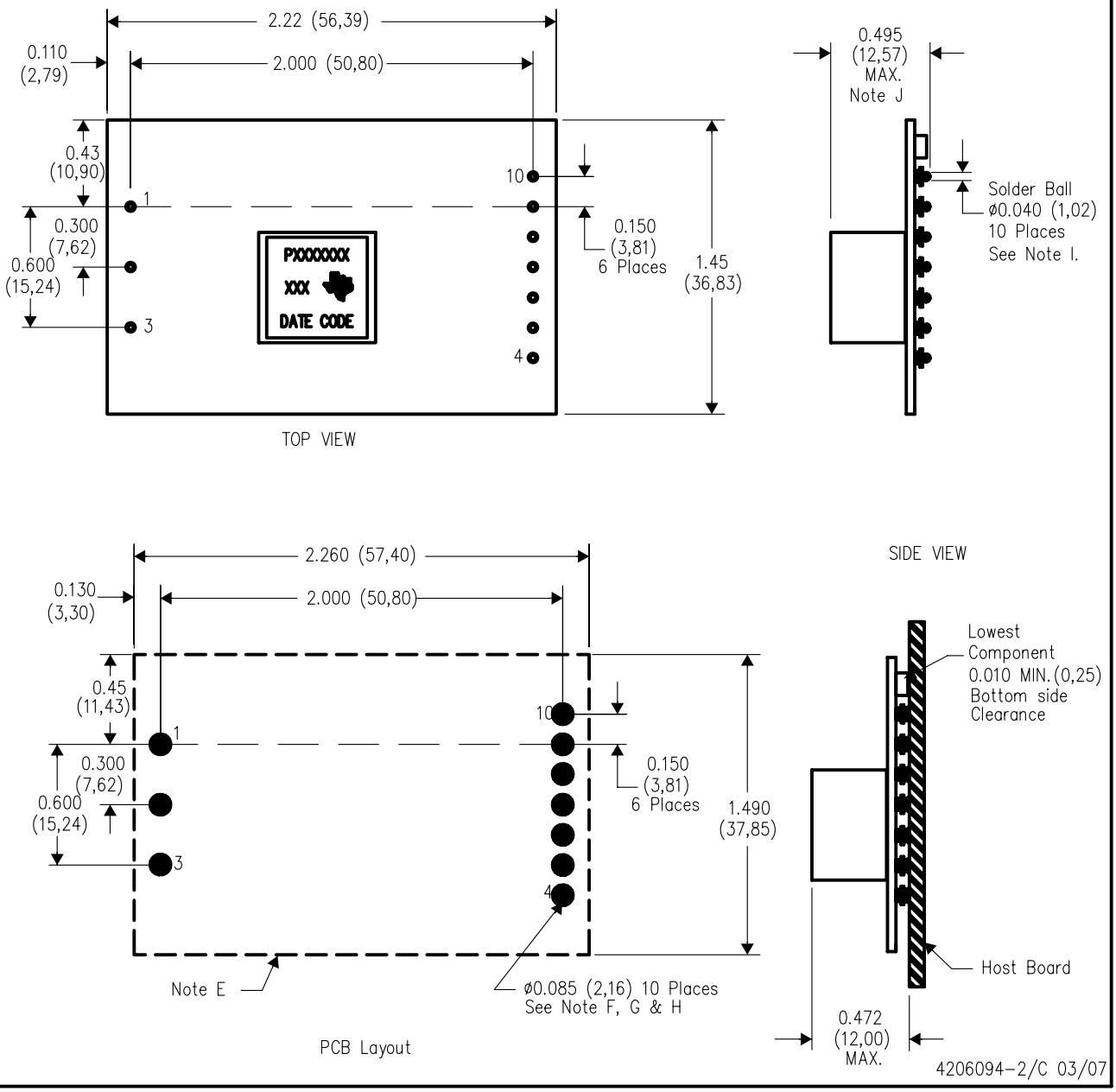
**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

## ERP (R–PDSS–T10) DOUBLE SIDED MODULE




NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.020 (±0,51mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components.
F. Pins are 0.040" (1,02) diameter with 0.070" (1,78) diameter standoff shoulder.
G. All pins: Material – Copper Alloy
Finish – Tin (100%) over Nickel plate

## ERQ (R–PDSS–T10) DOUBLE SIDED MODULE




NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.020 (±0,51mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components.
F. Power pin connection should utilize four or more vias to the interior power plane of 0.025 (0,63) I.D. per input, ground and output pin (or the electrical equivalent).
G. Paste screen opening: 0.080 (2,03) to 0.085 (2,16). Paste screen thickness: 0.006 (0,15).
H. Pad type: Solder mask defined.
I. All pins: Material – Copper Alloy
Finish – Tin (100%) over Nickel plate
Solder Ball – See product data sheet.
J. Dimension prior to reflow solder.

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