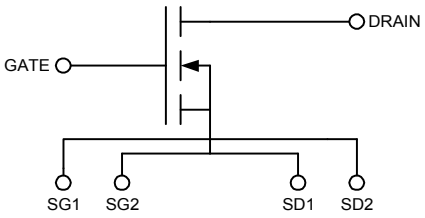
# DE475-501N44A
## RF Power MOSFET

- N-Channel Enhancement Mode
- Low $Q_g$ and $R_g$
- High dv/dt
- Nanosecond Switching
- 30MHz Maximum Frequency

| | | |
|---|---|---|
| $V_{DSS}$ | = | 500 V |
| $I_{D25}$ | = | 48 A |
| $R_{DS(on)}$ | ≤ | 0.13 Ω |
| $P_{DC}$ | = | 1800W |

| Symbol | Test Conditions | Maximum Ratings | |
|---|---|---|---|
| $V_{DSS}$ | $T_J$ = 25°C to 150°C | 500 | V |
| $V_{DGR}$ | $T_J$ = 25°C to 150°C; $R_{GS}$ = 1 MΩ | 500 | V |
| $V_{GS}$ | Continuous | ±20 | V |
| $V_{GSM}$ | Transient | ±30 | V |
| $I_{D25}$ | $T_c$ = 25°C | 48 | A |
| $I_{DM}$ | $T_c$ = 25°C, pulse width limited by $T_{JM}$ | 288 | A |
| $I_{AR}$ | $T_c$ = 25°C | 44 | A |
| $E_{AR}$ | $T_c$ = 25°C | 30 | mJ |
| dv/dt | $I_S \le I_{DM}$, di/dt ≤ 100A/μs, $V_{DD} \le V_{DSS}$, $T_j \le 150°C$, $R_G$ = 0.2Ω | 5 | V/ns |
| | $I_S$ = 0 | >200 | V/ns |
| $P_{DC}$ | | 1800 | W |
| $P_{DHS}$ | $T_c$ = 25°C<br>Derate 4.0W/°C above 25°C | 730 | W |
| $P_{DAMB}$ | $T_c$ = 25°C | 4.5 | W |
| $R_{thJC}$ | | 0.08 | C/W |
| $R_{thJHS}$ | | 0.20 | C/W |




| Symbol | Test Conditions | Characteristic Values<br>$T_J$ = 25°C unless otherwise specified | | | |
|---|---|---|---|---|---|
| | | min. | typ. | max. | |
| $V_{DSS}$ | $V_{GS}$ = 0 V, $I_D$ = 3 ma | 500 | | | V |
| $V_{GS(th)}$ | $V_{DS} = V_{GS}$, $I_D$ = 4 ma | 3.5 | 4.5 | 5.5 | V |
| $I_{GSS}$ | $V_{GS}$ = ±20 $V_{DC}$, $V_{DS}$ = 0 | | | ±100 | nA |
| $I_{DSS}$ | $V_{DS}$ = 0.8 $V_{DSS}$ $T_J$ = 25°C<br>$V_{GS}$ = 0 $T_J$ = 125°C | | | 50<br>1 | μA<br>mA |
| $R_{DS(on)}$ | $V_{GS}$ = 15 V, $I_D = 0.5I_{D25}$<br>Pulse test, t ≤ 300μS, duty cycle d ≤ 2% | | | 0.13 | Ω |
| $g_{fs}$ | $V_{DS}$ = 15 V, $I_D = 0.5I_{D25}$, pulse test | | 14 | | S |
| $T_J$ | | -55 | | +175 | °C |
| $T_{JM}$ | | | 175 | | °C |
| $T_{stg}$ | | -55 | | +175 | °C |
| $T_L$ | 1.6mm (0.063 in) from case for 10 s | | 300 | | °C |
| **Weight** | | | 3 | | g |

### Features

- Isolated Substrate
  - high isolation voltage (>2500V)
  - excellent thermal transfer
  - Increased temperature and power cycling capability
- IXYS advanced low $Q_g$ process
- Low gate charge and capacitances
  - easier to drive
  - faster switching
- Low $R_{DS(on)}$
- Very low insertion inductance (<2nH)
- No beryllium oxide (BeO) or other hazardous materials

### Advantages

- Optimized for RF and high speed switching at frequencies to 30MHz
- Easy to mount—no insulators needed
- High power density

| Symbol | Test Conditions | Characteristic Values ($T_J$ = 25°C unless otherwise specified) min. | typ. | max. | |
|---|---|---|---|---|---|
| $R_G$ | | | 0.3 | | Ω |
| $C_{iss}$ | | | 5100 | | pF |
| $C_{oss}$ | $V_{GS}$ = 0 V, $V_{DS}$ = 0.8 $V_{DSS(max)}$, f = 1 MHz | | 300 | | pF |
| $C_{rss}$ | | | 92 | | pF |
| $C_{stray}$ | Back Metal to any Pin | | 46 | | pF |
| $T_{d(on)}$ | | | 5 | | ns |
| $T_{on}$ | $V_{GS}$ = 15 V, $V_{DS}$ = 0.8 $V_{DSS}$ $I_D$ = 0.5 $I_{DM}$ | | 5 | | ns |
| $T_{d(off)}$ | $R_G$ = 0.2 Ω (External) | | 5 | | ns |
| $T_{off}$ | | | 8 | | ns |
| $Q_{g(on)}$ | | | 155 | | nC |
| $Q_{gs}$ | $V_{GS}$ = 10 V, $V_{DS}$ = 0.5 $V_{DSS}$ $I_D$ = 0.5 $I_{D25}$ | | 35 | | nC |
| $Q_{gd}$ | | | 87 | | nC |

| Source-Drain Diode | | Characteristic Values ($T_J$ = 25°C unless otherwise specified) min. | | max. | |
|---|---|---|---|---|---|
| Symbol | Test Conditions | | | | |
| $I_S$ | $V_{GS}$ = 0 V | | | 44 | A |
| $I_{SM}$ | Repetitive; pulse width limited by $T_{JM}$ | | | 288 | A |
| $V_{SD}$ | $I_F$ = $I_S$, $V_{GS}$ = 0 V, Pulse test, t ≤ 300 μs, duty cycle ≤ 2% | | | 1.5 | V |
| $T_{rr}$ | | | 200 | | ns |
| $Q_{RM}$ | $I_F$ = $I_S$, -di/dt = 100A/μs, $V_R$ = 100V | | 0.6 | | μC |
| $I_{RM}$ | | | 14 | | A |

CAUTION: Operation at or above the Maximum Ratings values may impact device reliability or cause permanent damage to the device.

Information in this document is believed to be accurate and reliable. IXYSRF reserves the right to make changes to information published in this document at any time and without notice.

For detailed device mounting and installation instructions, see the "*Device Installation & Mounting Instructions*" technical note on the IXYSRF web site at;

http://www.ixysrf.com/pdf/switch_mode/appnotes/7de_series_mosfet_installation_instructions.pdf

Fig. 1

**Typical Transfer Characteristics**
**$V_{DS}$ = 50V, PW = 15µS**

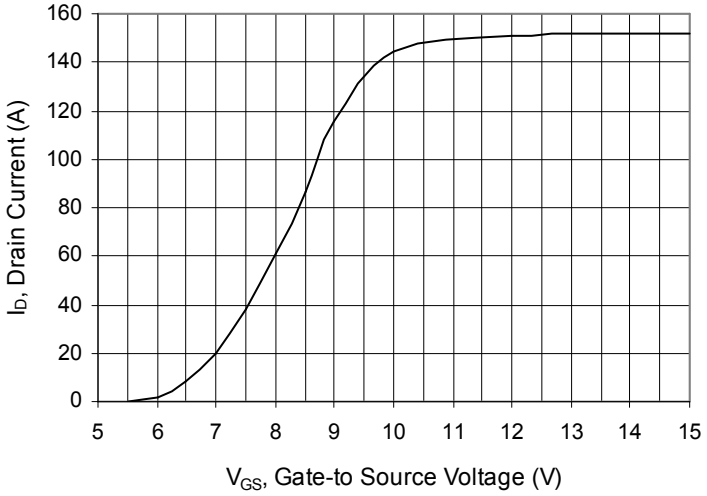



Fig. 2

**Typical Output Characteristics**

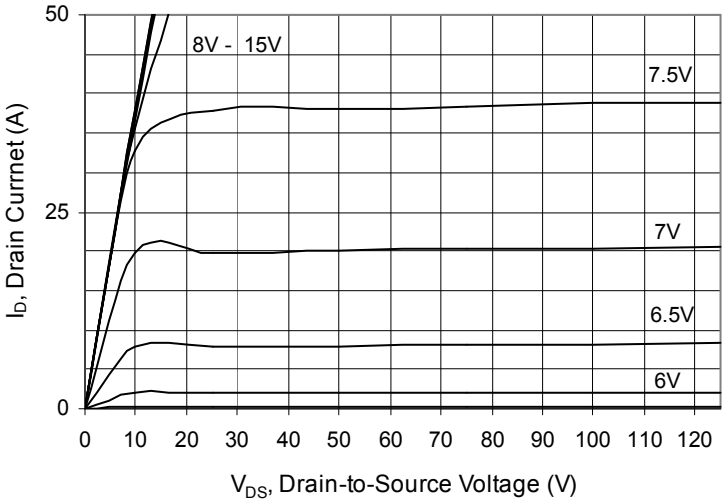



Fig. 3

Gate Charge vs. Gate-to-Source Voltage
$V_{DS}$ = 250V, $I_D$ = 22A

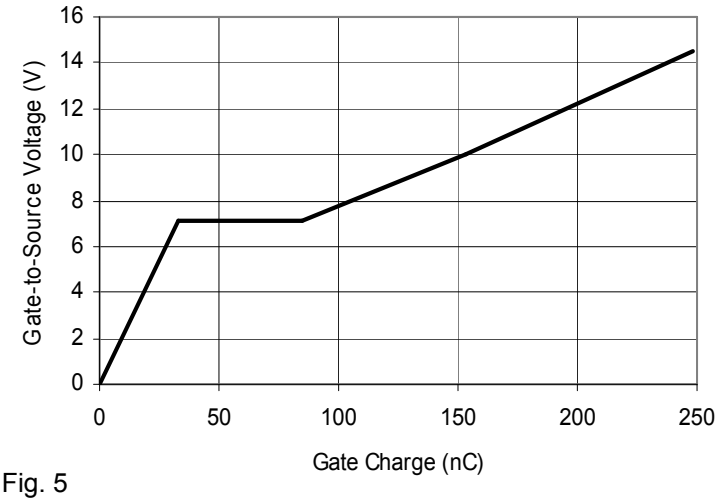



Fig. 4

**Extended Typical Output Characteristics**

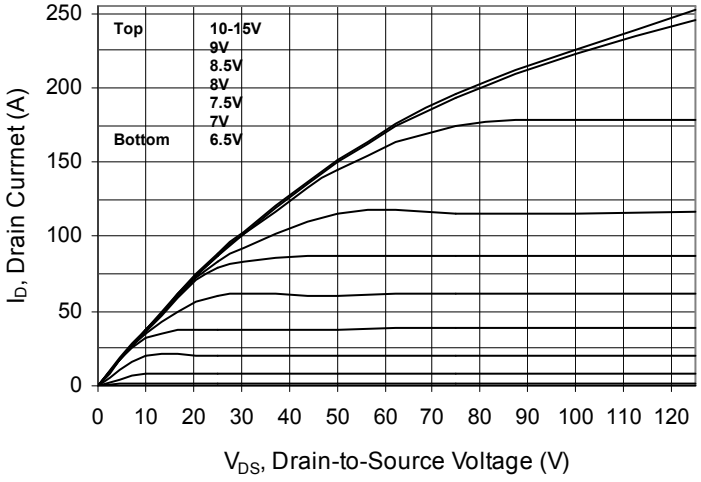



Fig. 5

**$V_{DS}$ vs. Capacitance**

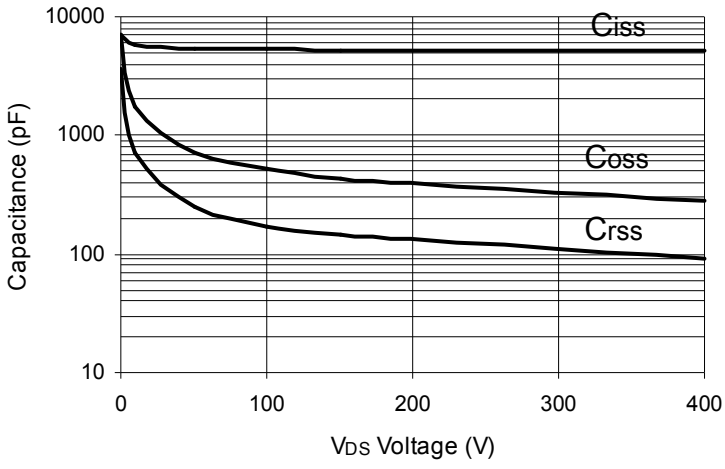
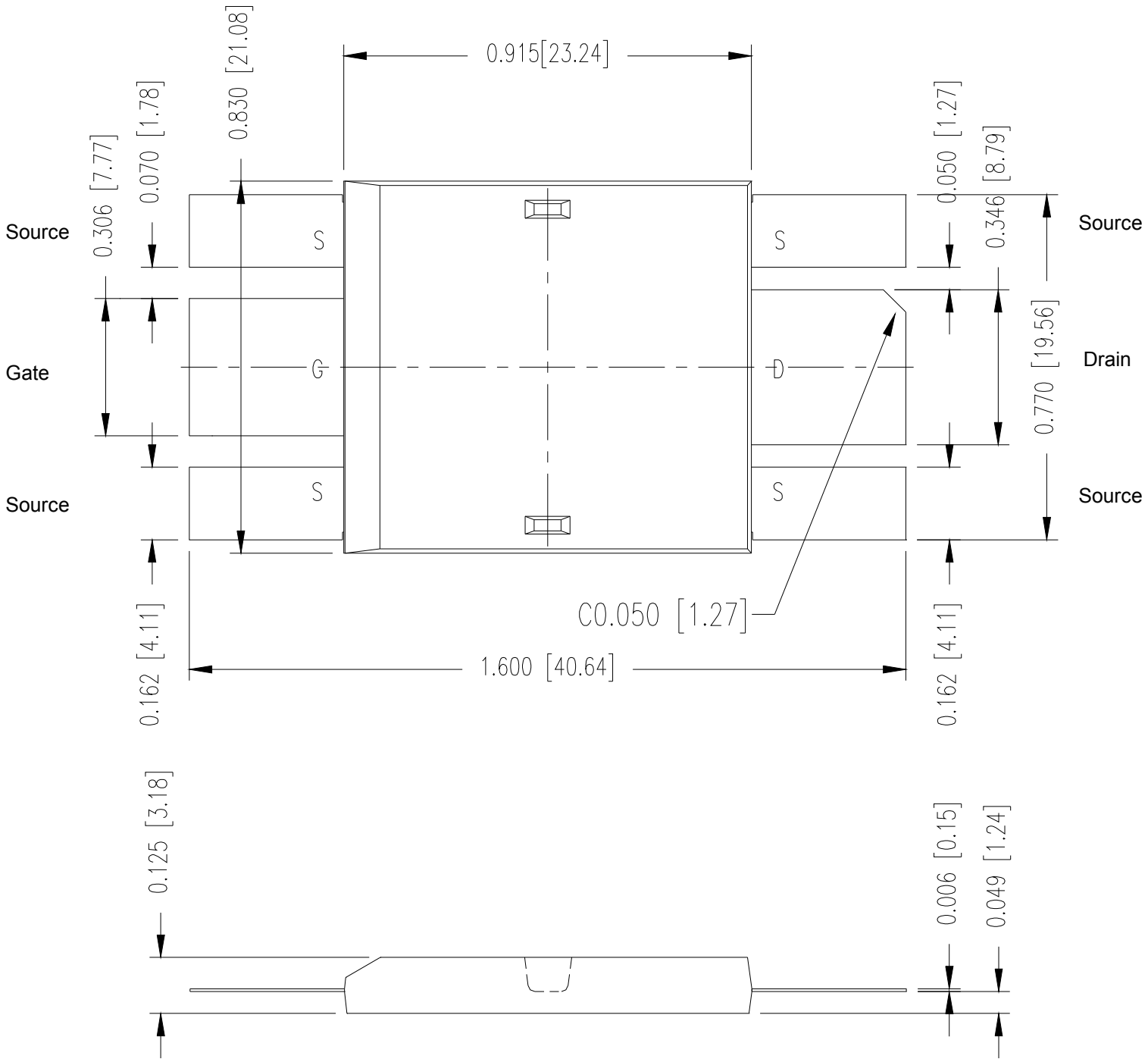


Fig. 6 Package Drawing



## 501N44A DE-SERIES SPICE Model (Preliminary)

The DE-SERIES SPICE Model is illustrated in Figure 7. The model is an expansion of the SPICE level 3 MOSFET model. It includes the stray inductive terms $L_G$, $L_S$ and $L_D$. Rd is the $R_{DS(ON)}$ of the device, Rds is the resistive leakage term. The output capacitance, $C_{OSS}$, and reverse transfer capacitance, $C_{RSS}$ are modeled with reversed biased diodes. This provides a varactor type response necessary for a high power device model. The turn on delay and the turn off delay are adjusted via Ron and Roff.

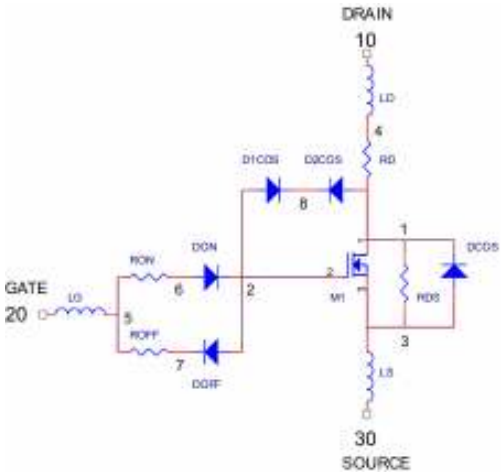



Figure 7 DE-SERIES SPICE Model

This SPICE model may be downloaded as a text file from the IXYSRF web site at

http://www.ixysrf.com/products/switch_mode.html

http://www.ixysrf.com/spice/de475-501n44a.html

Net List:

```
.SUBCKT 501N44A   10 20 30
*  TERMINALS:  D  G  S
*  500 Volt  44 Amp  0.13 ohm  N-Channel Power MOSFET
*  REV.A  01-09-02
M1   1  2  3  3  DMOS L=1U W=1U
RON   5  6  0.3
DON   6  2  D1
ROF   5  7 .1
DOF   2  7  D1
D1CRS 2  8  D2
D2CRS 1  8  D2
CGS   2  3  5.2N
RD    4  1  0.13
DCOS  3  1  D3
RDS   1  3  5.0MEG
LS    3  30 .5N
LD   10  4  1N
LG   20  5  1N
.MODEL DMOS NMOS (LEVEL=3 VTO=3.0 KP=3.8)
.MODEL D1 D (IS=.5F CJO=1P BV=100 M=.5 VJ=.6 TT=1N)
.MODEL D2 D (IS=.5F CJO=400P BV=500 M=.4 VJ=.6 TT=400N RS=10M)
.MODEL D3 D (IS=.5F CJO=900P BV=500 M=.3 VJ=.4 TT=400N RS=10M)
.ENDS
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