

MOSFET

OptiMOS™ 5 Power-Transistor, 100 V

Features

- Optimized for high performance SMPS, e.g. synchronous rectification
- N-channel
- 100% avalanche tested
- Superior thermal resistance
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

Product validation

Fully qualified according to JEDEC for Industrial Applications

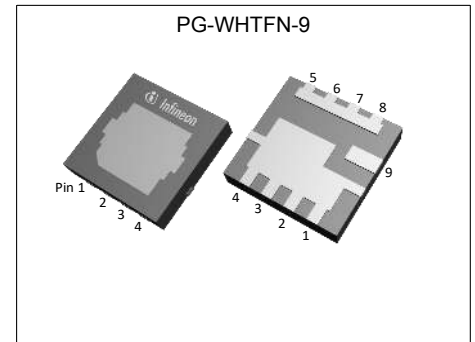
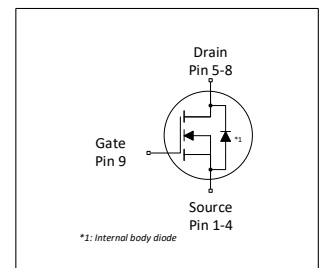


Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	100	V
$R_{DS(on),max}$	6.5	m Ω
I_D	85	A
Q_{oss}	40	nC
$Q_G(0V...10V)$	34	nC



RoHS

Type / Ordering Code	Package	Marking	Related Links
IQE065N10NM5CGSC	PG-WHTFN-9	S	-

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1 Maximum ratings

at $T_A=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	85 60 46 13	A	$V_{GS}=10\text{ V}$, $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$, $T_C=100\text{ °C}$ $V_{GS}=6\text{ V}$, $T_C=100\text{ °C}$ $V_{GS}=10\text{ V}$, $T_A=25\text{ °C}$, $R_{thJA}=60\text{ °C/W}^2)$
Pulsed drain current ³⁾	$I_{D,pulse}$	-	-	340	A	$T_A=25\text{ °C}$
Avalanche energy, single pulse ⁴⁾	E_{AS}	-	-	147	mJ	$I_D=20\text{ A}$, $R_{GS}=25\text{ }\Omega$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	100 2.5	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}$, $R_{thJA}=60\text{ °C/W}^2)$
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	IEC climatic category; DIN IEC 68-1: 55/175/56

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	0.8	1.5	°C/W	-
Thermal resistance, junction - case, top	R_{thJC}	-	0.7	-	°C/W	-
Thermal resistance, junction - ambient, 6 cm ² cooling area ²⁾	R_{thJA}	-	-	60	°C/W	-

¹⁾ Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

³⁾ See Diagram 3 for more detailed information

⁴⁾ See Diagram 13 for more detailed information

3 Electrical characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	100	-	-	V	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2.2	3.0	3.8	V	$V_{DS}=V_{GS}$, $I_D=48\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	0.1 10	1.0 100	μA	$V_{DS}=100\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$ $V_{DS}=100\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$
Gate-source leakage current	I_{GSS}	-	10	100	nA	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	5.7 7.2	6.5 11	$\text{m}\Omega$	$V_{GS}=10\text{ V}$, $I_D=20\text{ A}$ $V_{GS}=6\text{ V}$, $I_D=10\text{ A}$
Gate resistance	R_G	-	0.7	-	Ω	-
Transconductance	g_{fs}	-	55	-	S	$ V_{DS} \geq 2 I_D /R_{DS(on)max}$, $I_D=20\text{ A}$

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance ¹⁾	C_{iss}	-	2300	3000	pF	$V_{GS}=0\text{ V}$, $V_{DS}=50\text{ V}$, $f=1\text{ MHz}$
Output capacitance ¹⁾	C_{oss}	-	340	440	pF	$V_{GS}=0\text{ V}$, $V_{DS}=50\text{ V}$, $f=1\text{ MHz}$
Reverse transfer capacitance ¹⁾	C_{rss}	-	18	32	pF	$V_{GS}=0\text{ V}$, $V_{DS}=50\text{ V}$, $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	8.9	-	ns	$V_{DD}=50\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=20\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Rise time	t_r	-	3.8	-	ns	$V_{DD}=50\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=20\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	21.1	-	ns	$V_{DD}=50\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=20\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Fall time	t_f	-	7.5	-	ns	$V_{DD}=50\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=20\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$

Table 6 Gate charge characteristics²⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	10.1	-	nC	$V_{DD}=50\text{ V}$, $I_D=20\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	6.8	-	nC	$V_{DD}=50\text{ V}$, $I_D=20\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge ¹⁾	Q_{gd}	-	7.4	11.1	nC	$V_{DD}=50\text{ V}$, $I_D=20\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Switching charge	Q_{sw}	-	10.7	-	nC	$V_{DD}=50\text{ V}$, $I_D=20\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total ¹⁾	Q_g	-	34	43.0	nC	$V_{DD}=50\text{ V}$, $I_D=20\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	4.4	-	V	$V_{DD}=50\text{ V}$, $I_D=20\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total, sync. FET	$Q_{g(sync)}$	-	29	-	nC	$V_{DS}=0.1\text{ V}$, $V_{GS}=0\text{ to }10\text{ V}$
Output charge ¹⁾	Q_{oss}	-	40	53	nC	$V_{DS}=50\text{ V}$, $V_{GS}=0\text{ V}$

¹⁾ Defined by design. Not subject to production test.

²⁾ See "Gate charge waveforms" for parameter definition

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	74	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	340	A	$T_C=25\text{ °C}$
Diode forward voltage	V_{SD}	-	0.83	1.1	V	$V_{GS}=0\text{ V}, I_F=20\text{ A}, T_j=25\text{ °C}$
Reverse recovery time ¹⁾	t_{rr}	-	36	72	ns	$V_R=50\text{ V}, I_F=20\text{ A}, di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge ¹⁾	Q_{rr}	-	40	80	nC	$V_R=50\text{ V}, I_F=20\text{ A}, di_F/dt=100\text{ A}/\mu\text{s}$

¹⁾ Defined by design. Not subject to production test.

4 Electrical characteristics diagrams

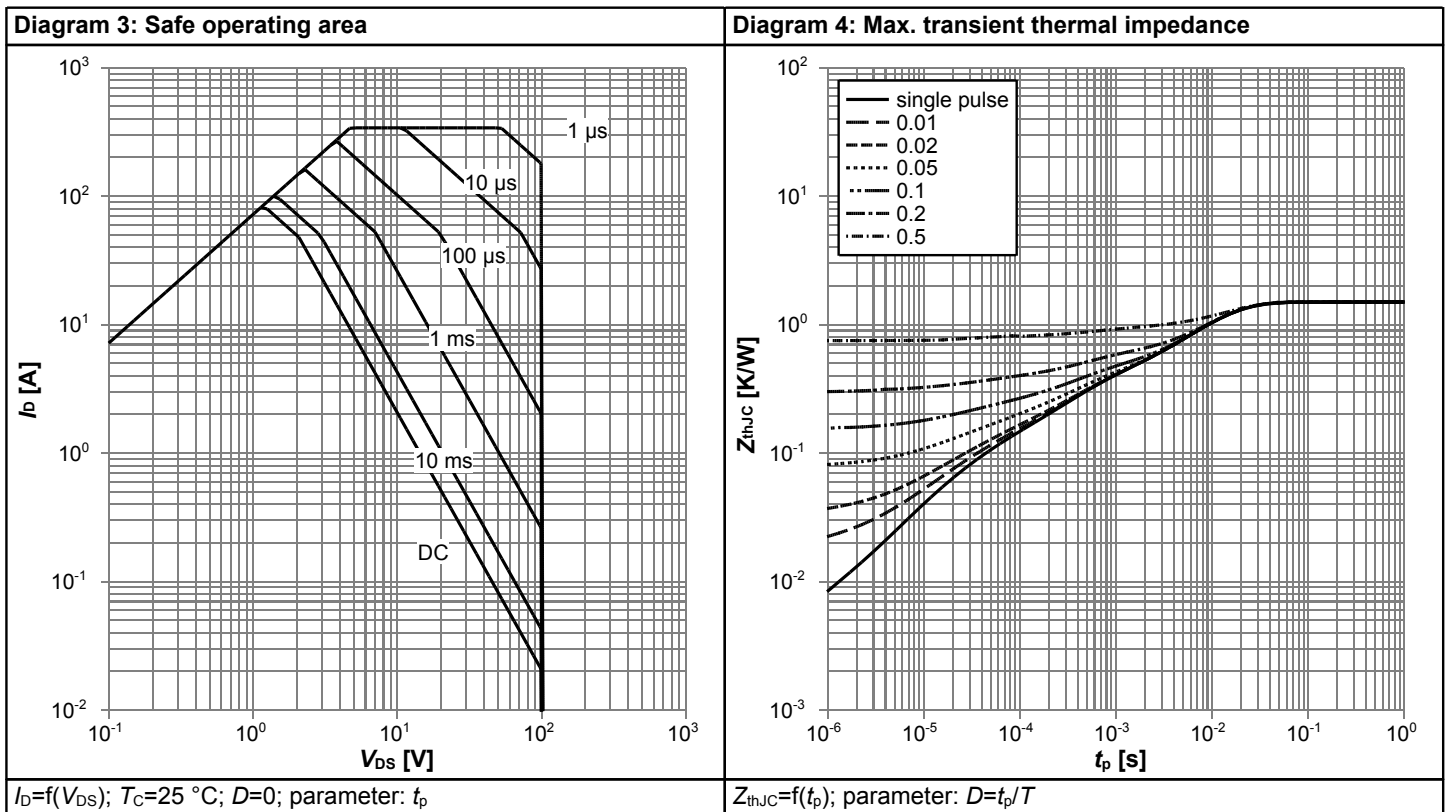
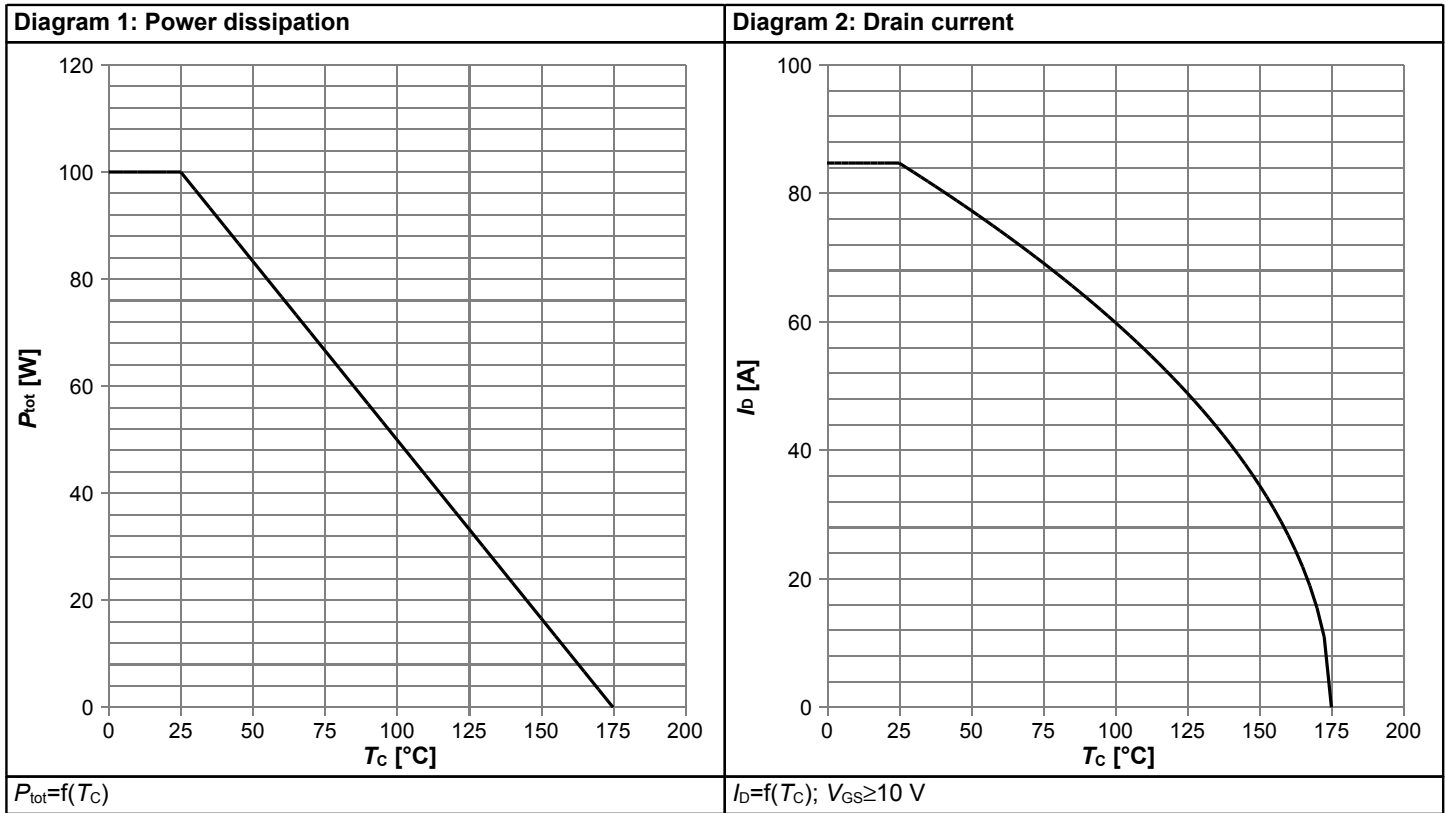
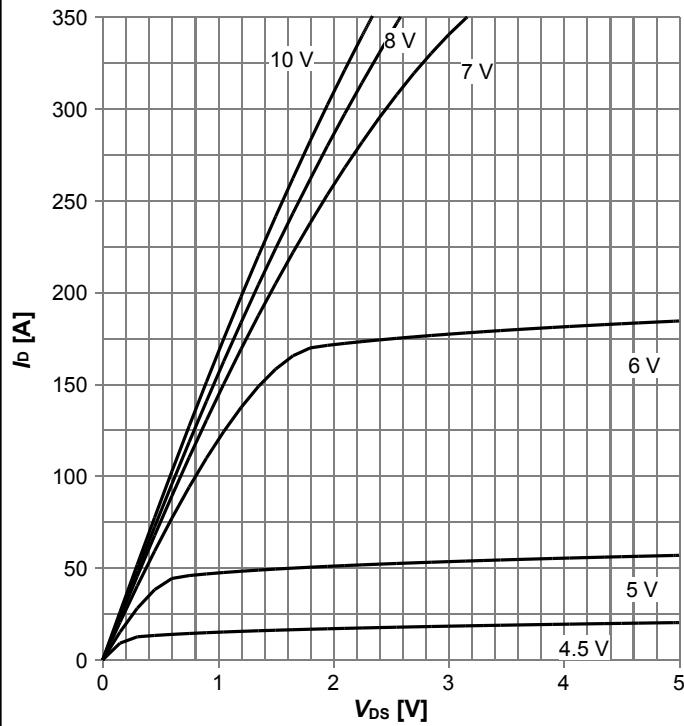
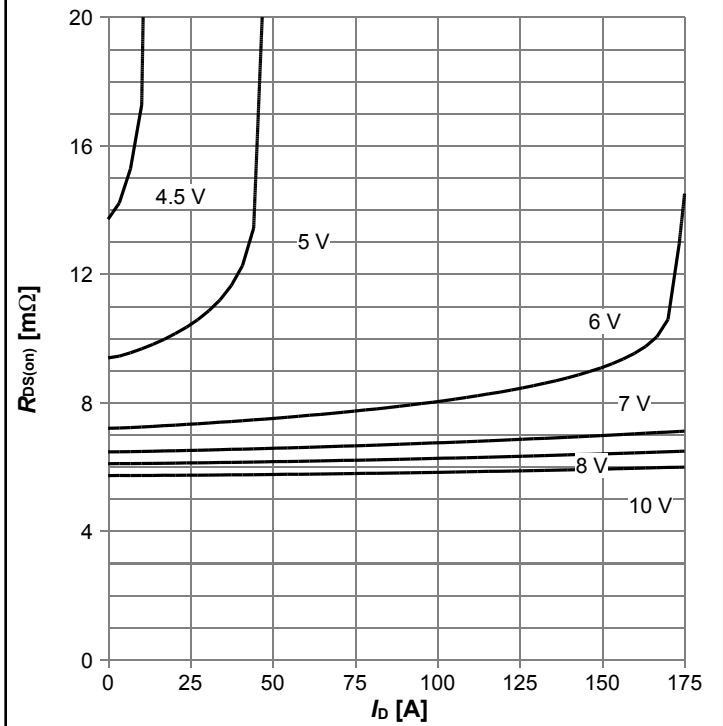


Diagram 5: Typ. output characteristics



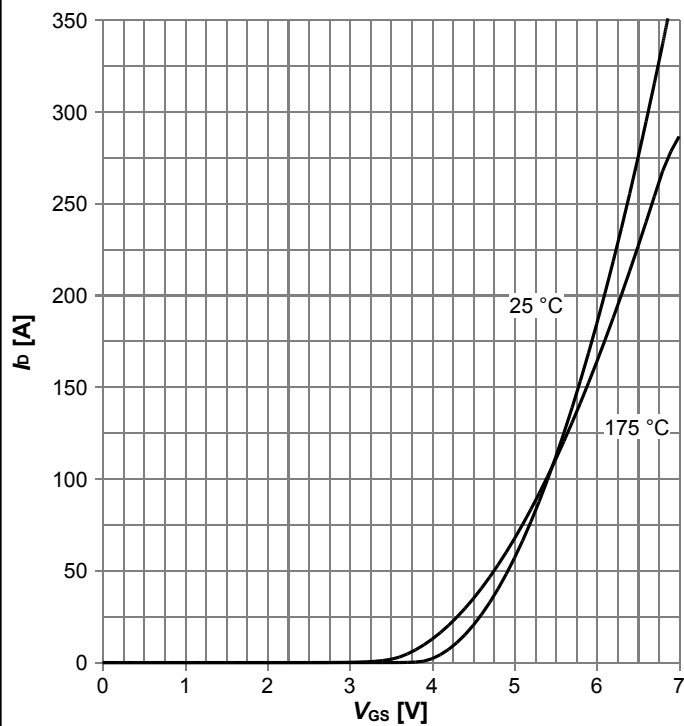
$I_D = f(V_{DS}), T_j = 25\text{ °C};$ parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



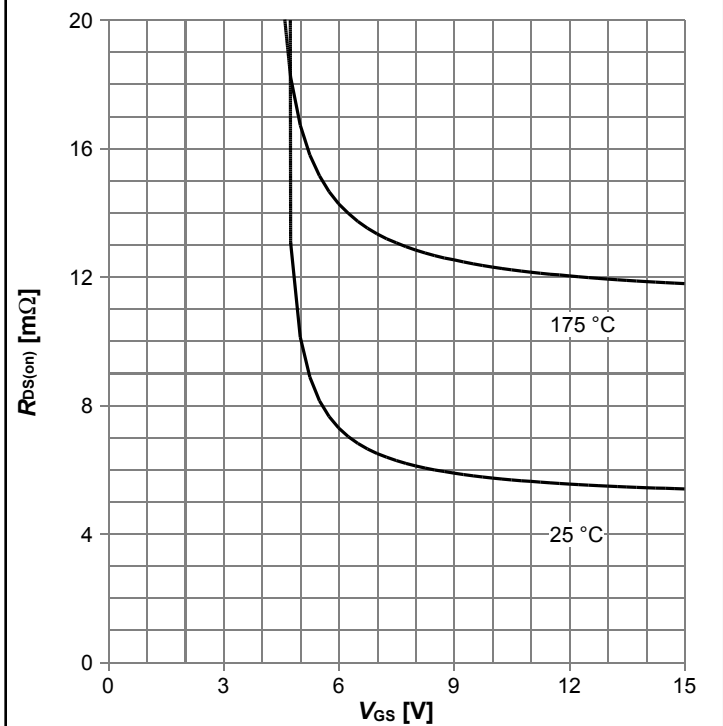
$R_{DS(on)} = f(I_D), T_j = 25\text{ °C};$ parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



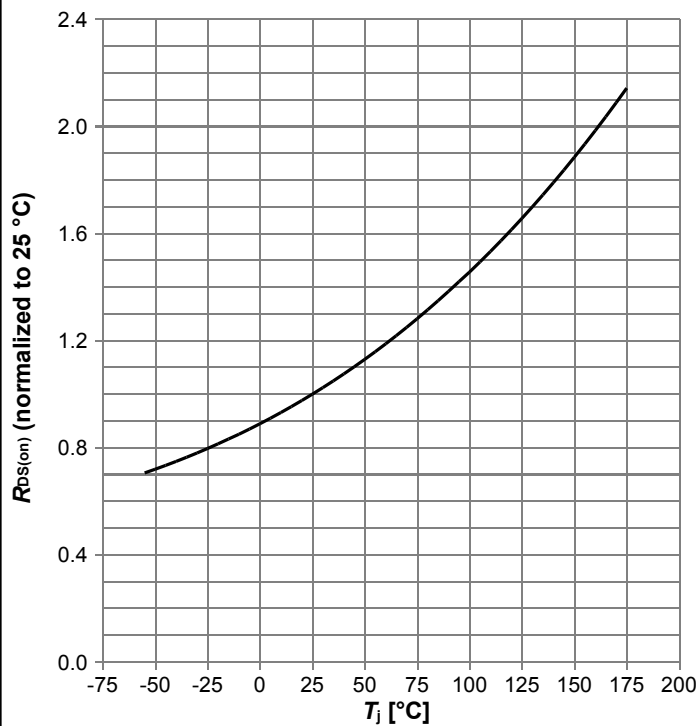
$I_D = f(V_{GS}), |V_{DS}| > 2|I_D|R_{DS(on)max};$ parameter: T_j

Diagram 8: Typ. drain-source on resistance



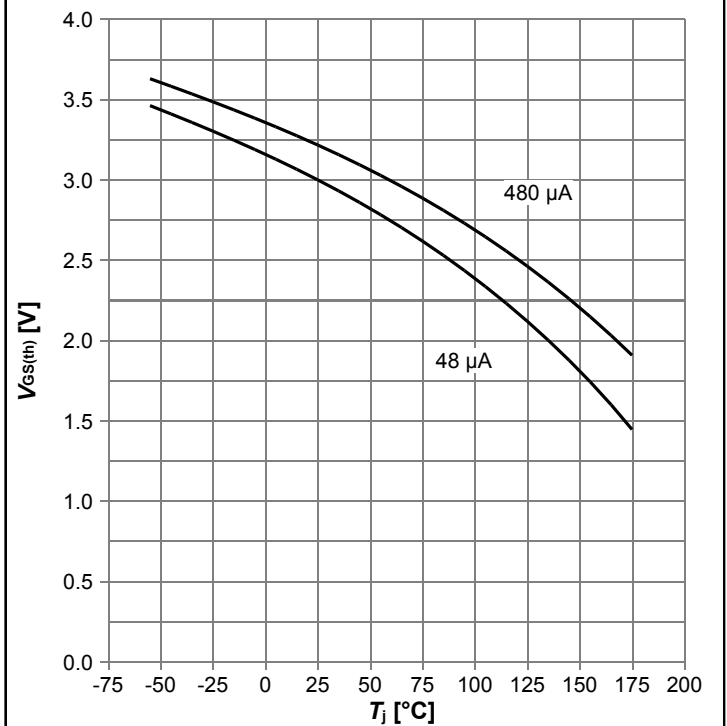
$R_{DS(on)} = f(V_{GS}), I_D = 20\text{ A};$ parameter: T_j

Diagram 9: Normalized drain-source on resistance



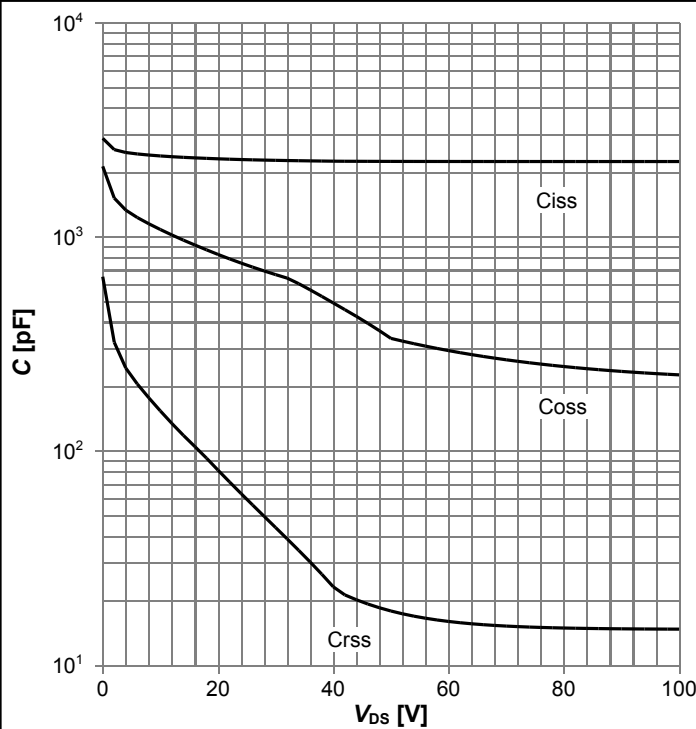
$R_{DS(on)}=f(T_j)$, $I_D=20$ A, $V_{GS}=10$ V

Diagram 10: Typ. gate threshold voltage



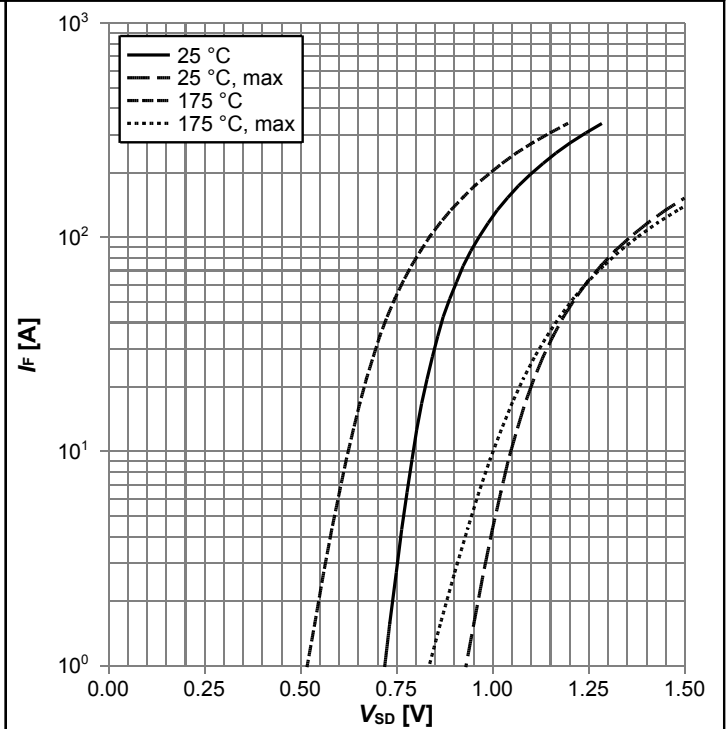
$V_{GS(th)}=f(T_j)$, $V_{GS}=V_{DS}$; parameter: I_D

Diagram 11: Typ. capacitances



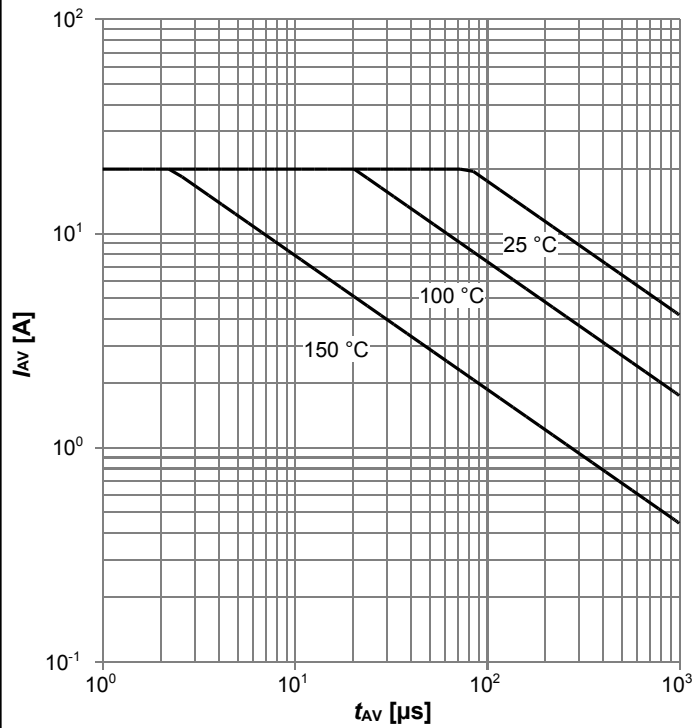
$C=f(V_{DS})$; $V_{GS}=0$ V; $f=1$ MHz

Diagram 12: Forward characteristics of reverse diode



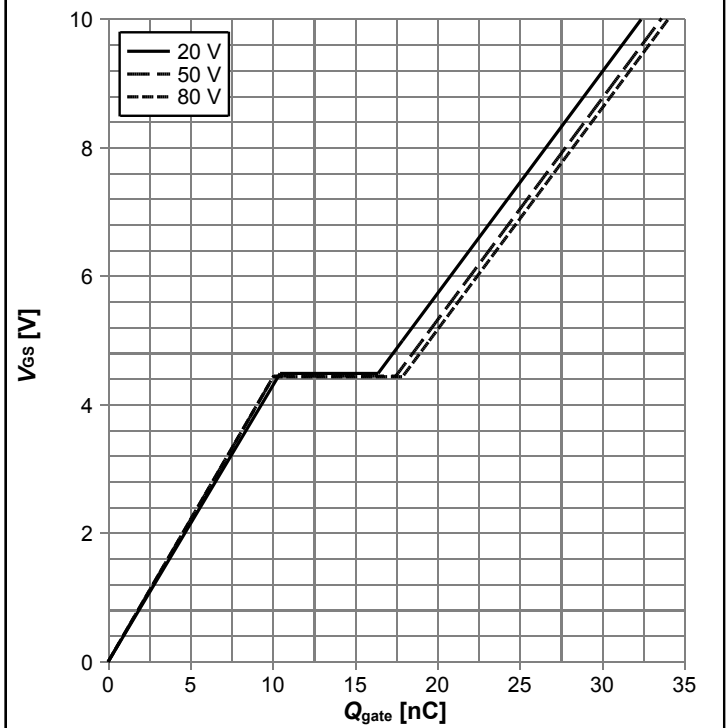
$I_F=f(V_{SD})$; parameter: T_j

Diagram 13: Avalanche characteristics



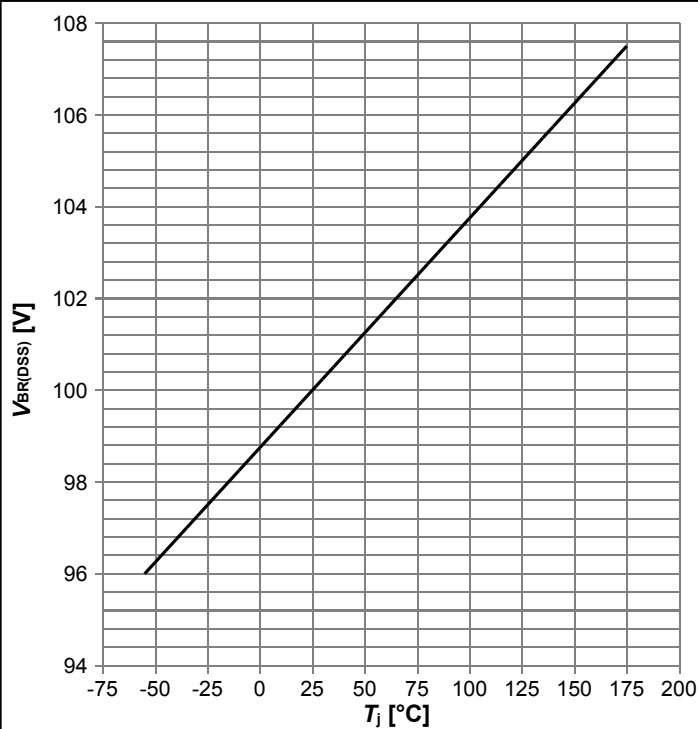
$I_{AS}=f(t_{AV})$; $R_{GS}=25 \Omega$; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



$V_{GS}=f(Q_{gate})$, $I_D=20$ A pulsed, $T_j=25$ °C; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage



$V_{BR(DSS)}=f(T_j)$; $I_D=1$ mA

Diagram Gate charge waveforms



5 Package Outlines

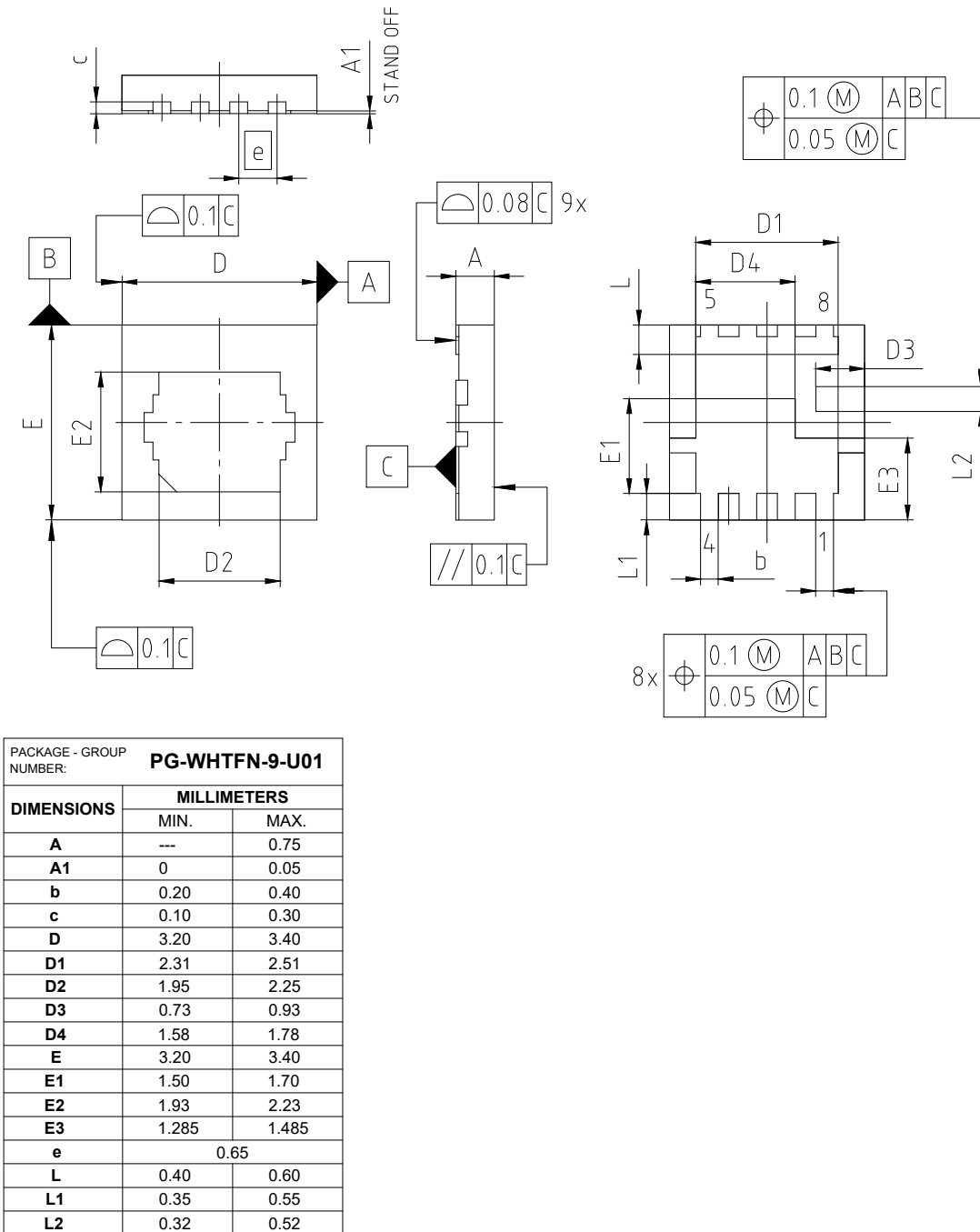


Figure 1 Outline PG-WHTFN-9, dimensions in mm

OptiMOS™ 5 Power-Transistor, 100 V

IQE065N10NM5CGSC

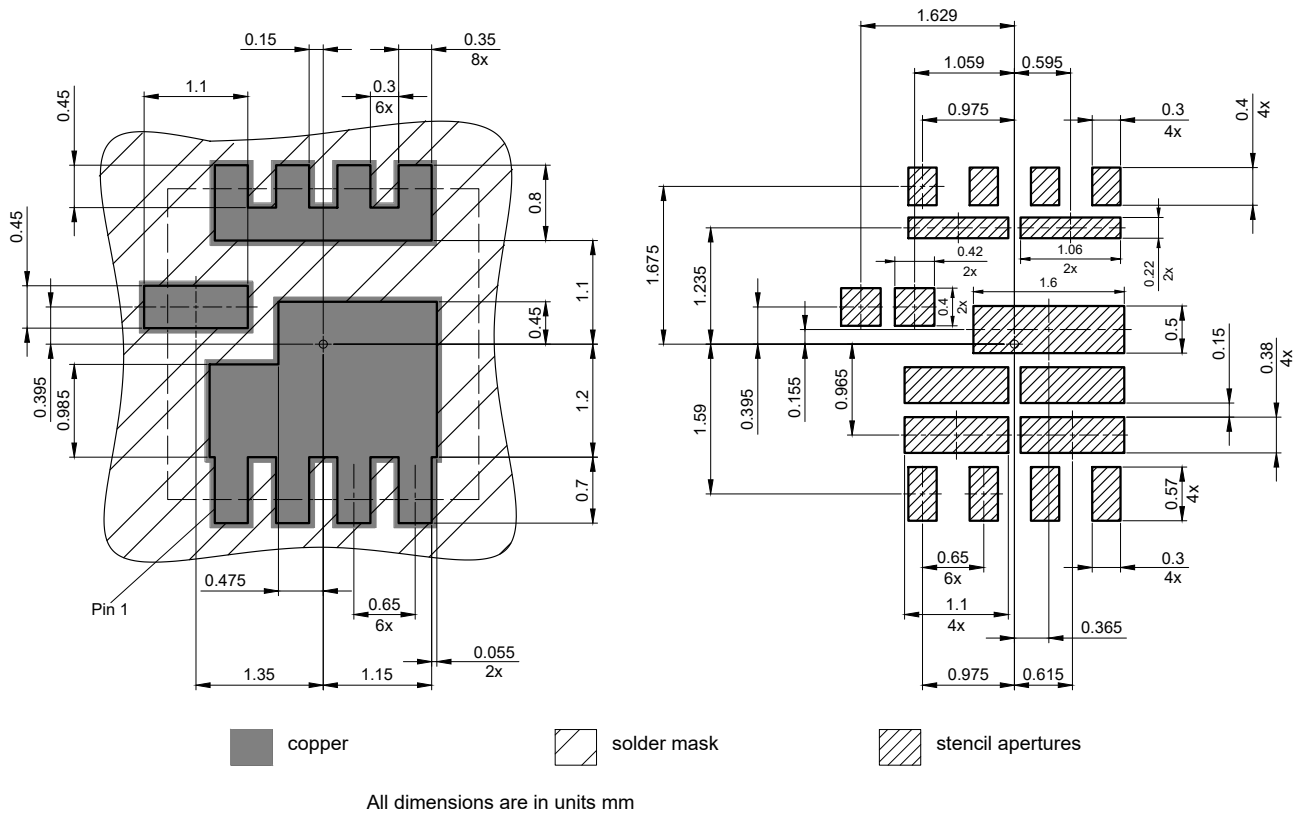


Figure 2 Outline Footprint (PG-WHTFN-9-1), dimensions in mm

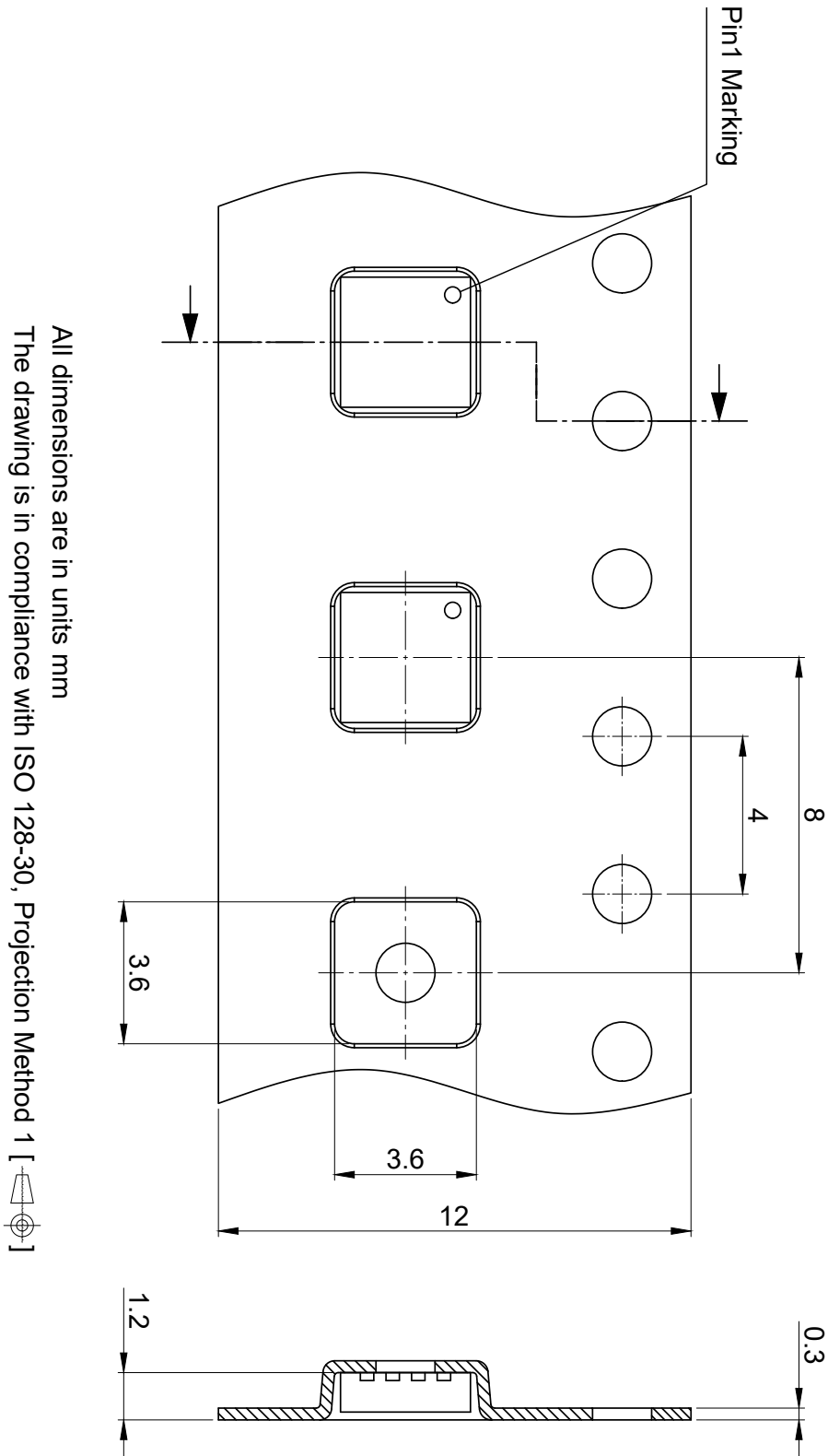


Figure 3 Outline Tape (PG-WHTFN-9-1), dimensions in mm

Revision History

IQE065N10NM5CGSC

Revision: 2022-05-02, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2022-05-02	Release of final version

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