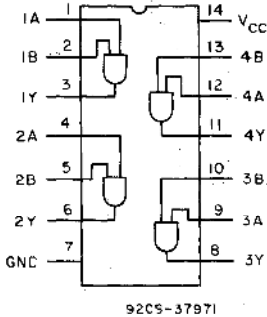


# CD54/74AC08 CD54/74ACT08



## Quad 2-Input AND Gate

**Type Features:**

- Buffered inputs
- Typical propagation delay (AC08):  
4.3 ns @  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $C_L = 50\text{ pF}$

92CS-37971  
**FUNCTIONAL DIAGRAM & TERMINAL ASSIGNMENT**

The GE/RCA-CD54/74AC08 and CD54/74ACT08 are quad 2-input AND gates that utilize GE/RCA's new ADVANCED CMOS LOGIC technology. The CD54AC08 and CD54ACT08 are supplied in 14-lead dual-in-line ceramic packages (F suffix). The CD74AC08 and CD74ACT08 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line small-outline plastic packages (M suffix).

**TRUTH TABLE**

Inputs		Output
nA	nB	nY
L	L	L
H	L	L
L	H	L
H	H	H

**Family Features:**

- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latch-up-resistant CMOS process and circuit design
- Speed of bipolar FAST\*/AS/S with significantly reduced power
- Balanced propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply
- $\pm 24\text{-mA}$  output drive current
  - Fanout to 15 FAST\* ICs
  - Drives 50-ohm transmission lines

\*FAST is a Trademark of Fairchild Semiconductor Corp.

**MAXIMUM RATINGS, Absolute-Maximum Values:**

DC SUPPLY-VOLTAGE ( $V_{CC}$ )	-0.5 to 6 V
DC INPUT DIODE CURRENT, $I_{IK}$ (for $V_i < -0.5\text{ V}$ or $V_i > V_{CC} + 0.5\text{ V}$ )	$\pm 20\text{ mA}$
DC OUTPUT DIODE CURRENT, $I_{OK}$ (for $V_o < -0.5\text{ V}$ or $V_o > V_{CC} + 0.5\text{ V}$ )	$\pm 50\text{ mA}$
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, $I_o$ (for $V_o > -0.5\text{ V}$ or $V_o < V_{CC} + 0.5\text{ V}$ )	$\pm 50\text{ mA}$
DC $V_{CC}$ or GROUND CURRENT ( $I_{CC}$ or $I_{GND}$ )	$\pm 100\text{ mA}$ *
<b>POWER DISSIPATION PER PACKAGE (<math>P_D</math>):</b>	
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE F)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE F)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+100^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+70^\circ\text{C}$ (PACKAGE TYPE M)	400 mW
For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M)	Derate Linearly at 6 mW/ $^\circ\text{C}$ to 70 mW
<b>OPERATING-TEMPERATURE RANGE (<math>T_A</math>):</b>	
PACKAGE TYPE F	-55 to $+125^\circ\text{C}$
PACKAGE TYPE E, M	-40 to $+125^\circ\text{C}$
STORAGE TEMPERATURE ( $T_{stg}$ )	-65 to $+150^\circ\text{C}$
<b>LEAD TEMPERATURE (DURING SOLDERING):</b>	
At distance $1/16 \pm 1/32$ in. ( $1.59 \pm 0.79$ mm) from case for 10 s maximum	$+265^\circ\text{C}$
Unit inserted into PC board min. thickness $1/16$ in. ( $1.59$ mm) with solder contacting lead tips only	$+300^\circ\text{C}$

\*(For up to 4 outputs per device; add  $\pm 25\text{ mA}$  for each additional output.)

Technical Data  
**CD54/74AC08**  
**CD54/74ACT08**

**RECOMMENDED OPERATING CONDITIONS:**

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, $V_{CC}^*$ : (For $T_A$ = Full Package-Temperature Range) AC Types ACT Types	1.5	5.5	V
	4.5	5.5	V
DC Input or Output Voltage, $V_i, V_o$	0	$V_{CC}$	V
Operating Temperature, $T_A$ : CD74 Types CD54 Types	-40	+125	°C
	-55	+125	°C
Input Rise and Fall Slew Rate, $di/dv$ at 1.5 V to 3 V (AC Types) at 3.6 V to 5.5 V (AC Types) at 4.5 V to 5.5 V (ACT Types)	0	50	ns/V
	0	20	ns/V
	0	10	ns/V

\*Unless otherwise specified, all voltages are referenced to ground.

**STATIC ELECTRICAL CHARACTERISTICS: AC Series**

CHARACTERISTICS	TEST CONDITIONS		$V_{CC}$ (V)	AMBIENT TEMPERATURE ( $T_A$ ) - °C						UNITS
				+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)		
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage $V_{IH}$			1.5	1.2	—	1.2	—	1.2	—	V
			3	2.1	—	2.1	—	2.1	—	
			5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage $V_{IL}$			1.5	—	0.3	—	0.3	—	0.3	V
			3	—	0.9	—	0.9	—	0.9	
			5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage $V_{OH}$	$V_{IH}$ or $V_{IL}$	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
		-0.05	3	2.9	—	2.9	—	2.9	—	
		-0.05	4.5	4.4	—	4.4	—	4.4	—	
		-4	3	2.58	—	2.48	—	2.4	—	
		-24	4.5	3.94	—	3.8	—	3.7	—	
		# *	-75	5.5	—	—	3.85	—	—	
Low-Level Output Voltage $V_{OL}$	$V_{IH}$ or $V_{IL}$	0.05	1.5	—	0.1	—	0.1	—	0.1	V
		0.05	3	—	0.1	—	0.1	—	0.1	
		0.05	4.5	—	0.1	—	0.1	—	0.1	
		12	3	—	0.36	—	0.44	—	0.5	
		24	4.5	—	0.36	—	0.44	—	0.5	
		# *	75	5.5	—	—	—	1.65	—	
Input Leakage Current $I_i$	$V_{CC}$ or GND		5.5	—	±0.1	—	±1	—	±1	μA
			5.5	—	—	—	—	—	—	—
Quiescent Supply Current, SSI $I_{CC}$	$V_{CC}$ or GND	0	5.5	—	4	—	40	—	80	μA
			5.5	—	—	—	—	—	—	—

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

# CD54/74AC08

# CD54/74ACT08

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS	$V_{CC}$ (V)	AMBIENT TEMPERATURE ( $T_A$ ) - °C						UNITS		
			+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)				
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.			
High-Level Input Voltage	$V_{IH}$		4.5 to 5.5	2	—	2	—	2	—	V	
Low-Level Input Voltage	$V_{IL}$		4.5 to 5.5	—	0.8	—	0.8	—	0.8	V	
High-Level Output Voltage	$V_{OH}$	$V_{IH}$ or $V_{IL}$ # *	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
			-24	4.5	3.94	—	3.8	—	3.7	—	
			-75	5.5	—	—	3.85	—	—	—	
			-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage	$V_{OL}$	$V_{IH}$ or $V_{IL}$ # *	0.05	4.5	—	0.1	—	0.1	—	0.1	V
			24	4.5	—	0.36	—	0.44	—	0.5	
			75	5.5	—	—	—	1.65	—	—	
			50	5.5	—	—	—	—	—	1.65	
Input Leakage Current	$I_i$	$V_{CC}$ or GND	5.5	—	+0.1	—	+1	—	+1	$\mu$ A	
Quiescent Supply Current, SSI	$I_{CC}$	$V_{CC}$ or GND	0	5.5	—	4	—	40	—	80	$\mu$ A
Additional Quiescent Supply Current per Input Pin, TTL Inputs High, 1 Unit Load	$\Delta I_{CC}$	$V_{CC}$ -2.1	4.5 to 5.5		2.4	—	2.8	—	3	mA	

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

**ACT INPUT LOADING TABLE**

INPUT	UNIT LOADS*
All	0.3

\*Unit load is  $\Delta I_{CC}$  limit specified in Static Characteristic Chart, e.g., 2.4 mA max. @ 25°C.

# CD54/74AC08

## CD54/74ACT08

**SWITCHING CHARACTERISTICS: AC Series;  $t_r, t_f = 3 \text{ ns}, C_L = 50 \text{ pF}$**

CHARACTERISTICS	SYMBOL	$V_{CC}$ (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Input to Output	$t_{PLH}$	1.5	—	102	—	109	ns
	$t_{PHL}$	3.3*	2.5	11.3	2.2	12.2	
		5†	1.7	8.1	1.5	8.7	
Power Dissipation Capacitance	$C_{PD}§$	—	100 Typ.		100 Typ.		pF
Input Capacitance	$C_I$	—	—	10	—	10	pF

**SWITCHING CHARACTERISTICS: ACT Series;  $t_r, t_f = 3 \text{ ns}, C_L = 50 \text{ pF}$**

CHARACTERISTICS	SYMBOL	$V_{CC}$ (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Input to Output	$t_{PLH}$	5†	2.6	12.9	2.4	13.8	ns
	$t_{PHL}$						
Power Dissipation Capacitance	$C_{PD}§$	—	115 Typ.		115 Typ.		pF
Input Capacitance	$C_I$	—	—	10	—	10	pF

\*3.3 V: min. is @ 3.6 V  
max. is @ 3 V

†5 V: min. is @ 5.5 V  
max. is @ 4.5 V

5 V: min. is @ 5.25 V for 0 to +70°C  
max. is @ 4.75 V for 0 to +70°C

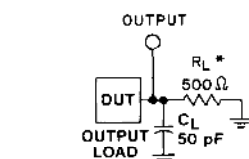
§ $C_{PD}$  is used to determine the dynamic power consumption, per gate.

For AC series:  $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$

For ACT series:  $P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$  where  $f_i$  = input frequency

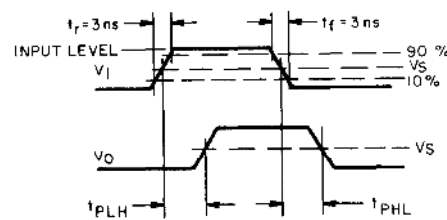
$C_L$  = output load capacitance

$V_{CC}$  = supply voltage.



\*FOR AC SERIES ONLY: WHEN  
 $V_{CC} = 1.5 \text{ V}, R_L = 1 \text{ k}\Omega$

92CS-42389



92CS-42443

	CD54/74AC	CD54/74ACT
Input Level	$V_{CC}$	3 V
Input Switching Voltage, $V_S$	$0.5 V_{CC}$	1.5 V
Output Switching Voltage, $V_S$	$0.5 V_{CC}$	$0.5 V_{CC}$

Fig. 1 - Propagation delay times and test circuit.