TLV752-EVM Evaluation Module

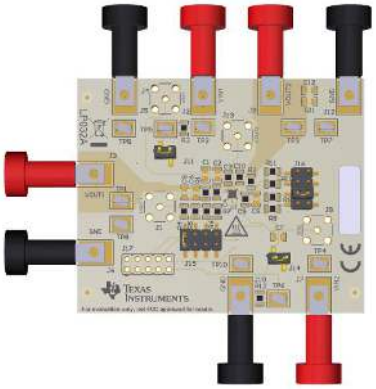

Figure 1. TLV752-EVM Evaluation Module

This user's guide describes the operational use of the TLV752-EVM evaluation module (EVM) as a reference design for engineering demonstration and evaluation of the TLV75201DSQ, dual, high-accuracy, adjustable linear regulator (LDO). Included in this user's guide are setup and operating instructions, thermal and layout guidelines, a printed circuit board (PCB) layout, a schematic diagram, and a bill of materials (BOM).

Throughout this document, the terms *demonstration kit*, *evaluation board*, and *evaluation module* are synonymous with the TLV752-EVM.

Table 1 lists the related documentation available through the Texas Instruments web site at www.ti.com.

Table 1. Related Documentation

DEVICE	LITERATURE NUMBER
TLV752	SBVS383

Contents

List of Figures

List of Tables

Trademarks

1 Introduction

Texas Instruments' TLV752-EVM helps design engineers evaluate the operation and performance of the TLV752 family of linear regulators for possible use in their own circuit application. This particular EVM configuration contains a single high-accuracy, small size, dual-input linear regulator for a wide range of applications. The regulator is capable of delivering up to 1 A to the load for each input channel with low V_{IN} to V_{OUT} dropout voltage. For stability, use a minimum derated capacitance of 0.47-µF (or larger) output capacitor for each output channel.

1.1 Before You Begin

The following warnings and cautions are noted for the safety of anyone using or working close to the TLV752-EVM. Observe all safety precautions.

Warning Warning Hot surface. Contact may cause burns. Do not touch.

CAUTION

The circuit module may be damaged by over temperature. To avoid damage, monitor the temperature during evaluation and provide cooling, as needed, for your system environment.

CAUTION

Some power supplies can be damaged by application of external voltages. If using more than one power supply, check your equipment requirements and use blocking diodes or other isolation techniques, as needed, to prevent damage to your equipment.

CAUTION

The circuit module is not a finished product or electrical appliance. The module does not contain current or voltage thresholds for circuit protection. It must be used by qualified personnel with additional equipment for evaluation only.

2 EVM Setup

This section describes how to properly connect and set up the TLV752-EVM, including the jumpers and connectors on the EVM board.

2.1 Inputs/Outputs Connectors and Jumper Descriptions

2.1.1 J1 – OUT1_S

Regulated output voltage one sense

2.1.2 J2 – IN1

Input power supply one voltage connector. Twist together the positive input lead and ground return lead from the input power supply one, and keep them as short as possible to minimize input inductance.

2.1.3 J3 – OUT1

Regulated output voltage one connector

2.1.4 J4 – IN1_S

Input voltage one sense

2.1.5 J5 –GND

Input supply one ground return connector

2.1.6 J6 – GND

Regulated output voltage one ground return connector

2.1.7 J7 – IN2

Input power supply two voltage connector. Twist together the positive input lead and ground return lead from the input power supply two, and keep them as short as possible to minimize input inductance.

2.1.8 J8 – OUT2

Regulated output voltage two connector

2.1.9 J9 – IN2_S

Input voltage two sense

2.1.10 J10 – GND

Input supply two ground return connector

2.1.11 J11 – EN1

Output voltage one enable. To enable output voltage one, connect a jumper to short VIN1 to EN1.

2.1.12 J12 – GND

Regulated output voltage two ground return connector

2.1.13 J13 – OUT2_S

Regulated output voltage two sense

2.1.14 J14 – EN2

Output voltage two enable. To enable output voltage two, connect a jumper to short VIN2 to EN2.

2.1.15 J15 – OUT1 Set

For convenience, the EVM is prepopulated with four resistor divider options. Place a shunt on J15 next to the schematic label of your desired output voltage one.

2.1.16 J16 – OUT2 Set

For convenience, the EVM is prepopulated with four resistor divider options. Place a shunt on J15 next to the schematic label of your desired output voltage two.

2.1.17 J17 – Test Hookup

Intended for test purposes only

2.1.18 TP1 – OUT1_S

Regulated output voltage one test point

2.1.19 TP2 – IN1_S

Input voltage one test point

2.1.20 TP3 – OUT2_S

Regulated output voltage two test point

2.1.21 TP4 – IN2_S

Input voltage two test point

2.1.22 TP5 – EN1

Output voltage one enable test point

2.1.23 TP6 – EN2

Output voltage two enable test point

2.1.24 TP7 – GND

Ground test point

2.1.25 TP8 – GND

Ground test point

2.1.26 TP9 – GND

Ground test point

2.1.27 TP10 – GND

Ground test point

2.2 Soldering Guidelines

To avoid damaging the integrated circuit (IC), use a hot-air system for any solder rework to modify the EVM for the purpose of repair or other application reasons.

2.3 Equipment Connection

Connect the equipment as shown in the following steps:

1. Set the input power supplies one and two up to 6 V (max), and turn them off.
2. Connect the GND leads of both supplies together.
3. Connect the positive voltage lead from the input power supply one to IN1 at the J2 connector of the EVM.
4. Connect the ground lead from the input power supplies one and two to GND at the J5 connector of the EVM.
5. Connect the positive voltage lead from the input power supply two to IN2 at the J7 connector of the EVM.
6. Connect the ground lead from the input power supplies one and two to GND at the J10 connector of the EVM.
7. Connect a 0-A to 1-A load between OUT1 and GND.
8. Connect a 0-A to 1-A load between OUT2 and GND.
9. Disable output voltage one by floating J11.
10. Disable output voltage two by floating J14.

3 Operation

Operate the equipment using the following steps:

1. Turn on the power supplies.
2. Enable the outputs by jumping J11 (the EN1 pin) to VIN1 and J14 (the EN2 pin) to VIN2.
3. Vary the respective loads and input voltages, as necessary, for test purposes.

4 PCB Layout

Figure 2 to Figure 6 illustrate the PCB layout for this EVM.

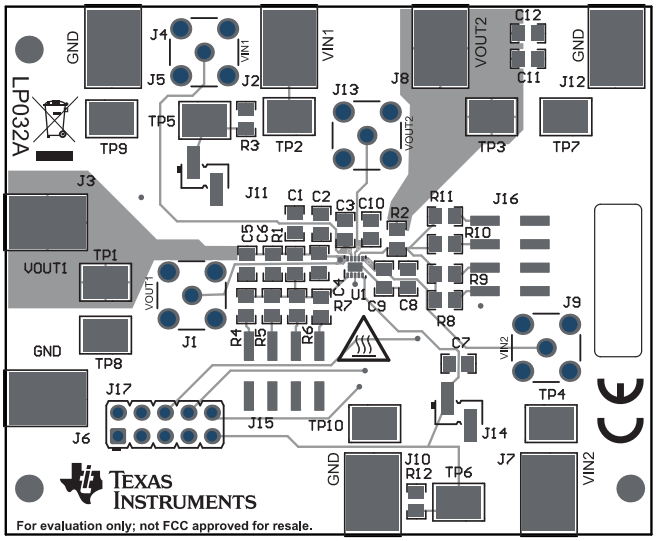

Figure 2. Assembly Layer

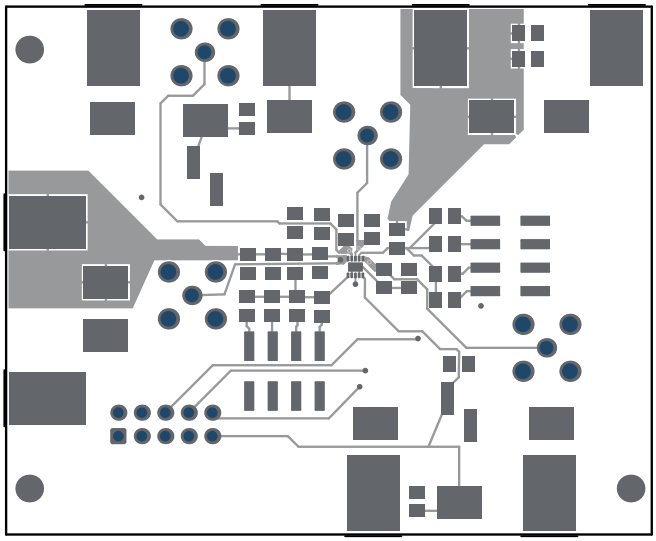

Figure 3. Top Layer Routing

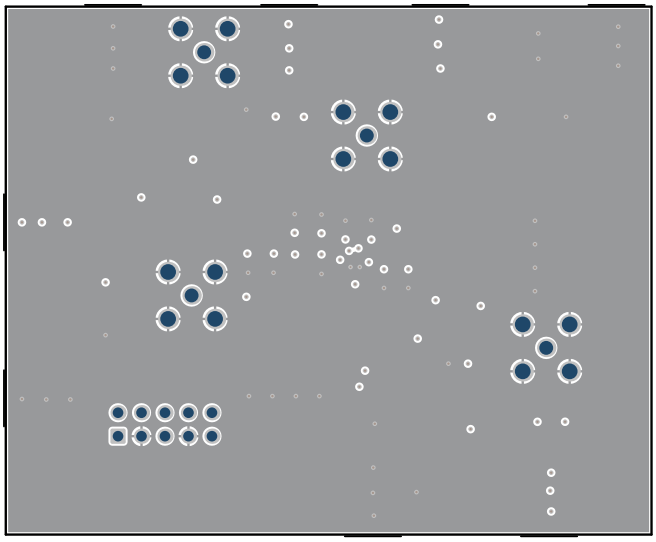

Figure 4. First Middle Layer

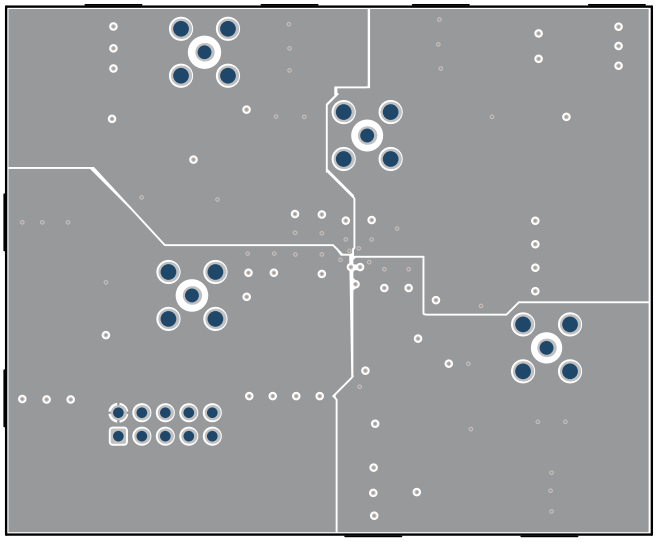

Figure 5. Second Middle Layer

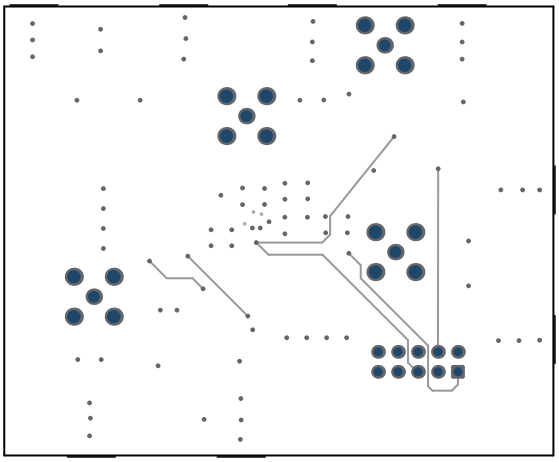

Figure 6. Bottom Layer Routing

5 Schematic

Figure 7 shows the schematic for this EVM.

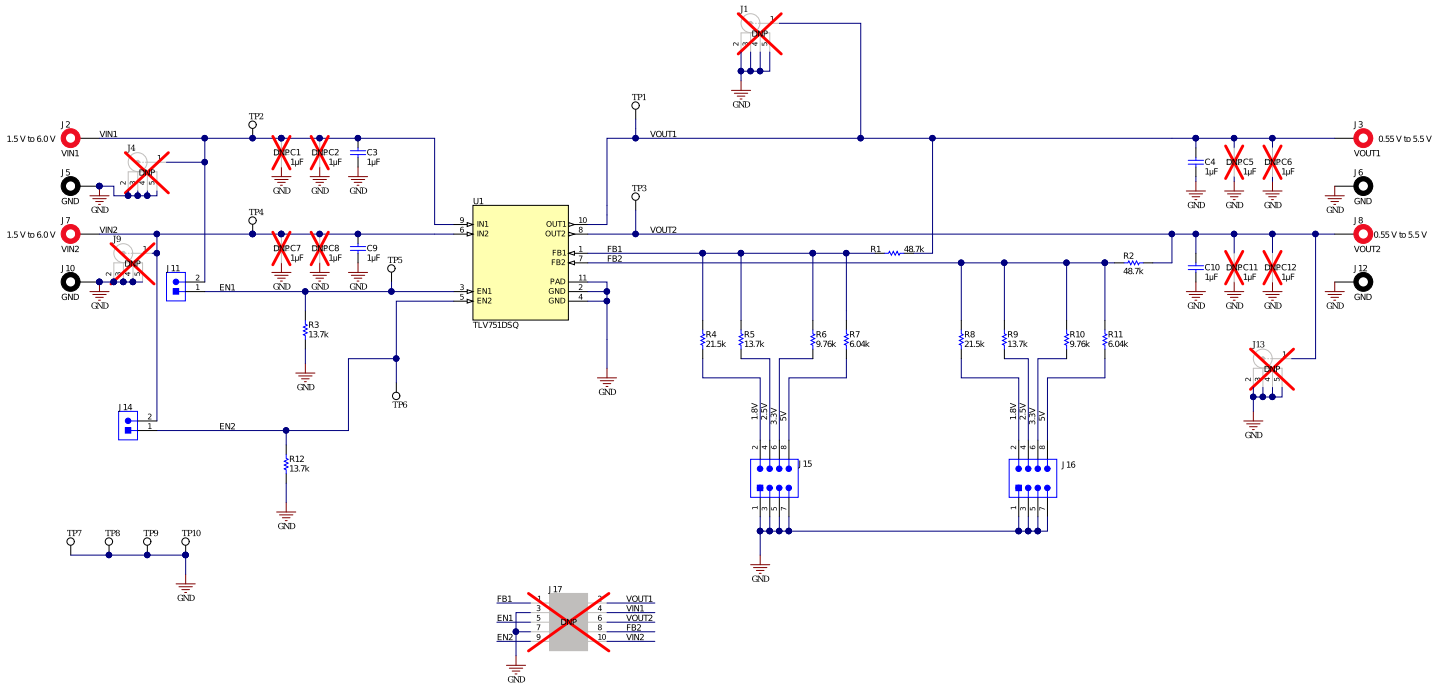

Figure 7. TLV752-EVM Schematic

6 Bill of Materials

Table 2 shows the BOM for this EVM.

Table 2. TLV752-EVM BOM(1)(2)(3)(4)

DESIGNATOR	QTY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PART NUMBER	MANUFACTURER	ALTERNATE PART NUMBER	ALTERNATE PART NUMBER
!PCB1	1		Printed Circuit Board		LP032	Any		
C3, C4, C9, C10	4	1 µF	CAP, CERM, 1 µF, 50 V, ±10%, X7R, 0805	0805	08055C105KAT2A	AVX		
J2, J3, J7, J8	4		Standard Banana Jack, Insulated, Red	6091	6091	Keystone		
J5, J6, J10, J12	4		Standard Banana Jack, Insulated, Black	6092	6092	Keystone		
J11, J14	2		Header, 2.54 mm, 2x1, Tin, SMT	Header, 2.54 mm, 2x1, SMT	TSM-102-03-T-SV	Samtec		
J15, J16	2		Header, 2.54 mm, 4x2, Gold, SMT	Header, 2.54 mm, 4x2, SMT	61000821121	Wurth Elektronik		
LBL1	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10 000 per roll	PCB Label 0.650 x 0.200 inch	THT-14-423-10	Brady		
R1, R2	2	48.7 k	RES, 48.7 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	0805	CRCW080548K7FKEA	Vishay-Dale		
R3, R5, R9, R12	4	13.7 k	RES, 13.7 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	0805	CRCW080513K7FKEA	Vishay-Dale		
R4, R8	2	21.5 k	RES, 21.5 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	0805	CRCW080521K5FKEA	Vishay-Dale		
R6, R10	2	9.76 k	RES, 9.76 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	0805	CRCW08059K76FKEA	Vishay-Dale		
R7, R11	2	6.04 k	RES, 6.04 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	0805	CRCW08056K04FKEA	Vishay-Dale		
SH-J1, SH-J2, SH-J3, SH-J4	4	1x2	Shunt, 100 mil, Gold plated, Black	Shunt	SNT-100-BK-G	Samtec	969102-0000-DA	3M
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10	10		Test Point, Compact, SMT	Testpoint_Keystone_Compact	5016	Keystone		
U1	1		Dual, 1-A, high-accuracy, adjustable-LDO in a small size package, DSQ0010A (WSON-10)	DSQ0010A	TLV752DSQ	Texas Instruments		Texas Instruments
C1, C2, C5, C6, C7, C8, C11, C12	0	1 µF	CAP, CERM, 1 µF, 50 V, ±10%, X7R, 0805	0805	08055C105KAT2A	AVX		
FID1, FID2, FID3	0		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A		
J1, J4, J9, J13	0		SMA Straight Jack, Gold, 50 Ohm, TH	SMA Straight Jack, TH	901-144-8RFX	Amphenol RF		
J17	0		Header, 2.54 mm, 5x2, Gold, TH	Header, 2.54 mm, 5x2, TH	61301021121	Wurth Elektronik		

(1) These assemblies are ESD sensitive, observe ESD precautions.
(2) These assemblies must be clean and free from flux and all contaminants. Use of no-clean flux is not acceptable.
(3) These assemblies must comply with workmanship standards IPC-A-610 Class 2.
(4) Unless otherwise noted in the *Alternate Part Number* or *Alternate Manufacturer* columns, all parts can be substituted with equivalents.

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