2.5V or 3.3V, 200-MHz, 1:10 Clock Distribution Buffer

Features

- **2.5V or 3.3V operation**
- **200-MHz clock support**
- **Two LVCMOS-/LVTTL-compatible inputs**
- **Ten clock outputs: drive up to 20 clock lines**
- **1× or 1/2× configurable outputs**
- **Output three-state control**
- **250-ps max. output-to-output skew**
- **Pin-compatible with MPC946, MPC9446**
- **Available in commercial and industrial temperature range**
- **32-pin TQFP package**

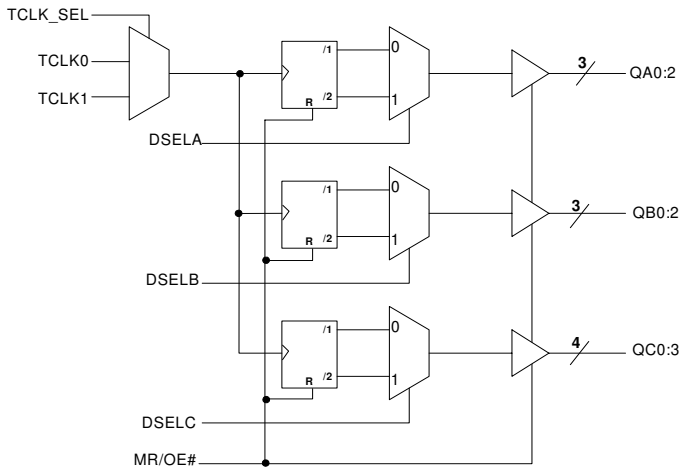
Description

The CY29946 is a low-voltage 200-MHz clock distribution buffer with the capability to select one of two LVCMOS/LVTTL compatible input clocks. These clock sources can be used to provide for test clocks as well as the primary system clocks. All other control inputs are LVCMOS/LVTTL compatible. The 10 outputs are LVCMOS or LVTTL compatible and can drive 50Ω series or parallel terminated transmission lines. For series terminated transmission lines, each output can drive one or two traces giving the device an effective fanout of 1:20.

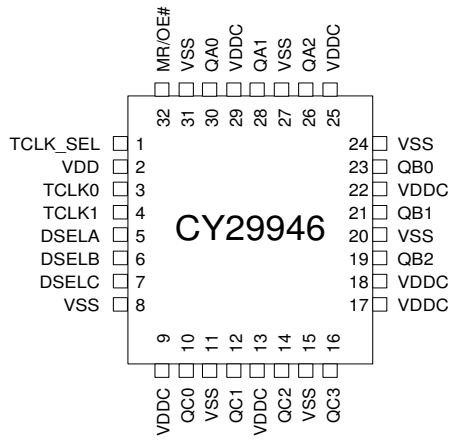
The CY29946 is capable of generating 1× and 1/2× signals from a 1× source. These signals are generated and retimed internally to ensure minimal skew between the 1× and 1/2× signals. SEL(A:C) inputs allow flexibility in selecting the ratio of 1× to1/2× outputs.

The CY29946 outputs can also be three-stated via MR/OE# input. When MR/OE# is set HIGH, it resets the internal flip-flops and three-states the outputs.

Block Diagram



Pin Configuration



Pin Description[1]

Pin	Name	PWR	I/O	Description
3, 4	TCLK(0,1)		I, PU	External Reference/Test Clock Input
26, 28, 30	QA(2:0)	VDDC	O	Clock Outputs
19, 21, 23	QB(2:0)	VDDC	O	Clock Outputs
10, 12, 14, 16	QC(0:3)	VDDC	O	Clock Outputs
5, 6, 7	DSEL(A:C)		I, PD	**Divider Select Inputs**. When HIGH, selects ÷2 input divider. When LOW, selects ÷1 input divider.
1	TCLK_SEL		I, PD	**TCLK Select Input**. When LOW, TCLK0 clock is selected and when HIGH TCLK1 is selected.
32	MR/OE#		I, PD	**Output Enable Input**. When asserted LOW, the outputs are enabled and when asserted HIGH, internal flip-flops are reset and the outputs are three-stated. If more than 1 Bank is being used in /2 Mode, a reset must be performed (MR/OE# Asserted High) after power-up to ensure all internal flip-flops are set to the same state.
9, 13, 17, 18, 22, 25, 29	VDDC			2.5V or 3.3V Power Supply for Output Clock Buffers
2	VDD			2.5V or 3.3V Power Supply
8, 11, 15, 20, 24, 27, 31	VSS			Common Ground

Note:
1. PD = Internal pull-down. PU = Internal pull-up.

Absolute Maximum Conditions[2]

Maximum Input Voltage Relative to V_{SS}: ..... V_{SS} – 0.3V
Maximum Input Voltage Relative to V_{DD}: ..... V_{DD} + 0.3V
Storage Temperature: .....–65°C to + 150°C
Operating Temperature: .....–40°C to +85°C
Maximum ESD protection .....2 kV
Maximum Power Supply: 5.5V
Maximum Input Current: .....± 20 mA

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, V_{in} and V_{out} should be constrained to the range:

$V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (either V_{SS} or V_{DD}).

DC Electrical Specifications: $V_{DD} = V_{DDC}$ = 3.3V ±10% or 2.5V ±5%, over the specified temperature range

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage		V_{SS}		0.8	V
V_{IH}	Input High Voltage		2.0		V_{DD}	V
I_{IL}	Input Low Current[3]				–100	µA
I_{IH}	Input High Current[3]				100	µA
V_{OL}	Output Low Voltage[4]	I_{OL} = 20 mA			0.4	V
V_{OH}	Output High Voltage[4]	I_{OH} = –20 mA, V_{DD} = 3.3V	2.5			V
		I_{OH} = –20 mA, V_{DD} = 2.5V	1.8			
I_{DDQ}	Quiescent Supply Current			5	7	mA
I_{DD}	Dynamic Supply Current	V_{DD} = 3.3V, Outputs @ 100 MHz, CL = 30 pF		130		mA
		V_{DD} = 3.3V, Outputs @ 160 MHz, CL = 30 pF		225		
		V_{DD} = 2.5V, Outputs @ 100 MHz, CL = 30 pF		95		
		V_{DD} = 2.5V, Outputs @ 160 MHz, CL = 30 pF		160		
Z_{Out}	Output Impedance	V_{DD} = 3.3V	12	15	18	W
		V_{DD} = 2.5V	14	18	22	
C_{in}	Input Capacitance			4		pF

AC Electrical Specifications $V_{DD} = V_{DDC}$ = 3.3V ±10% or 2.5V ±5%, over the specified temperature range[5]

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
Fmax	Input Frequency[6]	V_{DD} = 3.3V			200	MHz
		V_{DD} = 2.5V			170	
Tpd	TTL_CLK To Q Delay[6]		5.0		11.5	ns
FoutDC	Output Duty Cycle[6, 7]	Measured at $V_{DD}/2$	45		55	%
tpZL, tpZH	Output enable time (all outputs)		2		10	ns
tpLZ, tpHZ	Output disable time (all outputs)		2		10	ns
Tskew	Output-to-Output Skew[6, 8]			150	250	ps
Tskew(pp)	Part-to-Part Skew[9]			2.0	4.5	ns
Tr/Tf	Output Clocks Rise/Fall Time[8]	0.8V to 2.0V, V_{DD} = 3.3V	0.10		1.0	ns
		0.6V to 1.8V, V_{DD} = 2.5V	0.10		1.3	

Notes:
2. **Multiple Supplies:** The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.
3. Inputs have pull-up/pull-down resistors that effect input current.
4. Driving series or parallel terminated 50Ω (or 50Ω to $V_{DD}/2$) transmission lines.
5. Parameters are guaranteed by design and characterization. Not 100% tested in production. All parameters specified with loaded outputs.
6. Outputs driving 50Ω transmission lines.
7. 50% input duty cycle.
8. See *Figure 1*.
9. Part-to-Part skew at a given temperature and voltage.

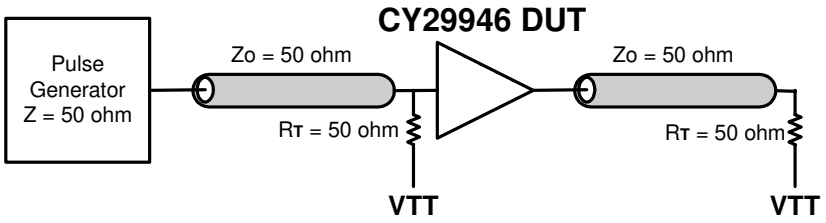


Figure 1. LVCMOS_CLK CY29946 Test Reference for V_{CC} = 3.3V and V_{CC} = 2.5V

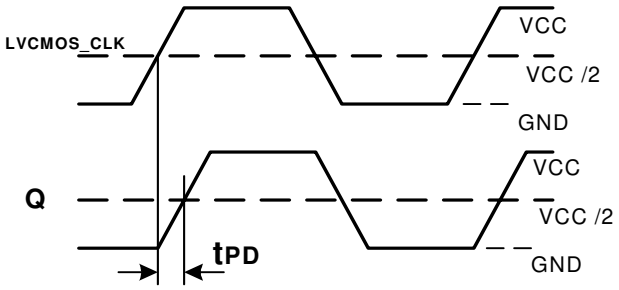


Figure 2. LVCMOS Propagation Delay (TPD) Test Reference

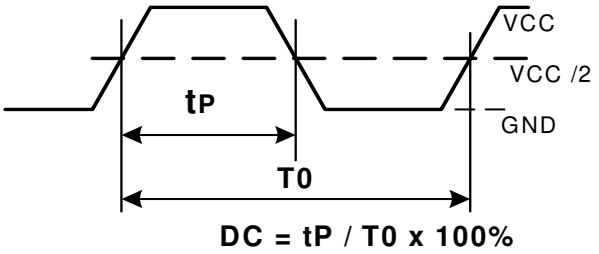


Figure 3. Output Duty Cycle (FoutDC)

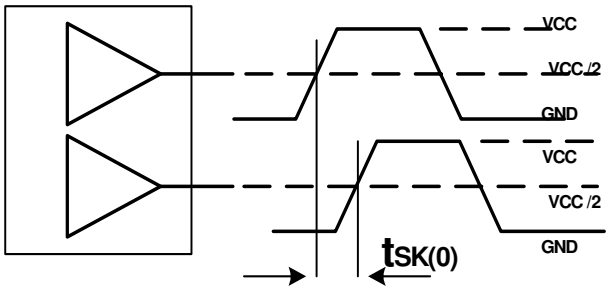


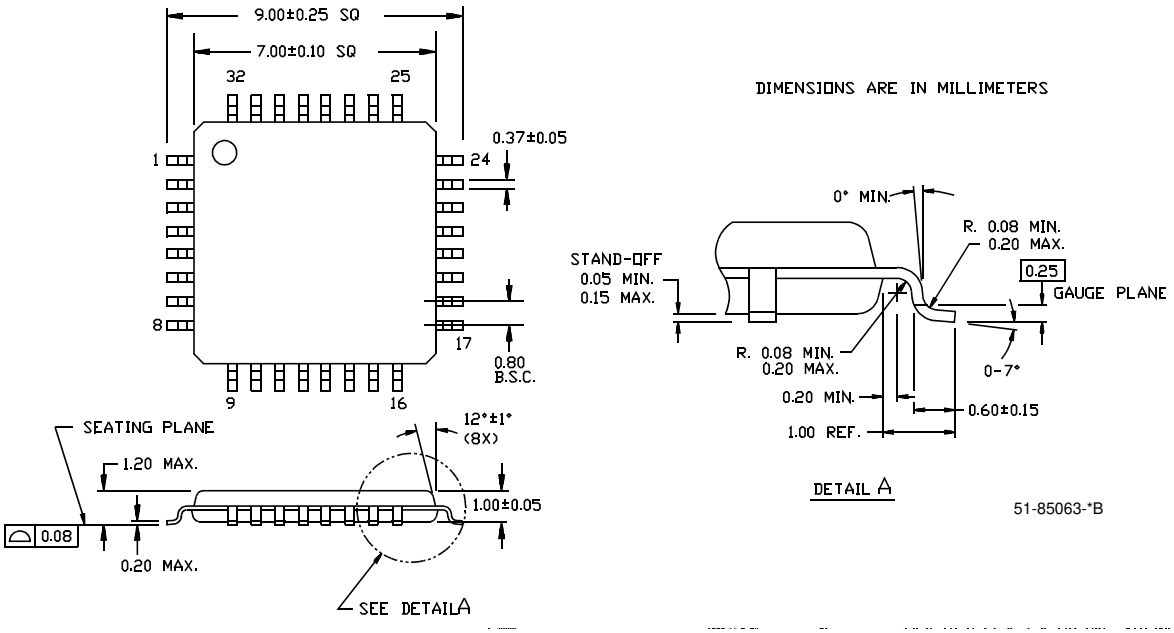
Figure 4. Output-to-Output Skew tsk(0)

Ordering Information

Part Number	Package Type	Production Flow
CY29946AXI	32-pin TQFP	Industrial, –40°C to +85°C
CY29946AIXT	32-pin TQFP – Tape and Reel	Industrial, –40°C to +85°C
CY29946AXC	32-pin TQFP	Commercial, 0°C to +70°C
CY29946AXCT	32-pin TQFP – Tape and Reel	Commercial, 0°C to +70°C

Package Drawing and Dimensions

32-Lead Thin Plastic Quad Flatpack 7 x 7 x 1.0mm A32



Document History Page

Document Title: CY29946 2.5V or 3.3V, 200-MHz, 1:10 Clock Distribution Buffer Document Number: 38-07286				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	111097	02/07/02	BRK	New data sheet
*A	116780	08/15/02	HWT	Added the commercial temperature range in the Ordering Information
*B	122878	12/22/02	RBI	Added power-up requirements to Maximum Ratings
*C	130007	10/15/03	RGL	Fixed the block diagram. Fixed the MK/OE# description in the pin description table.
*D	131375	11/21/03	RGL	Updated document history page (revision *C) to reflect changes that were not listed.
*E	221587	See ECN	RGL	Minor Change: Moved up the word Block Diagram in the first page.