SN75LVCP600 6-Gbps SATA PCB and Cable Equalizer

1 Features

- SATA Express Support
- Selectable Equalization and De-Emphasis
- Hot Plug Capable
- Receiver Detect and OOB Support
- Multirate Operation: 1.5 Gbps, 3 Gbps, and 6 Gbps
- Suitable to Receive 6-Gbps Data Over Up to 40 Inches (1 Meter) of FR4
- Compensates Up to 14-dB Loss on the Receive Side and 1.2-dB Loss on the Transmit Side at 3 GHz
- Integrated Output Squelch
- Auto Low Power Feature Lowers Power by > 90%
  - < 100 mW (Active Mode, Typical)
  - < 11 mW (Auto Low Power Mode, Typical)
- Single 3.3-V Supply
- High Protection Against ESD Transient
  - HBM: 6 kV
  - CDM: 1.5 kV
- Ultra-Small Footprint: 2 mm × 2 mm WSON Package

2 Applications

- Notebooks
- Desktops
- Docking Stations
- Servers
- Workstations

3 Description

The SN75LVCP600 is a versatile single channel, SATA Express signal conditioner supporting data rates up to 6 Gbps. The device supports SATA Gen 1, 2, and 3 specifications as well as PCIe 1.0, 2.0, and 3.0. The SN75LVCP600 operates from a single 3.3-V supply and has 100-Ω line termination with self-biasing feature, making the device suitable for AC coupling. The inputs incorporate an out-of-band (OOB) detector, which automatically squelches the output when the input differential voltage falls below threshold while maintaining a stable common-mode voltage. The device is also designed to handle spread spectrum clocking (SSC) transmission per SATA standard.

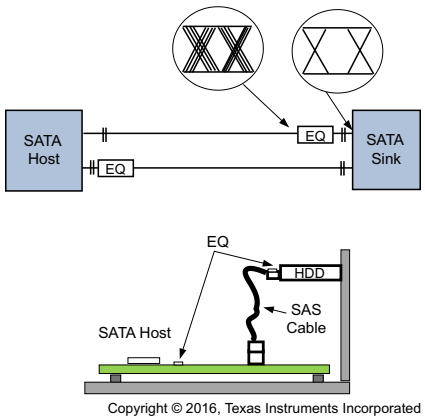
The SN75LVCP600 handles interconnect losses at its input with selectable equalization settings that can be programmed to match the loss in the channel. For data rates of 3 Gbps and lower the SN75LVCP600 equalizes signals for a span of up to 50 inches of FR4 board material. For data rates of 8 Gbps the device compensates up to 40 in of FR4 material. The equalization level is controlled by the setting of the signal control pin EQ.

Device Information(1)

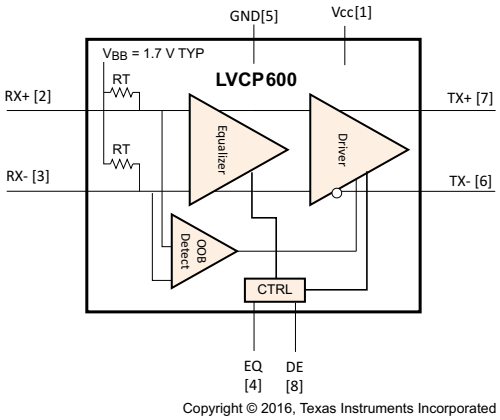
PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN75LVCP600	WSON (8)	2.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application



Data Flow Block Diagram



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4 Revision History

Changes from Original (December 2010) to Revision A **Page**

- Added Device Information table, ESD Ratings table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Changed RX+ from I, VML to I, CML in *Pin Functions* table ... 3
- Changed Noninverting and inverting VML differential inputs to Noninverting and inverting CML differential inputs in the *Pin Functions* table Description ... 3
- Changed RX- from I, VML to I, CML in *Pin Functions* table ... 3
- Changed TX+ from I, VML to O, VML in *Pin Functions* table ... 3
- Changed TX- from I, VML to O, VML in *Pin Functions* table ... 3
- Added *Parameter Measurement Information* section ... 9
- Changed RX to Rx0. in Figure 7 ... 9

5 Description (continued)

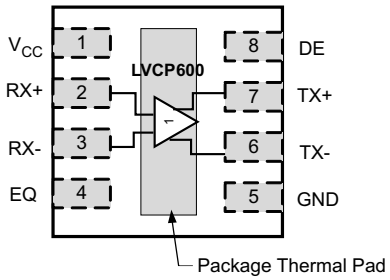
Two de-emphasis levels can be selected on the transmit side to provide 0 dB or 1.2 dB of additional high-frequency loss compensation at the output.

The device is hot-plug capable(1) preventing device damage under device *hot*-insertion such as async signal plug and removal, unpowered plug and removal, powered plug and removal, or surprise plug and removal.

(1) Requires use of AC coupling capacitors at differential inputs and outputs.

6 Pin Configuration and Functions

DRF Package
8-Pin WSON
Top View



Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
HIGH SPEED DIFFERENTIAL I/O			
RX+	2	I	Noninverting and inverting CML differential inputs. These pins are tied to an internal voltage bias by dual termination resistor circuit.
RX–	3	I	
TX+	7	O	Noninverting and inverting VML differential outputs. These pins are tied to an internal voltage bias by dual termination resistor circuit.
TX–	6	O	
CONTROL PINS			
EQ	4	I	Selects equalization settings per Table 1. Internally tied to GND.
DE	8	I	Selects de-emphasis settings per Table 1. Internally tied to GND.
POWER			
V_{CC}	1	P	Positive supply must be 3.3 V ±10%
GND	5	G	Supply ground

(1) G = Ground, I = Input, O = Output, P = Power

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_{CC}(2)		–0.5	4	V
Voltage	Differential I/O	–0.5	4	V
	Control I/O	–0.5	V_{CC} + 0.5	
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground pin.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±6000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

typical values for all parameters are at V_{CC} = 3.3 V and T_A = 25°C; all temperature limits are specified by design

		MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
	Coupling capacitor	75	100	200	nF
T_A	Operating free-air temperature	0		85	°C

7.4 Thermal Information

THERMAL METRIC(1)		SN75LVCP600 DRF (WSON) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	97.8	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	81.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	65.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	65.6	°C/W
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	19.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DEVICE PARAMETERS						
ICC_{Max-s}	Active mode supply current	EQ/DE = NC, K28.5 pattern at 6 Gbps, V_{ID} = 700 mV_{pp}		29	40	mA
I_{CCPS}	Auto power save mode I_{CC}	When auto low power conditions are met		3.3	5.9	mA
	Maximum data rate				6	Gbps

Electrical Characteristics (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OOB						
V_{OOB}	Input OOB threshold	F = 750 MHz	50	70	90	mV_{pp}
$D_{VdiffOOB}$	OOB differential delta				25	mV
D_{VCMOOB}	OOB common-mode delta				50	mV
CONTROL LOGIC						
V_{IH}	High-level input voltage	For all control pins	1.4			V
V_{IL}	Low-level input voltage				0.5	V
VIN_{HYS}	Input hysteresis			115		mV
I_{IH}	High-level input current	$V_{IH} = V_{CC}$ (DE/EQ)			20	µA
I_{IL}	Low-level input current	V_{IL} = 0 V (DE/EQ)			10	µA
RECEIVER AC/DC						
Z_{DIFFRX}	Differential input impedance		85	100	115	Ω
Z_{SERX}	Single-ended input impedance		40			Ω
VCM_{RX}	Common-mode voltage			1.7		V
RL_{DiffRX}	Differential mode return loss (RL)	f = 150 MHz to 300 MHz	18	26		dB
		f = 300 MHz to 600 MHz	14	22		
		f = 600 MHz to 1.2 GHz	10	17		
		f = 1.2 GHz to 2.4 GHz	8	12		
		f = 2.4 GHz to 3 GHz	3	11		
$RX_{DiffRLSlope}$	Differential mode RL slope	f = 300 MHz to 6 GHz (see Figure 7)		–13		dB/dec
RL_{CMRX}	Common-mode return loss	f = 150 MHz to 300 MHz	5	9.4		dB
		f = 300 MHz to 600 MHz	5	17		
		f = 600 MHz to 1.2 GHz	2	18		
		f = 1.2 GHz to 2.4 GHz	1	9.9		
		f = 2.4 GHz to 3 GHz	1	8.6		
V_{diffRX}	Differential input voltage PP	f = 1.5 GHz and 3 GHz	120		1600	mV_{pp}
IB_{RX}	Impedance balance	f = 150 MHz to 300 MHz	30	41		dB
		f = 300 MHz to 600 MHz	30	41		
		f = 600 MHz to 1.2 GHz	20	34		
		f = 1.2 GHz to 2.4 GHz	10	24		
		f = 2.4 GHz to 3 GHz	10	26		
		f = 3 GHz to 5 GHz	4	18		
		f = 5 GHz to 6.5 GHz	4	18		
TRANSMITTER AC/DC						
Z_{diffTX}	Pair differential impedance		85	100	122	Ω
Z_{SETX}	Single-ended input impedance		40			Ω
$V_{TXtrans}$	Sequencing transient voltage	Transient voltages on the serial data bus during power sequencing (lab load)	–1.2	0.3	1.2	V
RL_{DiffTX}	Differential mode return loss	f = 150 MHz to 300 MHz	13	22		dB
		f = 300 MHz to 600 MHz	8	21		
		f = 600 MHz to 1.2 GHz	6	19		
		f = 1.2 GHz to 2.4 GHz	6	14		
		f = 2.4 GHz to 3 GHz	3	14		
$TX_{DiffRLSlope}$	Differential mode RL slope	f = 300 MHz to 3 GHz (see Figure 7)		–13		dB/dec

Electrical Characteristics (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RL_{CMTX}	Common-mode return loss	f = 150 MHz to 300 MHz	5	20		dB
		f = 300 MHz to 600 MHz	5	16		
		f = 600 MHz to 1.2 GHz	2	13		
		f = 1.2 GHz to 2.4 GHz	1	8		
		f = 2.4 GHz to 3 GHz	1	8		
IB_{TX}	Impedance balance	f = 150 MHz to 300 MHz	30	38		dB
		f = 300 MHz to 600 MHz	30	38		
		f = 600 MHz to 1.2 GHz	20	33		
		f = 1.2 GHz to 2.4 GHz	10	25		
		f = 2.4 GHz to 3 GHz	10	25		
		f = 3 GHz to 5 GHz	4	21		
		f = 5 GHz to 6.5 GHz	4	21		
$Diff_{VppTX}$	Differential output voltage swing	f = 3 GHz (under no interconnect loss)	400	650	900	mV_{pp}
VCM_{AC_TX}	TX AC CM voltage	At 1.5 GHz		15	50	mV_{pp}
		At 3 GHz		10	26	dBmV (rms)
		At 6 GHz		12	30	dBmV (rms)
VCM_{TX}	Common-mode voltage			1.7		V
TRANSMITTER JITTER(1)						
DJ_{TX}	Residual deterministic jitter	VID = 500 mV_{pp}, UI = 333 ps, K28.5 control character, see Figure 8		0.12	0.19	UI_{pp}
RJ_{TX}	Random jitter	VID = 500 mV_{pp}, UI = 333 ps, K28.7 control character, see Figure 8		1	2	ps-rms
DJ_{TX}	Residual deterministic jitter	VID = 500 mV_{pp}, UI = 167 ps, K28.5 control character, see Figure 8		0.12	0.34	UI_{pp}
RJ_{TX}	Random jitter	VID = 500 mV_{pp}, UI = 167 ps, K28.7 control character, see Figure 8		0.95	2	ps-rms

(1) $T_J = (14.1 \times RJ_{SD} + DJ)$ where RJ_{SD} is one standard deviation value of RJ Gaussian distribution. Jitter measurement is at the SATA connector and includes jitter generated at the package connection on the printed-circuit board, and at the board interconnect as shown in Figure 8.

7.6 Timing Requirements

			MIN	TYP	MAX	UNIT
DEVICE PARAMETERS						
t_{PDelay}	Propagation delay	Measured using K28.5 pattern (see Figure 1)		275	350	ps
$AutoLP_{ENTRY}$	Auto low power entry time	Electrical idle at input (see Figure 3)		11		µs
$AutoLP_{EXIT}$	Auto low power exit time	After first signal activity (see Figure 3)		33	50	ns
OOB						
t_{OOB1}	OOB mode enter	See Figure 2		1	5	ns
t_{OOB2}	OOB mode exit	See Figure 2		1	5	ns
RECEIVER AC/DC						
$t_{20\text{-}80RX}$	Rise and fall time	Rise times and fall times measured between 20% and 80% of the signal. SATA 3 Gbps speed measured 1" from device pin.	62		75	ps
t_{skewRX}	Differential skew	Difference between the single-ended mid-point of the RX+ signal rising and falling edge, and the single-ended mid-point of the RX– signal falling and rising edge.			30	ps
TRANSMITTER AC/DC						

Timing Requirements (continued)

			MIN	TYP	MAX	UNIT
$t_{20\text{-}80TX}$	Rise and fall time	Rise times and fall times measured between 20% and 80% of the signal. At 3 Gbps under no load conditions measured at the pin.	44	58	85	ps
t_{skewTX}	Differential skew	Difference between the single-ended mid-point of the TX+ signal rising edge and falling edge, and the single-ended mid-point of the TX– signal falling edge and rising edge, D1, D0 = V_{CC}		2	15	ps
$t_{xR/Flmb}$	TX rise and fall imbalance	At 3 Gbps		6%	20%	
$t_{xAmplmb}$	TX amplitude imbalance			1%	10%	
TRANSMITTER JITTER						
	Rise and Fall time		46.5 %	47.5 %	48.3 %	
	Rise and Fall mismatch			1.5%	3%	

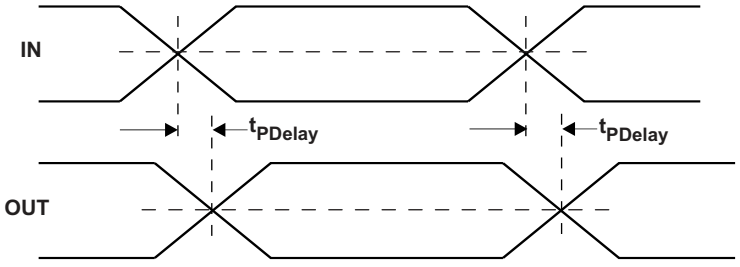


Figure 1. Propagation Delay Timing Diagram

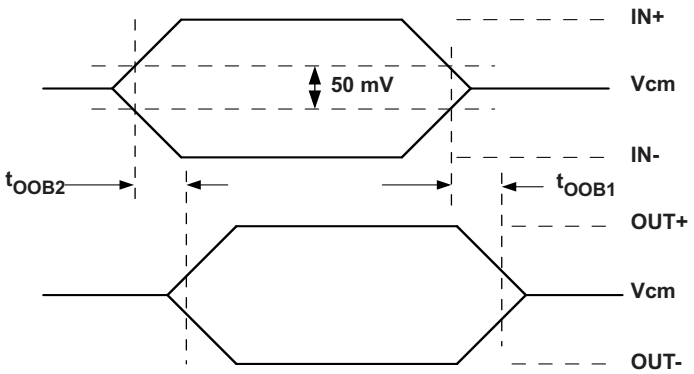


Figure 2. OOB Enter and Exit Timing

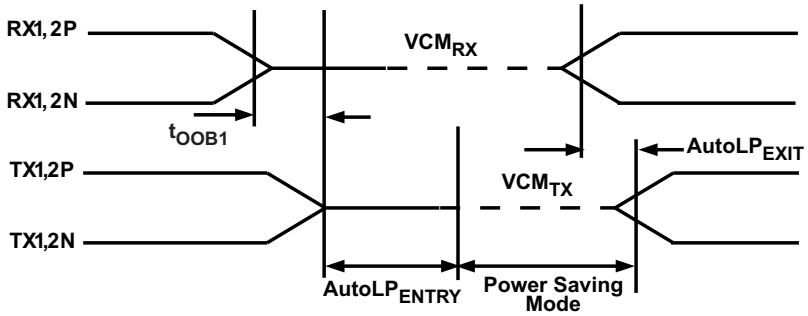


Figure 3. Auto Low Power Mode Entry and Exit Timing

7.7 Typical Characteristics

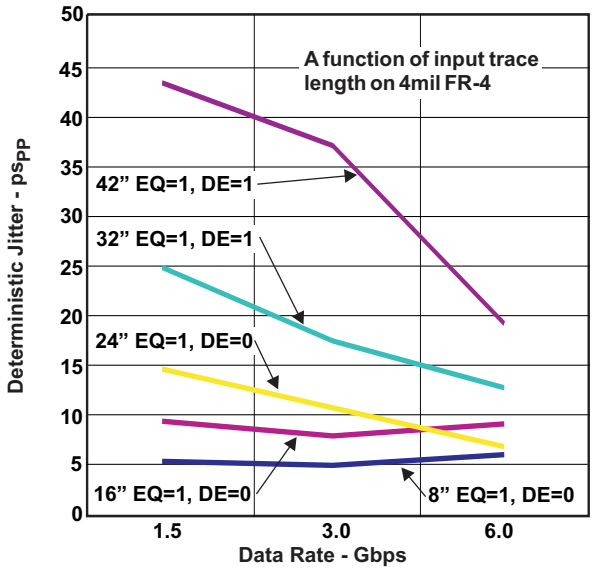


Figure 4. Deterministic Jitter vs Data Rate

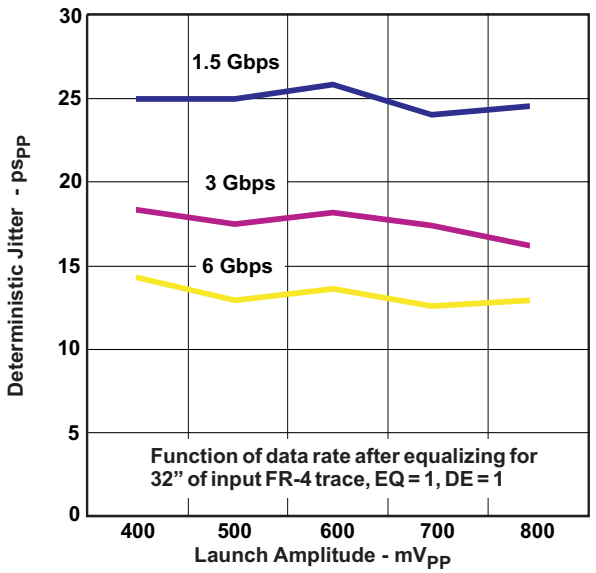


Figure 5. Deterministic Jitter vs Launch Amplitude

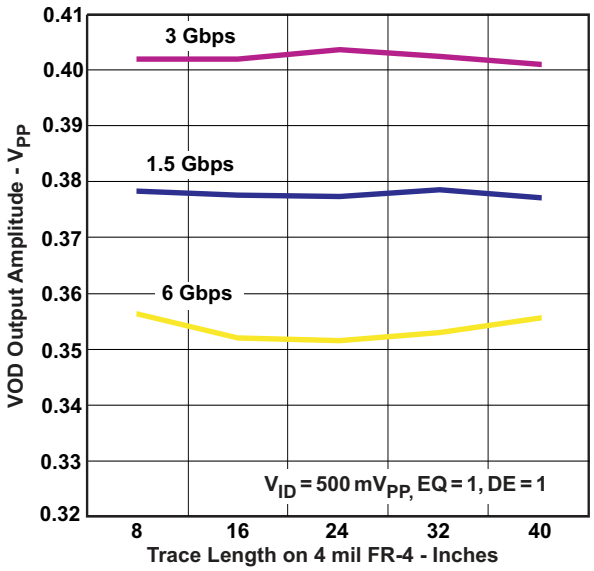


Figure 6. VOD Output Amplitude vs Trace Length

8 Parameter Measurement Information

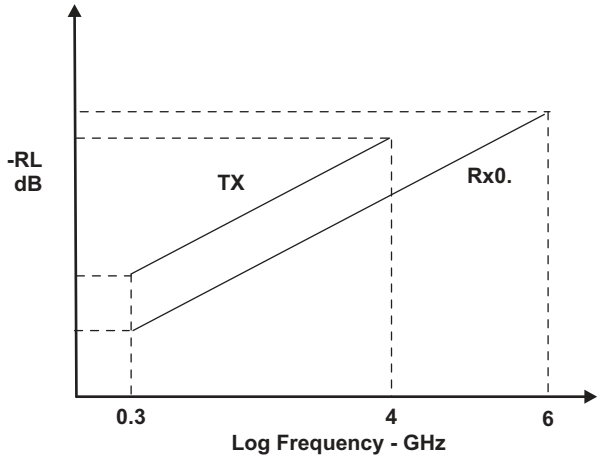


Figure 7. TX, RX Differential Return Loss Limits

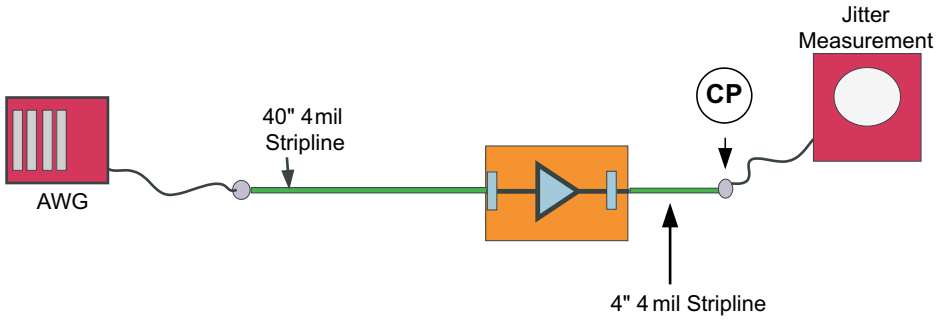


Figure 8. Jitter Measurement Test Condition

9 Detailed Description

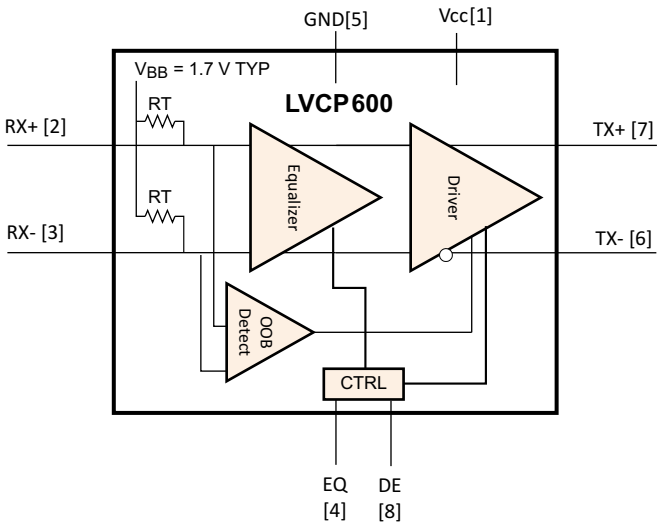
9.1 Overview

The SN75LVCP600 is a single-channel, SATA Express, and PCIe signal conditioner supporting data rates up to 6 Gbps. The device supports SATA Gen 1, 2, and 3 specifications as well as PCIe 1, 2, and 3. The SN75LVCP600 operates from a single 3.3-V supply and has 100-Ω line termination with self-biasing feature, making the device suitable for AC coupling. The inputs incorporate an out-of-band (OOB) detector, which automatically squelches the output when the input differential voltage falls below threshold while maintaining a stable common-mode voltage. The device is also designed to handle spread spectrum clocking (SSC) transmission per SATA standard. The SN75LVCP600 handles interconnect losses at its input with selectable equalization settings that are programmable to match the loss in the channel.

For data rates of 3 Gbps and lower the SN75LVCP600 equalizes signals for a span of up to 50 inches of FR4. For data rates of 8 Gbps the device compensates up to 40 inches of FR4.

The device is hot-plug capable preventing device damage under device *hot*-insertion such as async signal plug or removal, unpowered plug or removal, powered plug or removal, or surprise plug or removal.

9.2 Functional Block Diagram



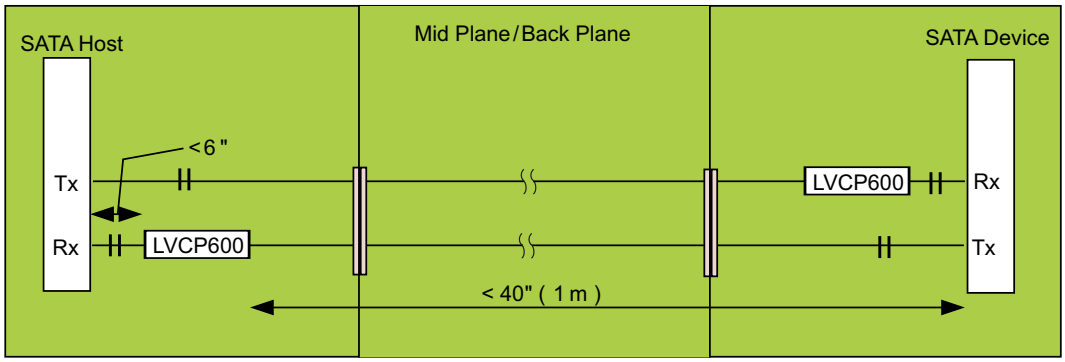
9.3 Feature Description

9.3.1 Input Equalization

The SN75LVCP600 supports programmable equalization in its front stage; Table 1 lists the equalization settings. The input equalizer is designed to recover a signal even when no eye is present at the receiver and effectively supports FR4 trace at the input anywhere from 4" to 40" at SATA 6G speed.

Table 1. EQ and DE Settings

EQ	EQUALIZATION (at 6 Gbps)	DE	DE-EMPHASIS (at 6 Gbps)
0 (*default*)	7 dB	0 (*default*)	0 dB
1	14 dB	1	–1.2 dB



Note:
Trace lengths are suggested values based on TI HSPICE simulations (done over programmable limits of input EQ) to meet SATA loss and jitter spec.

Actual trace length supported by the LVCP600 may be more or less than suggested values and will depend on board layout, trace widths and number of connectors used in the high speed signal path.

Figure 9. Trace Length Example

9.3.2 Auto Low Power (ALP) Mode

Auto Low Power (ALP) Mode is triggered when a channel is in the electrical idle state for > 10 µs. The device enters and exits Low Power Mode by actively monitoring input signal (VID_{pp}) level. When the input signal is in the electrical idle state, that is, VID_{pp} < 50 mV and stays in this state for > 10 µs, the device automatically enters the low power state. In this state the output is driven to VCM and the device selectively shuts off internal circuitry to lower power by > 90% of its normal operating power. While in ALP mode the device continues actively to monitor input signal levels. When the input signal exceeds the SATA OOB upper threshold level, the device reverts to the active state. Exit time from Auto Low Power Mode is < 50 ns (maximum). See *Auto Low Power*.

9.3.3 Out-of-Band (OOB) Support

The squelch detector circuit within the device enables full detection of OOB signaling as specified in the SATA spec. When differential signal amplitude at the receiver input is 50 mV_{pp} or less, the output is squelched. Differential signal amplitude of 90 mV_{pp} or more is detected as an activity and therefore passed to the output indicating activity. Squelch circuit ON/OFF time is 5 ns (maximum). While in squelch mode outputs are held to VCM.

9.4 Device Functional Modes

9.4.1 Active

Active mode is the normal operating mode. When power is applied to the device, and the differential input signal to the receiver is greater than 90 mV_{pp}, the device is in active mode and meets all the specifications in the data sheet.

9.4.2 Squelch

When the device is powered, and the differential input signal to the receiver is less than 50 mV_{pp}, the device is in squelch mode. In squelch mode the transmitter outputs are both set to VCM_{TX} or 1.7 V.

9.4.3 Auto Low Power

When the device is powered and the differential input signal to the receiver has been less than 50 mV_{pp} for greater than 10 ns, the device transitions to Auto Low Power (ALP) mode. In ALP, the transmitter outputs are both set to VCM_{TX}. In addition, while in ALP, the device shuts off internal circuitry to lower power to less than 10% of the power in the Active mode.

10 Application and Implementation

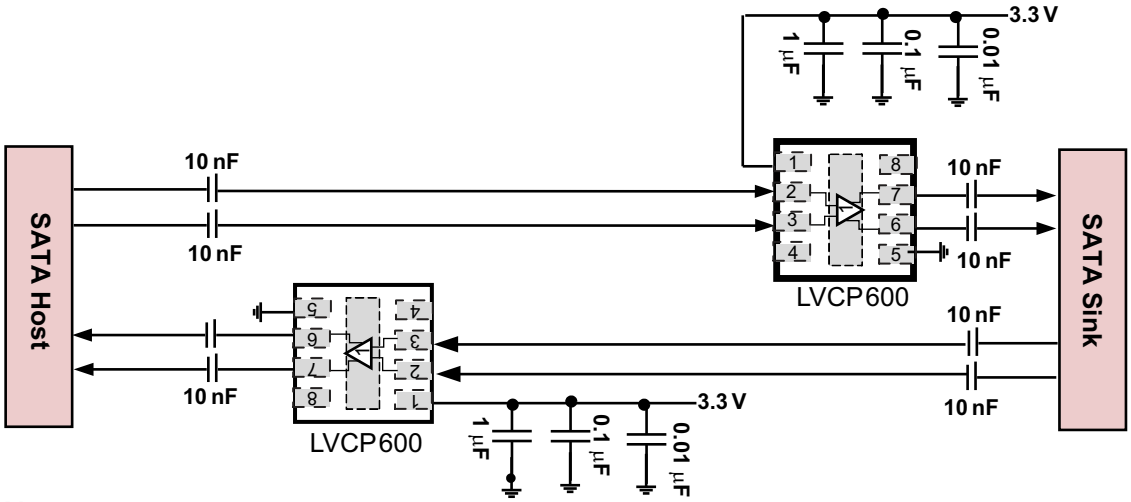
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The SN75LVCP600 is a single-channel SATA redriver and signal conditioner supporting data rates up to 6 Gbps. The inputs incorporate an out-of-band (OOB) detector, which automatically squelches the output while maintaining a stable common-mode voltage compliant to the SATA link.

10.2 Typical Application



Note:

1) Place supply caps close to device pin
2) EQ and DE selection at 7 dB and 0dB respectively
3) Actual EQ /DE settings will depend on device placement relative to host and SATA connector

Figure 10. Typical Device Implementation

10.2.1 Design Requirements

This design requires layout flexibility to place 0-Ω resistors. If a redriver is needed, go to step 3 in *Detailed Design Procedure*.

Table 2. Design Parameters

DESIGN PARAMETER	VALUE
V_{CC}	3.3 V
I_{CC}	29 mA
Input voltage	120 mV_{pp} to 1.6 V_{pp}
Output voltage	400 mV_{pp} to 900 mV_{pp}

10.2.2 Detailed Design Procedure

The LVCP600 allows the user to take the guess work of using a signal conditioning device in a SATA link. With the SN75LVCP600, the user has the option to use or remove the device based on signal conditioning needs. See Figure 11.

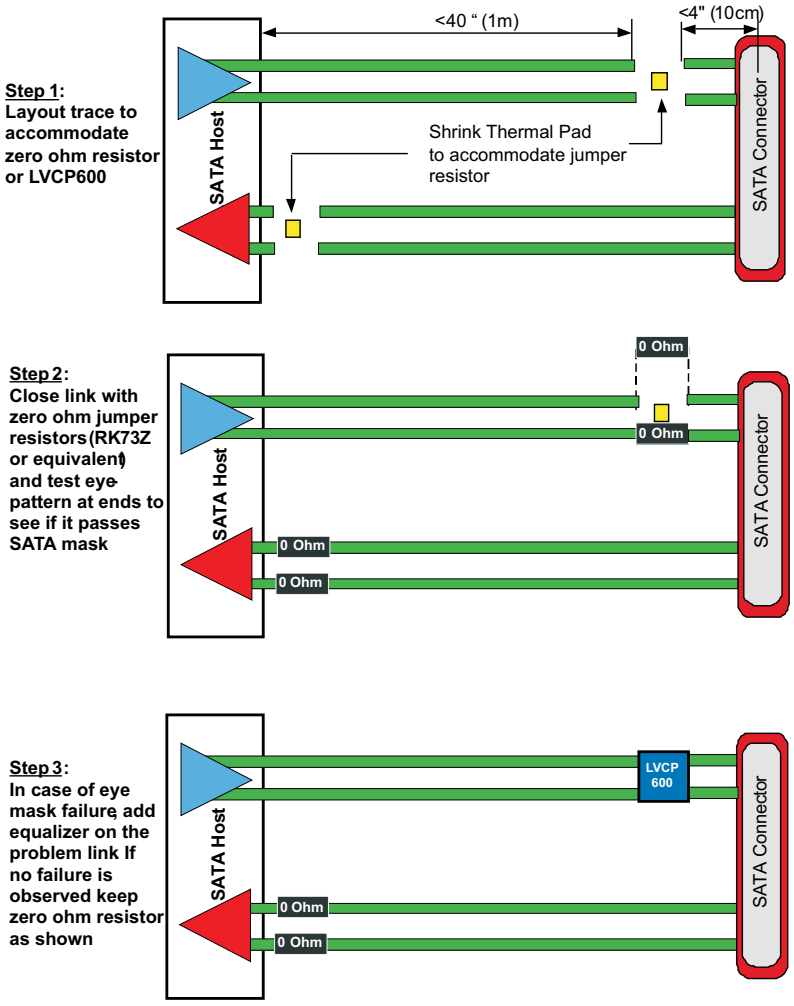


Figure 11. Implementation Guideline

Figure 13 through Figure 22 show SN75LVCP600 typical performance plots when connected to various trace lengths with V_{CC} = 3.3 V and T_A = 25°C. All eye diagrams measured using K28.5 pattern at 6 Gbps. Figure 12 shows the setup for the performance plots in *Application Curves*.

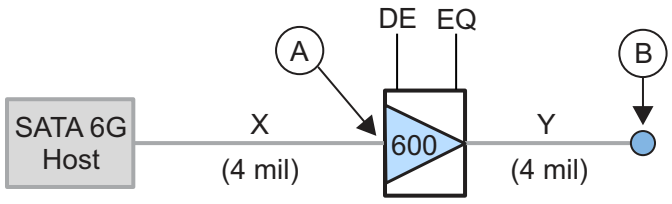
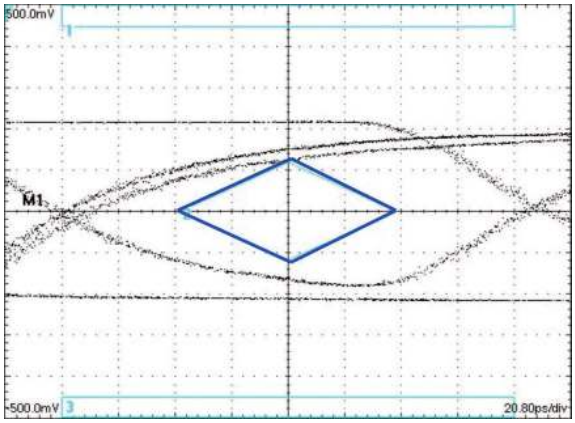


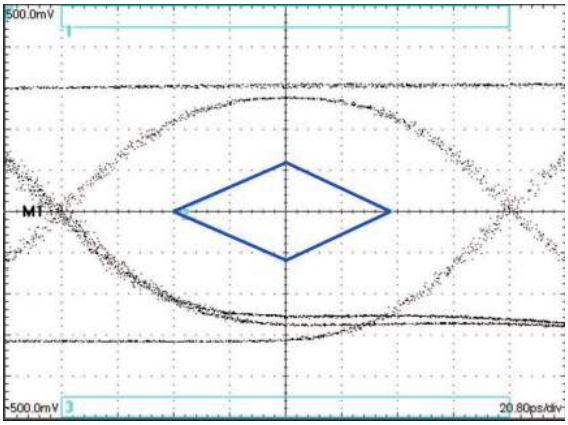
Figure 12. Test Points

10.2.3 Application Curves



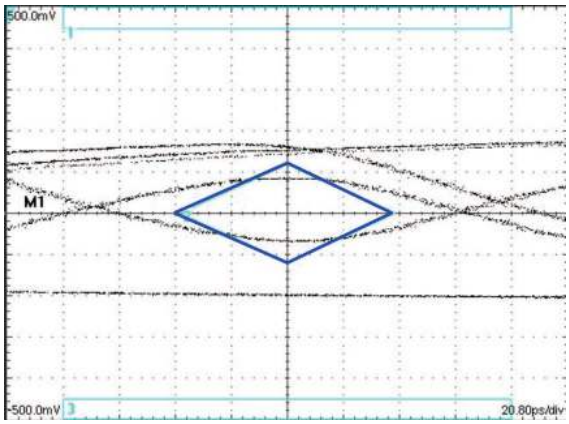
DE = 1 EQ = 0

Figure 13. Eye Pattern at A → X = 8”; Y = 2”



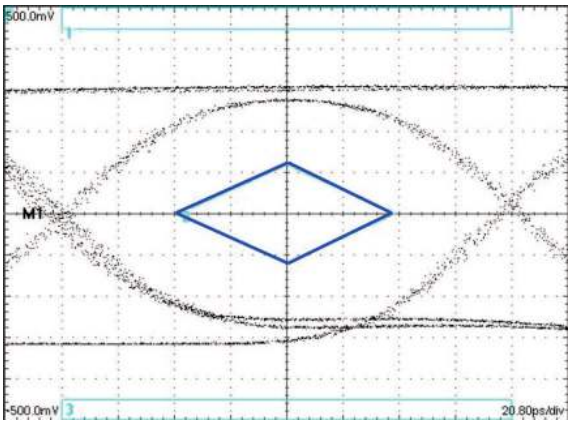
DE = 1 EQ = 0

Figure 14. Eye Pattern at B → X = 8”; Y = 2”



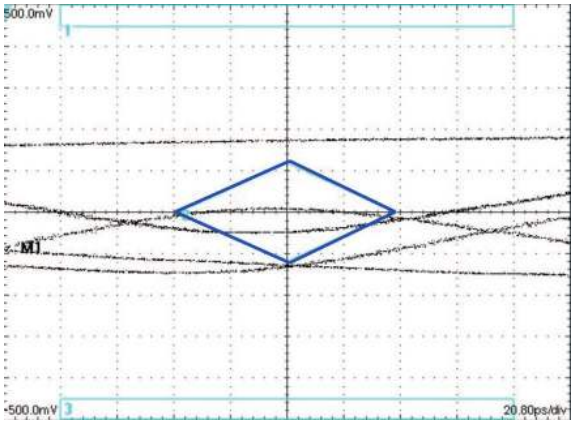
DE = 1 EQ = 0

Figure 15. Eye Pattern at A → X = 16”; Y = 2”



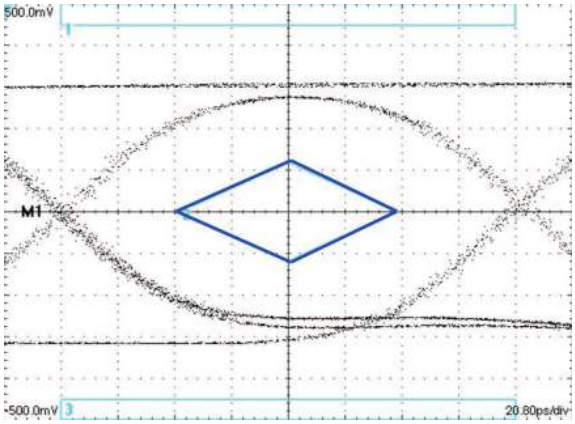
DE = 1 EQ = 0

Figure 16. Eye Pattern at B → X = 16”; Y = 2”



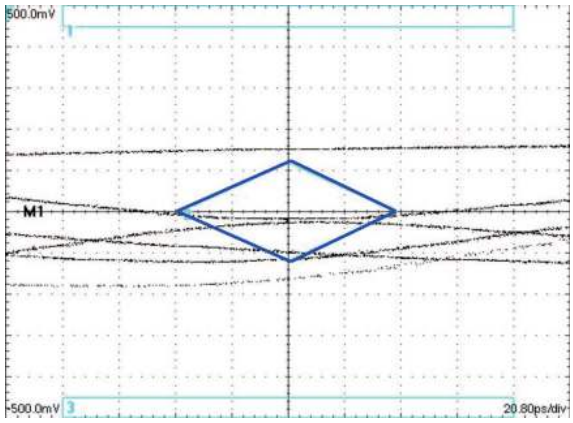
DE = 1 EQ = 0

Figure 17. Eye Pattern at A → X = 24”; Y = 2”



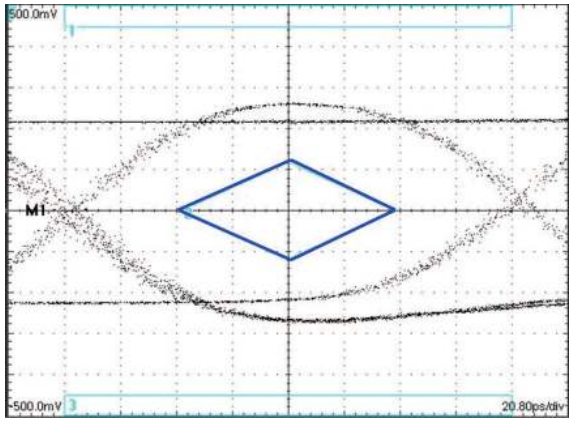
DE = 1 EQ = 0

Figure 18. Eye Pattern at B→ X = 24”; Y = 2”



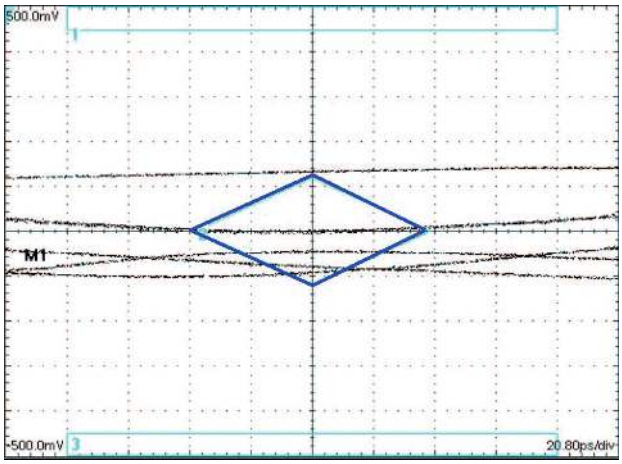
DE = 1 EQ = 1

Figure 19. Eye Pattern at A → X = 32”; Y = 2”



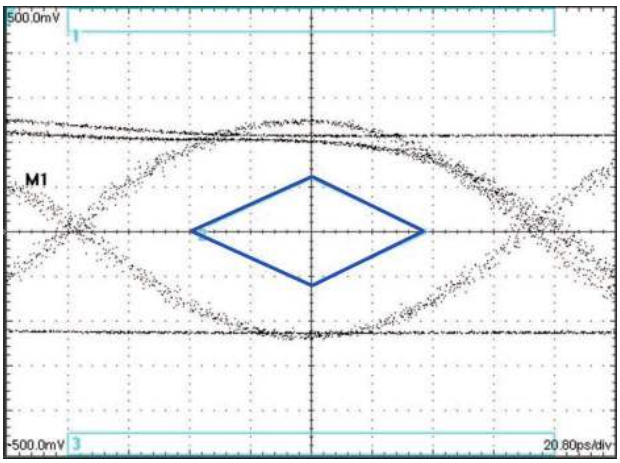
DE = 1 EQ = 1

Figure 20. Eye Pattern at B → X = 32”; Y = 2”



DE = 1 EQ = 1

Figure 21. Eye Pattern at A → X = 40”; Y = 2”



DE = 1 EQ = 1

Figure 22. Eye Pattern at B → X = 40”; Y = 2”

11 Power Supply Recommendations

The SN75LVCP600 is designed to operate from a single 3.3-V supply. Always practice proper power-supply sequencing procedure. Apply V_{CC} first before any input signals are applied to the device. The power-down sequence is in reverse order.

12 Layout

12.1 Layout Guidelines

12.1.1 Return Current and Plane References

High frequency return signal/current is defined as the path that a signal follows back to its original source as all signals flow in a closed loop. Minimizing the loop area of the closed loop is beneficial for both EMI (Electro-Magnetic Interference) reduction and signal integrity.

The best way to minimize loop area is to always have a signal reference their nearest solid ground or power plane. Obstructions to the return signal causes signal integrity problems like reflections, crosstalk, undershoot and overshoot.

Signals can reference either power or ground planes, but ground is preferred. Without solid plane references, single ended and differential impedance control is very hard to accomplish; crosstalk to other signals may happen as the return signals have no other path. This type of crosstalk is difficult to troubleshoot.

Symmetric pairing of solid planes in the layer stackup can significantly reduce warping of the PCB during the manufacturing process. Warping of the PCB is crucial to minimize on boards that uses BGA components.

12.1.2 Split Planes – What to Avoid

Never route signals over splits in their perspective reference planes.

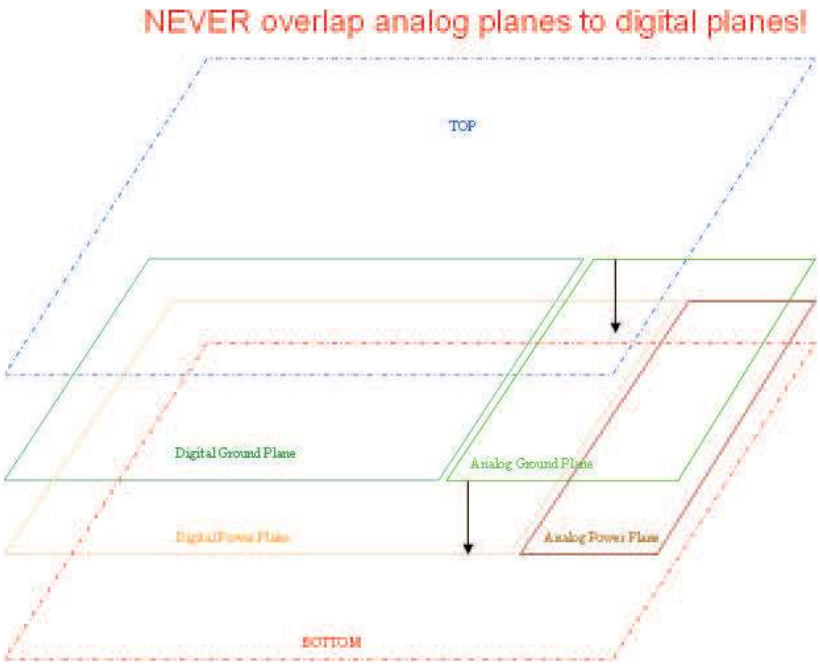


Figure 23. Overlapping Analog and Digital Planes

Layout Guidelines (continued)

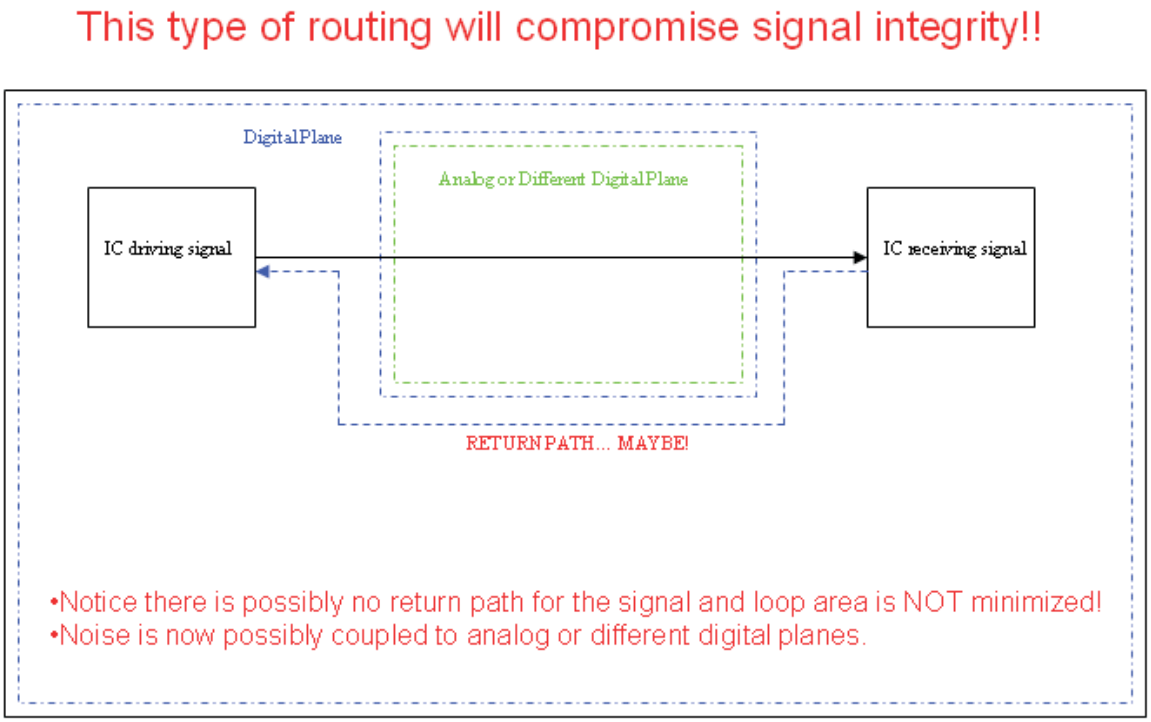


Figure 24. Incorrect Routing

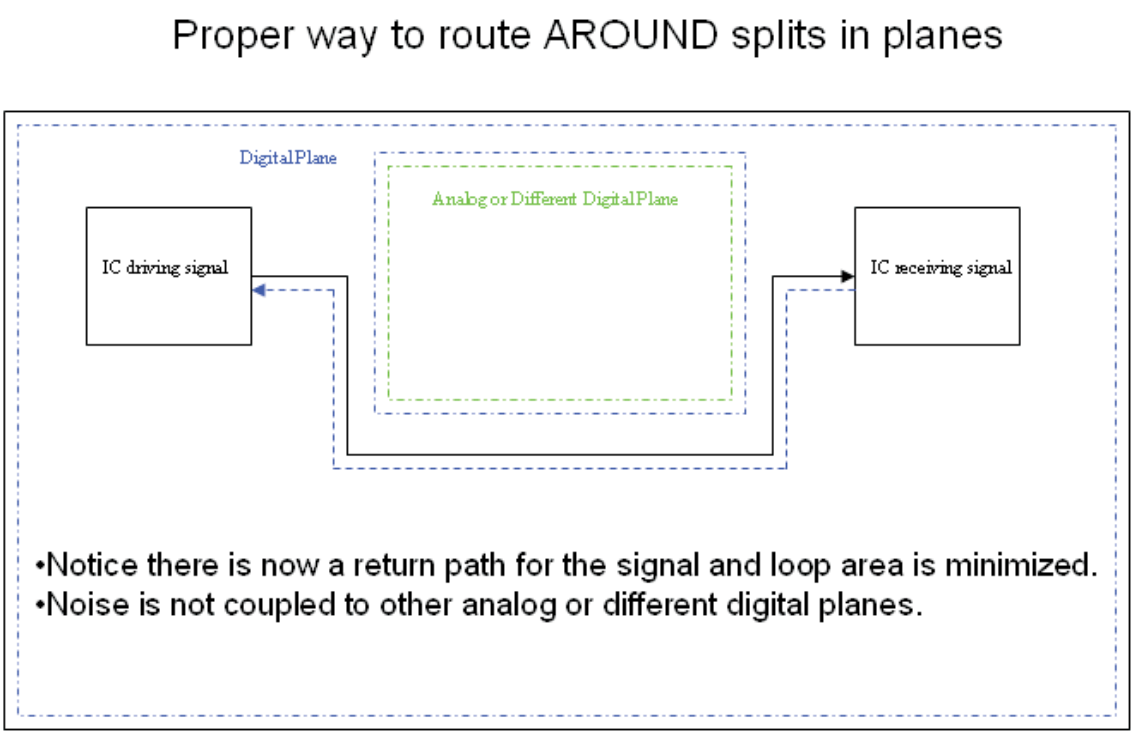


Figure 25. Proper Routing

Layout Guidelines (continued)

12.1.3 Avoiding Crosstalk

Crosstalk is defined as interference from one trace to another by either or both inductive and capacitive coupling. Best ways to avoid crosstalk are:

- Provide stable reference planes for all high speed signals (as noted in previous sections).
- Use the 3W rule (3 times the width of trace for separation) where applicable on all signals, but absolutely use on clock signals.
- Use ground traces/guards around either *victim* or *aggressor* signals prone to crosstalk.
- When space is constrained and limited on areas of the PCB to route parallel buses, series or end termination resistors can be used to route traces closer than what is normally recommended. However, calculations and simulations must be done to validate the use of series or end termination resistors to eliminate crosstalk.

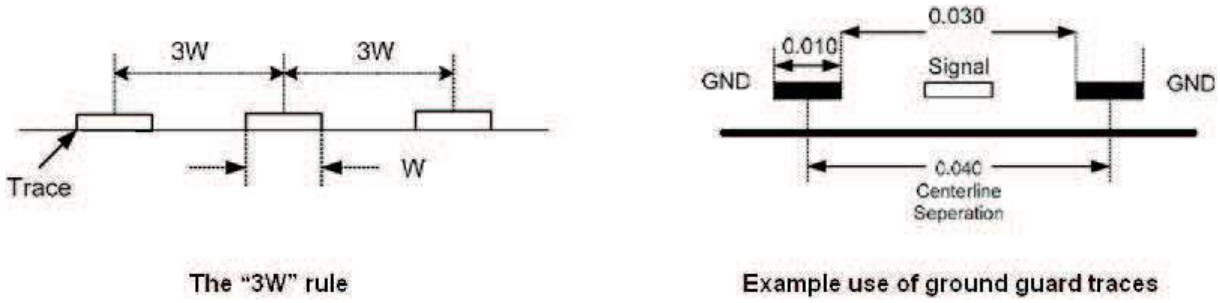


Figure 26. Ways to Avoid Crosstalk

12.2 Layout Example

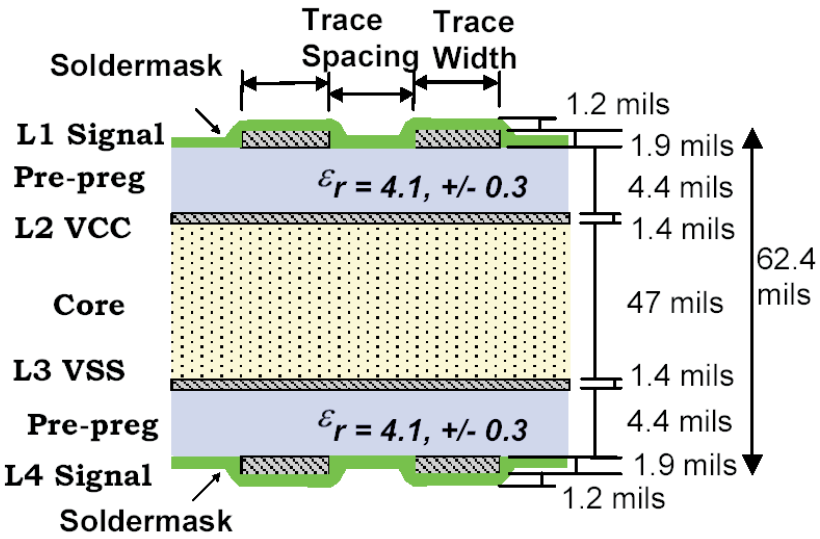


Figure 27. Printed-Circuit Board Stackup (FR-4 Example)

Layout Example (continued)

4 Layer

Layer 1	(Top)
Layer 2	(GND)
Layer 3	(PWR)
Layer 4	(Bottom)

6 Layer

Layer 1	(Top)
Layer 2	(GND)
Layer 3	(Signal)
Layer 4	(Signal)
Layer 5	(PWR)
Layer 6	(Bottom)

10 Layer

Layer 1	(Top)
Layer 2	(GND)
Layer 3	(Signal)
Layer 4	(Signal)
Layer 5	(PWR)
Layer 6	(GND)
Layer 7	(Signal)
Layer 8	(Signal)
Layer 9	(GND)
Layer 10	(Bottom)

PCB layer configuration suggestions for stackup symmetry and signal integrity.

Figure 28. PCB Layer Configuration Suggestions

13 Device and Documentation Support

13.1 Device Support

13.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.4 Trademarks

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All other trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75LVCP600DRFR	ACTIVE	WSON	DRF	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 85	600	Samples
SN75LVCP600DRFT	ACTIVE	WSON	DRF	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 85	600	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

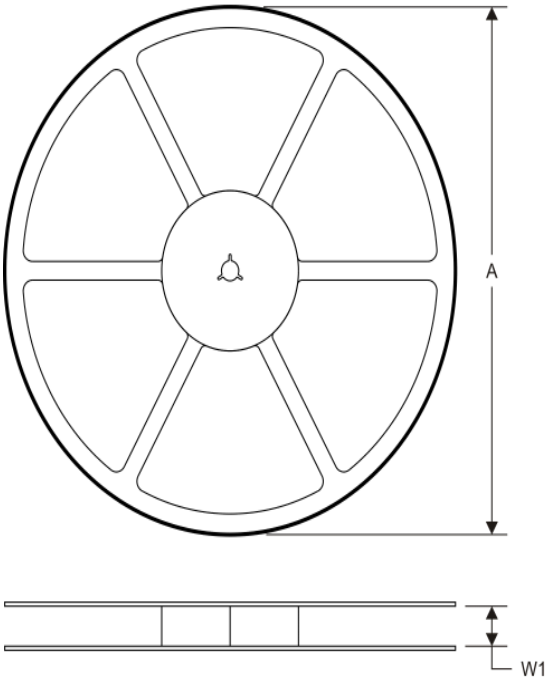
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

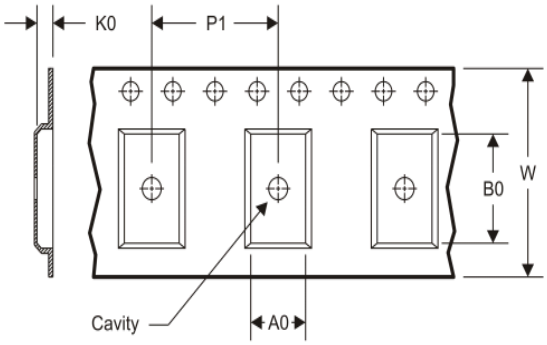
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



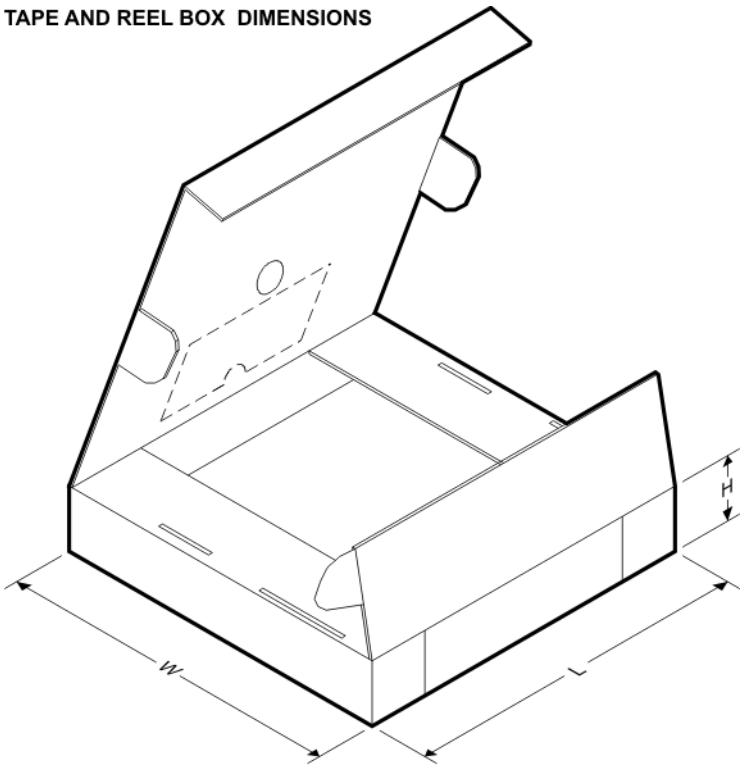
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75LVCP600DRFR	WSON	DRF	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
SN75LVCP600DRFT	WSON	DRF	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

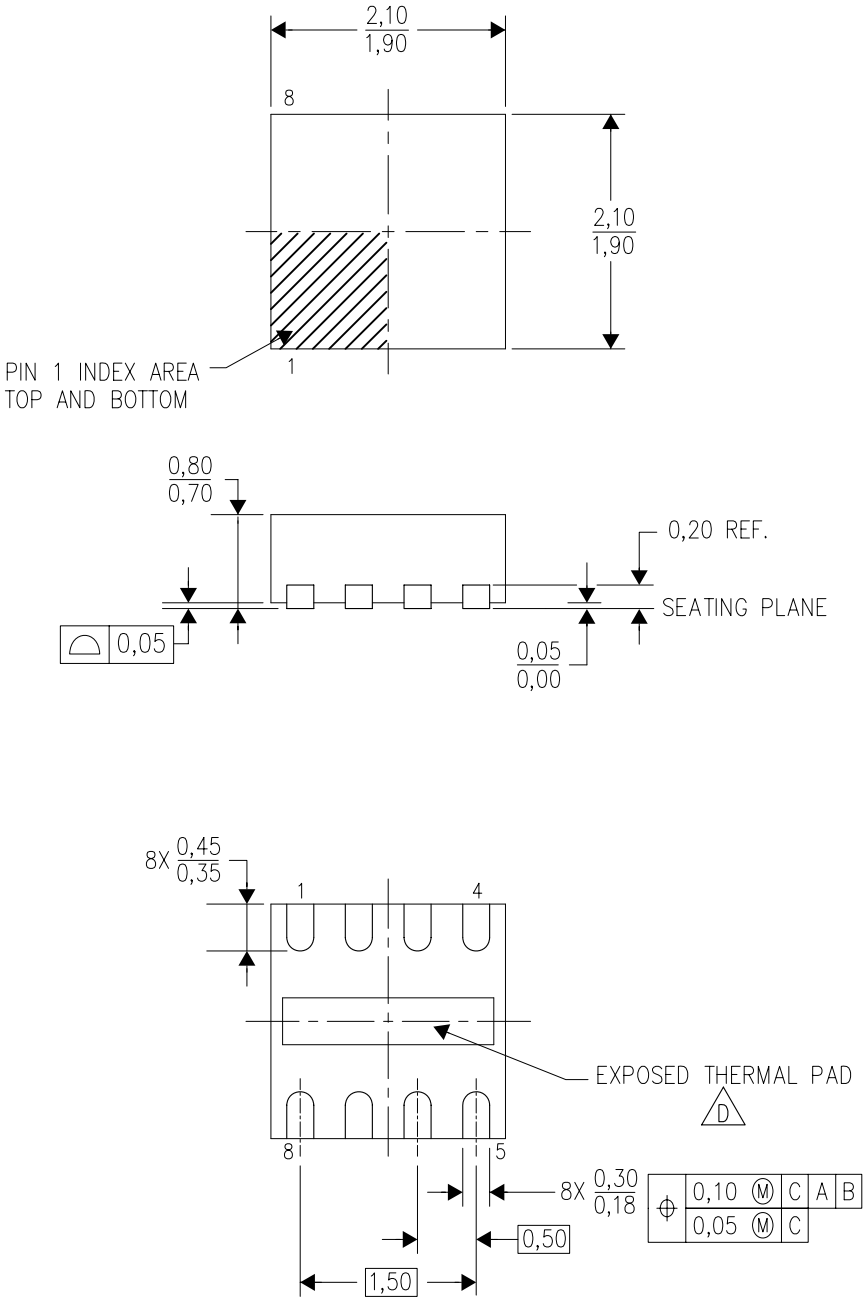
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75LVCP600DRFR	WSON	DRF	8	3000	210.0	185.0	35.0
SN75LVCP600DRFT	WSON	DRF	8	250	210.0	185.0	35.0

DRF (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



4205287/E 10/10

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The Package thermal pad must be soldered to the board for thermal and mechanical performance. See product data sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–229.

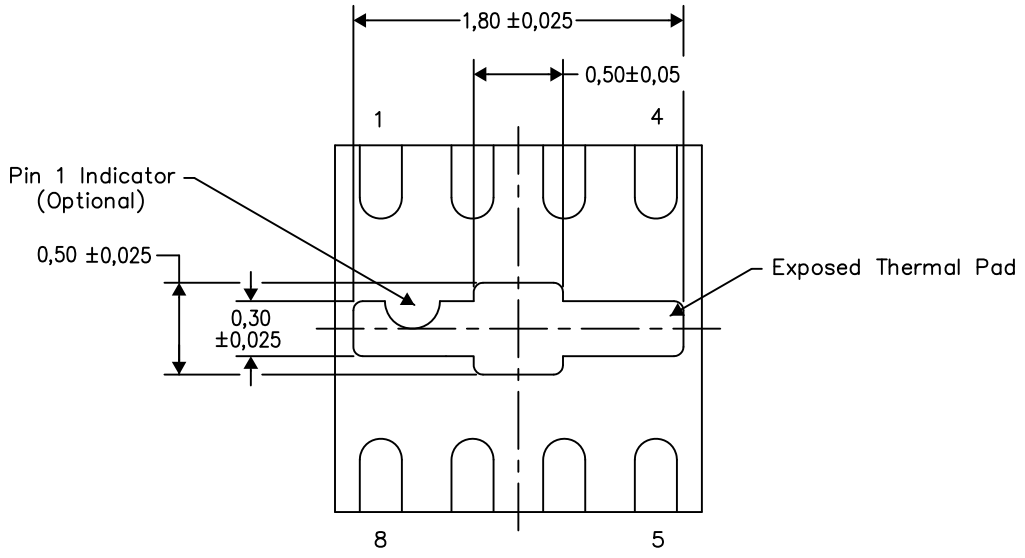
DRF (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



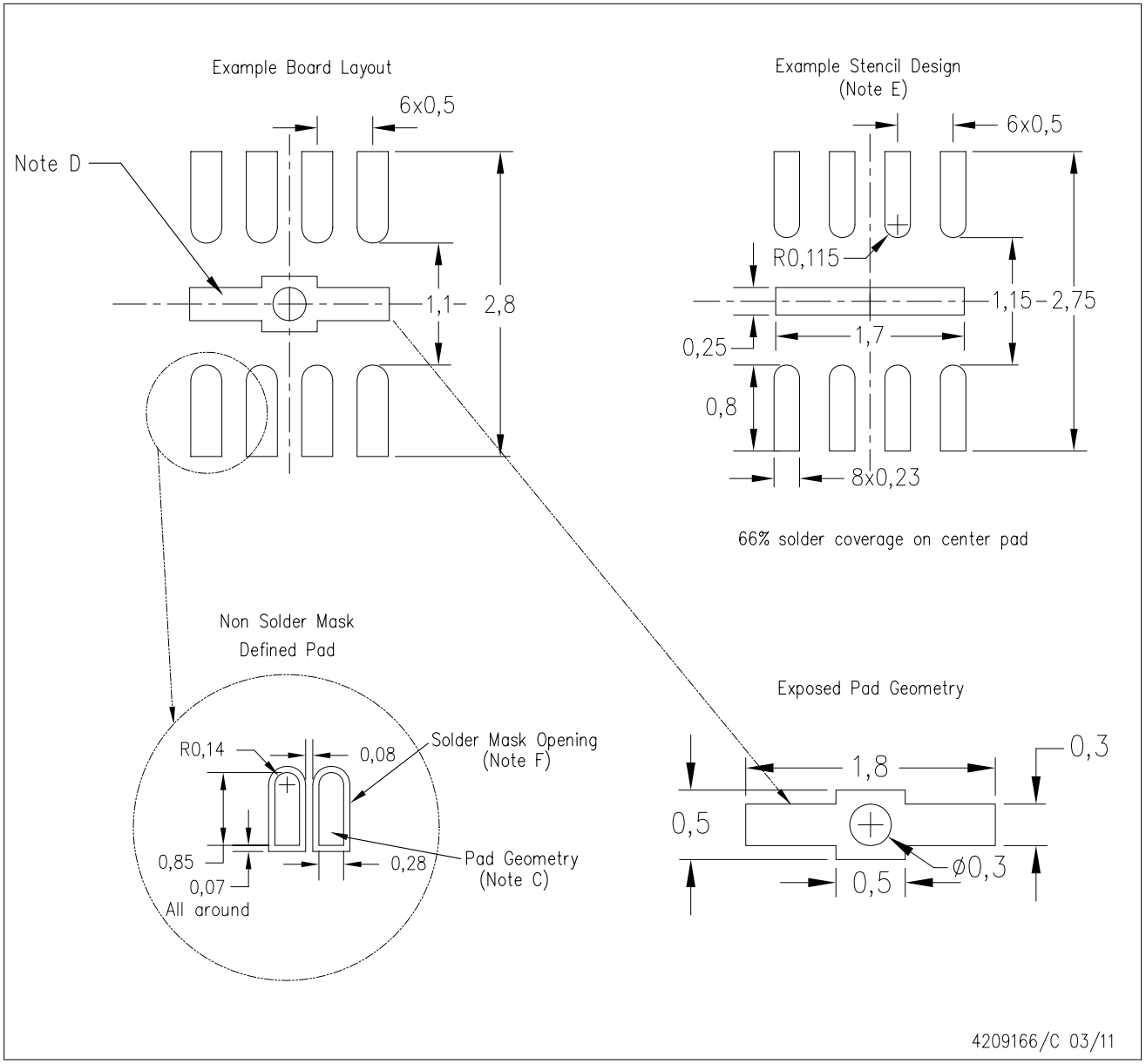
Bottom View

Exposed Thermal Pad Dimensions

4206840/H 12/14

NOTE: A. All linear dimensions are in millimeters

DRF (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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