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AS3658

Data Sheet Confidential

Power and Audio Management Unit for Portable Devices

1 General Description

The AS3658 is highly integrated power and audio management unit. The AS3658 is designed to include sophisticated audio features like high performance audio DAC and ADC. It has several analog and digital audio interface which are explained in detail in the following sections. The AS3658 is an integrated solution for power supply generation and monitoring, battery management including charging.

2 Key Features

- System Control
  - Serial Control Interface
  - On/Off Control Module with Boot-ROM / GPIO
  - Reset Generation for system controller
  - Programmable Interrupt Controller and Watchdog
  - Low power off mode (9µA; 2.5V LDO on)
  - 88 bit unique ID or Boot fuse array
  - Reset with long ON-Keypress (SW-Interuptable)
  - Touchscreen Interface (10 bit, interrupt)
- Supply Voltage Generation
  - 2 RF Programmable Low Noise LDOs (250mA) (1 LDO can be a current controlled switch for hotplug (200mA ± 40%))
  - 1 RF Programmable Low Noise LDO (400mA)
  - 4 Programmable Dig. Low Power LDOs(200mA)
  - 2 General Purpose PWM DC/DC step up converter with three programmable current sinks (e.g. for-white led); for current mode feedback is automatically slected (DCDC_CURR1,2,3)
  - 3 General Purpose high efficiency DC/DC step down converter (DCDC 1 support DVM)
  - 1 Low noise charge pump with 5V output voltage
  - 1 Ultra Low Power 2.5V LDO (always on)
- Current sinks
  - 4 programmable(8-bit) from 0.15mA to 38.25mA (±5%) optional useable as GPIOs
  - 3 programmable high voltage (15V) (8-bit) from 0.15mA to 38.25mA (±5%)
  - internal PWM generator (extended time range) (can control DCDC_CURR1,2,3)
- 10-bit 40µs Successive Approximation ADC
  - Two external Inputs (ADC_IN1, ADC_IN2)
- Battery Management
  - Full featured chemistry independent step down charger with Gas Gauge and Current limitation
  - High Current (1.0A) Linear Charger with external pass transistor (no step down charger)
  - 0.1 Ω Battery switch for start-up and trickle charge
  - Integrated USB charger up to 880mA (can be used as wall adapter charger); current accuracy 440-500mA for USB specification, in-circuit trimmable (±1.2% trimsteps)
  - Autonomous Battery Temperature Supervision (0ºC-45ºC or 0ºC- 50ºC) for 10k and 100k NTC
  - Charging Timeout (1h-8h in 30min steps)
  - Charging in Stanby mode
  - Completely Autonomous (no SW)
- Power Management Features
  - Wide Battery Supply Range 3.0…5.5V
  - On-Chip Bandgap Tuning for High Accuracy (±1%)
  - Thermal and Current Protection (int. sensor)
  - Standby Mode exit by interrupt e.g. Onkey/RTC
- Audio
  - 94dB Audio DAC, 16-48kHz sampling rate
  - Two Digital Audio Inputs (2 x I2S interface)
  - 2.9V low Noise LDO for Audio DAC
  - Two Headphone Amplifier Output with GND separation
  - Two I2S Inputs and one I2S Output
  - I2S master mode with programmable sample rate (controlled by internal PLL)
  - GND Buffer for Headphone Amplifier
  - Line/ Headphone outputs with GND separation
  - Audio ADC, 82dB SNR with 16ksps
  - Microphone Bias Supply and Amplifier (mono)
  - 5 Band Adjustable Audio Equalizer (± 12dB in 3dB gain steps)
  - SPDIF Output
  - Audio Mixer and Gain Stages
  - PCM Interface
- Real Time Clock (RTC)
  - Alarm and Time function
  - Repeated Wakeup (every second or minute)
  - 32kHz output
  - Backup Battery Charger and Switchover
- Programmable System clock
  - 1.6 MHz to 2.3 MHz with 100 kHz steps
- Package
  - BGA124 8x8mm, 0.5mm pitch (can be assembled without micro via boards)

3 Applications

The AS3658 is ideal for PDA, PMP, GPS-Navigation Systems and 1 Cell Li+ or 3 Cell NiMH powered devices.

Figure 1. Blockdiagram AS3658

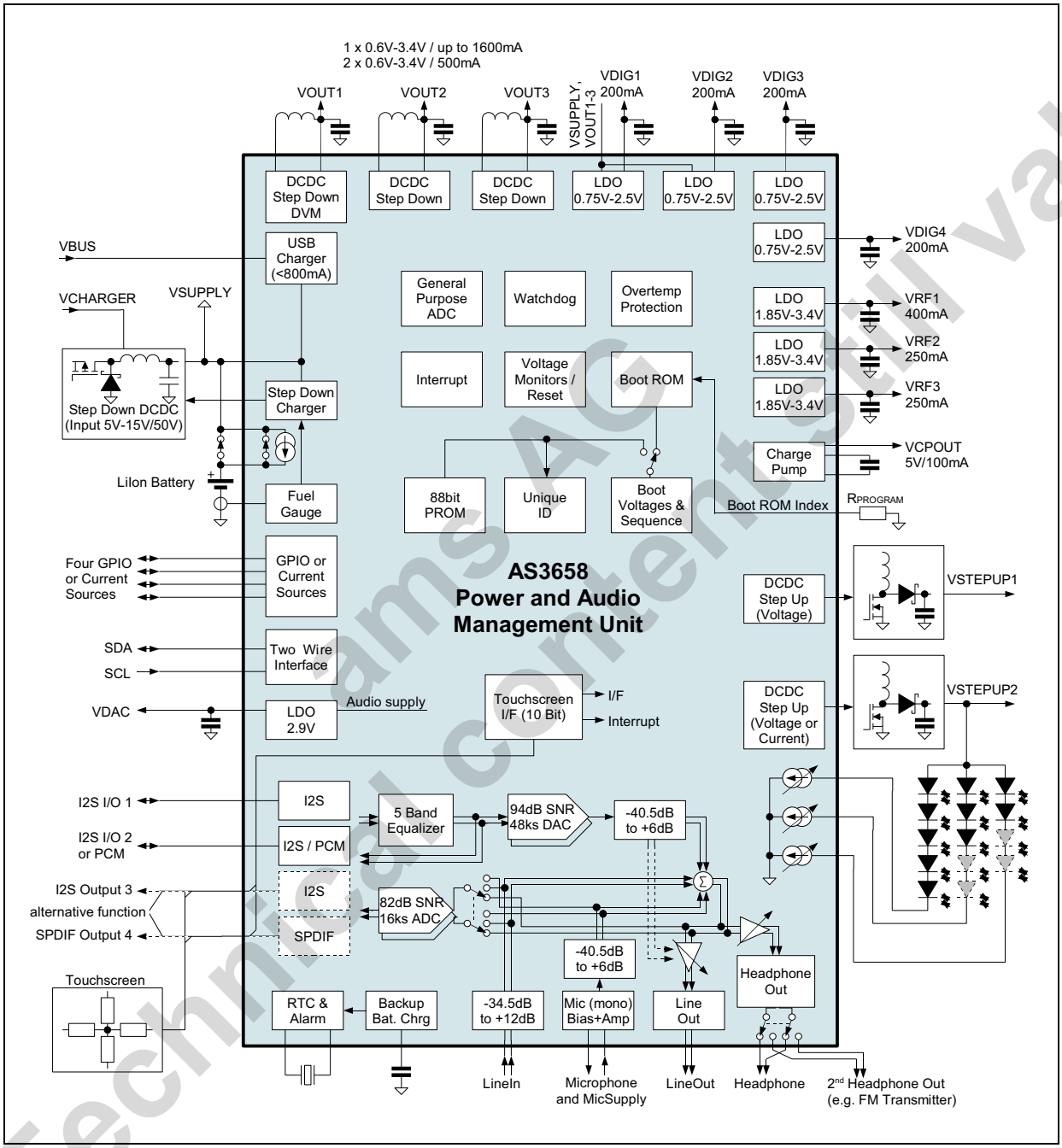
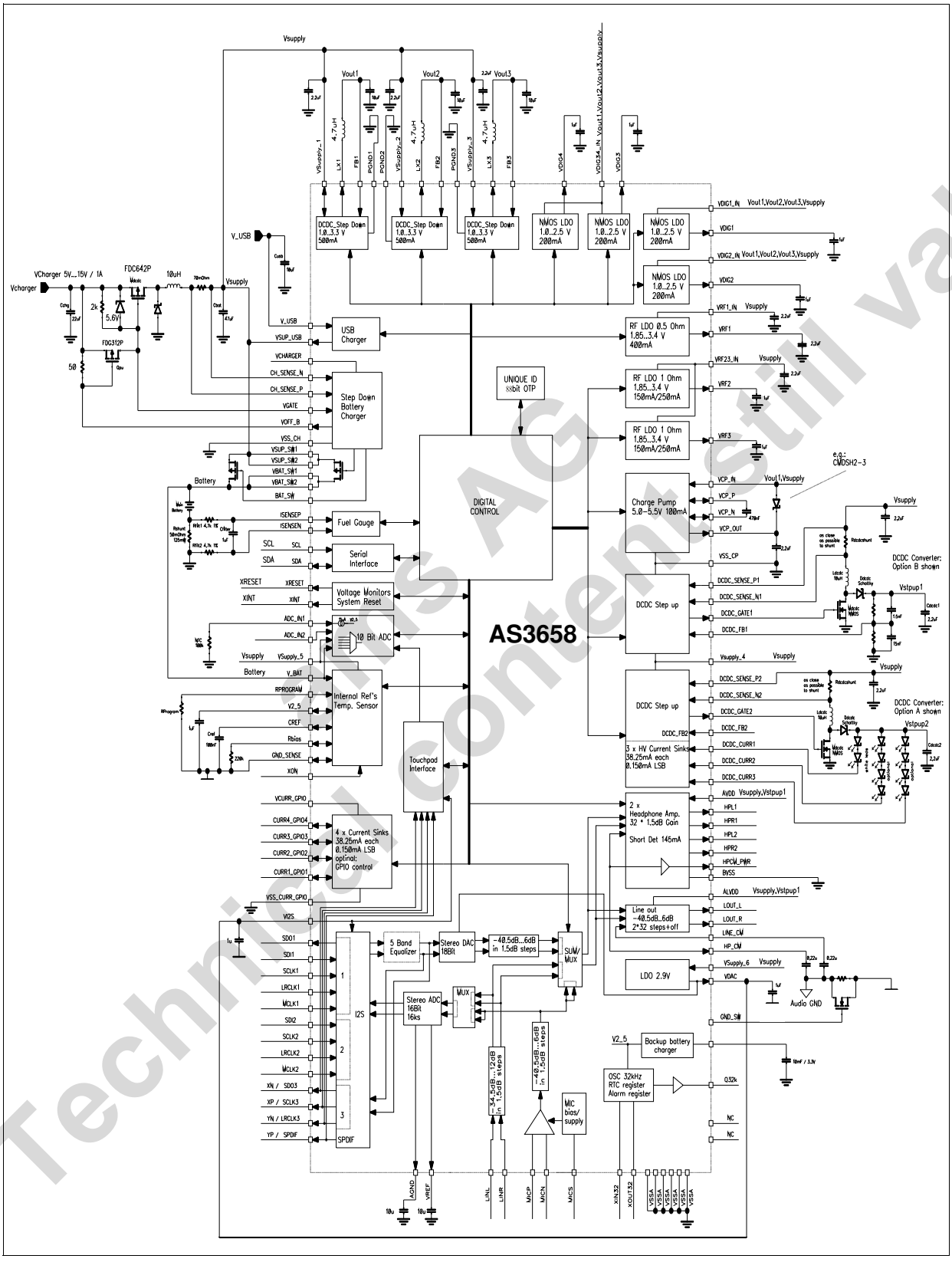


Figure 2. Application Diagram



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Document Revision History

Table 1. Revision History

Chapter	Rev	Description of Changes	Date	Author
	1v00	-	23.3.2009	pkm
9.1; 12	1v10	- updated package drawings - updated audio path drawings	15.4.2009	pkm
12,13	1v11	- updated packagemarkings and ordering information	23.9.2009	pkm
12,13	1v12	- updated packagemarkings and ordering information	23.10.2009	pkm
	1v13	- typo corrections	23.9.2010	pkm

4 Pin Assignments

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	NC/ VSS _CP	LRC LK1	SCL K3	VI2S	SDO 1	VCP _N	VCP _P	VCP _OU T	VDI G34 _IN	VDI G1_I N	LOU T_R	LINE _CM	HPL 1	NC/ BV SS
B	SDI2		SCLK1	SDI1	SDA	VSS_C P	VCP_I N	VDIG_ 2	VDIG2 _IN	VDIG_ 1	LOUT_ L	HP_C M		HPR 2
C	Q32k	SCLK2											HPR1	HPL2
D	DCDC _SENS E_P1	MCLK 2			SDO3	SCL	VDIG_ 4	VDIG_ 3	MCLK 1	LRCLK 2			ALVD D	HP_ CM_ PWR
E	VSUP PLY_4	DCDC _SENS E_N1		LRCLK 3							BVSS		AVDD	LINR
F	VSUP PLY_3	DCDC _GATE 1		SPDIF			XRES ET	XINT			MICS		VDAC	LINL
G	LX3	DCDC _GATE 2		DCDC _SENS E_N2		DCDC _SENS E_P2			VSSA		MICN		VSUP PLY_6	VSU P_S W12
H	PGND 3	PGND 2		DCDC _FB1		FB3			VSSA		MICP		VBAT_ SW12	VSU P_S W12
J	LX2	VSS_C H		DCDC _FB2			FB2	VSSA			VREF		BAT_S W	VBAT _SW 12
K	VSUP PLY_1	VSUP PLY_2		FB1							AGND		ISENS N	ISEN SP
L	LX1	VOFF_ B			CURR 4_GPI O4	DCDC _CUR R1	DCDC _CUR R3	GND_ SW	RPRO GRAM	CREF			GND_ SENS E	RBIA S
M	PGND 1	VGAT E											V_BAT	VBA CK
N	PGAT E1		VSUP PLY_5	XON	CURR 1_GPI O1	CURR 3_GPI O3	DCDC _CUR R2	ADC_I N1	ADC_I N2	VRF_2	VCHA RGER	V2_5		XOU T32
P	NC/ VSSA	CH_S ENSE_ P	CH_S ENSE_ N	VCUR R_GPI O	VSS_C URR	CURR 2_GPI O2	VSUP_ USB	V_USB	VRF1_ IN	VRF_1	VRF23 _IN	VRF_3	XIN32	NC/ VSS A

4.1 Pin Description

*Table 2. Pin list CTBGA124, 8x8MM (*AS3658*)*

Pin Name	Pin Number	Pin Type	Supply	Description
Charger				
V_USB	P8	P		USB voltage supply input
VSUP_USB	P7	P		Supply output of USB charger (connect to Vsupply)
VCHARGER	N11	P		High voltage input coming from the charger; if the charger is used connect a ceramic capacitor of 1µF
VGATE	M2	A		Switch ON control pin for the external PMOS Fet transistor of the charger step down converter
VOFF_B	L2	A		Switch OFF control pin for the external PMOS Fet transistor of the charger step down Buck converter
VSS_CH	J2	P		Ground pad of Step down Charger
VBAT_SW12	H13	P	V_{BAT}	Battery switch input1 (battery side)
VBAT_SW12	J14	P	V_{BAT}	Battery switch input2 (battery side)
VSUP_SW12	G14	P	V_{SUPPLY}	Battery switch input1 (supply side)
VSUP_SW12	H14	P	V_{SUPPLY}	Battery switch input2 (supply side)
BAT_SW	J13	A		Battery switch output for external PMOS
CH_SENSE_N	P3	A	V_{SUPPLY}	Charger step down converter, external shunt resistor negative connection
CH_SENSE_P	P2	A	V_{SUPPLY}	Charger step down converter, external shunt resistor positive connection
ISENSP	K14	A	V2_5	Positive sensing input voltage for the external charging current shunt resistor
ISENSN	K13	A	V2_5	Negative sensing input voltage for the external charging current shunt resistor
Serial Interface				
SCL	D6	DI	V_{SUPPLY}	SCL input in I^2C mode
SDA	B5	DIO	V_{SUPPLY}	SDA input / output in I^2C mode
Control Interfaces				
XRESET	F7	OD	V_{SUPPLY}	Bidirectional Reset Pin – add an external pull-up resistor to the digital supply
XINT	F8	OD	V_{SUPPLY}	Interrupt Pin - add an external pull-up resistor to the digital supply
XON	N4	IPU	V2_5	Input pin to startup the system (power on), internal pull-up, apply zenerzap-programming voltage here
RTC				
Q32K	C1	OD	V_{SUPPLY}	32kHz oscillator digital output
XIN32	P13	A	V2_5	32kHz crystal oscillator input
XOUT32	N14	A	V2_5	32kHz crystal oscillator output

*Table 2. Pin list CTBGA124, 8x8MM (*AS3658*)*

Pin Name	Pin Number	Pin Type	Supply	Description
Internal Refs				
VSUPPLY_5	N3	P		Supply for voltage Measurement, **always** connect to VSUPPLY
V_BAT	M13	P	V_{BAT}	Battery supply for Reference blocks.
RPROGRAM	L9	A	V2_5	Select register setup at startup.
V2_5	N12	P		Internal regulator analogue output
CREF	L10	A	V2_5	Reference voltage bypass capacitor connection
RBIAS	L14	A	V2_5	Internal Bias Reference Resistor (connect 220kΩ resistor)
GND_SENSE	L13	P	VSSA	GND reference for analog blocks (connect to GND plane separate)
ADC_IN1	N8	A	V2_5	Analog input1 for ADC10
ADC_IN2	N9	A	V2_5	Analog input2 for ADC10
VBACK	M14	A		Backup battery connection
Current Sinks				
CURR1_GPIO1	N5	A	V_{CURR_GPIO}	Current sink 1, or GPIO1
CURR2_GPIO2	P6	A	V_{CURR_GPIO}	Current sink 2, or GPIO2
CURR3_GPIO3	N6	A	V_{CURR_GPIO}	Current sink 3, or GPIO3
CURR4_GPIO4	L5	A	V_{CURR_GPIO}	Current sink 4, or GPIO4
DCDC_CURR1	L6	A	V_{CURR_GPIO}	Step up DC/DC converter2 current source 1
DCDC_CURR2	N7	A	V_{CURR_GPIO}	Step up DC/DC converter2 current source 2
DCDC_CURR3	L7	A	V_{CURR_GPIO}	Step up DC/DC converter2 current source 3
VCURR_GPIO	P4	A		Supply voltage of GPIOs and current sinks
VSS_CURR_GPIO	P5	A	V_{CURR_GPIO}	Ground pad of Current sink / GPIO pads
General Purpose DC/DC Step up Converter 1 and 2				
VSUPPLY_4	E1	P		Supply for DCDC step up and control interface, always connect to VSUPPLY
DCDC_FB1	H4	A	V_{SUPPLY}	Step up DC/DC converter1 feedback input
DCDC_GATE1	F2	A	V_{SUPPLY}	Step up DC/DC converter1 control for external mosfet
DCDC_SENSE_P1	D1	A	V_{SUPPLY}	Step up DC/DC converter1 external shunt resistor positive connection
DCDC_SENSE_P2	G6	A	V_{SUPPLY}	Step up DC/DC converter2 external shunt resistor positive connection
DCDC_SENSE_N1	E2	A	V_{SUPPLY}	Step up DC/DC converter1 external shunt resistor negative connection
DCDC_SENSE_N2	G4	A	V_{SUPPLY}	Step up DC/DC converter2 external shunt resistor negative connection

*Table 2. Pin list CTBGA124, 8x8MM (*AS3658*)*

Pin Name	Pin Number	Pin Type	Supply	Description
DCDC_GATE2	G2	A	V_{SUPPLY}	Step up DC/DC converter2 control for external mosfet
DCDC_FB2	J4	A	V_{SUPPLY}	Step up DC/DC converter2 feedback input
Linear Regulators (LDOs)				
VRF1_IN	P9	P	V_{SUPPLY}	Supply Pad for RF1 LDO (VRF_1), always connect to Supply>3.0V
VRF_1	P10	A	V_{RF1_IN}	Output voltage of one of the RF LDO's; can be used as High-Side Switch, if used as LDO connect a ceramic capacitor of 1µF (±20%) or 2.2µF (+100%/-50%)
VRF23_IN	P11	P	V_{SUPPLY}	Supply Pad for RF2 and RF3 LDO (VRF_2, VRF_3), always connect to Supply>3.0V
VRF_2	N10	A	V_{RF23_IN}	Output voltage of one of the RF LDO's; can be used as High-Side Switch, if used as LDO connect a ceramic capacitor of 1µF (±20%) or 2.2µF (+100%/-50%)
VRF_3	P12	A	V_{RF23_IN}	Output voltage of one of the RF LDO's; can be used as High-Side Switch, if used as LDO connect a ceramic capacitor of 1µF (±20%) or 2.2µF (+100%/-50%)
VDIG1_IN	A10	P	V_{SUPPLY}	Supply Pad for DIG1 LDO (VDIG_1)
VDIG_1	B10	A	V_{DIG1_IN}	Output voltage of one of the DIG LDO's. Connect a ceramic capacitor of 1µF (±20%) or 2.2µF (+100%/-50%)
VDIG2_IN	B9	P	V_{SUPPLY}	Supply Pad for DIG2 LDO (VDIG_2)
VDIG_2	B8	A	V_{DIG2_IN}	Output voltage of one of the DIG LDO's. Connect a ceramic capacitor of 1µF (±20%) or 2.2µF (+100%/-50%)
VDIG34_IN	A9	P	V_{SUPPLY}	Supply Pad for DIG3 and DIG4 LDO (VDIG_3, VDIG_4)
VDIG_3	D8	A	V_{DIG3_IN}	Output voltage of one of the DIG LDO's. Connect a ceramic capacitor of 1µF (±20%) or 2.2µF (+100%/-50%)
VDIG_4	D7	A	V_{DIG4_IN}	Output voltage of one of the DIG LDO's. Connect a ceramic capacitor of 1µF (±20%) or 2.2µF (+100%/-50%)
Charge Pump				
VCP_IN	B7	P	V_{SUPPLY}	Supply Pad for Charge Pump, **always** connect to Supply>3.0V
VCP_N	A6	A	V_{SUPPLY}	HVS charge pump flying capacitor positive side
VCP_P	A7	A		HVS charge pump flying capacitor negative side
VCP_OUT	A8	A		Charge pump output, connect a ceramic capacitor of 2.2µF (+100%/-50%)
VSS_CP	B6	A	V_{SUPPLY}	Ground pad of charge pump
DCDC Step Down Converters				
PGATE1	N1	A	V_{SUPPLY}	Gate output for external PMOS.(DCDC step down controller 1)
VSUPPLY_1	K1	P		Supply Pad for DCDC_Step down converter1, **always** connect to VSUPPLY
LX1	L1	A	V_{SUPPLY}	DC/DC step down converter1 output
FB1	K4	A	V_{SUPPLY}	DC/DC step down converter1 feedback
PGND1	M1	A	V_{SUPPLY}	Power Ground of DCDC step down converter1

*Table 2. Pin list CTBGA124, 8x8MM (*AS3658*)*

Pin Name	Pin Number	Pin Type	Supply	Description
VSUPPLY_2	K2	P		Supply Pad for DCDC_Step down converter2, **always** connect to VSUPPLY
LX2	J1	A	V_{SUPPLY}	DC/DC step down converter2 output
FB2	J7	A	V_{SUPPLY}	DC/DC step down converter2 feedback
PGND2	H2	A	V_{SUPPLY}	Power Ground of DCDC step down converter2
VSUPPLY_3	F1	P		Supply Pad for DCDC_Step down converter3, **always** connect to VSUPPLY
LX3	G1	A	V_{SUPPLY}	DC/DC step down converter3 output
FB3	H6	A	V_{SUPPLY}	DC/DC step down converter3 feedback
PGND3	H1	A	V_{SUPPLY}	Power Ground of DCDC step down converter3
Audio				
VSUPPLY_6	G13	P		Supply for VI2S Regulator
VI2S	A4	P		Supply Pad for I2S Interface, Connect to VDAC Supply
SDI1	B4	I	VI2S	I2S_1 Data input to DAC
SDO1	A5	O	VI2S	I2S_1 Data output from ADC
SCLK1	B3	I/O	VI2S	I2S_1 Shift clock input or output
LRCLK1	A2	I/O	VI2S	I2S_1 Left/Right clock input or output
MCLK1	D9	I/O	VI2S	Master clock input or output for I2S1: DAC (128*Fsdac or 256 *Fsdac)
SDI2	B1	I	VI2S	I2S_2 Data input to DAC
SCLK2	C2	I	VI2S	I2S_2 Shift clock
LRCLK2	D10	I	VI2S	I2S_2 Left/Right clock
MCLK2	D2	I	VI2S	Master clock input for I2S2: DAC (128*Fsdac or 256 *Fsdac)
SDO3(X-)	D5	I/O	VI2S	I2S_3 Data output (if touchpen interface disabled) Touchpen Interface X- Input/Output (if touchpen interface enabled)
SCLK3(X+)	A3	I/O	VI2S	I2S_3 Shift clock output (if touchpen interface disabled) Touchpen Interface X+ Input/Output (if touchpen interface enabled)
LRCLK3(Y-)	E4	I/O	VI2S	I2S_3 Left/Right clock output (if touchpen interface disabled) Touchpen Interface Y- Input/Output (if touchpen interface enabled)
SPDIF(Y+)	F4	I/O	VI2S	SPDIF digital output (if touchpen interface disabled) Touchpen Interface Y+ Input/Output (if touchpen interface enabled)
AGND	K11	A	VDAC	CM voltage bypass capacitor connection (1.45V)
VREF	J11	A	VDAC	VDAC voltage bypass capacitor connection (2.9V)
LINL	F14	A	VDAC	Line input left channel.
LINR	E14	A	VDAC	Line input right channel
GND_SW	L8	O	V_{SUPPLY}	Digital output for controlling the external NMOS

*Table 2. Pin list CTBGA124, 8x8MM (*AS3658*)*

Pin Name	Pin Number	Pin Type	Supply	Description
VDAC	F13	A	VDAC	2.9V Output voltage of one of DAC LDO; Connect a ceramic capacitor of 1µF (±20%) or 2.2µF (+100%/-50%)
HP_CM	B12	A	AVDD	Bypass capacitor connection of common mode voltage of Audio headphone amplifier (AVDD/2)
HP_CM_PWR	D14	A	AVDD	Buffered voltage of HP_CM
LINE_CM	A12	A	ALVDD	Bypass capacitor connection of common mode voltage of Audio line out amplifier (ALVDD/2)
LOUT_L	B11	A	ALVDD	Line out output Left channel
LOUT_R	A11	A	ALVDD	Line out output Right channel
ALVDD	D13	P		Supply pad of Line out amplifier
AVDD	E13	P		Supply pad of headphone amplifier
HPL1	A13	A	AVDD	Headphone output1 left channel
HPR1	C13	A	AVDD	Headphone output1 right channel
HPL2	C14	A	AVDD	Headphone output2 left channel
HPR2	B14	A	AVDD	Headphone output2 right channel
MICN	G11	A	VDAC	Microphone Input N
MICP	H11	A	VDAC	Microphone Input P
MICS	F11	A	V_{SUPPLY}	Microphone Supply (2.95V) / Remote Input
VSS				
BVSS	E11	P	AVDD	Power ground of headphone amplifier
VSSA	G9	VSS		Analog Ground Pad
VSSA	H9	VSS		Analog Ground Pad
VSSA	J8	VSS		Analog Ground Pad
NC/VSS_CP	A1	VSS		Analog Ground Pad
NC/VSSA	P1	VSS		Analog Ground Pad
NC/VSSA	P14	VSS		Analog Ground Pad
NC/BVSS	A14	VSS		Power ground of headphone amplifier

Note: The following are the Pin Types

- **I**: Digital Input Pin
- **IPD**: Digital Input Pin with internal pull-down resistor
- **IPU**: Digital Input Pin with internal pull-up resistor
- **IODPU**: Digital Input / Open Drain Output Pin with internal pull-up resistor
- **O**: Digital Output Pin
- **OD**: Digital Open Drain Output Pin; requires external pull-up resistor
- **IO**: Digital Input / Output Pin
- **A**: Analog Pin
- **P**: Power Pin

5 Absolute Maximum ratings

Stresses beyond those listed in Table 3 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Section 6 Electrical Characteristics on page 13 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Absolute Maximum Ratings

Parameter	Min	Max	Unit	Note
High voltage pins (V_{IN_HV})	-0.3	17.0	V	Applicable for high voltage pins[1]
5V pins (V_{IN_MV})	-0.3	7.0	V	Applicable for pins 5V-pins[2]
3.3V pins (V_{IN_LV})	-0.3	5.0	V	Applicable for 3.3V-Pins[3]
Input pin current (I_{IN})	-25	+25	mA	At 25 ºC, Norm: Jedec 78
Storage Temperature Range (T_{strg})	-55	125	ºC	
Humidity	5	85	%	Noncondens
Electrostatic discharge 1kV (V_{ESD})	-1000	1000	V	Norm: MIL 883 E Method 3015; Setup[4] Applicable for pins: all
Total Power Dissipation		1	W	T_A = 70ºC
		0.72	W	T_A = 84ºC
Package Body Temperature		260	°C	*IPC/JEDEC J-STD-020C, reflects moisture sensitivity level only* The lead finish for Pb-free leaded packages is matte tin (100% Sn).
Solder Profile[5]	235	245	°C	T_{PEAK}
	30	45	s	D_{Well}, above 217 °C
Moisture Sensitive Level	3		1	Represents a max. floor live time of 168h

1. HV pins
   VCHARGER, VGATE, VOFF_B, DCDC_CURR1, DCDC_CURR2, DCDC_CURR3
2. 5V pins are
   V_USB, CH_SENSE_N, CH_SENSE_P, VSUP_SW1, VSUP_SW2, VBAT_SW1, VBAT_SW2, V_BAT, SCL, SDA, XRESET, XINT, VSUPPLY_3, CURR1_GPIO1…CURR4_GPIO4, DCDC_GATE1, DCDC_GATE2, DCDC_SENSE_P1, DCDCSENSE_P2, DCDC_SENSE_N1, DCDC_SENSE_N2, DCDC_FB1, DCDC_FB2, VCL, VCP_OUT, VCP_N, VCP_P, VCP_IN, VCP_IN, VRF1, VREF1_IN, VRF2, VRF23_IN, VRF3, VDIG1, VDIG1_IN, VDIG2, VDIG2_IN, VDIG34_IN, VDIG_3, VDIG_4, PGATE1 VSUPPLY_1, VSUPPLY_2, LX1, LX2, GND_SW, VSUPPLY_4, LINE_CM, HP_CM_PWR, HP_CM, HPLx, HPRx, ALVDD, AVDD, LSP_R, BVSS, LSP_L, AVDD, VSUPPLY_5, VSUPPLY_6
3. 3.3V pins are
   ISENSEP, ISENSEN, ADC_INx, RPROGRAM, V2_5, CREF, ON, VI2S, SDIx, SCLKx, MCLKx, LRCLKx, SDOx, SPDIF, AGND, VREF, LINL,LINR, VDAC, Q32K, XIN32, XOUT32, VBACK, MICS, MICN, MICP
4. The following pins are connected to ESD setup:

   VSUPPLY_1...VSUPPLY_6, VCP_IN, VRF1_IN, VRF2_IN, VCURR connected together
   VDIG1_IN, VDIG2_IN, VDIG34_IN connected together
   AVDD, ALVDD connected together
   VBAT_SW1 and VBAT_SW2 connected together
   VSUP_SW1 and VSUP_SW2 connected together
   All VSS connected together

5. austriamicrosystems strongly recommends to use underfill.

6 Electrical Characteristics

Table 4. Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
Operating Conditions						
VHV	High Voltage	VCHARGER, VGATE, DCDC_CURR1,DCDC_CURR2, DCDC_CURR3	0.0		15.0	V
VBAT, VSUPPLY, VCURR_GPIO	Battery, Supply Voltage	For pins V_BAT, VSUPPLY1-6 (always connect all VSUPPLY1-6 pins together), VSUP_SW1-2, VBAT_SW1-2, VRF1_IN, VRF2_IN, VCP_IN, AVDD, ALVDD	3.0	3.6	5.5	V
V2_5	Voltage on Pin V2_5	Internally generated	2.4	2.5	2.6	V
VCP_OUT	Output Voltage charge pump	Voltage generated by charge pump	4.9	5.2	5.6	V
TAMB	Ambient Temperature		-40	25	85	ºC
ILOWPOWER	Low power mode current consumption	Current consumption in low power mode with step down charger on[1]		7		mA
		With step down charger off[2]		280		µA
IPOWEROFF	Power Off mode current consumption	Current consumption in power off mode[3]		10		µA

1. With register bit low_power_on = 1, only Rf1=3.3V,Vout2=1.2V, Battery 3.6V,Vcharger=6.0V, no additional external loads
2. With register bit low_power_on = 0, All regulators switched off, no additional external loads
3. After setting register bit xon_enable=1 and power_off=1; only V2_5 is active in Power Off mode
4. During startup from the AC/DC adapter, the battery voltage can be below 3.0V

7 Typical Operating Characteristics

see individual block description

8 Detailed Description-Power Management Functions

The power management function consist of the DCDC Step up converters, Current Sink, GPIOs, general purpose 10 bit ADC, backup battery charger, main battery charger and power path management (consisting of the battery switch, external step down/linear charger, USB charger and battery charge controller), step down dc/dc converters, low dropout regulators (LDOs) and 5V charge pump.

8.1 Step Up DC/DC Converters

Figure 3. DC/DC step-up Converter 1

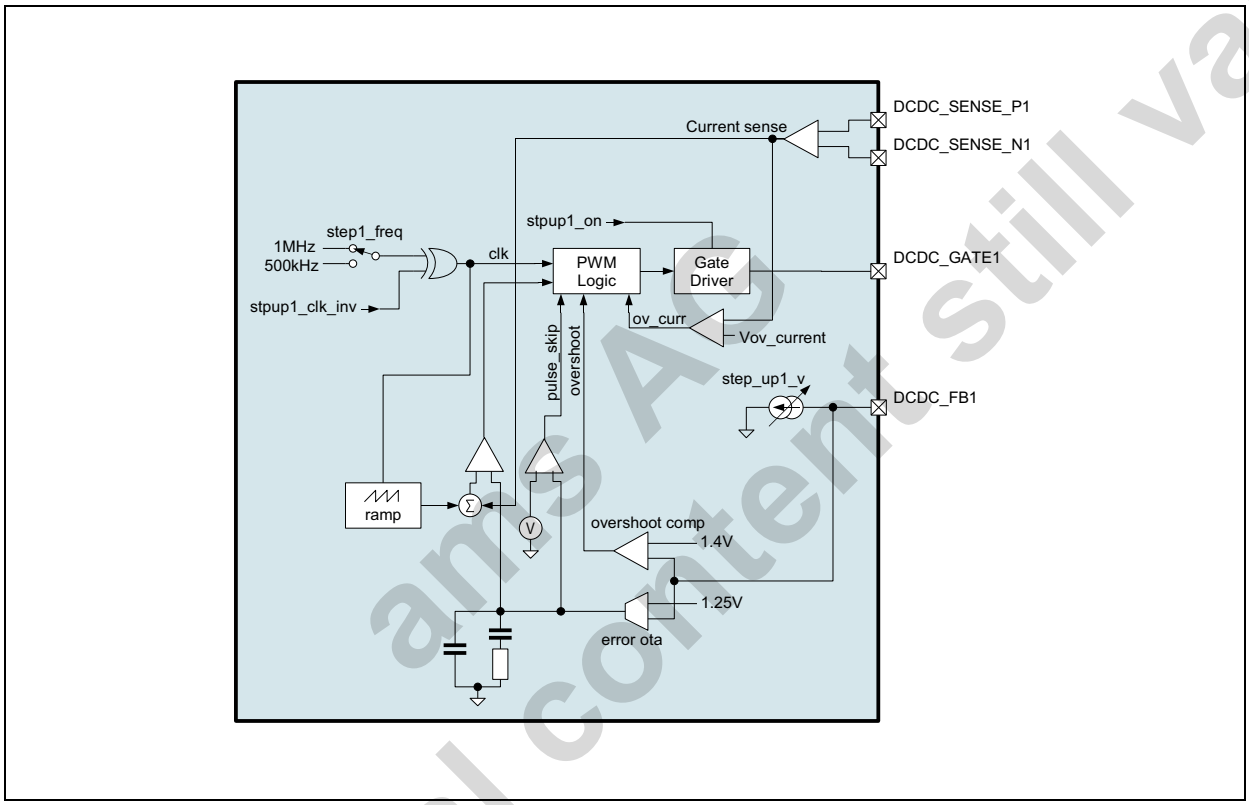


Figure 4. DC/DC step-up Converter 2

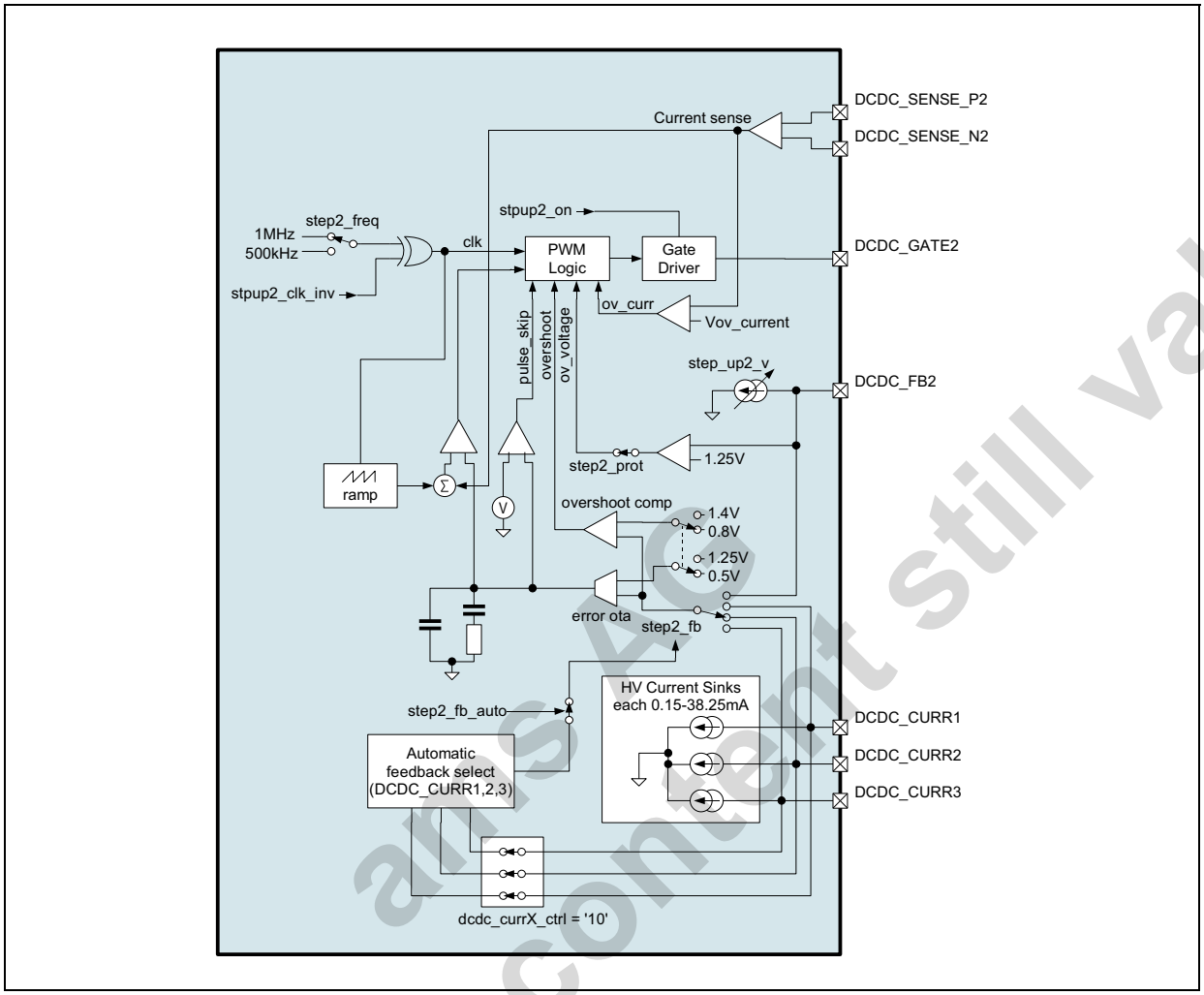


Table 5. DC/DC Converter parameters

Symbol	Parameter	Min	Typ	Max	Unit	Note
I_{VDD}	Quiescent Current		140		µA	Pulse skipping mode
V_{FB1}	Feedback voltage for external resistor divider:	1.20	1.25	1.30	V	for constant voltage control
V_{FB2}	Feedback voltage for current sink regulation		0.5		V	DCDC_CURR1, DCDC_CURR2 or DCDC_CURR3
I_{DCDC_FB}	Additional tuning current at DCDC_FB	0		31	µA	adjustable by software in 1µA steps
	Accuracy of feedback current	-5		5	%	@ full scale
V_{rsense_max}	Current limit voltage at Rsense		100		mV	E.g.: 0.65A for 0.15Ω sense resistor
R_{SW}	switch resistance			1	Ω	ON-resistance of external switching transistor
I_{load}	Load current	0		50	mA	at 15V output voltage
f_{IN}	Switching frequency		$f_{clk\_int}/2$		MHz	internal CLK frequency/2 Programmable: 0.8 to 1.15 MHz

Table 5. DC/DC Converter parameters

Symbol	Parameter	Min	Typ	Max	Unit	Note
C_{out}	Output capacitor		2.2		µF	ceramic, ±20%
L	Inductor		10		µH	Use inductors with small $C_{parasitic}$ (<100pF) to get high efficiency
t_{MIN_ON}	Minimum on time		130		ns	
MDC	Maximum duty cycle		91		%	

The DC/DC Step Up converter is a high efficiency current mode PWM regulator, which provides an output voltage dependent on the maximum VDS voltage of the external transistor, and maximum load current selectable by the external shunt resistor.
For Example:

5V,500mA @ 1.1Mhz

25V,50mA @ 1.1MHz

40V,20mA @ 550kHz

A constant switching frequency results in a low noise on supply and output voltage.

8.1.1 Feedback selection

For step up DCDC 1, the feedback is always DCDC_FB1.

For step up DCDC 2 following feedback selections are possible:

Stpup2_fb selects the type of feedback for the DCDC_step_up2 converter:

DCDC_CURR1, DCDC_CURR2, DCDC_CURR3 or DCDC_FB2 feedback (see Figure 5)

Setting stpup2_fb to 00b enables the feedback on DCDC_FB2, stpup2_fb to 01b enables feedback at pin DCDC_CURR1, setting step_up_fb to 10b enables feedback at pin DCDC_CURR2 and setting step_up_fb to 11b enables feedback at pin DCDC_CURR3. The Step-up converter is regulated such that the required current at the feedback path can be supported.

Always choose the path with the higher voltage drop as feedback to guarantee adequate supply for the other, unregulated path.

To protect the DCDC output voltage against overvoltage, if a LED string is broken, set stpup2_prot=1. In this mode the output voltage will be limited by limiting the DCDC_FB voltage to 1.25V (select the external resistor network to adjust this limitation voltage).

Figure 5. DC/DC step up 2 converter with regulation of LED string on pin DCDC_CURR1,2 or 3

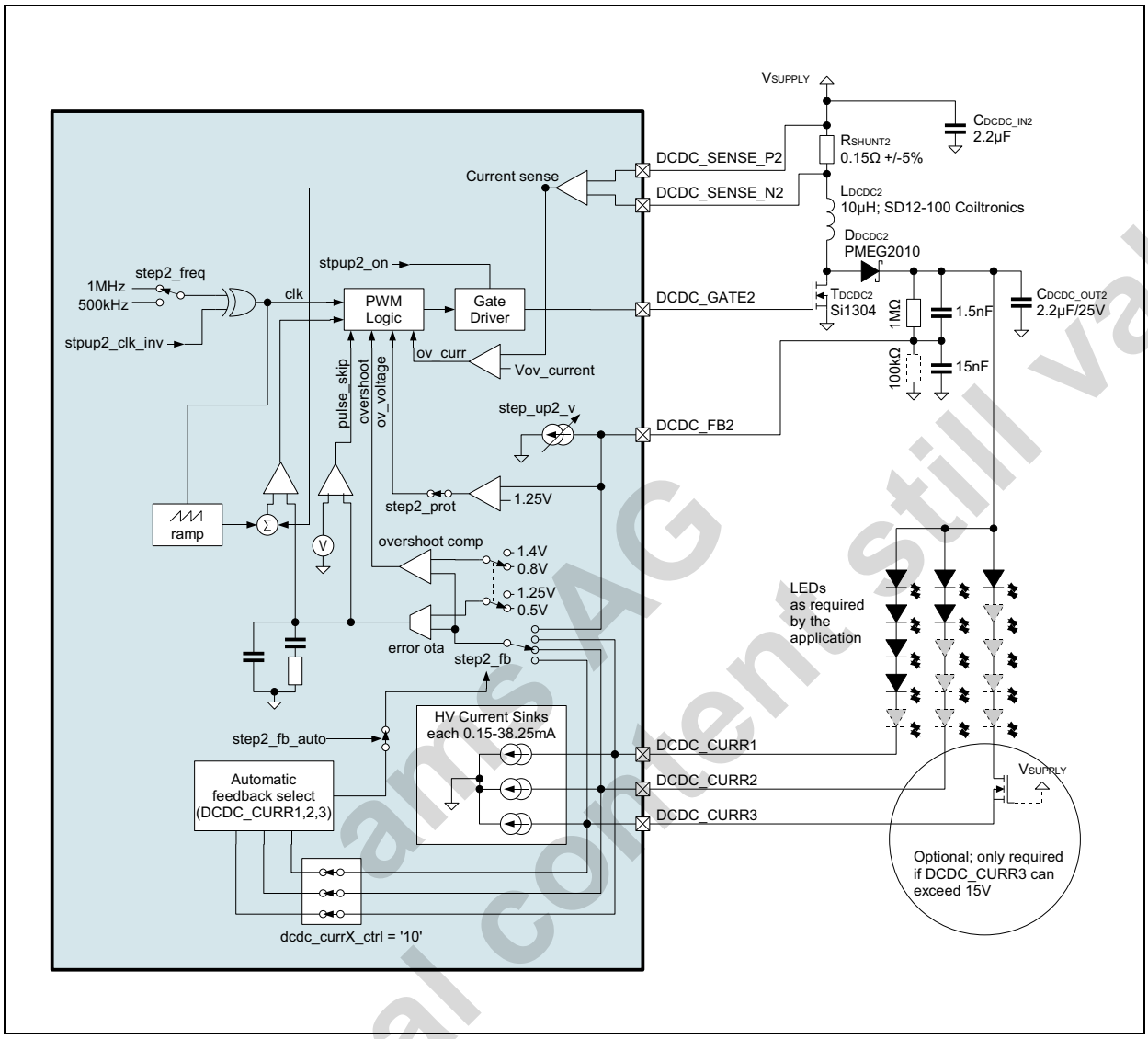
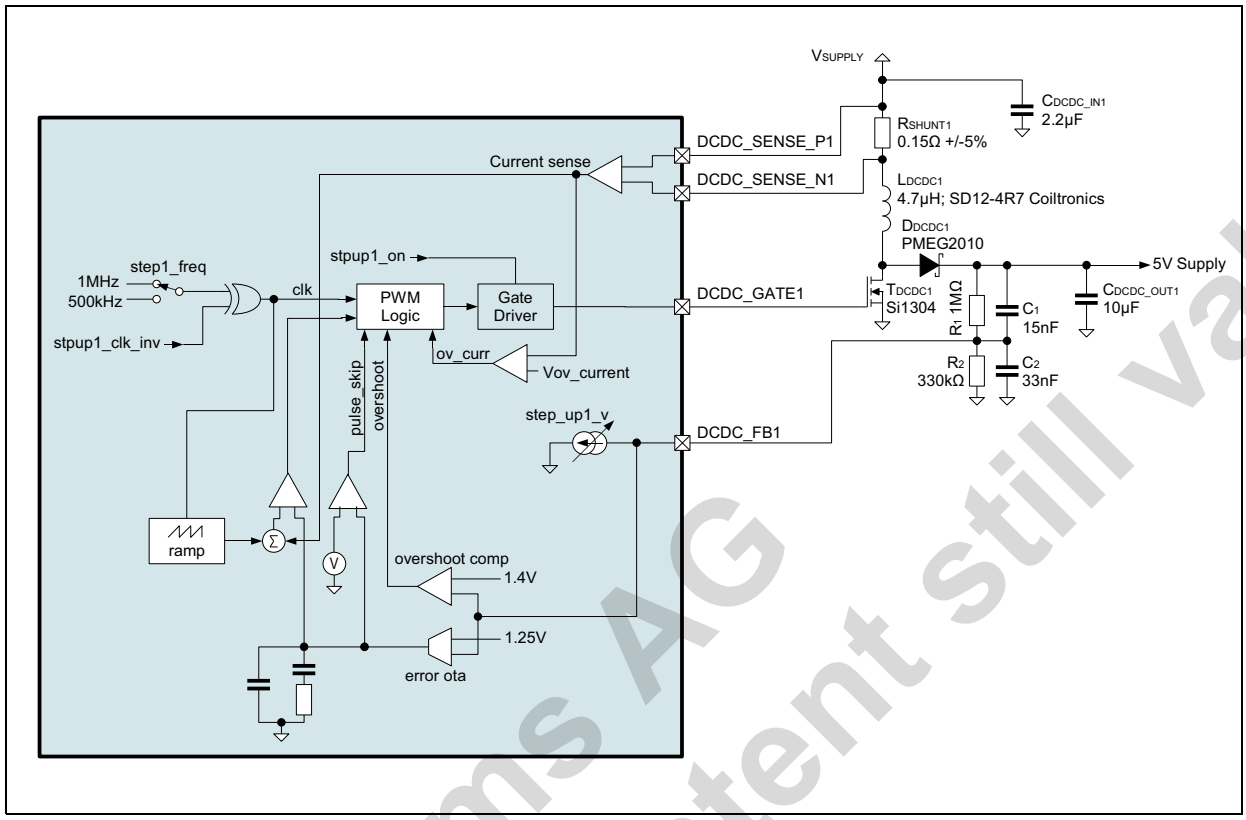


Figure 6. DC/DC step up 1 converter with regulated output voltage of 5V. Feedback is at pin DCDC_FB1



Voltage Feedback: (see Figure 6)

For Step UP DCDC 1 voltage feedback is always selected on pin DCDC_FB1. For Step-up UP DCDC 2 set step2_fb to 00 to enable voltage feedback at pin DCDC_FB2.

Bit stepX_res (X = 1 or 2) should be set to 1 in voltage feedback mode using two resistors.

The output voltage is regulated to a constant value, given by:

$$V_{stepup\_out} = \frac{R_1 + R_2}{R_2} 1.25 + I_{I_{DCDC\_FB}} \bullet R_1$$

If R2 is not used, the output voltage is:

$$V_{stepup\_out} = 1.25 + I_{I_{DCDC\_FB}} \bullet R_1$$

V_{stepup_out}: Step up regulator output voltage

R_1 Feedback resistor R1

R_2 Feedback resistor R2

$I_{Vturning}$: Tuning current on DCDC_FB pin: stpupX_v (0µA to 15µA (1µA steps)) (X= 1 or 2)

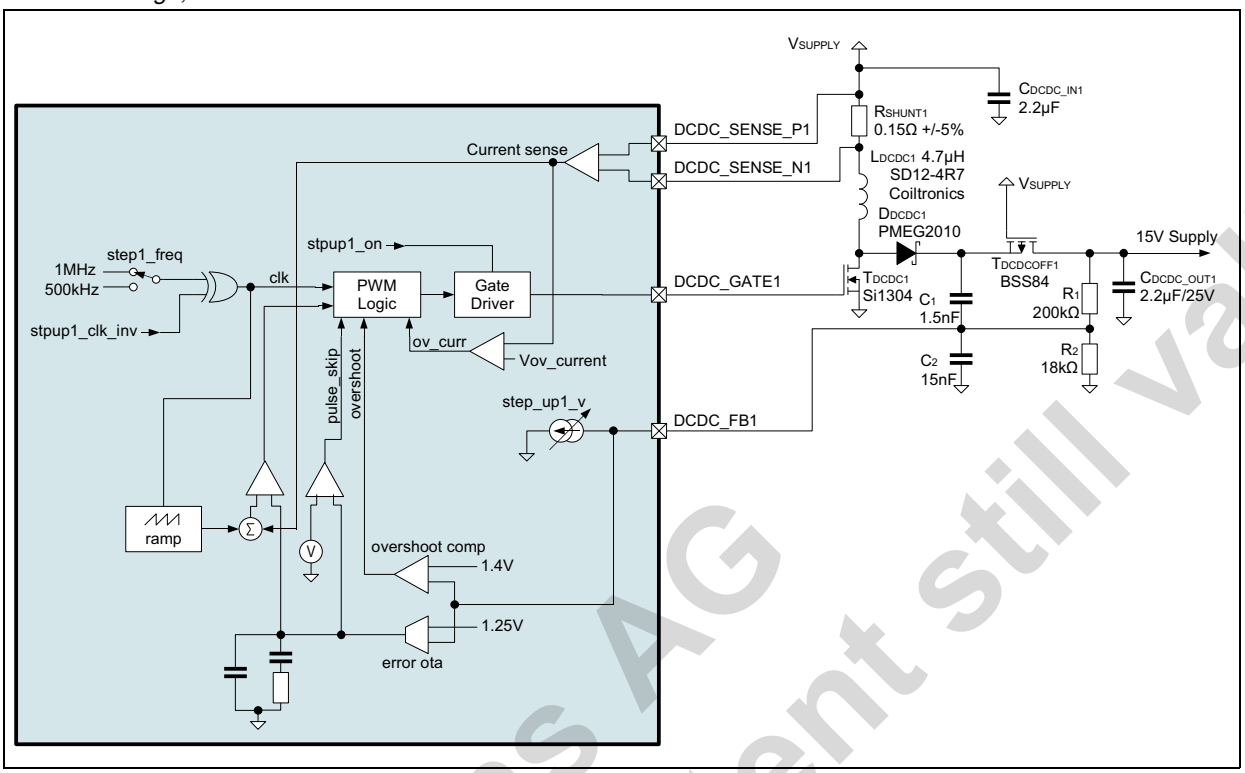
Example:

Table 6. Step Up Output Voltage (Voltage mode or protection voltage)

$I_{vtuning}$	V_{stepup_out}	V_{stepup_out}
µA	**R1=1M Ω,R2 not used**	**R1=500k Ω,R2=64k Ω**
0	-	11
1	-	11.5
2	-	12
3	-	12.5
4	-	13
5	6.25	13.5
6	7.25	14
7	8.25	14.5
8	9.25	15
9	10.25	15.5
10	11.25	16
11	12.25	16.5
12	13.25	17
13	14.25	17.5
14	15.25	18
15	16.25	18.5

Note: The voltage on pin DCDC_CURR1, DCDC_CURR2 and DCDC_CURR3 must never exceed 15V

Figure 7. DC/DC step up converter 1 with regulated output voltage (15V), and switch off function of output voltage, to reduce shutdown current



As the output voltage is always on, an additional output transistor can be added to reduce shutdown current through R1, R2 and the connected output circuit.

Note: A similar circuit can be used for step up converter 2.

8.1.2 StepUp1 Load Detection and Overcurrent Protection Circuit

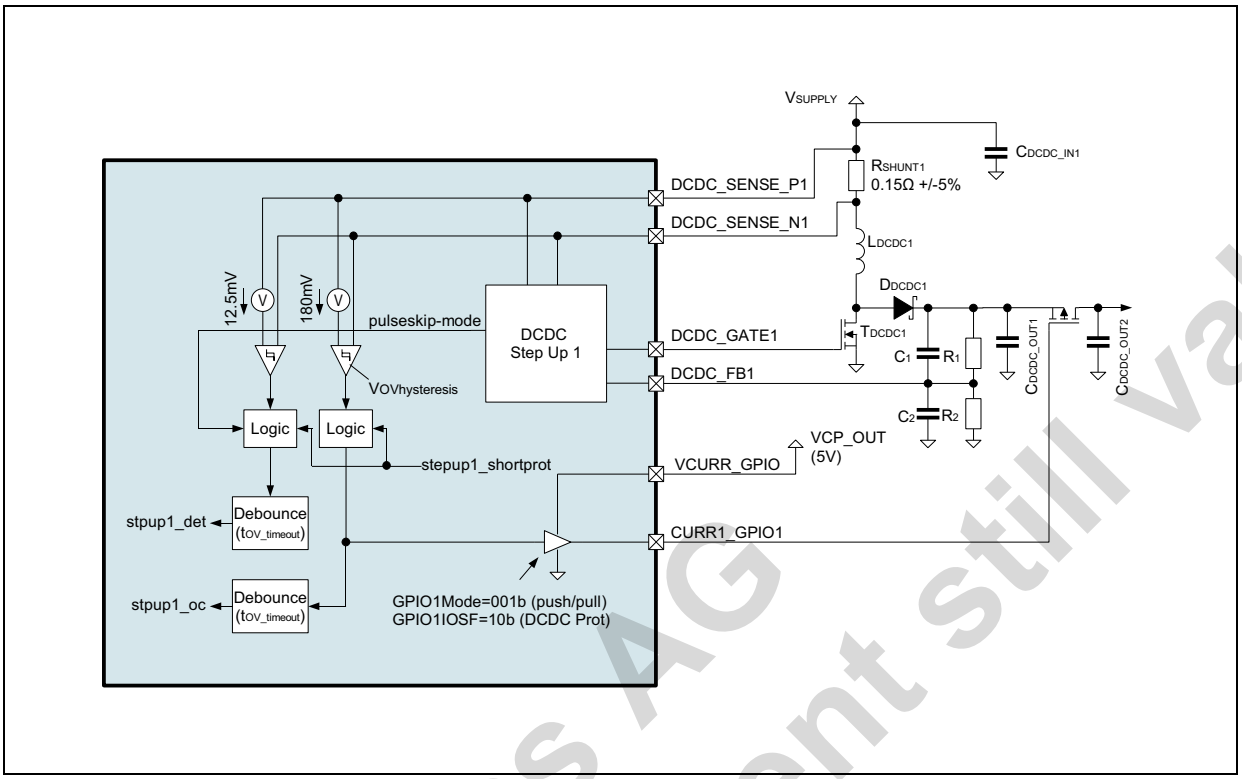
This circuit protects the DCDC step up1 converter during short circuit and startup, by regulation of the output current. An additional feature is the detection of a minimum output load of the Step-up converter. It is also possible to use this circuit without the DCDC step up converter, by using the sense resistor only:

- Detection circuit: If the voltage on R_{sense} exceeds V_{DETECT} for more than 1msecond, or the DCDC Step up converter is not in Pulseskip for more than 1 millisecond, the stepup1_det bit will be set.
- Overcurrent protection: If the Overcurrent voltage $V_{OVCURRENT}$ has been exceeded by more than 5 msec the Bit stpup1_oc will be set and can only reset, by switching off and on the Protection circuit by writing Stpup1_shortprot 0 – 1. If stepup1_oc is set the load will be disconnected, if Stpup1_oc_timeout=1

Table 7. StepUp1 protection/detection circuit parameters

Symbol	Parameter	Min	Typ	Max	Unit	Note
VDETECT	Detection Threshold	2	12.5	25	mV	For Rsense=0.150Ω => 83mA typ.
VOVCURRENT	Overcurrent Threshold rising	150	180	215	mV	For Rsense=0.150Ω => 1.2A typ.
VOVhysteresis	Overcurrent Hysteresis		50		mV	
tOV_timeout	Overcurrent timeout		5		ms	Interrupt and/or external PMOS switching off after timeout f_{clk_int} = 2.2MHz
tdetect	Detection denounce time		1		ms	f_{clk_int} = 2.2MHz

Figure 8. StepUp 1 Load Detection and Overcurrent Protection Application Circuit



8.1.3 Step Up DCDC Converter Registers

Table 8. Step Up DC/DC Bit definitions

Addr: 30		Step Up DC/DC control		
		This register controls the different modes of the step up DCDC converter		
Bit	**Bit Name**	**Default**	**Access**	**Description**
5	stpup1_on	ROM	R/W	On/Off control of the step up dc/dc converter1
6	stpup2_on	ROM	R/W	On/Off control of the step up dc/dc converter2

Table 9. Step Up DC/DC Bit definitions

Addr: 32		Step Up DC/DC control			
		This register controls the different modes of the step up DCDC converter			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
0	stpup2_clkinv	00h	R/W	Invert input clock of step up2 converter	
				0	Use positive edge of internal clk
				1	Use negative edge of internal clk
1	stpup1_freq	00h	R/W	Defines the clock frequency of the step up1 dc/dc converter; 0 f_{clk_int}/2 (0.8 to 1.15 MHz) 1 f_{clk_int}/4 (0.4 to 0.575 MHz)	
2	-	00h	n/a	Always set to 0	
3	stpup1_res	00h	R/W	Gain selection for DCDC step_up1:	
				0	Select 0 if DCDC is used with current feedback (DCDC_CURR1,DCDC_CURR2,DCDC_CURR3) or if DCDC_FB is used with current feedback only (Only R1,C1 connected; (see Figure 6))
				1	Select 1 if DCDC_FB1 or DCDC_FB2 is used with external resistor divider (2 resistors)
4	stpup2_fb_auto	00h	RW	0	step_up_fb select the feedback of the DCDC converter
				1	The feedback is automatically chosen within the current sinks DCDC_CURR1,DCDC_ CURR2 and DCDC_CURR3 (never DCDC_FB). Only those are used for this selection, which are enabled and connected to the step up converter (currX_ctrl must be 10)
5	stpup2_freq	00h	R/W	Defines the clock frequency of the step up2 dc/dc converter	
				0	f_{clk_int}/2 (0.8 to 1.15 MHz)
				1	f_{clk_int}/4 (0.4 to 0.575 MHz)
6	-	00h	n/a		Always set to 0
7	stpup2_res	00h	R/W	Gain selection for DCDC step_up2:	
				0	Select 0 if DCDC is used with current feedback (DCDC_CURR1,DCDC_CURR2,DCDC_CURR3) or if DCDC_FB is used with current feedback only (Only R1,C1 connected; (see Figure 6))
				1	Select 1 if DCDC_FB1 or DCDC_FB2 is used with external resistor divider (2 resistors)

Table 10. Step Up DC/DC Bit definitions

Addr: 33		Step Up1 DC/DC control This register controls the different modes of the step up1 DCDC converter			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
4:0	stpup1_v	00h	R/W	Defines the tuning current at DCDC_fb1 pin;	
				00000	0 µA
				00001	1 µA
				.....	
				11111	31 µA
5	stpup1_clkinv	00h	R/W	Invert input clock of step up1 converter;	
				0	Use positive edge of internal clk
				1	Use negative edge of internal clk
6	stpup1_shortprot	00h	RW	Enables Protection and Detection circuit for DCDC step up1	
				0	No protection and load detection
				1	Short protection and load detection enabled
7	stpup1_oc_timeout	00h	RW	Controls GPIO1 switch off, after overcurrent timeout (5ms) for DCDC step up1	
				0	disabled
				1	enabled

Table 11. Step Up DC/DC Bit definitions

Addr: 34		Step Up2 DC/DC control This register controls the different modes of the step up2 DCDC converter			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
4:0	stpup2_v	00h	R/W	Defines the tuning current at DCDC_fb2 pin;	
				00000	0 µA
				00001	1 µA
				.....	
				11111	31 µA
6:5	stpup2_fb	00h	R/W	Controls the feedback source	
				00	DCDC_FB enabled (external resistor divider)
				01	DCDC_CURR1 feedback enabled (feedback through white LEDs)
				10	DCDC_CURR2 feedback enabled (feedback through white LEDs)
				11	DCDC_CURR3 feedback enabled (feedback through white LEDs)

Table 11. Step Up DC/DC Bit definitions

Addr: 34		Step Up2 DC/DC control			
		This register controls the different modes of the step up2 DCDC converter			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
7	stpup2_prot	00h	RW	DCDC converter 2 overvoltage protection to prevent damage of external NFET, if DCDC_CURR1 or DCDC_CURR2 or DCDC_CURR3 feedback selected, and no LED string connected:	
				0	Overvoltage protection disabled
				1	Switch off DCDC step up 2 if the voltage on DCDC_FB2 exceeds 1.25V

Table 12. stpup1_det and stpup1_oc Bit definitions

Addr: 53		Low voltage status bit definitions			
		This register shows the status of the overcurrent protection of the stepup1dcdc			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
6	stpup1_oc	NA	R	Step up overcurrent status bit	
				0	$V_{Rsense} < V_{OVCURRENT}$
				1	$V_{Rsense} > V_{OVCURRENT}$ for more than 5 msec (latched state)
7	stpup1_det	NA	R	Step up detection status register	
				0	$V_{Rsense} < V_{DETECT}$ for more than 1msecond, and DCDC Step up converter is in Pulseskip for more than 1 millisecond
				1	$V_{Rsense} > V_{DETECT}$ for more than 1msecond, or the DCDC Step up converter is not in Pulseskip for more than 1 millisecond

8.2 Current Sinks

These are general-purpose current sinks intended to control the backlight(s), buzzer and vibrator. The low voltage current sink has an integrated protection against over voltage and can therefore also drive inductive loads ($V_{PROTECT}$). DCDC_CURR1 and DCDC_CURR2, DCDC_CURR3 are high voltage (15V) current sinks, e.g. for series of white LEDs

CURR1_GPIO, CURR2_GPIO, CURR3_GPIO, CURR4_GPIO are four 5V, 38.25mA current sinks, e.g. for buzzer, vibrator, LEDs

CURR1_GPIO, CURR2_GPIO, CURR3_GPIO, CURR4_GPIO can be used as general propose Input/Output (GPIO) functions optional (described in section General Purpose Input / Output (CURR1_GPIO1 … CURR4_GPIO4)).

8.2.1 High voltage Current Sinks (DCDC_CURR1, DCDC_CURR2 and DCDC_CURR3)

Current sinks DCDC_CURR3, DCDC_CURR1 and DCDC_CURR2 can be controlled individually. The step-up DCDC converter may supply them with voltages up to 15V. If any of these current sinks is used, connected VCURR_GPIO to a supply with at least 3.0V.

Table 13. Current Sinks Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Note
$I_{DCDC\_Curr1,2,3}$	DCDC_CURR1,2 and DCDC_CURR3 current, 00h-3Fh	0		38.25	mA	For V(DCDC_CURRx) > 0.45V resolution = 0.15mA
$I_{DCDC\_protect}$	Current sink protection Current		2		µA	Protection Current if stpup2_on=1 and dcdc_currx_current=00h
Δ	absolute Accuracy	-5		+5	%	All Current sinks
V_{DCDC_CURR1}, V_{DCDC_CURR2}, V_{DCDC_CURR3}	Voltage compliance	0.45		15	V	during normal operation

Table 14. DCDC_CURR1 Current sink current bit definition

Addr: 39		DCDC_CURR1 Value			
		This register controls the current value of the dcdc_curr1 current sink			
Bit	Bit Name	Default	Access	Description	
7:0	dcdc_curr1_current	00h	R/W	Defines the current into DCDC_CURR1 if enabled by dcdc_curr1_ctrl	
				00h	power down (default state)
				01h	0.15mA (LSB)
				....	
				FFh	38.25mA

Table 15. DCDC_CURR2 Current sink current bit definition

Addr: 40		DCDC_CURR2 Value			
		This register controls the current value of the dcdc_curr2 current sink			
Bit	Bit Name	Default	Access	Description	
7:0	dcdc_curr2_current	00h	R/W	Defines the current into DCDC_CURR2 if enabled by dcdc_curr2_ctrl	
				00h	power down (default state)
				01h	0.15mA (LSB)
				....	
				FFh	38.25mA

Table 16. DCDC_CURR3 Current sink current bit definition

Addr: 45		DCDC_CURR3 Value			
		This register controls the current value of the dcdc_curr3 current sink			
Bit	Bit Name	Default	Access	Description	
7:0	dcdc_curr3_current	00h	R/W	Defines the current into DCDC_CURR3 if enabled by dcdc_curr3_ctrl	
				00h	power down (default state)
				01h	0.15mA (LSB)
				....	
				FFh	38.25mA

Table 17. Current sink control bit definition

Addr: 58		CURR control			
		This register controls the mode of the DCDC current sinks			
Bit	Bit Name	Default	Access	Description	
1:0	dcdc_curr1_ctrl	00b	R/W	On/Off control of the pad DCDC_CURR1	
				00	Current sink is turned off
				01	Current sink is active
				10	Current sink is active and LED string connected to stpup2. Required for automatic feedback selection
				11	Controlled by PWM generator (do not set pwm_div)
3:2	dcdc_curr2_ctrl	00b	R/W	On/Off control of the pad DCDC_CURR2	
				00	Current sink is turned off
				01	Current sink is active
				10	Current sink is active and LED string connected to stpup2. Required for automatic feedback selection
				11	Controlled by PWM generator (do not set pwm_div)
5:4	dcdc_curr3_ctrl	00b	R/W		On/Off control of the pad DCDC_CURR3
				00	Current sink is turned off
				01	Current sink is active
				10	Current sink is active and LED string connected to stpup2. Required for automatic feedback selection
				11	Controlled by PWM generator (do not set pwm_div)

8.2.2 Low voltage Current Sink (CURR1_GPIO1 … CURR4_GPIO4)

CURR1_GPIO1 … CURR4_GPIO4 can be controlled individually. Each one can sink up to 38.25mA. The voltage on the current sinks must not exceed the supply VCURR_GPIO (can be connected e.g. to VSUPPLY).

The low voltage current sinks and the gpio pins share the same pins (see General Purpose Input / Output (CURR1_GPIO1 … CURR4_GPIO4) on page 30) for enabling/disabling of the current sinks / gpio functions.

Table 18. Current Sinks Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Note
$I_{CURR1,2,3,4}$	CURR1_GPIO1.... CURR4_GPIO4 current, 00h-1Fh	0		38.25	mA	For V(CURRx_GPIOx) > 0.2V resolution = 0.15mA, each current sink
Δ	absolute Accuracy	-5		+5	%	All Current sinks
$V_{Curr1,2,3,4}$	Voltage compliance	0.2		V(VCURR)	V	during normal operation

Table 19. CURR1 Current sink current Bit definition

Addr: 41		CURR1 control			
		This register controls the mode of the curr1 current sinks			
Bit	Bit Name	Default	Access	Description	
7:0	curr1_current	(00)h	R/W	Defines the current into CURR1_GPIO1 if GPIO1_Mode = 011b and output enabled (e.g. GPIO1=1)	
				00h	power down (default state)
				01h	0.15mA (LSB)
				....	
				FFh	38.25mA

Table 20. CURR2 Current sink current Bit definition

Addr: 42		CURR2 control			
		This register controls the mode of the curr2 current sinks			
Bit	Bit Name	Default	Access	Description	
7:0	curr2_current	(00)h	R/W	Defines the current into CURR2_GPIO2 if GPIO2_Mode = 011b and output enabled (e.g. GPIO2=1)	
				00h	power down (default state)
				01h	0.15mA (LSB)
				....	
				FFh	38.25mA

Table 21. CURR3 Current sink current Bit definition

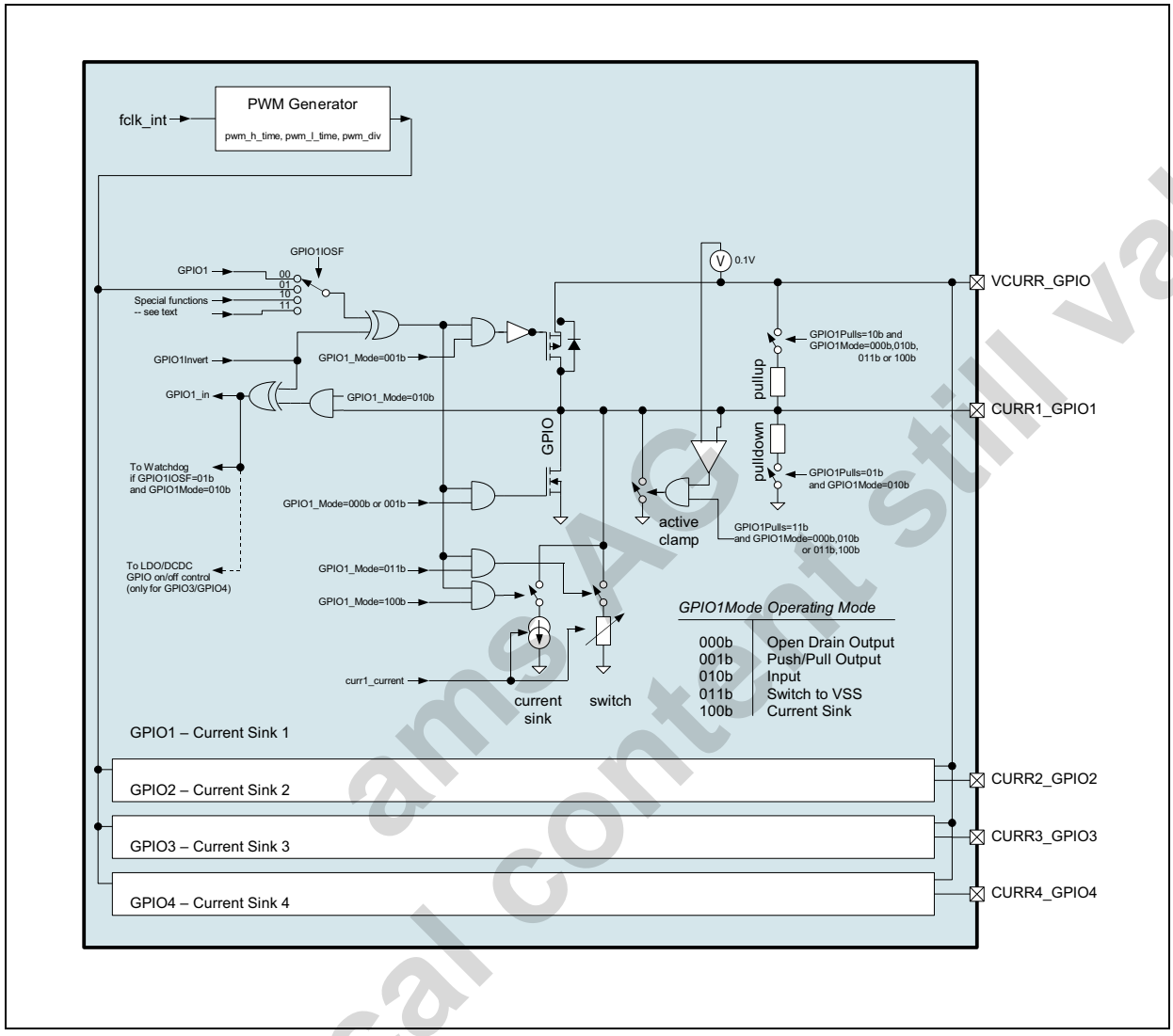
Addr: 43		CURR3 control			
		This register controls the mode of the curr3 current sinks			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
7:0	curr3_current	(00)h	R/W	Defines the current into CURR3_GPIO3 if GPIO3_Mode = 011b and output enabled (e.g. GPIO3=1)	
				00h	power down (default state)
				01h	0.15mA (LSB)
				....	
				FFh	38.25mA

Table 22. CURR4 Current sink current Bit definition

Addr: 44		CURR4 control			
		This register controls the mode of the curr4 current sinks			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
7:0	curr4_current	(00)h	R/W	Defines the current into CURR4_GPIO3 if GPIO4_Mode = 011b and output enabled (e.g. GPIO4=1)	
				00h	power down (default state)
				01h	0.15mA (LSB)
				....	
				FFh	38.25mA

8.3 General Purpose Input / Output (CURR1_GPIO1 … CURR4_GPIO4)

Figure 9. CURR1_GPIO1 … CURR4_GPIO4 block diagram



The device contains 4 high current GPIO pins, which share the same pins as the low voltage current sinks and are capable of sinking 100mA from VCURR_GPIO voltage. Each of the pins can be configured as open drain NMOS or push-pull output with VCURR_GPIO high levels, as high impedance output or as digital input. When configured as output the output source can be a register bit, or the PWM generator, furthermore the output signal can be inverted. Integrated active clamp circuits can be enabled for the open drain NMOS output mode by setting *GPIOxPulls*=11b, thus allowing to use the high current GPIO pins for driving inductive loads. A pull-up resistor to VCURR_GPIO can be enabled for the open drain NMOS output mode by setting *GPIOxPulls*=10b. When configured as digital input the logic level (*GPIOxInvert*='0') or the inverted logic level (*GPIOxInvert*='1') of the pin is reflected by bit *GPIOxBit* in the *GPIO Bit* register.

Moreover, a special function can be selected for each digital input pin and a pull-up resistor to VCURR_GPIO or a pull-down resistor can be enabled.

Table 23. High Current GPIO Pin Characteristics (VCURR1_GPIO1 … VCURR4_GPIO4)

$V_{VSUPPLY}$=3.0 to 5.5V; T_{amb}= –20 to +70°C; unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Unit	Note
$V_{GPIOMAX}$	Maximum voltage on CURR1...4_GPIO 1…4 pins			V_{CURR_GPIO}+ 0.3	V	Pin VCURR_GPIO is used as supply for the GPIO pins
V_{OLH}	Low level output voltage switch mode	–0.3		+0.35	V	I_{OL}=+100mA; digital output (GPIOxMode=100b and currX_current=3Fh)
V_{OL}	Low level output voltage	–0.3		+0.4	V	I_{OL}=+1mA; digital output (GPIOxMode=000b ... 010b)
V_{OH}	High level output voltage	0.8·V_{CURR_GPIO}.		V_{CURR_GPIO}	V	I_{OH}=–1mA; digital push-pull output
V_{IL}	Low level input voltage	–0.3		0.4	V	digital input
V_{IH}	High level input voltage	1.3		V_{CURR_GPIO}	V	digital input
$I_{LEAKAGE}$	Leakage current			10	µA	high impedance
$R_{pull-up}$	Pull-up resistance		78		kΩ	*GPIOxMode*=x0b; *GPIOxPulls*=10b; VCURR_GPIO=3.6V
$R_{pull-down}$	Pull-down resistance		161		kΩ	digital input; *GPIOxPulls*=01b; VCURR_GPIO=3.6V

Table 24. CURR1_GPIO1 Bit definition

Addr: 18		GPIO1			
		This register controls the mode of the CURR1_GPIO1 Pin			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
2…0	GPIO1Mode	ROM	R/W	000b	digital open drain NMOS output (only NMOS enabled)
				001b	digital push-pull output (NMOS & PMOS enabled, no PWM out possible)
				010b	digital input (NMOS & PMOS disabled, digital input logic enabled)
				011b	digital open drain current sink operation Current defined by curr1_current
				100b	digital open drain switch operation On resistance defined by curr1_current
				101b to 111b	high impedance (or SD1 in DCDC step down external controller mode (sd1_1A_mode = 1100b)).NMOS & PMOS disabled, digital input logic disabled)

Table 24. CURR1_GPIO1 Bit definition

Addr: 18		GPIO1			
		This register controls the mode of the CURR1_GPIO1 Pin			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
4…3	GPIO1IOSF	ROM	R/W	00b	input / output signal is written to or set by *GPIO1Bit* in the *GPIO Bit* register
				01b	PWM (O) / WDOG (I) if used for PWM, pwm_h_time and pwm_l_time define the high and low time of this output and only allowed for *GPIO1Mode*=011b,100b
				10b	Protection of DCDC stepUp1 GPIO 1 (O)
				11b	Battery charging EOC indication output GPIO 1 (O) If EOC=1 then GPIO1=1. DCDC_CURR3 is used as output, if CURR_GPIO1 is used for external DCDC controller
5	GPIO1Invert	ROM	R/W	0	normal polarity of input / output signal
				1	inverted polarity of input / output signal (not possible for PWM out)
7…6	GPIO1Pulls	ROM	R/W	00b	no pull-up or pull-down resistor is enabled in all modes
				01b	pull-down resistor is enabled in digital input mode (clamp disabled)
				10b	pull-up resistor is enabled for *GPIO1Mode*=000b,010b,011b,100b (clamp disabled)
				11b	enable active clamp circuit for *GPIO1Mode*=000b,010b,011b,100b (pull-up/down disabled)

Table 25. CURR2_GPIO2 Bit definition

Addr: 19		GPIO2			
		This register controls the mode of the CURR1_GPIO2 Pin			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
2…0	GPIO2Mode	ROM	R/W	000b	digital open drain NMOS output
				001b	digital push-pull output (no PWM out possible)
				010b	digital input
				011b	digital open drain current sink operation Current defined by curr2_current
				100b	digital open drain switch operation On resistance defined by curr2_current
				101b to 111b	high impedance

Table 25. CURR2_GPIO2 Bit definition

Addr: 19		GPIO2			
		This register controls the mode of the CURR1_GPIO2 Pin			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
4…3	GPIO2IOSF	ROM	R/W	00b	input / output signal is written to or set by *GPIO2Bit* in the *GPIO Bit* register
				01b	PWM (O) / WDOG (I) if used for PWM, pwm_h_time and pwm_l_time define the high and low time of this output and only allowed for *GPIO2Mode*=011b,100b
				10b	Battery charging active indication output GPIO2 (O) If Battery charging = 1 then GPIO2=1
				11b	NA
5	GPIO2Invert	ROM	R/W	0	normal polarity of input / output signal
				1	inverted polarity of input / output signal (not possible for PWM out)
7…6	GPIO2Pulls	ROM	R/W	00b	no pull-up or pull-down resistor is enabled in all modes
				01b	pull-down resistor is enabled in digital input mode (clamp disabled)
				10b	pull-up resistor is enabled for *GPIO2Mode*=000b,010b,011b,100b (clamp disabled)
				11b	enable active clamp circuit for *GPIO2Mode*=000b,010b,011b,100b (pull-up/down disabled)

Table 26. CURR3_GPIO3 Bit definition

Addr: 20		GPIO3			
		This register controls the mode of the CURR3_GPIO3 Pin			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
2…0	GPIO3Mode	ROM	R/W	000b	digital open drain NMOS output
				001b	digital push-pull output (no PWM out possible)
				010b	digital input
				011b	digital open drain current sink operation Current defined by curr3_current
				100b	digital open drain switch operation On resistance defined by curr3_current
				101b to 111b	high impedance
4…3	GPIO3IOSF	ROM	R/W	00b	input / output signal is written to or set by *GPIO3Bit* in the *GPIO Bit* register
				01b	PWM (O) / WDOG (I) if used for PWM, pwm_h_time and pwm_l_time define the high and low time of this output and only allowed for *GPIO2Mode*=011b,100b
				10b	GPIO3 control of regulators if regX_gpio = 1 and regX_on = 1
				11b	Touchpen ADC wait input

Table 26. CURR3_GPIO3 Bit definition

Addr: 20		GPIO3			
		This register controls the mode of the CURR3_GPIO3 Pin			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
5	GPIO3Invert	ROM	R/W	0	normal polarity of input / output signal
				1	inverted polarity of input / output signal (not possible for PWM out)
7…6	GPIO3Pulls	ROM	R/W	00b	no pull-up or pull-down resistor is enabled in all modes
				01b	pull-down resistor is enabled in digital input mode (clamp disabled)
				10b	pull-up resistor is enabled for *GPIO3Mode*=000b,010b,011b,100b (clamp disabled)
				11b	enable active clamp circuit for *GPIO3Mode*=000b,010b,011b,100b (pull-up/down disabled)

Table 27. CURR4_GPIO4 Bit definition

Addr: 21		GPIO4			
		This register controls the mode of the CURR4_GPIO4 Pin			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
2…0	GPIO4Mode	ROM	R/W	000b	digital open drain NMOS output
				001b	digital push-pull output (no PWM out possible)
				010b	digital input
				011b	digital open drain current sink operation Current defined by curr4_current
				100b	digital open drain switch operation On resistance defined by curr4_current
				101b to 111b	high impedance
4…3	GPIO4IOSF	ROM	R/W	00b	input / output signal is written to or set by *GPIO4Bit* in the *GPIO Bit* register
				01b	PWM (O) / WDOG (I) if used for PWM, pwm_h_time and pwm_l_time define the high and low time of this output and only allowed for *GPIO4Mode*=011b,100b
				10b	GPIO4 control of regulators if regX_gpio = 1 and regX_on = 0
				11b	Touchpen dedicated interrupt output
5	GPIO4Invert	ROM	R/W	0	normal polarity of input / output signal
				1	inverted polarity of input / output signal (not possible for PWM out)

Table 27. CURR4_GPIO4 Bit definition

Addr: 21		GPIO4			
		This register controls the mode of the CURR4_GPIO4 Pin			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
7…6	GPIO4Pulls	ROM	R/W	00b	no pull-up or pull-down resistor is enabled in all modes
				01b	pull-down resistor is enabled in digital input mode (clamp disabled)
				10b	pull-up resistor is enabled for *GPIO4Mode*=000b,010b,011b,100b (clamp disabled)
				11b	enable active clamp circuit for *GPIO4Mode*=000b,010b,011b,100b (pull-up/down disabled)

Table 28. GPIO Signal Bit definition

Addr: 55		GPIO Signal		
		This register controls the GPIO state / status		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	GPIO1	0	R/W	This bit determines the output signal of the GPIO1 pin when selected as output source
1	GPIO2	0	R/W	This bit determines the output signal of the GPIO2 pin when selected as output source
2	GPIO3	0	R/W	This bit determines the output signal of the GPIO3 pin when selected as output source
3	GPIO4	0	R/W	This bit determines the output signal of the GPIO4 pin when selected as output source
4	GPIO1_in	NA	R	This bit reflects the logic level of the GPIO1 pin when configured as digital input pin
5	GPIO2_in	NA	R	This bit reflects the logic level of the GPIO2 pin when configured as digital input pin
6	GPIO3_in	NA	R	This bit reflects the logic level of the GPIO3 pin when configured as digital input pin
7	GPIO4_in	NA	R	This bit reflects the logic level of the GPIO4 pin when configured as digital input pin

The gpio block includes an internal programmable PWM generator (can be connected to any of the GPIO1_CURR1 … GPIO4_CURR4 outputs). Its timing is defined by the following tables:

Table 29. PWM Frequency Control High Time Registers

Addr: 56		PWM Frequency Control High Time Registers			
		This register controls the PWM high time			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
7:0	pwm_h_time	00h	R/W		This bit defines the high time of the pwm generator in 2/fclk_int units
				0	pwm_div * 2/ fclk_int
				1	pwm_div * 4/ fclk_int
				2	pwm_div * 6/ fclk_int
				....	
				FFh	pwm_div * 512/ fclk_int

Table 30. PWM Frequency Control Low Time Registers

Addr: 57		PWM Frequency Control Low Time Registers			
		This register controls the PWM Low time			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
7:0	pwm_l_time	00h	R/W	This bit defines the high time of the pwm generator in 2/fclk_int units	
				0	pwm_div * 2/ fclk_int
				1	pwm_div * 4/ fclk_int
				2	pwm_div * 6/ fclk_int
				....	
				FFh	pwm_div * 512/ fclk_int

Table 31. PWM Divider Registers bits

Addr: 58		CURR control			
		This register controls the PWM divider			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
7:6	pwm_div	00h	R/W	This bit defines the divider ratio of the prescaler for the PWM generator	
				00	Divide by 1
				01	Divide by 2
				10	Divide by 4
				11	Divide by 16

All Step Down DCDC converters and several LDOs can be directly on/off controlled by CURR3_GPIO3 or CURR4_GPIO4. The CURR3_GPIO3 and/or CURR4_GPIO4 pin should be set to digital input mode (GPIO3Mode = 010b, GPIO4Mode = 010b) and the following register should be set accordingly:

Note: The original digital interface on/off signal is used to switch between CURR3_GPIO3 and CURR4_GPIO4; e.g. if ldo_rf1_gpio is set, ldo_rf1_on is (re-)used to selected either CURR3_GPIO3 (ldo_rf1_on=1) or CURR4_GPIO4 (ldo_rf1_on=0) as input.

Table 32. Regulator GPIO Control Registers

Addr: 31		Reg GPIO Ctrl			
		This register enables/disables GPIO control of the regulators			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
0	ldo_rf1_gpio	0	R/W	ldo_rf1 on/off control	
				0	Controlled by software (ldo_rf1_on)
				1	Controlled by CURR3_GPIO3, if ldo_rf1_on=1 and GPIO3IOSF=10b Controlled by CURR4_GPIO4, if ldo_rf1_on=0 and GPIO4IOSF=10b
1	ldo_rf2_gpio	0	R/W	ldo_rf2 on/off control	
				0	Controlled by software (ldo_rf2_on)
				1	Controlled by CURR3_GPIO3, if ldo_rf2_on=1 and GPIO3IOSF=10b Controlled by CURR4_GPIO4, if ldo_rf2_on=0 and GPIO4IOSF=10b
2	ldo_dig1_gpio	0	R/W	ldo_dig1 on/off control	
				0	Controlled by software (ldo_dig1_on)
				1	Controlled by CURR3_GPIO3, if ldo_dig1_on=1 and GPIO3IOSF=10b Controlled by CURR4_GPIO4, if ldo_dig1_on=0 and GPIO4IOSF=10b; do not set ldo_dig1_gpio if DCDC SD1 is in external controller mode (sd1_1A_mode = 1100b)
3	ldo_dig2_gpio	0	R/W	ldo_dig2 on/off control	
				0	Controlled by software (ldo_dig2_on)
				1	Controlled by CURR3_GPIO3, if ldo_dig2_on=1 and GPIO3IOSF=10b Controlled by CURR4_GPIO4, if ldo_dig2_on=0 and GPIO4IOSF=10b do not set ldo_dig2_gpio if DCDC SD1 is in external controller mode (sd1_1A_mode = 1100b)
4	sd1_gpio	0	R/W	sd1 on/off control	
				0	Controlled by software (sd1_on)
				1	Controlled by CURR3_GPIO3, if sd1_on=1 and GPIO3IOSF=10b Controlled by CURR4_GPIO4, if sd1_on=0 and GPIO4IOSF=10b
5	sd2_gpio	0	R/W	sd2 on/off control (or sd2 on/off control in 1A mode)	
				0	Controlled by software (sd2_on)
				1	Controlled by CURR3_GPIO3, if sd2_on=1 and GPIO3IOSF=10b Controlled by CURR4_GPIO4, if sd2_on=0 and GPIO4IOSF=10b

Table 32. Regulator GPIO Control Registers

Addr: 31		Reg GPIO Ctrl			
		This register enables/disables GPIO control of the regulators			
Bit	Bit Name	Default	Access	Description	
6	sd3_gpio	0	R/W	Sd3 on/off control	
				0	Controlled by software (sd3_on)
				1	Controlled by CURR3_GPIO3, if sd3_on=1 and GPIO3IOSF=10b Controlled by CURR4_GPIO4, if sd3_on=0 and GPIO4IOSF=10b
7	ldo_dig3_gpio	0	R/W	ldo_dig3 on/off control	
				0	Controlled by software (ldo_dig3_on)
				1	Controlled by CURR3_GPIO3, if ldo_dig3_on=1 and GPIO3IOSF=10b Controlled by CURR4_GPIO4, if ldo_dig3_on=0 and GPIO4IOSF=10b

8.4 Backup Battery Charger

The backup battery charger operates as a programmable voltage limited current source with a selectable output resistor. It is enabled by setting BBCMode in the Backup Battery Charger register to a value other than '00'b and offers the following features:

- Backup battery presence detection
- Selectable output resistor (R_{BBCOUT}) to reduce the current at higher voltages
- Programmable charge current I_{BBC}
- programmable maximum charging voltage V_{BBC}
- Reverse current protection turns off backup battery charger automatically if $V_{SUPPLY}<V_{VBACK}$; as soon as V_{SUPPLY} exceeds V_{VBACK} charging is started again automatically
- Charging is stopped automatically as soon as the backup battery is fully charged; if the voltage on pin VBACK drops charging is started again automatically
- In case the main supply voltage V_{SUPPLY} is larger than V_{VBACK} charging of the backup battery is possible in state "Off" as well; the device will check V_{VBACK} every minute to determine if charging is required.

Figure 10. Backup Battery Charger Block Diagram

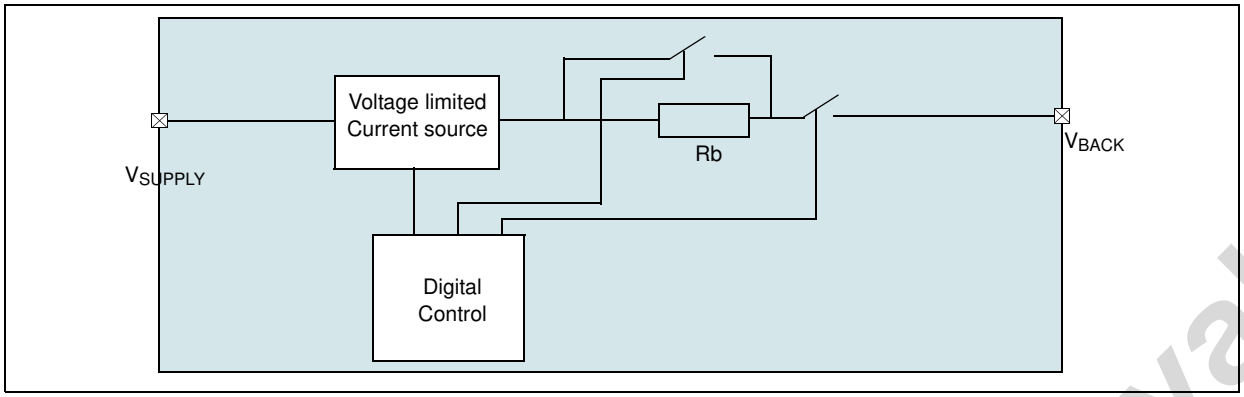


Table 33. Backup Battery Charger Characteristics

symbol	Parameter	Min	Typ	Max	Unit	Note
V_{SUPPLY}	Supply voltage range	3.0		5.5	V	BBCVolt='0'
		3.3		5.5		BBCVolt='1'
V_{BBC}	Maximum charging voltage	2.4	2.5	2.6	V	BBCVolt='0'
		2.9	3.0	3.1		BBCVolt='1'
I_{BBC}	Charge current	-30%	BBCCur	+30%	A	Value is set by BBCCur in the Backup Battery Charger register
V_{DELTA}	Delta voltage for resistive mode	160	220	300	mV	BBCResOff='0'
$I_{VSUPPLY}$	Supply current			20	µA	BBCResOff='0'
				30		BBCResOff='1'
				0.5		BBCPwrSave='1'; backup battery full.

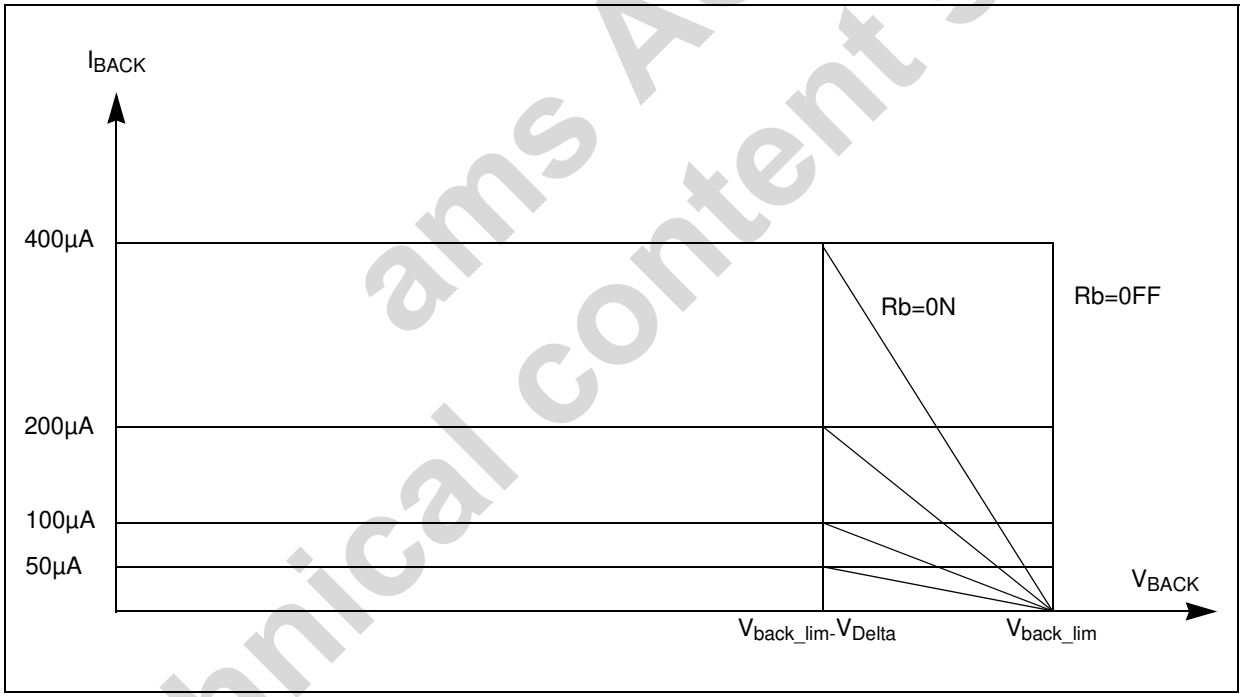
Table 34. Backup Battery Charger Register

Addr: 38		Backup Battery Charger			
		This register controls the Backup battery charger mode			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
1:0	BBCMode	00b	R/W	00b	Backup battery charger is disabled
				01b	Backup battery charger is enabled in states "Power Off mode", "standby mode" and "Active mode". (32kHz OSC has to be enabled in that mode rtcmode=01b or 10b)
				1Xb	Backup battery charger is enabled in state "Active mode" and "standby mode". (32kHz OSC has to be enabled in that mode rtcmode=01b or 10b)
2	BBCResOff	0	R/W	0	Enable output resistor
				1	Bypass output resistor
4:3	BBCCur	00b	R/W	This value determines the charge current I_{BBC}.	
				00b	I_{BBC}=50µA
				10b	I_{BBC}=200µA
				01b	I_{BBC}=100µA
				11b	I_{BBC}=400µA

Table 34. Backup Battery Charger Register

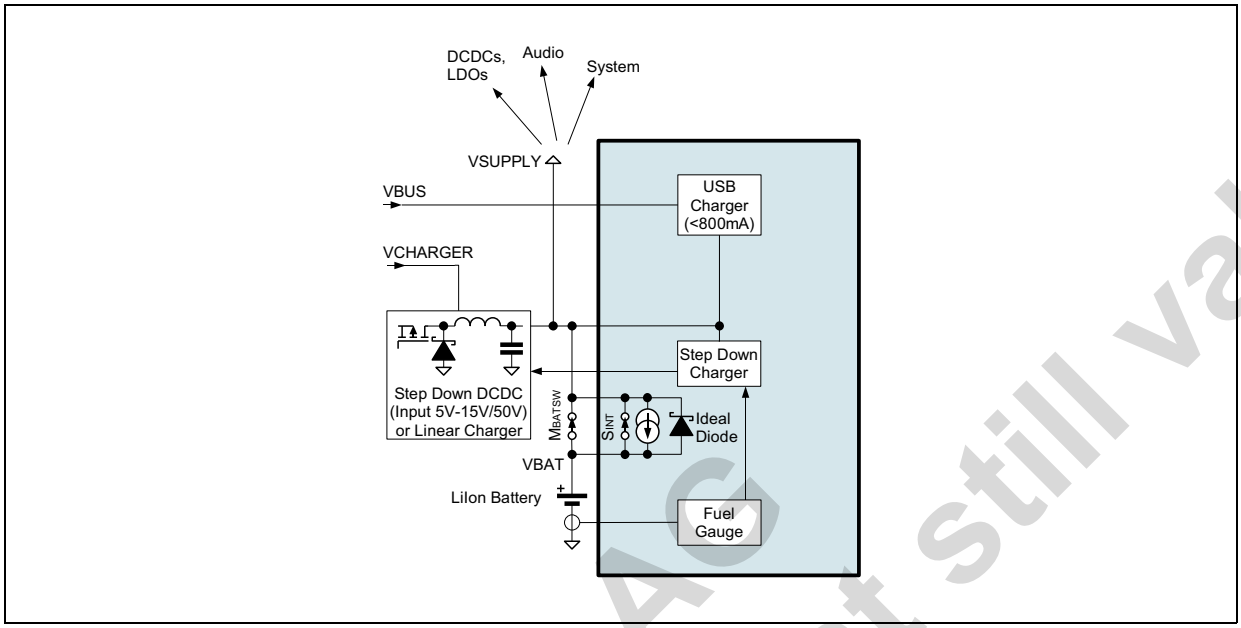
Addr: 38		Backup Battery Charger			
		This register controls the Backup battery charger mode			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
5	BBCVolt	0	R/W	This value determines the maximum charging voltage V_{BBC}.	
				0	V_{BBC}=2.5V
				1	V_{BBC}=3.0V
6	BBCPwrSave	1	R/W	0	Normal operation of the backup battery charger
				1	The backup battery charger checks if it is actually charging the battery (bit BUChAct='1') and it is disabled if it is not. Every 10s (every 64s in state "Off") the voltage of the backup battery is checked again to determine if charging is required. This practically reduces the current consumption to 0 if the backup battery is full.
7	-		-		reserved

Figure 11. Backup Battery Charger Characteristics



8.5 Smooth switchover Power Management Overview

Figure 12. Power Source Management Architecture



The power source management architecture handles the smooth transitions between the two chargers (USB Charger on VBUS, DCDC Step Down charger or Linear Charger on VCHARGER) and the battery. It takes care about the system power supply VSUPPLY and its power requirements.

There are following operating conditions possible

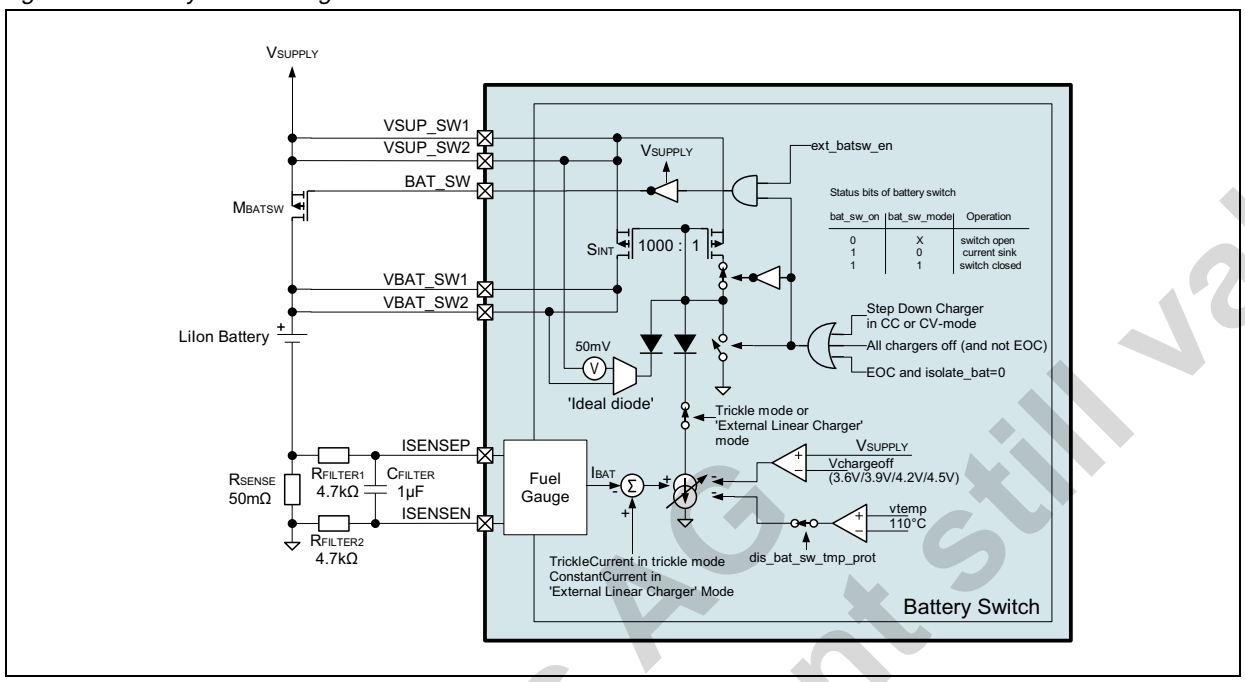
1. No Charger connected
   The internal switch SINT and the (optional) external switch MBATSW are closed and VSUPPLY is directly supplied by VBAT. Because of the very low impedance of the switches the energy losses are minimized.
2. The active charger can deliver more current than the system requires
   The system is directly supplied by the charger and the remaining energy can be used to charge the battery (CC/CV charger). In case of deeply discharged batteries, the system is always immediately started and the internal current source between VSUPPLY and VBAT delivers the trickle current to the battery.
3. The current limited (e.g. for USB with 500mA) charger cannot deliver the current, the system requires
   In this case, the ideal diode starts conducting and delivers the remaining current to the system

The transitions between the different power states are done autonomously by the AS3658 allowing an uninterrupted operation of the system.

The blocks are described in more detail in the following sections.

8.6 Battery switch SINT (Vsupply, Battery)

Figure 13. Battery Switch Diagram



The internal Battery switch enables normal operation of the System during trickle charging of a deeply discharged battery.

The Switch provides the following functions:

- Trickle charging, if VBAT is smaller than ResVolt. The current is defined in TrickleCurrent[1:0] PMOS is switched on if VBAT is greater then ResVolt.
- Constant current charging, if the external charger is in linear operation, or the USB charger is used. the current is defined by constant_current[2:0].
- Current limitation during tricklecharge, to avoid inrush current: $I_{trickle\_Ilimit}$
- Current limitation during Constant current charging to avoid inrush current: I_{CC_Ilimit}
- Undervoltage protection of Vsupply during trickle charge or constant current charge with linear charger. The charging current is regulated down, if Vsupply drops below V_{supply_min}
- Ideal diode operation in Isolate Battery mode and disable charging mode, during charger is unplugged. This operation is for the internal battery switch only. External battery switch is open in that mode. Regulation will start, if the VSUPPLY voltage drops by more then V_{Diode} below the VBAT voltage. After three milliseconds debounce time, if no charger is recognized, the internal and external battery switch (if enabled) is closed to have a low Ω ic connection between VBAT and VSUPPLY.

Table 35. Battery switch parameters

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{Supply}	Input voltage	3.0		5.5	V	PIN VSUP_SW1,VSUP_SW2
$I_{trickle\_limit}$	Trickle current limit		400		mA	
I_{CC_limit}	Constant current current limit	800			mA	Current Limit in constant current mode (Linear charger mode or USB charger only) Note: applies only for the battery switch alone

Table 35. Battery switch parameters

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{Diode}	Ideal Diode start voltage		50		mV	
V_{supply_min}	Vsupply level for charging current regulation (reduction), to avoid voltage drop on vsupply	-6%	3.9 3.6 4.2 4.5	3%	V	Trickle current (or constant current in linear mode) will be regulated down, if vsupply drops below this level
R_{SW}	SINT P-Switch ON resistance		0.10		Ω	VSUP_SW=3.6V

Table 36. USB-Charger Bit definitions

Addr: 10		USB Charger Control			
		This register controls the mode of the USB charger, and the charger state machine			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
5	dis_batsw_tmp_prot	ROM	R/W	0	Over temperature protection of battery switch enabled. (If battery switch is in current source mode, charging is stopped if chip temperature exceeds 110°)
				1	Over temperature protection of battery switch disabled
7	ext_batsw_en	ROM	R/W	0	External battery switch disabled (Pin BAT_SW = max(VSUPPLY,VBAT))
				1	External battery switch enabled (Pin BAT_SW=0V, if status bits batsw_on=1 and batsw_mode=1. These bits are controlled by the charger state machine)

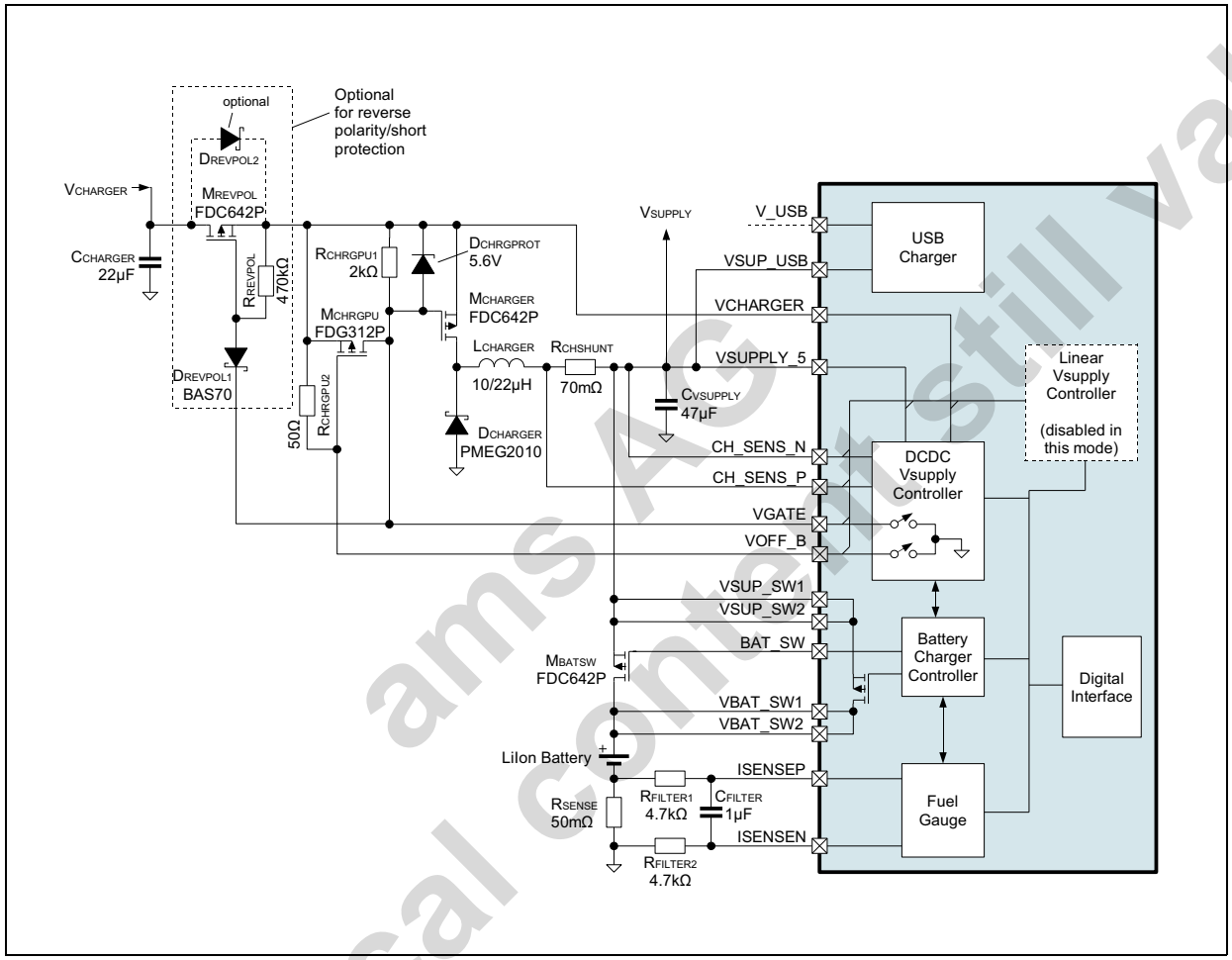
Table 37. Battery switch status Bit definitions

Addr: 100		Charger status_usb			
		These bits show the status of the battery switch			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
2	batsw_mode	NA	R	0	Trickle charging (or constant current charging in linear mode), if batsw_on=1. External PMOS switch disabled
				1	Switch on Battery switch, if batsw_on=1. External PMOS switch enabled
3	batsw_on	NA	R	0	Battery switch off
				1	Battery switch on (Mode defined by batsw_mode)

8.7 External Step Down/Linear Charger

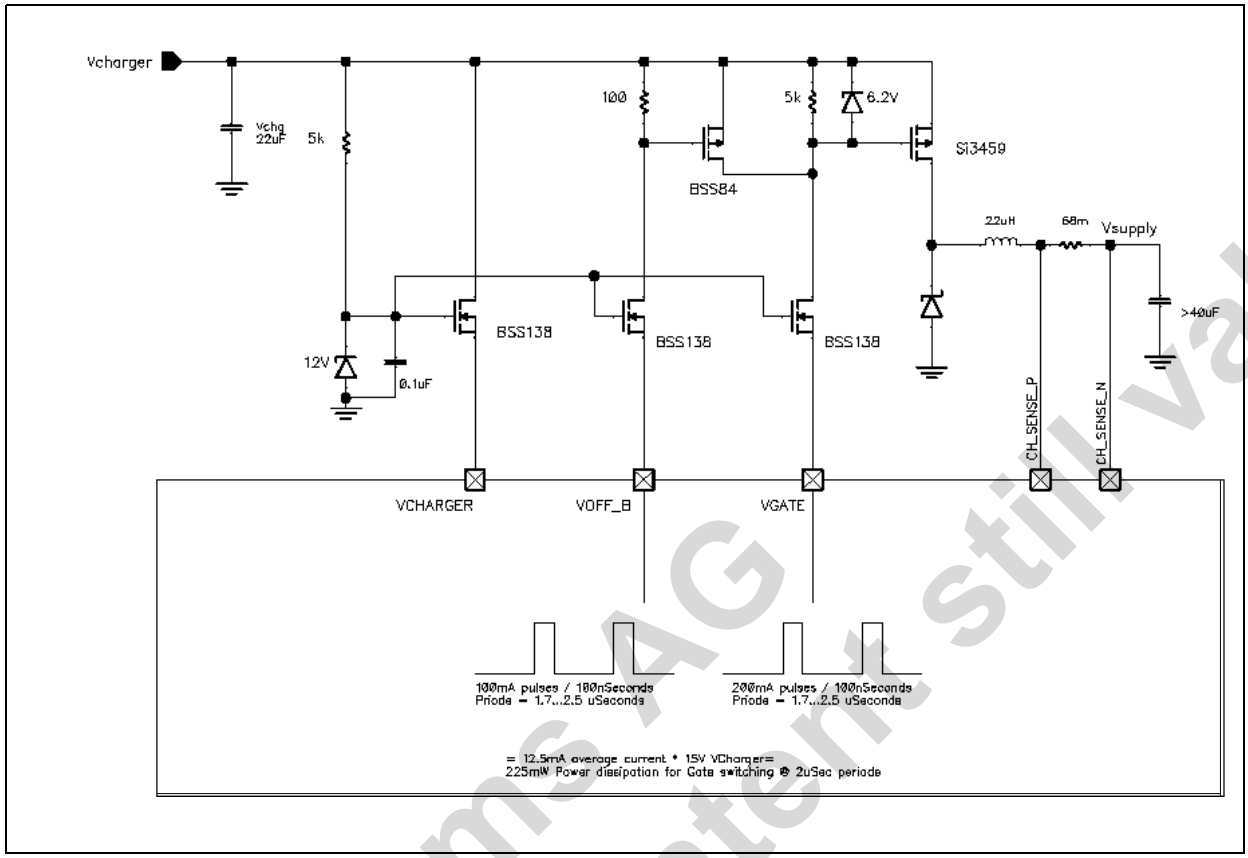
The inductive dcdc step down charger (or the external linear charger) converts the input voltage from VCHARGER to VSUPPLY. The system (DCDC converters, LDOs…) are connected directly to VSUPPLY; the ideal diode and the internal battery switch SINT (together with the external battery switch MBATSW) connect VSUPPLY to VBAT to allow charging of the battery.

Figure 14. Step Down Charger Application Diagram with optional reverse polarity and short protection



If the input voltage can be up to 50V additional three transistors and a simple voltage regulator with a zener diode are required. These circuit 'isolates' the AS3658 from the high input voltage and keep the pins VCHARGER, VOFF_B and VGATE within its operating limits (<15V). The actual circuit is shown in the following figure:

Figure 15. Charger Block Diagram for voltages >15V (Protection up to 50V; minimum Vcharger voltage 8V)



Instead of using an inductive DCDC step down charger, the AS3658 supports external linear charging mode with an PMOS transistor. The operating mode is selected by connecting the pin VOFF_B to GND (for 5.5V limited chargers, the USB charger can be used alternatively):

Figure 16. External Linear Charger Application Diagram (VOFF_B connected to GND)

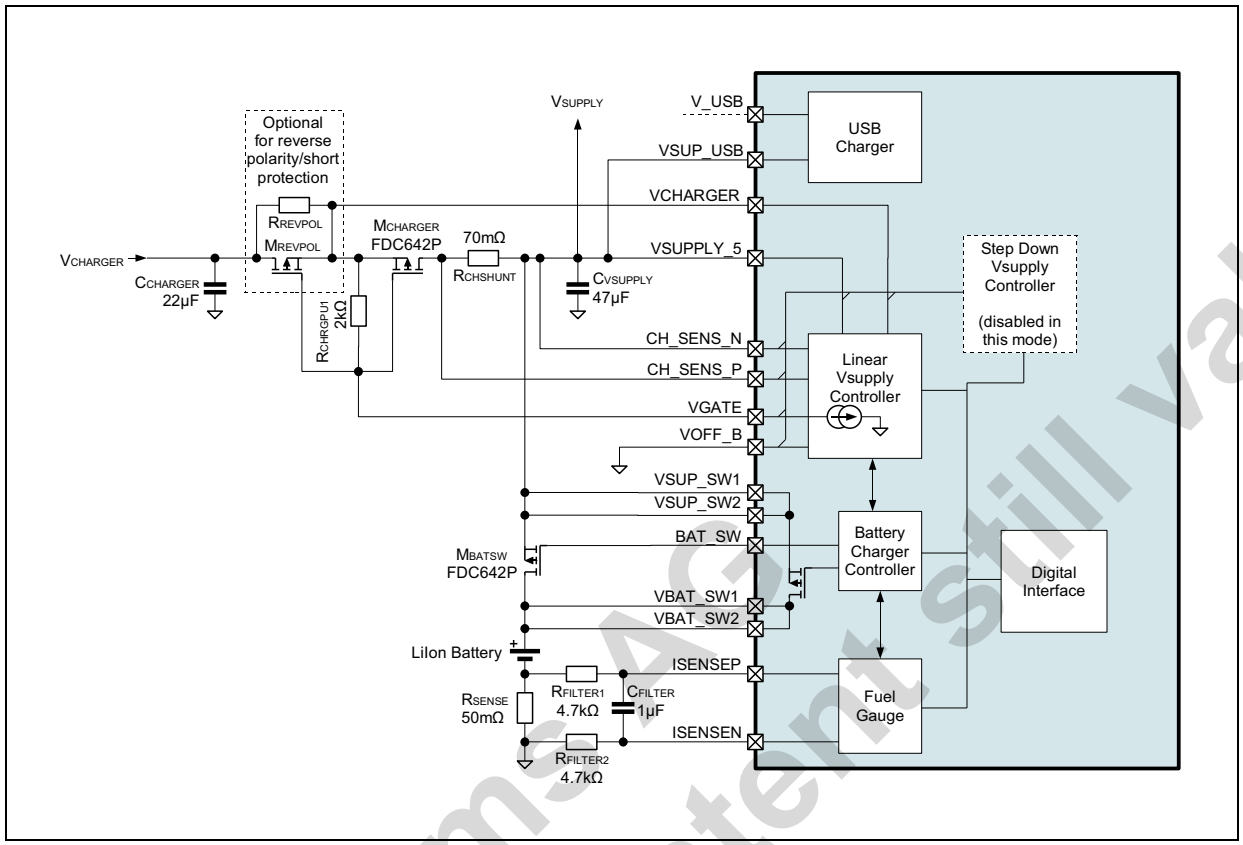


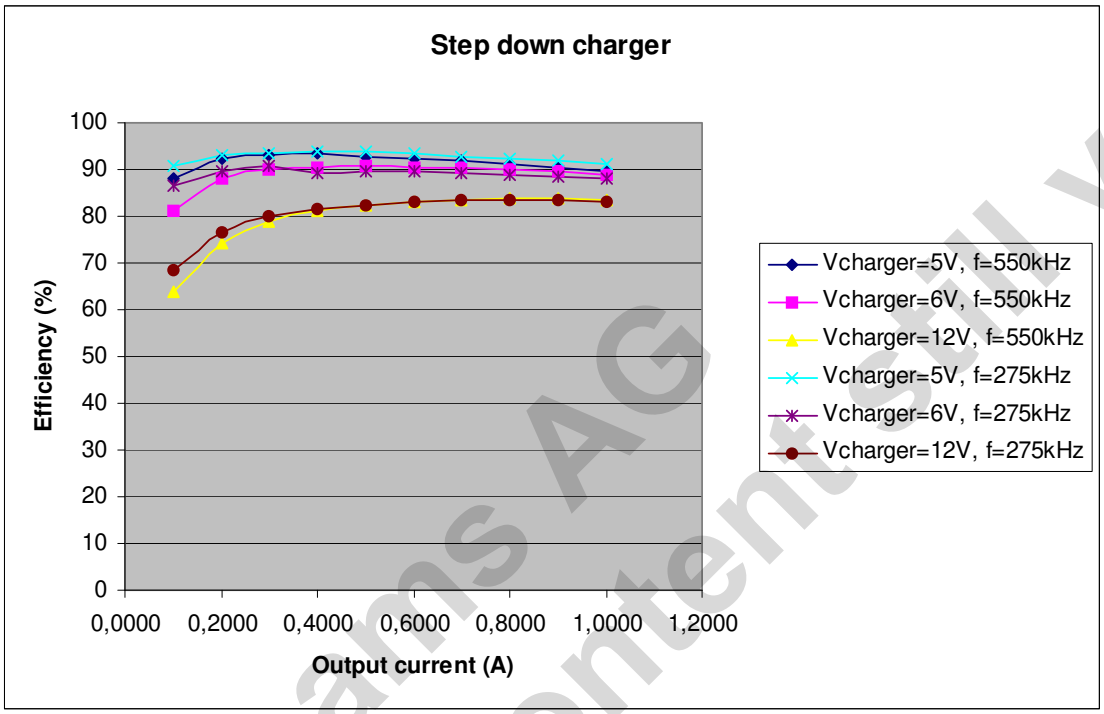
Table 38. Charger External Components

Symbol	Component	Value	Note
MCHARGER, MBATSW, MREVPOL	P-channel MOSFET	Si1403, FDC642P or FDC5614P similar	
MCHRGPU	P-channel MOSFET	BSS84 or FDG312P or similar	
RCHRGPU1	Pull-up resistor1	2kΩ ± 5%	
RCHRGPU2	Pull-up resistor2	100Ω ± 5%	for MCHRGPU =BSS84
		50Ω ± 5%	for MCHRGPU=FDG312P
LCHARGER	Inductor for charging	10µH	5V or 6V Vcharger input
		22µH	12V Vcharger input
DCHARGER	Diode	MBRS130 or PMEG2010	
DCHRGPROT	Zener Diode	5.6V Zener Diode	
RCHSHUNT	Current sense resistor charger	70mΩ ± 5%, 125mW	e.g. Vishay Dale WSL0805 series
RSENSE	Current sense resistor	50mΩ ± 1%, 125mW for $I_{VBAT,DC}$<1.5A	e.g. Vishay Dale WSL0805 series
RFILTER1,2	Filter resistor	4.7kΩ ± 1%	Can be omitted if fuel gauge and charger functionality is not used
CFILTER	Filter capacitor	1µF ± 20%, X5R or X7R dielectric	
CCHARGER	Bypass capacitor on charger pin	1µF ± 20%, X5R or X7R dielectric + 22µF ± 20%, Tantal dielectric	

Table 38. Charger External Components

Symbol	Component	Value	Note
CVSUPPLY	Minimum total capacitance parallel to Vsupply	22µF± 20%, X5R or X7R dielectric	10 µH inductor
		47µF± 20%, X5R or X7R dielectric	22 µH inductor

Figure 17. Step down charger Efficiency (Measured) VSupply=4.4V



8.7.1 External Step Down/Linear Charger Characteristics

The battery charge controller controls the external Step Down/ Linear charger.

During Trickle charge of the deeply discharged battery the step down/Linear converter regulates the Vsupply to $V_{chlimit}$.

In step down charger mode, If the VBAT voltage exceeds ResVoltRise, the internal battery switch is switched on, the Vsupply voltage drops down to VBAT immediately, and the step down converter operates as controlled current source to Vsupply. The battery current is regulated to the value defined in ConstantCurrent register.

In linear charger mode, the Vsupply is still regulated to $V_{chlimit}$, if the VBAT voltage exceeds ResVoltRise. The current is regulated by the battery switch to the value defined in the constant current register.

In EOC operation (see Battery Charge Controller on page 51), the operation of the charger depends on the bit isolate_battery:

If isolate_battery = 1 and EOC the output is regulated to Vchlimit.

If isolate_battery = 0 and EOC the output is not allowed to drop below VEOC (3.6V).

Table 39. Step down Charger parameters

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{rsense_max}	Current limit voltage at Rsense	70	100	130	mV	e.g.: 1.4A for 0.07O sense resistor typ.
C_{out_10}	Output capacitor with 10µH inductor	20		60	µF	X7R ceramic

Table 39. Step down Charger parameters

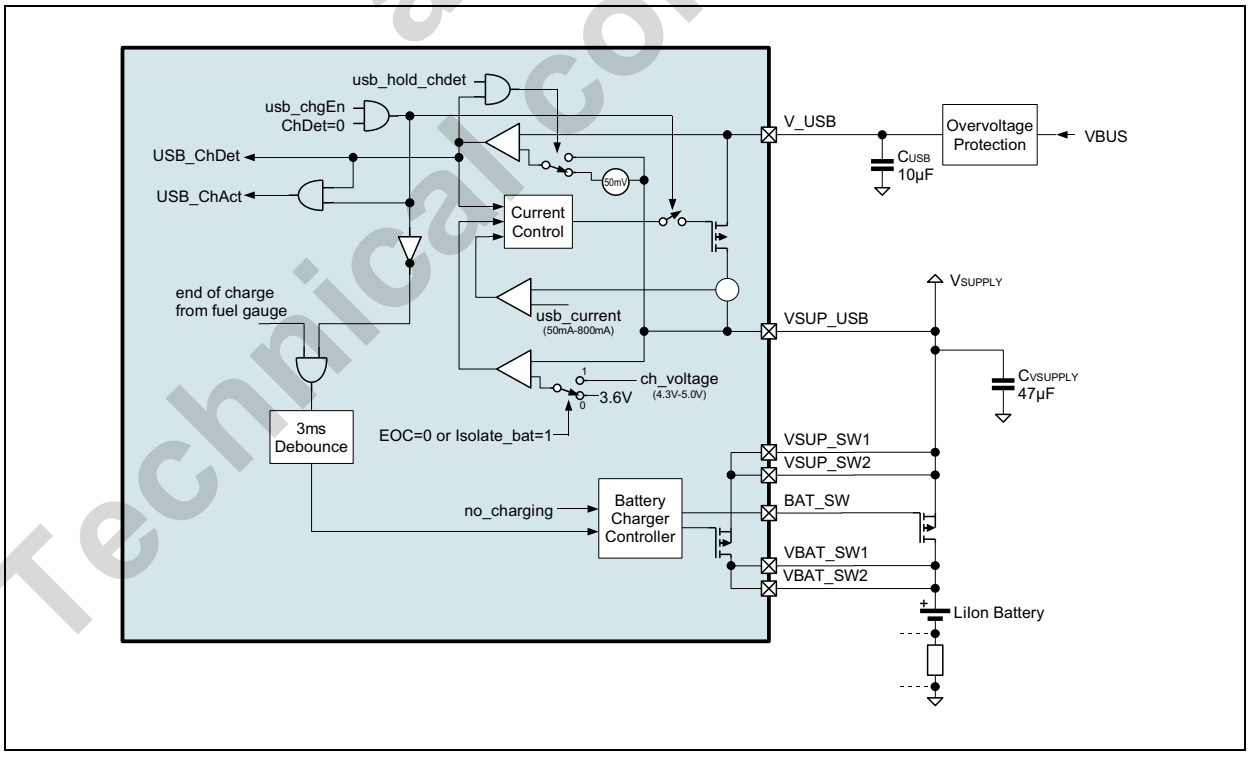
Symbol	Parameter	Min	Typ	Max	Unit	Note
C_{out_22}	Output capacitor with 22µH inductor	40		60	µF	X7R ceramic
C_{out_Linear}	Output capacitor in linear mode	20		60	µF	X7R ceramic
L	Inductor		10/22		µH	(see Table 38)
$I_{trickle\_limit}$	Trickle current limit		400		mA	

Table 40. Step down Charger Bit definitions

Addr: 37		Step Down charger control			
		These bits configures the step down charger			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
0	sdc_frequ	0	R/W	0	fclk_int/4 (use as default, if Vcharger>6V)
				1	fclk_int/8 (use as default, if Vcharger<6V)
1	sdc_pon	1	R/W	0	Disable 100% PMOS on mode for step down charger
				1	Enable 100% PMOS on mode to reduce voltage drop in low dropout regulation
2	sdc_pass_mode	0	R/W	0	Normal mode of step down charger mode
				1	step down charger in pass through mode. Use this mode with max. 5.5V charger only. Vsupply=Vcharger in that mode, if no_charging=1.

8.8 USB Charger

Figure 18. USB Charger Block Diagram



The AS3658 serves an integrated USB charger for Li+ batteries. The USB Charger is a current and voltage limited charger, which can be used to charge Li+ batteries directly from the USB supply. The V_{BAT} voltage limit is set by the register ChVoltEOC (3.9V – 4.25V in 50mV steps; identical for USB charger and step down charger) and the current limit is set by the register usb_current (94mA to 881mA). The Vsupply voltage limit is set to $V_{chlimit}$ during trickle and constant current charging.

For USB charging, it is recommended to start with a current limit of 94mA and after negotiates via the USB bus (this has to be done by e.g. the uProcessor directly) a different current setting can be set to speed up charging (e.g. 470mA).

If Bit usb_chgEn=1 in the Boot ROM is set, VSUPPLY can start up with USB supply allowing startup from the USB supply.

If ChEn=1 and chdet=1 (external charger enabled and connected) the usb_charger will be deactivated automatically. (The Battery charger overrides the USB charger). It's not possible to use the internal and the external charger in parallel.

End of charge of the USB charger is reached, if the current through the battery falls below the value set in the Tricklecurrent [1:0] register.

Table 41. USB-Charger Bit definitions

Addr: 10		**USB Charger control**			
		This register controls the mode of the USB charger, and the charger state machine			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
3:0	usb_Current	ROM	R/W	Sets the USB input current limit.	
				(0000)b	94mA (USB low current)
				(0001)b	141mA
				(0010)b	189mA
				(0011)b	237mA
				(0100)b	285mA
				(0101)b	332mA
				(0110)b	380mA
				(0111)b	428mA
				(1000)b	470mA (USB high current)
				(1001)b	517mA
				(1010)b	598mA
				(1011)b	668mA
				(1100)b	759mA
				(1101)b	881mA
				(1110)b	881mA (do not use)
				(1111)b	881mA (do not use)
4	usb_chgEn	ROM	R/W	ON/OFF control of USB charger	
				0	USB charger disabled.
				1	USB charger enabled.

Table 41. USB-Charger Bit definitions

Addr: 10		USB Charger control			
		This register controls the mode of the USB charger, and the charger state machine			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
5	dis_batsw_tmp_prot	ROM	R/W	0	Overtemperature protection of battery switch enabled. (If battery switch is in current source mode, charging is stopped if chip temperature exceeds 110ºC)
				1	Overtemperature protection of battery switch disabled
6	no_charging	ROM	R/W	0	Normal battery charger operation (usb charger and/or step down charger)
				1	USB and Step down charger is supplying VSUPPLY, but battery switch is open. USB charger or external charger regulate to $V_{chlimit}$
7	ext_batsw_en	ROM	R/W	0	External battery switch disabled (Pin BAT_SW= VSUPPLY,V_{BAT})
				1	External battery switch enabled (Pin BAT_SW=0V, if status bits batsw_on=1 and batsw_mode=1. These bits are controlled by the charger state machine)

Table 42. Charger status Bit definitions

Addr:100		Charger status_usb		
		These bits show the status of the USB charger		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	USB_ChDet	NA	R	set to 1 if charger is detected
1	USB_Chact	NA	R	Set to 1 if charger is active
4	Ch_overvoltage	NA	R	Set to 1 if overvoltage on pin VCHARGER is applied

Charger Detection:

The Charger will be detected by comparison of the V_USB voltage with the Vsupply voltage.

If V_USB is 50mV higher than VSupply voltage or V_USB > 4.3V or the USB_ChDet is set to 1.

Table 43. USB Charger Characteristics,VUSB=4.3…5.5V; Tamb=–20…+85°C; unless otherwise specified.

Symbol	Parameter	Min	Typ	Min	Unit	Note
$I_{usbcurrent500mA}$	USBcurrent for 500mA selection	440	470	500	mA	Resistor on pin RBias to ground of 220kΩ
$I_{usbcurrent100A}$	USBcurrent for 100mA selection	84	95	104	mA	Resistor on pin RBias to ground of 220kΩ

Table 44. USB-Charger additional trimming

Addr:130		USB Current control			
		This register adds or subtracts current limit			
Bit	Bit Name	Default	Access	Description	
2:0	usb_add_trim_current	00h	R/W	Increase or decrease The USB current limit for additional in system trimming:	
				100	usbcurrent-5.1%
				101	usbcurrent-3.8%
				110	usbcurrent-2.5%
				111	usbcurrent-1.2%
				000	usbcurrent+0%
				001	usbcurrent+1.2%
				010	usbcurrent+2.5%
				011	usbcurrent+3.8%

8.9 Battery Charge Controller

The AS3658 device serves as a standalone battery charge controller supporting rechargeable lithium ion (Li+) and nickel metal hybrid (NiMH) batteries. Requiring only a few external components, a full-featured battery charger with a high degree of flexibility can easily be realized. The main features of the controller are:

- Charge adapter detection
- Charging of deeply discharged batteries
- Low current (trickle) charging
- Real constant current charging by regulation of the battery current instead of the charge current
- 2 different top-off charging modes: Pulse charging and constant voltage charging
- Fuel gauge enables highly accurate remaining capacity estimation of the battery
- Overvoltage protection for charge adapter input and main battery
- Battery presence indication
- Operation without battery
- Reverse polarity and short protection
- Charging timout timer
- Battery NTC supervision

8.9.1 Charge Controller Operating Modes and Building Blocks

Linear Step down Charger detection

The charging circuit automatically detects, if a step down charger or a linear charger is connected externally, by measuring the voltage on the pin VOFF_B. If this pin is tied to GND, the circuit detects a linear charger. Otherwise the step down charger is detected

Charge adapter detection

The charge controller uses an integrated detection circuit to determine if an external charge adapter has been applied to the VCHARGER or V_USB pin. If the adapter voltage exceeds the supply voltage at pin V_SUPPLY5 by V_{CHDET} the ChDet or USB_CHDet bit in the Charger Status register will be set. The detection circuit will reset the charge controller (ChDet or USB_CHDet is cleared) as soon as the voltage at the VCHARGER or USB_CHDet pin drops to only V_{CHMIN}

above the battery voltage. In case the AS3658 device is reset the charge controller will also be reset, even if a charge adapter is applied to the VCHARGER or V_USB pin.

Charging deeply discharged batteries

To be able to charge even completely discharged batteries the AS3658 device contains an internal voltage regulator that uses the voltage of the external charge adapter at pin VCHARGER or V_USB to generate a bootstrap voltage V_{2_5V} to supply the internal circuitry necessary for charging. As soon as the battery voltage exceeds 2.5V, the bootstrap regulator is disabled and the battery voltage will be used to generate the internal supply voltage to supply the charger circuitry.

Low current (trickle) charging

Trickle charge mode is started when an external charge adapter has been detected and ChEn or usb_chgEn is set, and the battery voltage at pin V_BAT is below the ResVoltRise threshold $V_{RESRISE}$. The Battery switch is open in that case (batsw_on=1 batsw_mode=0). Bits *ChAct* and/or USBChAct and *Trickle* will be set in the *Charger Status* registers. In this mode the charge current into the battery will be limited to *TrickleCurrent* (set in the *Charger Current* register) by the battery switch to prevent undue stress on either the battery or any of the charger components in case of deeply discharged batteries. if Vsupply drops below V_{supply_min} threshold the trickle current is regulated down, to keep the Vsupply voltage up, even with an current limited charger (e.g.:USB charger). Once $V_{RESRISE}$ has been exceeded, the battery switch will be closed and the charge controller will proceed to constant current charge mode. The Vsupply voltage of the step down charger will be set to Vcurr_preset to prevent undervoltage on vsupply during the transition between Trickle and constant current charging.

Constant current charging

Constant current charging is initiated by setting bit *ChEn and/or USBChEn* in the *Charger Control* register, and resetting the No_charging bit. Note that *ChEn* and/or USBChEn should be set by default to enable operation of the device without a battery connected to the system. The *ChAct and/or USBChAct* bit is set when the charger has started, and the charge current into the battery will be limited to *ConstantCurrent* (set in the *Charger Current* register) by the battery charge controller. When the battery approaches full charge, its instantaneous voltage will exceed the charge termination threshold V_{CHOFF}. V_{CHOFF} depends on the *ChVoltEOC*.The top-off charge mode will be started (bit *CVM* will be set).

Constant voltage charging

Constant voltage charge mode is initiated and the *CVM* bit will be set when the V_{CHOFF} threshold has been exceeded for the first time and bit *Pulse* is not set. In the following the charge controller will act to regulate the battery voltage to a value set by *ChVoltEOC* in the *Charger Config* register.

The charge current is monitored during constant voltage charging. It will be decreasing from its initial value during constant current charging and eventually drop below the value set by *TrickleCurrent* in the *Charger Current* register. If the measured charge current is less than or equal to *TrickleCurrent* and the battery voltage is larger than V_{CHRES}, the charging cycle is terminated and *EOC* is set. Then the charge controller starts the EOC operation.

EOC operation

There are two possibilities:

1. If **isolate_bat=1** the battery switch will be switch off and the battery charger regulates to its highest voltage $V_{chlimit.}$. The advantage of this mode is a longer lifetime of the Li+ battery, because there is no discharging after the EOC condition. If autoresume=1 and the battery voltage drops below V_{CHRES} the battery charger continues charging, by checking in trickle charge mode, if there is a battery connected, and then starting with constant voltage.
2. If isolate_bat=0 the battery switch remains closed for step down charger or will be closed for linear and usb charger, and the power to the system is supplied by the battery. The battery charger and the USB charger regulates to V_{EOC}, in case the battery is removed. If autoresume=1 and the battery voltage drops below V_{CHRES} the battery charger continues charging, by checking in trickle charge mode, if there is a battery connected, and then starting with battery charging.

Battery Detection and Restart of Charging:

In EOC state, If the battery voltage drops below VCHRES and the bit AutoResume is set, the battery detection is started. The battery switch will be switched into current source mode and VSUPPLY will be regulated to Vchlimit (all charger). The AS3658 measured the battery current with the fuel gauge in this mode. If there is no current, the AS3658 is kept in this state and the bit NoBat is set. Otherwise the bit NoBat is cleared and the charger and the AS3658 continues in battery charging mode. In addition, if the ntc_on<1:0>=01b (NTC temperature supervision is active) the NoBat bit is cleared and charging is restarted, if a NTC resistor with normal or high temperature is detected.

Overvoltage protection for external linear charger:

During charging with the external linear charger the battery charge controller constantly monitors the voltage of the charge adapter at pin VCHARGER. In case the charge adapter voltage exceeds $V_{VCHIN,MAX\ rise}$ for longer than 3mesec and bit ChOVDetEn in the Charger Control register is set to 1, charging is disabled immediately. If the voltage on the pin VCHARGER drops below $V_{VCHIN,MAX\ fall}$, the charger is re-enabled.

Figure 19. Typical charging cycle (step down charger)

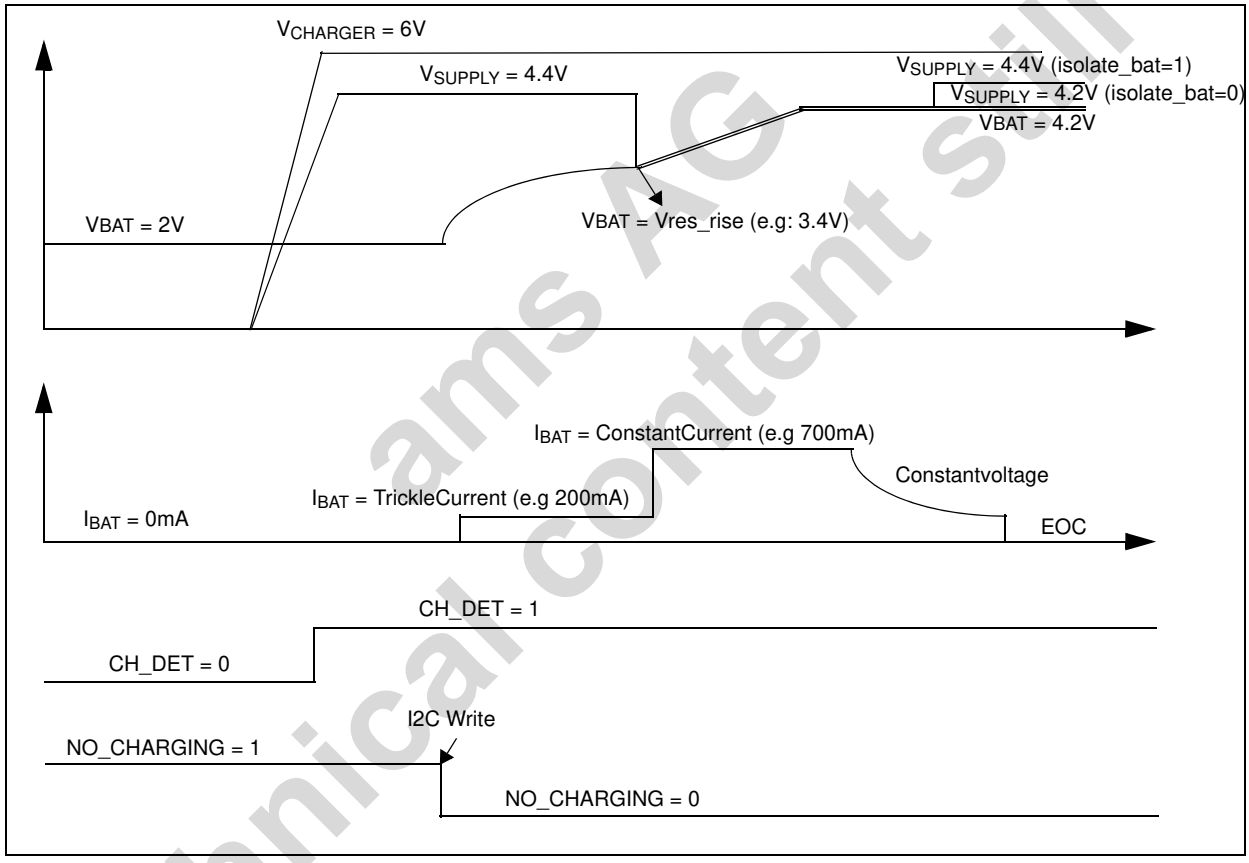


Figure 20. Typical charging cycle (External linear charger or USB charger)

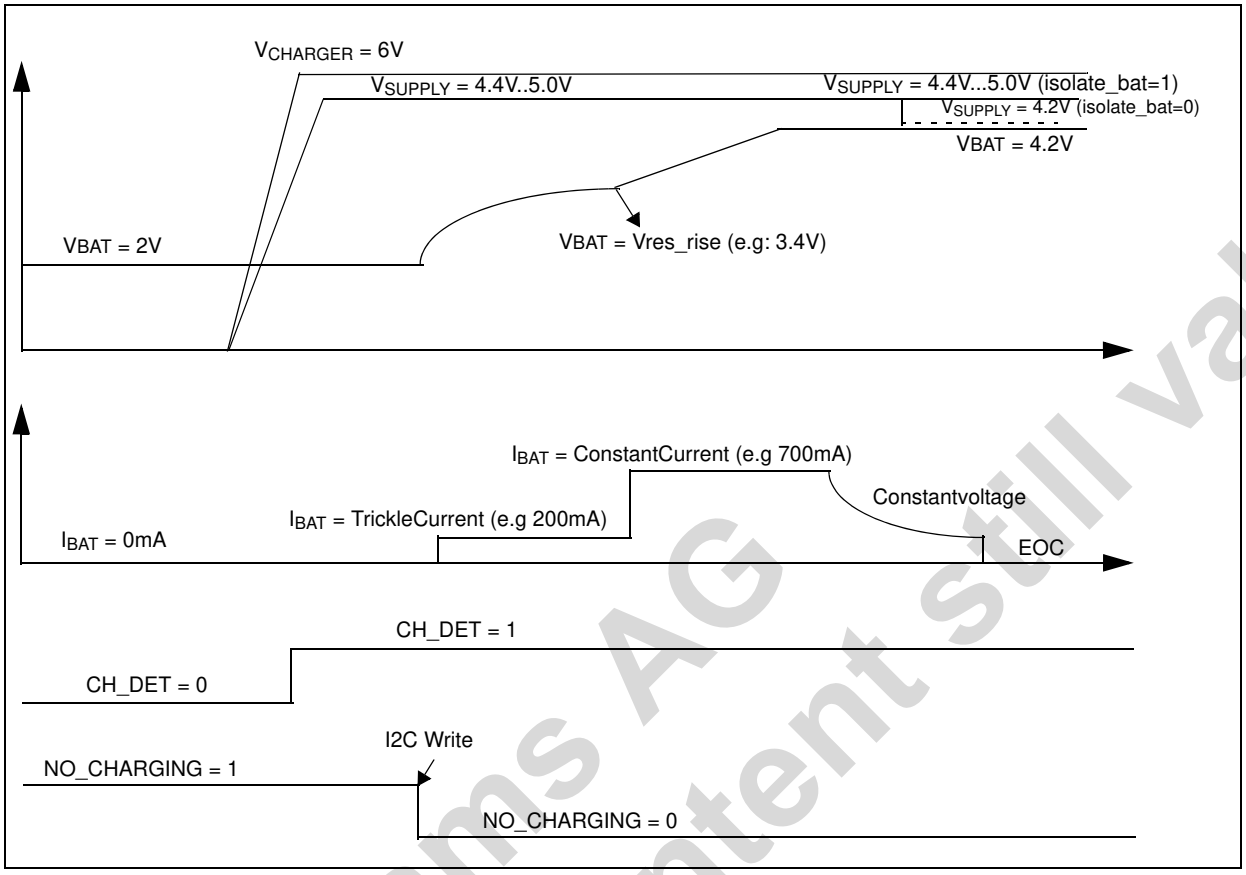


Table 45. Charger Characteristics VVBAT=3.0…5.5V; Tamb=–20…+85°C; unless otherwise specified

Symbol	Parameter	Min	Typ	Min	Unit	Note
$V_{chlimit}$	Voltage limit of charger (if not in current limitation mode)	-3%	ch_voltage	3%	V	Max. Vsupply voltage
VCHARGER	VCHARGER operating range	5.0		15.0	V	For input voltage higher than 15V see above protection circuit; for chargers with input voltages down to 4.5V see: 'Application Note for DC/DC Step down Charger for Chargers Supplying 4.5V to 5.5V'
V_{CHDET}	Charge adapter detection threshold	50	75	105	mV	Hysteresis is > 40mV; for USB and step down charger
V_{CHMIN}		0	20	35	mV	
V_{CHMIN_hold}	Charge adapter detection hold voltage	-5	-20	-40	mV	Vchdet falling threshold, if VSUPPLY>4.35V for V_USB and VCHARGER, and for V_USB, if usb_hold_chdet=1. Warning: Backcharging is possible if usb_hold_chdet=1
$V_{chin,max\ rise}$	Charger adapter overvoltage threshold rising	6.0	6.5	7.0	V	ChOVDetEn='1' for external linear charger only
$V_{chin,max\ fall}$	Charger adapter overvoltage threshold falling		6.0		V	ChOVDetEn='1' for external linear charger only

Table 45. Charger Characteristics VVBAT=3.0…5.5V; Tamb=–20…+85°C; unless otherwise specified

Symbol	Parameter	Min	Typ	Min	Unit	Note
$I_{STARTmax}$	Maximum load current during startup on Vsupply		5		mA	
V_{UVLO}	Undervoltage lockout threshold	–3%	2.7… 3.4	+3%	V	Value is set by *ResVoltRise* in the *Battery Voltage Monitor* register
V_{CHOFF}	Charge termination threshold	–0.06	3.90… 4.25	+0.06	V	Li+ battery; value is set by *ChVoltEOC* in the *Charger Config* register
V_{CHRES}	Charger resume voltage		3.85… 4.20		V	Value is set by *ChVoltResume* in the *Charger Config* register. Do not set V_{CHRES} higher than V_{CHOFF}!
V_{curr_preset}	Charger constant current pre-set voltage		$V_{RESRISE}$ + 100mV		V	
V_{EOC}	Charger EOC voltage		3.60		V	If isolate_bat=0; to prevent a system reset if the battery is removed in EOC operation

Table 46. Charger status Bit definitions

Addr:99		Charger status		
		These bits show the status of the charger		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	ChDet	NA	R	Bit is set when external charge adapter has been detected on pin VCHARGER
1	ChAct	NA	R	Bit is set when step down charger is operating (independent of Reg. bit no_charging)
2	Resume	NA	R	Bit is set when battery voltage has dropped below resume level
3	Trickle	NA	R	Bit is set when charger is in trickle charge mode
4	CVM	NA	R	Bit is set when charger is in top-off charge mode (constant voltage mode)
5	EOC	NA	R	Bit is set when charging has been terminated. Bit is cleared automatically when *ChEn* is cleared, no_charging is set or charging is resumed.
6	NoBat	NA	R	Bit is set when battery detection circuit indicates that no battery is connected to the system. Detection is started after EOC and if bit autoresume=1 only. Bit is cleared automatically when a battery is connected, when *DisBDet* is set and/or when *ChEn* is cleared.
7	ChLinear	NA	R	Bit is set, if Linear charger is detected, and chDet=1. This state is latched on the rising edge of chDet. Detected if VOFF_B is connected to ground

Table 47. Charger control Bit definitions

Addr:11		Charger Control1			
		These bits controls the charger			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
0	ChEn	ROM	R/W	0	Disable step down charger (Independent of bit no_charging)
				1	Enable step down charger (default) (Independent of bit no_charging)
1	Ch_pwroff_en	ROM	R/W	0	Startup of AS3658 if charger is connected in power_off mode
				1	Don't exit power off mode, if charger is already connected before entering power off mode; no autonomous charging upon static charger detect. Startup with rising edge of VCHARGER or V_USB, RTC wakeup and XON pin only
2	CHOVDetEn	ROM	R/W	0	Overvoltage detection with linear external charger enabled
				1	Overvoltage detection with linear external charger enabled. Battery charging disabled, if voltage exceeded
3	AutoResume	ROM	R/W	0	Charging does not restart automatically in EOC when bit *Resume* is set.
				1	Charging will restart automatically in EOC when bit *Resume* is set
4	usb_hold_chdet	ROM	R/W	0	Normal charge_detect operation
				1	Charger detect of USB charger will not be reset, if VUSB=V_{BAT}. (Allow Battery charging, with V_USB<4.4V down to 3.3V); for this case, software should detect the removal of the charger
5	charging_tmax	ROM	R/W	0	Read: no timeout reached Write: reset charger timeout counter
				1	$t_{CHARGING,MAX}$ timeout reached and charging stopped
6	Ch_det_500ms	ROM	R/W	Controls the charge detect debounce timer on pin VCHARGER, if external charger is connected. (If the charger is removed the debounce time is always 3msec)	
				0	$V_{CHARGER}$ debounce timer is 3msec
				1	$V_{CHARGER}$ debounce timer is 500msec

Table 48. Battery, supply voltage Bit definitions

Addr:12		Battery voltage monitor			
		These bits controls the battery/Supply voltage monitor (Reset levels)			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
2:0	ResVoltRise	ROM (101b)	R/W	This value determines the reset level $V_{RESRISE}$ for rising V_{BAT}. It is recommended to set this value at least 200mV higher than $V_{RESFALL}$.	
				000b	$V_{RESRISE}$=2.7V
				001b	$V_{RESRISE}$=2.8V
				010b	$V_{RESRISE}$=2.9V
				011b	$V_{RESRISE}$=3.0V
				100b	$V_{RESRISE}$=3.1V
				101b	$V_{RESRISE}$=3.2V
				110b	$V_{RESRISE}$=3.3V
				111b	$V_{RESRISE}$=3.4V
5:3	ResVoltFall	ROM (011b)	R/W	This value determines the reset level $V_{RESFALL}$ for falling V_{VBAT}. It is recommended to set this value at least 200mV lower than $V_{RESRISE}$.	
				000b	$V_{RESFALL}$=2.7V
				001b	$V_{RESFALL}$=2.8V
				010b	$V_{RESFALL}$=2.9V
				011b	$V_{RESFALL}$=3.0V
				100b	$V_{RESFALL}$=3.1V
				101b	$V_{RESFALL}$=3.2V
				110b	$V_{RESFALL}$=3.3V
				111b	$V_{RESFALL}$=3.4V
6	SupResEn	ROM (0b)	R/W	0	A reset is generated if Vsupply falls below 2.7V. (If VVBAT falls below VRESFALL only an interrupt is generated (if enabled) and the Processor can shut down the system)
				1	A reset is generated if Vsupply falls below $V_{RESFALL}$
7	FastResEn	ROM	R/W	0	Vresetfall debounce time = 3msec
				1	Vresetfall debounce time = 4µsec

Table 49. Charger Config Register

Addr:13		Charger Config			
		These bits configure the charger			
Bit	Bit Name	Default	Access	Description	
2:0	ChVoltEOC	ROM		Sets the end-of-charge voltage level V_{CHOFF}.	
				000b	3.90V
				001b	3.95V
				010b	4.00V
				011b	4.05V
				100b	4.10V
				101b	4.15V
				110b	4.20V
				111b	4.25V
4:3	Vsupply_min	ROM		Regulate down battery charging current on that level of Vsupply during trickle charging and/or linear charging, to prevent voltage drop on vsupply:	
				00b	3.90V
				01b	3.60V
				10b	4.20V
				11b	4.50V
7:5	ChVoltResume	ROM		Sets the resume voltage level V_{CHRES}	
				000b	3.85V
				001b	3.90V
				010b	3.95V
				011b	4.00V
				100b	4.05V
				101b	4.10V
				110b	4.15V
				111b	4.20V

8.9.2 Fuel Gauge

The fuel gauge circuit enables remaining capacity estimation of the battery by tracking the net current flow into and out of the battery using a voltage-to-frequency converter.

Voltage-to-Frequency Converter

The voltage-to-frequency (VFC) converter constantly monitors the voltage drop across an external current sense resistor R_{sense} connected in series between the negative battery terminal and ground. The use of an additional external RC lowpass filter is highly recommended. Using two 4.7kΩ resistors ($R_{filt1,2}$) and a 1µF ceramic capacitor (C_{filt}), the filter cut-off is approximately 16.9 Hz. This filter will capture the effect of most spikes, and will thus allow the current accumulators to accurately reflect the total charge that has gone into or out of the battery.

The key building block of the VFC is an integrator. It will integrate the voltage V_{SNS} across input pins ISENSP and ISENSN. If V_{SNS} is positive (battery is charged), the output voltage of the integrator increases; a negative input voltage (battery is discharged) will cause the integrator output voltage to decrease.

Table 50. Fuel Gauge parameters

Symbol	Parameter	Min	Typ	Max	Unit	Note
f_{CLK}	Internal reference clock		$f_{clk\_int}/2$		MHz	internal CLK frequency/2 Programmable: 0.8 to 1.15 MHz
f_{VFC}	Sample frequency		$f_{CLK}/59$		Hz	
V_{ISENSP} V_{ISENSN}	Input voltage	-0.1		0.1	V	
Z_{ISENSP} Z_{ISENSN}	Input impedance	4.67			MΩ	
A_{VFC}	Discharge and Charge gain		91.0		Hz / V	f_{CLK} = 1.1MHz
FR_{VFC}	Fundamental rate		3.05		µVh	
V_{OFF}	Uncompensated offset voltage	-500		500	µV	
$V_{OFF,COMP}$	Compensated offset voltage	-50	±10	50		

Charge Current Accumulator

The output signals of the charge count dividers are used as inputs for the charge current accumulator that is realized as a 15-bit up-down counter with separate inputs for incrementing and decrementing the counter. An additional sign bit indicates the polarity of the counter value that is maintained in two's complement format. The current accumulator is updated at a rate equivalent to one count per 3.05µVh, which is equivalent to one count per 61.03µAh when using a 50mΩ current sense resistor. It will roll over beyond (7FFF)h when incremented and (0000)h when decremented, and the value given by the counter will be ambiguous in that case. It is the responsibility of the host to read the counter before rollover occurs.

The content of the charge current accumulator will be transferred into the *DeltaCharge* register when the *UpdReq* bit in the *FuelGauge* register has been set. The update of the register has to be synchronized to the sample clock f_{VFC} and can take up to 1.5 clock cycles (max. 2.5µs). After the registers have been updated successfully, the *UpdReq* bit is cleared automatically and the charge current accumulator together with the sign bit will be reset.

Elapsed Time Counter

The sample clock f_{VFC} of the fuel gauge circuit is fed to a 14-bit clock count divider. Its output signal is used as a clocking signal for the 16-bit elapsed time counter, resulting in an equivalent rate of 1.1379 counts per second (4096.60 counts = 1 hour). The elapsed time counter will rollover beyond (FFFF)h, and the value given by the counter will be ambiguous in that case. It is the responsibility of the host to read the counter before rollover occurs.

The content of the elapsed time counter will be transferred into the *ElapsedTime* register when the *UpdReq* bit in the *FuelGauge* register has been set. The update of the register has to be synchronized to the sample clock f_{VFC} and can take up to 1.5 clock cycles (max. 2.5µs). After the registers have been updated successfully, the *UpdReq* bit is cleared automatically and the elapsed time counter will be reset.

Offset Calibration Mode

Although the VFC compensates for the offset of the integrator the fuel gauge features an additional offset calibration mode to enhance the measurement accuracy even further. By setting the *CalReq* bit in the *FuelGauge* register the integrator is reset and the offset calibration mode is activated. The charge count dividers are bypassed during offset calibration to allow a faster calibration procedure with adequate resolution. The offset is accumulated during 16 clocks of the elapsed time counter, the resulting offset calibration value *FGOffCal* has a resolution of 3.05µV and is

transferred to the *DeltaCharge* register. The *CalReq* bit is cleared automatically after the calibration has completed successfully and *FGOffCal* has been written to the register.

Please note that offset calibration is not possible while the charger is active. If the *CalReq* bit is set while the charger is active the calibration will start automatically after the charger has been disabled by clearing the *ChEn* bit or if the external charge adapter has been removed. If during an offset calibration procedure the charger is enabled the offset calibration mode is terminated, the *CalReq* bit is cleared, the current value of the elapsed time counter is transferred to the *ElapsedTime* register and the *DeltaCharge* register is loaded with (FFFF)h.

Calculation of Battery Status

The host system can calculate all the parameters necessary for estimating the remaining battery capacity by evaluating *ElapsedTime*, *DeltaCharge* and *FGOffCal*.

Calculating Elapsed Time

The host system can evaluate the change in time Δt by setting the *UpdReq* bit in the *FuelGauge* register and reading *ElapsedTime* after *UpdReq* has been automatically cleared. The change in time in seconds is given by:

$$\Delta t = ElapsedTime \times 3600 / 4096.60\ [s] \qquad (EQ\ 1)$$

Note that the absolute accuracy of Δt is directly related to the absolute accuracy of the internal reference oscillator. To cancel the error associated with the accuracy of the oscillator, a correction factor CV can be introduced. CV can be evaluated by comparing the change in time calculated by (1) with some reference value Δt_{REF} obtained from a RTC or measured during system calibration. CV is given by:

$$CV = \Delta t_{REF} / \Delta t \qquad (EQ\ 2)$$

By multiplying Δt and CV the correct value for the change in time can be calculated:

$$\Delta t_{CORR} = CV \times \Delta t\ [s] \qquad (EQ\ 3)$$

Calculating Average Current

The host system can calculate the average current during the last time period by setting the *UpdReq* bit in the *FuelGauge* register and reading *DeltaCharge* and *ElapsedTime* after *UpdReq* has been automatically cleared. Together with *FGOffCal* determined during offset calibration mode the average current is given by:

$$I_{AVG} = DeltaCharge / (\Delta t \times A_{VFC} \times R_{sense}) - FGOffCal \times 3.05\mu V / R_{sense}\ [A] \qquad (EQ\ 4)$$

Δt is the change in time in seconds calculated by (1), A_{VFC} is the gain of the VFC in Hz/V, R_{sense} is the value of the sense resistor in Ω and *FGOffCal* is the offset calibration value. As *DeltaCharge* and Δt both are proportional to the oscillator frequency, no correction factor needs to be introduced in the formula.

Calculating Accumulated Current

Accumulated current is used to calculate the absolute remaining capacity of the battery. It is given by:

$$I_{ACC} = I_{AVG} \times \Delta t_{CORR}\ [A] \qquad (EQ\ 5)$$

Calculating the Remaining Capacity

Remaining capacity is the entire goal of fuel gauging. It is given by:

$$RC = RC + I_{ACC}\ [As] \qquad (EQ\ 6)$$

Calculating the Time to Empty

The time to empty is calculated from the average current I_{AVG} given by (4). The longer the time period for which I_{AVG} is calculated, the more accurate the value for I_{AVG} and therefore the estimated time to empty will be. It is given by:

$$TTE = RC / I_{AVG} [s] \quad (EQ\ 7)$$

Table 51. Fuel Gauge Bit definitions

Addr:15		Fuel Gauge			
		These bits configures the fuel gauge			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
0	FGEn	ROM	R/W	0	Disable Fuel Gauge
				1	Enable Fuel Gauge
1	UpdReq	ROM	R/W	This bit controls the update of the *DeltaCharge* and *ElapsedTime* registers. When set, the bit is cleared automatically after the registers have been updated successfully. Bit should not be set to “0” by the host	
				0	Update of registers complete
				1	Request update of registers
2	CalReq	ROM	R/W	This bit controls the offset calibration. When set, the bit is cleared automatically after the calibration has completed successfully.	
				0	Calibration complete OR terminate offset calibration
				1	Request offset calibration
4:3	CalMod	ROM	R/W	Sets the mode for offset calibration	
				00	Connect inputs to ground internally
				01	Use ISENSP and ISENSN (do not use)
				10	do not use
				11	do not use

Table 52. Delta Charger MSB bit definitions

Addr:101		DeltaChargeMSB		
		These bits represent the MSB value of the fuel gauge Delta charge register		
Bit	**Bit Name**	**Default**	**Access**	**Description**
6:0	DeltaChargeMSB	(00)h	R	The register is maintained in two’s complement format with a resolution of 3.05µVh and a full-scale value of ±99.98mVh. When using a 50mΩ current sense resistor this is equivalent to a resolution of 61.03µAh and a full-scale value of 1.999Ah. Sign is set for negative values. Register will be updated after setting bit *UpdReq* to “1”.
7	sign	0	R	Sign bit of the delta charge register

Table 53. DeltaChargerLSB bit definitions

Addr:102		DeltaChargeLSB		
		These bits represent the LSB value of the fuel gauge Delta charge register		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	DeltaChargeLSB	(00)h	R	The register is maintained in two's complement format with a resolution of 3.05µVh and a full-scale value of ±99.98mVh. When using a 50mΩ current sense resistor this is equivalent to a resolution of 61.03µAh and a full-scale value of 1.999Ah. Sign is set for negative values. Register will be updated after setting bit *UpdReq* to "1".

Table 54. ElapsedTimeMSB bit definitions

Addr:103		ElapsedTimeMSB		
		These bits represent the MSB value of the fuel gauge Elapsed Time register		
Bit	**Bit Name**	**Default**	**Access**	**Description**
6:0	ElapsedTimeMSB	(00)h	R	The elapsed time count is stored in the register with a resolution of 0.8788s and a full-scale value of 15.997 hours. Register will be updated after setting bit *UpdReq* to "1".
7	sign	0	R	Sign bit of the elapsed time register

Table 55. ElapsedTimeLSB bit definitions

Addr:104		ElapsedTimeLSB		
		These bits represent the LSB value of the fuel gauge Elapsed Time register		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	ElapsedTimeLSB	(00)h	R	The elapsed time count is stored in the register with a resolution of 0.8788s and a full-scale value of 15.997 hours. Register will be updated after setting bit *UpdReq* to "1".

8.9.3 Charger Operation

The charger controls the battery current through the internal transistor between VSUP_SW1,2 and VBAT_SW1,2, the step down charger and the battery switch between VSUPPLY and V_{BAT}.

Charge Current Regulator

The regulator is programmed by setting *TrickleCurrent* and *ConstantCurrent* in the *ChargerCurrent* register and yields a resolution of 0.625mV or 12.5mA when using a sense resistor of 50mΩ.

Table 56. Charge Current Regulator parameters

Symbol	Parameter	Min	Typ	Max	Unit	Note
t_{MEAS}	Measurement period		68.65		ms	f_{clk_int} = 2.2MHz
$I_{MEAS,LSB}$			0.625		mV	

Table 57. Charger Current Bit definitions

Addr:16		Charger current			
		These bits define the battery charging current and voltage			
Bit	Bit Name	Default	Access	Description	
1:0	TrickleCurrent	ROM	R/W	Sets the trickle current. Default is (01)b = 2.5mV x R_{sense}^{-1}.	
				00b	1.25mV x R_{sense}^{-1}
				01b	2.50mV x R_{sense}^{-1}
				10b	5.00mV x R_{sense}^{-1}
				11b	10.0mV x R_{sense}^{-1}
4:2	ConstantCurrent	ROM	R/W		Sets the charging current in constant current mode from (0mV…35mV) x R_{sense}^{-1} in steps of 5mV x R_{sense}^{-1}.
				000	0mV x R_{sense}^{-1}
				001	5mV x R_{sense}^{-1}
				....	
				111	35mV x R_{sense}^{-1}
7:5	ch_voltage	ROM	R/W	Charger voltage after EOC and isolate_battery=1	
				000b	4.3V
				001b	4.4V
				010b	4.5V
				011b	4.6V
				100b	4.7V
				101b	4.8V
				110b	4.9V
				111b	5.0V

8.10 Charger supervision functions

The charger supervision functions allow charging without processor control by continuously checking the NTC temperature resistor within the battery pack using ADC_IN1 pin. The charging cycle is automatically paused, if the NTC indicates a temperature range out of 0º to 45º (or 0º to 50º). If the temperature gets into this range again the charging cycle is resumed.
In addition there is a charge timer that stops charging after a defined time, as additional security feature.

The timer will be reset at charger insertion (charger detect) or at EOC state. The timer is counting during active charging only (Trickle charging, Constant current charging, Constant voltage charging).

In case the battery voltage does not reach EOC voltage within $t_{CHARGINGMAX}$ after charging has been started, charging_tmax interrupt will be generated and charging will be stopped. Charging can be started again by writing charging_tmax=0 in the charger_control1 register.

Figure 21. Charger Supervision functions – internal circuit

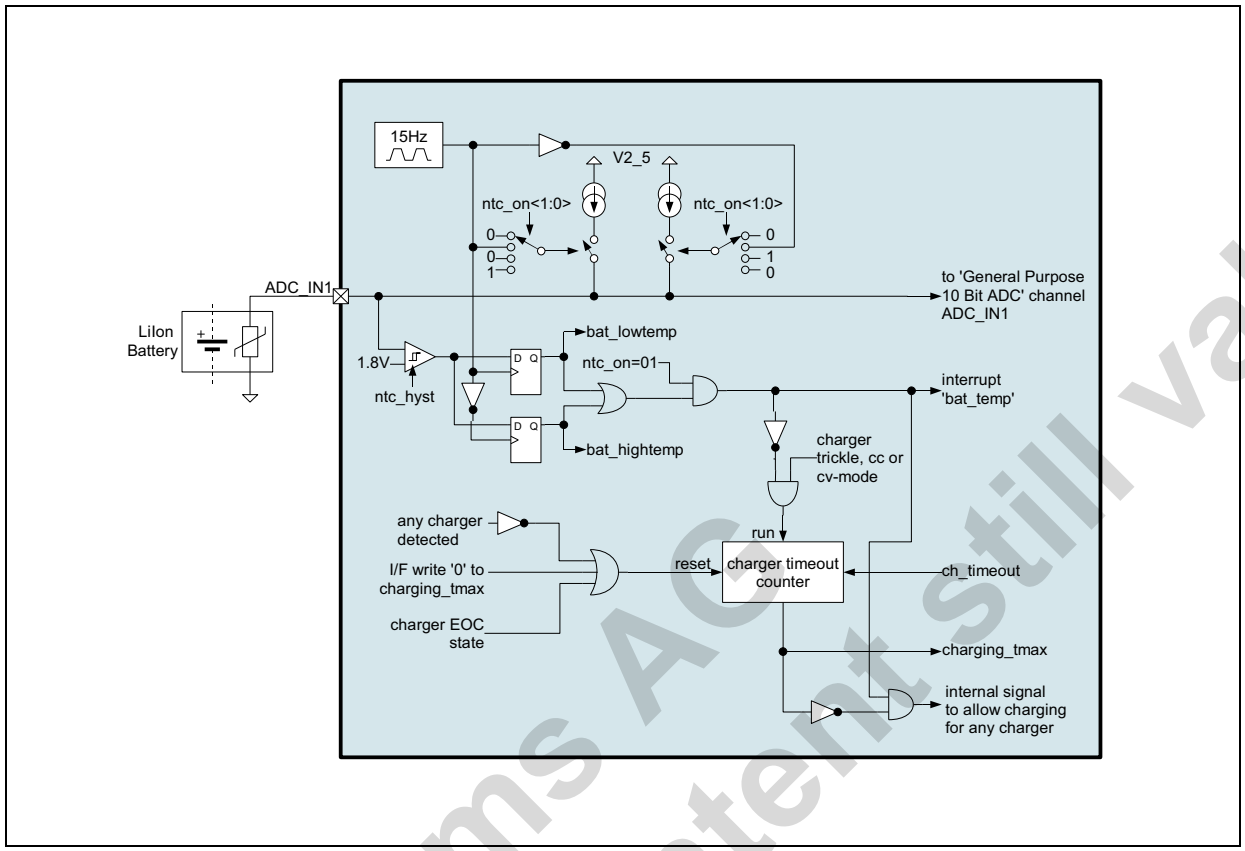


Table 58. NTC Chargersupervision Characteristics, VVBAT=3.0…5.5V; Tamb=–20…+85°C; unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Note
tsample	Sample time for NTC measurement high or low temperature		33		ms	Alternating measurement of the NTC sensor for high temperature and low temperature with two different currents
Vcomp	Comparator threshold for high and low temperature measurement		1.8		V	On pin ADC_IN1, if ntc_on<1:0>=1
IHightemp45deg_10k	High temperature current for 45 deg limit, 10k NTC	-7%	388	+7%	µA	ntc_type=0, ntc_high_temp=0, @ 1.8V threshold
			4.64		kΩ	
IHightemp50deg_10k	High temperature current for 50 deg limit, 10k NTC	-7%	457	+7%	µA	ntc_type=0, ntc_high_temp=1, @ 1.8V threshold
			3.94		kΩ	
IHightemp0deg_10k	High temperature current for 0 deg limit, 10k NTC		60.5		µA	ntc_type=0 @ 1.8V threshold
			29.7		kΩ	
IHightemp45deg_100k	High temperature current for 45 deg limit, 100k NTC		39.2		µA	ntc_type=1, ntc_high_temp=0, @ 1.8V threshold
			4.59		kΩ	
ILowtemp50deg_100k	Low temperature current for 50 deg limit, 100k NTC		46.8		µA	ntc_type=1, ntc_high_temp=1, @ 1.8V threshold
			38.5		kΩ	

Table 58. NTC Chargersupervision Characteristics, VVBAT=3.0…5.5V; Tamb=–20…+85°C; unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Note
ILowtemp0deg_100k	Low temperature current for 0 deg limit, 100k NTC		6.32		µA	ntc_type=1 @ 1.8V threshold
			284		kΩ	
Hystereses	NTC Current hystereses		±4%			(approx. 1º .), ntc_hyst=0
			±8%			(approx. 2º.), ntc_hyst=1
IHightempADC_10k	Current for ADC measurement High temp range, 10k NTC	-7%	234	+7%	µA	ntc_on<1:0>=2, ntc_type=0, ntc_high_temp=0
IHightempADC_100k	Current for ADC measurement High temp range, 100k NTC		23.6		µA	ntc_on<1:0>=2, ntc_type=1, ntc_high_temp=0
ILowtempADC_10k	Current for ADC measurement Low temp range, 10k NTC		36		µA	ntc_on<1:0>=3, ntc_type=0, ntc_high_temp=0
ILowtempADC_100k	Current for ADC measurement Low temp range, 100k NTC		3.7		µA	ntc_on<1:0>=3, ntc_type=1, ntc_high_temp=0

Table 59. Charger supervision bit definitions

Addr:14		Charger supervision			
		These bits define charging timer and battery temp. supervision settings			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
3:0	ch_timeout	ROM	R/W	Charging timeout timer	
				0000b	Charging timeout disabled
				0001b	1 hour
				0010b	1.5 hour
				0011b	2 hour
				0100b	2.5 hour
				0101b	3 hour
				0110b	3.5 hour
				0111b	4 hour
				1000b	4.5 hour
				1001b	5 hour
				1010b	5.5 hour
				1011b	6 hour
				1100b	6.5 hour
				1101b	7 hour
				1110b	7.5 hour
				1111b	8 hour
4	auto_shutdown	ROM	0		(see Reset generator and XON-Key on page 118)

Table 59. Charger supervision bit definitions

Addr:14		Charger supervision			
		These bits define charging timer and battery temp. supervision settings			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
5	ntc_high_temp	ROM	R/W	Selects the high temp level:	
				0	45 º maximum temp
				1	50º maximum temp
				Low temp is always 0º	
6	ntc_hyst	ROM	R/W	Selects the NTC temperature hysteresis	
				0	2º hysteresis
				1	1º hysteresis
7	ntc_type	ROM	R/W	Select the NTC resistor type	
				0	10kΩ NTC resistor
				1	100kΩ NTC resistor

Table 60. FuelGauge

Addr:15		FuelGauge			
		This bit controls first startup out of power on reset			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
7:6	ntc_on	ROM	R/W	00	Disable NTC supervision
				01	Enable NTC supervision
				10	Enable NTC for ADC measurement high temp
				11	Enable NTC for ADC measurement low temp

8.11 Step Down DC/DC Converters

8.11.1 Step Down DC/DC Converters Operating Modes

The step down dcdc converters have four operating modes to deliver different output currents for the applications. The operating mode is selected by setting the register sdx_1A_mode (the default is set by the Boot ROM).

Figure 22. DC/DC step-down SD1, SD2, SD3 Normal Operating Mode; sdx_1A_mode = 0000b

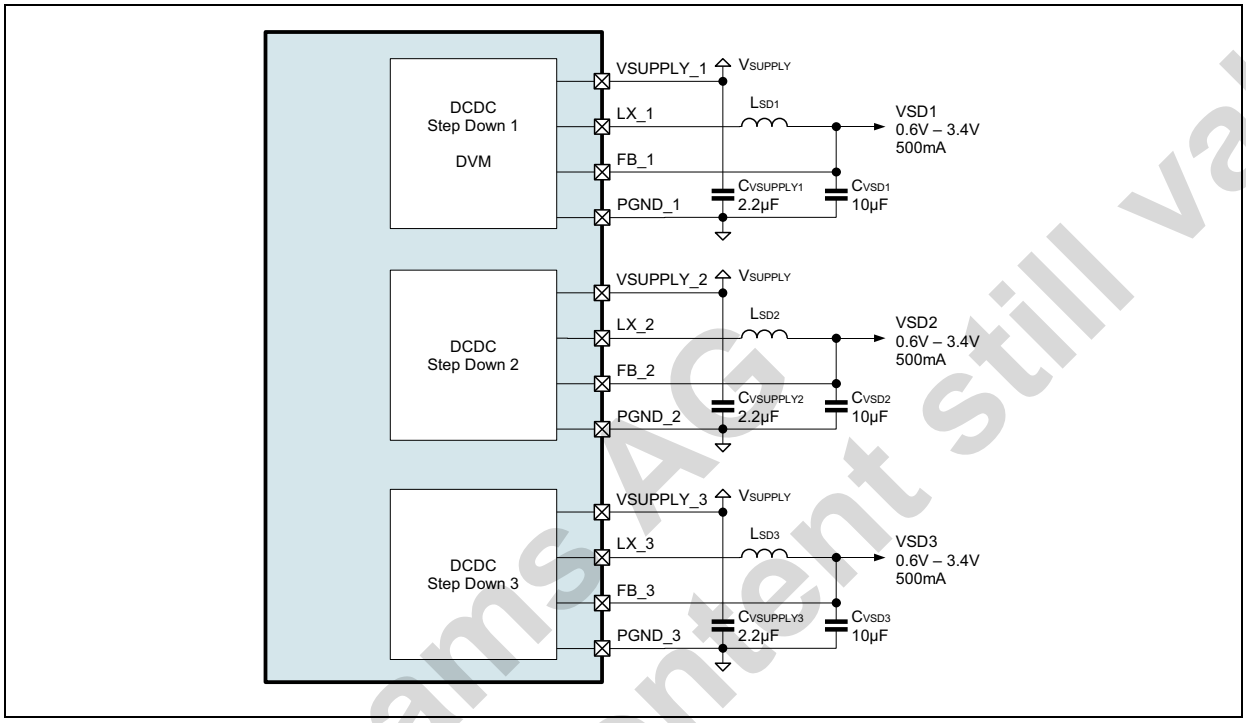
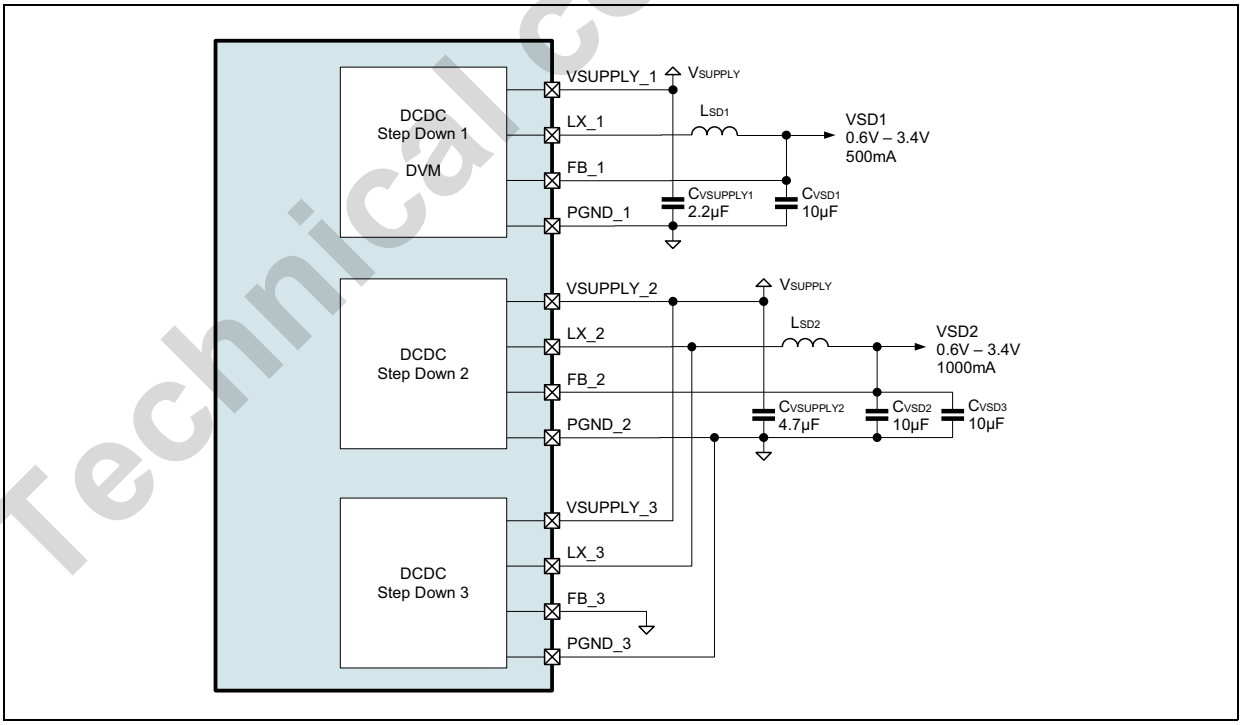


Figure 23. DC/DC step-down SD1, SD2, SD3 1A Operating Mode; sdx_1A_mode = 1010b



If one of the DCDC step down converters is not used for an application, connect it as follows:

Figure 24. DC/DC step-down SD3 (as example) not used

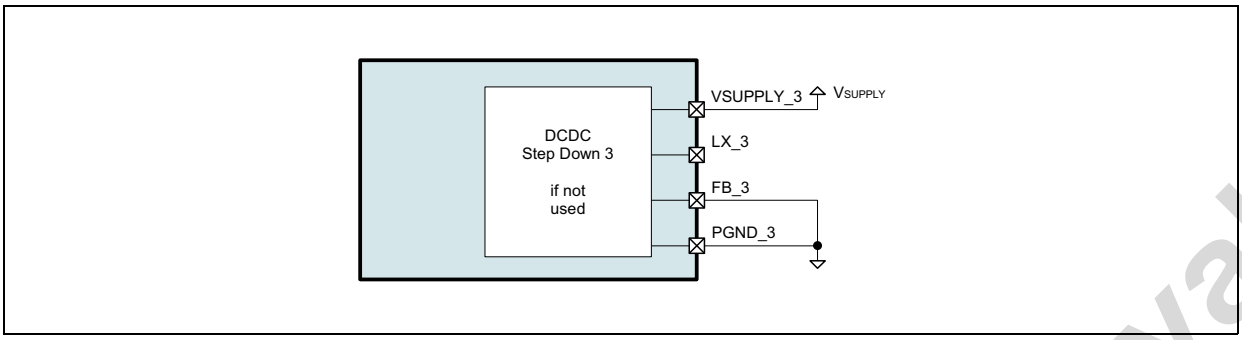
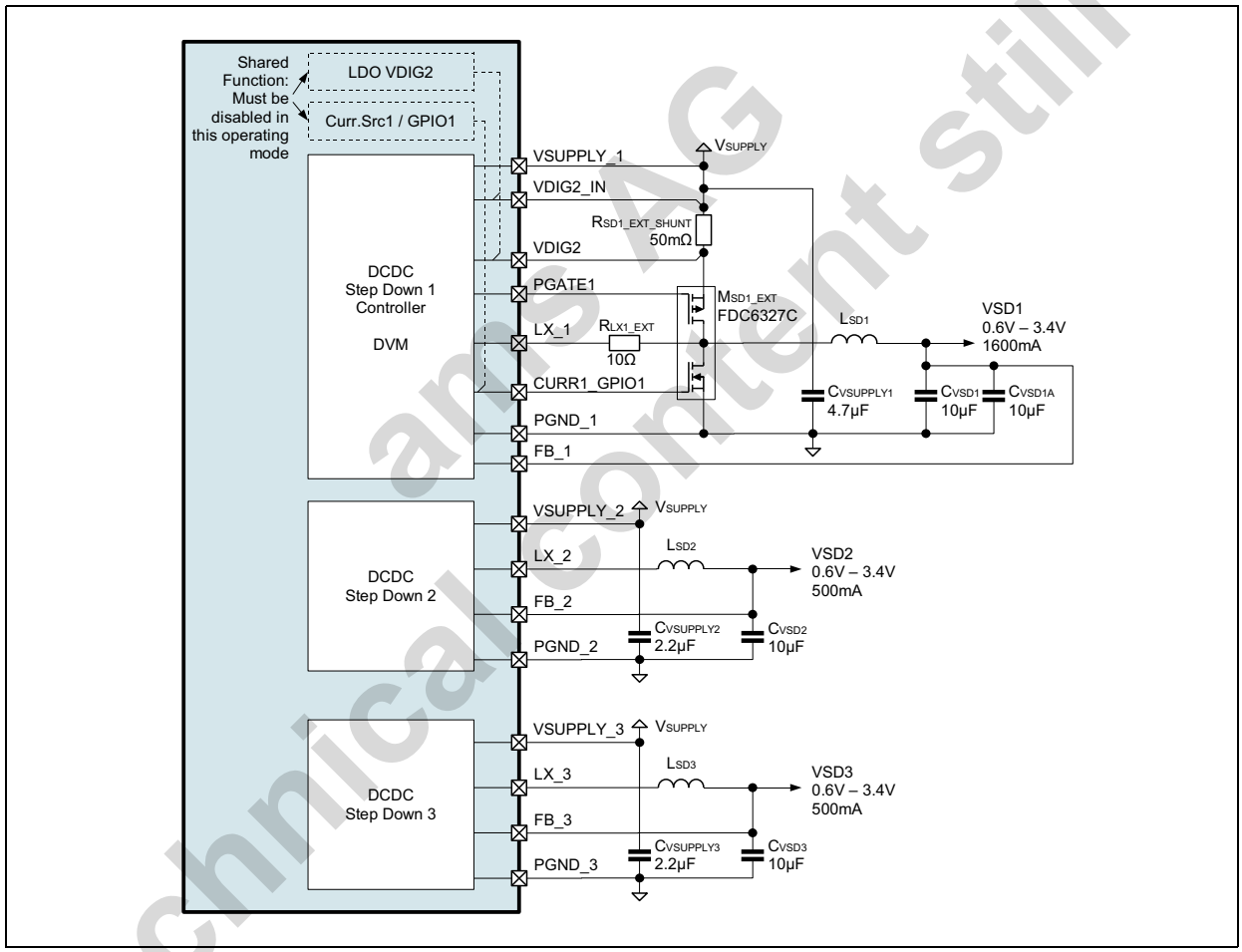
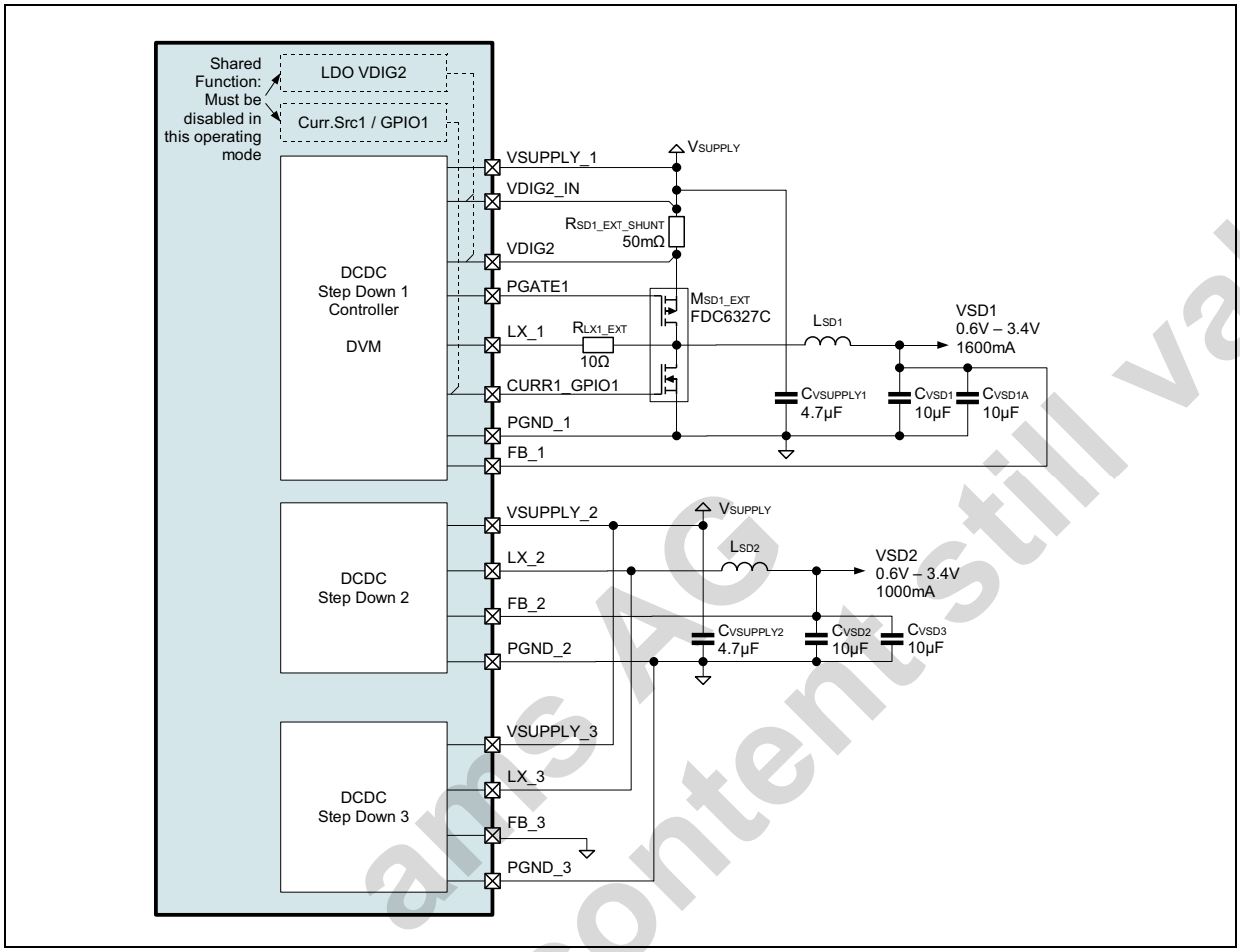


Figure 25. DC/DC step-down SD1, SD2, SD3 External Controller Operating Mode; sdx_1A_mode = 1100b



Note: VCURR_GPIO has to be connected to VSUPPLY if the external controler mode is used.

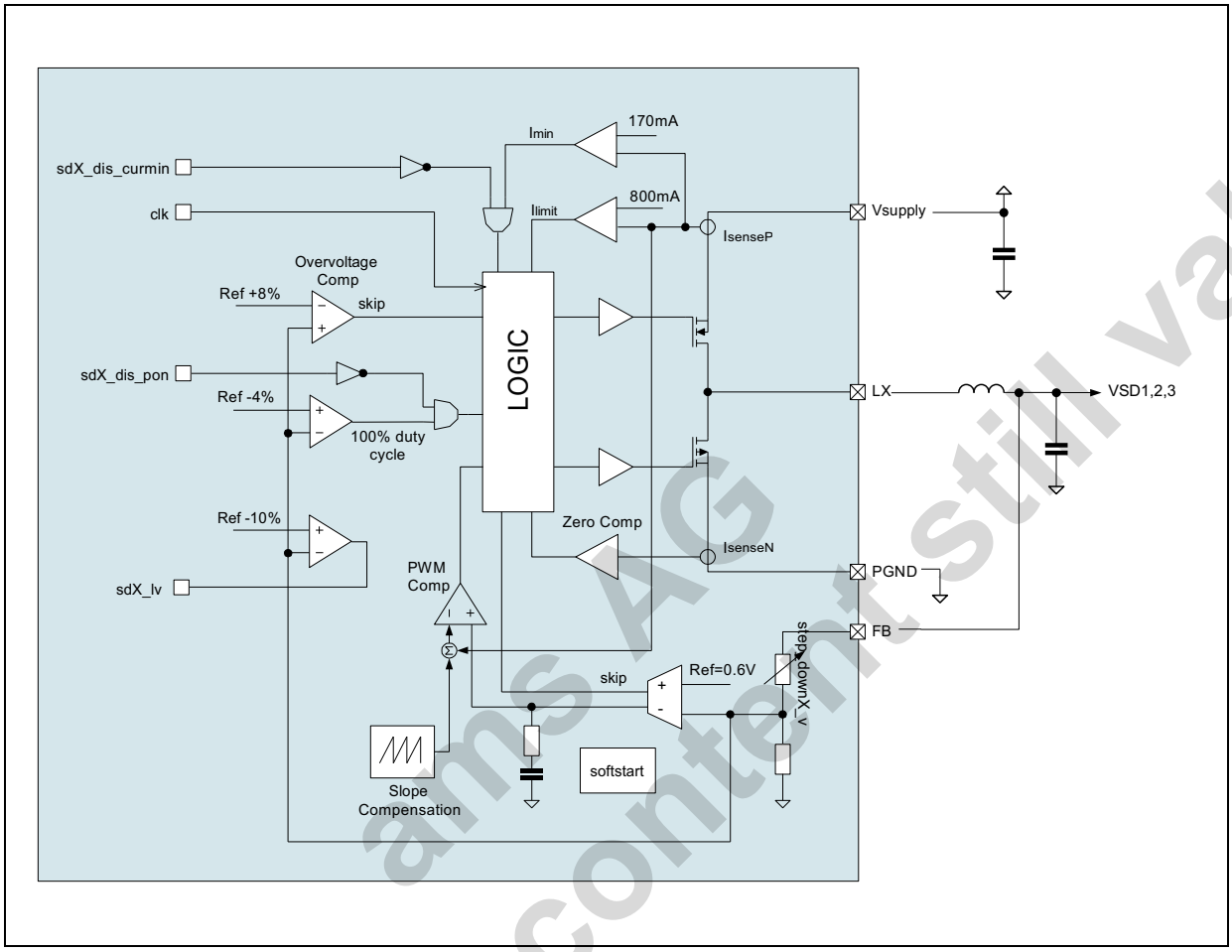
Figure 26. DC/DC step-down SD1, SD2, SD3 External Controller Operating Mode and SD2 in 1A mode; sd1_1A_mode = 1101b



Note: The LDO VDIG2 and the Low voltage current source / GPIO pin CURR1_GPIO1 cannot be used in the 'External Controller' operating mode configuration.
VCURR_GPIO has to be connected to VSUPPLY if the external controler mode is used.

8.11.2 Step Down DC/DC Converter Characteristics

Figure 27. Step Down DC/DC Converter Block diagram



Functional Description

The step-down converter is a high efficiency fixed frequency current mode regulator. By using low resistance internal PMOS and NMOS switches efficiency up to 95% can be achieved. The fast switching frequency allows using small inductors, without increasing the current ripple. The unique feedback and regulation circuit guarantees optimum load and line regulation over the whole output voltage range, up to an output current of 500mA, with an output capacitor of only 10µF. The implemented current limitation protects the DCDC and the coil during overload condition.

To allow optimized performance in different applications, there are bit settings possible, to get the best compromise between high efficiency and low input, output ripple:

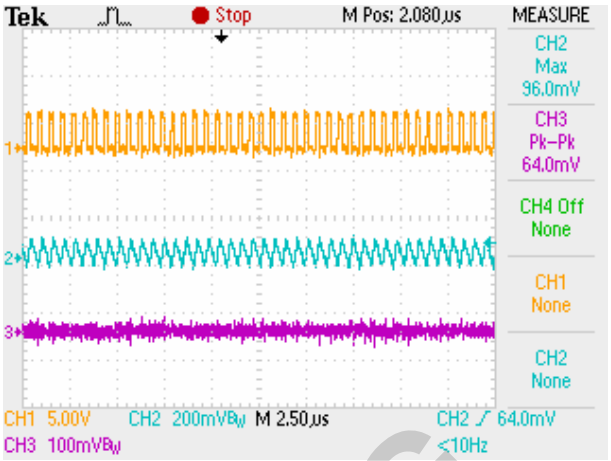
Low ripple, low noise operation:

Bit settings:
sdX_dis_curmin=1

In this mode there is no minimum coil current necessary before switching off the PMOS. As result, the ON time of the PMOS will be reduced down to tmin_on at no or light load conditions, even if the coil current is very small or the coil current is inverted. This results in a very low ripple and noise, but decreased efficiency, at light loads, especially at low input to output voltage differences. Because of the inverted coil current in that case the regulator will not operate in pulse skip mode.

Figure 28. sdX_dis_curmin=1 operation

1: LX voltage, 2:coil current (1mV=1mA) 3: Vout



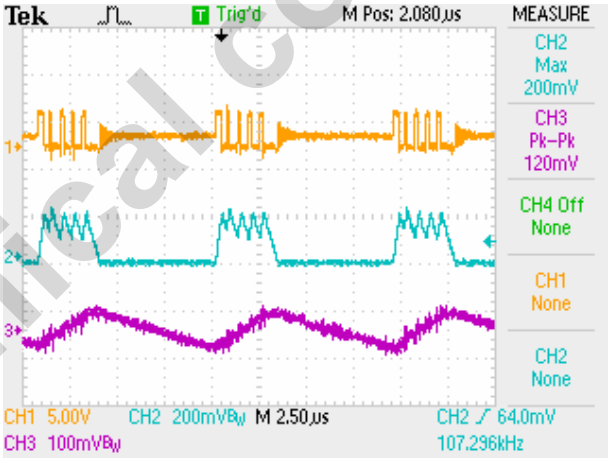
High efficiency operation (default setting):

Bit settings:
sdX_dis_curmin=0

In this mode there is a minimum coil current necessary before switching off the PMOS. As result there are less pulses at low output load necessary, and therefore the efficiency at low output load is increased. This results in higher ripple, and noisy pulse skip operation up to a higher output current.

Figure 29. sdX_dis_curmin=0 operation

1: LX voltage, 2:coil current (1mV=1mA) 3: Vout



It's also possible to switch between these two modes during operation:

For Example:

sdX_dis_curmin=0: System is in idle state. No audio, RF signal. Decreased supply current preferred. Increased ripple doesn't affect system performance.

sdX_dis_curmin=1: System is operating. Audio signal on and/or RF signal used. Decreased ripple and noise preferred. Increased power supply current can be tolerated.

100% PMOS ON mode for low dropout regulation: For low input to output voltage difference the sdX_dis_pon bit can be set, to allow 100% duty cycle of the PMOS transistor.

Low power mode: The sdX_lpo mode bit can be set all the time. This mode allows internal power down, of not used blocks during pulseskip mode, which results in a better efficiency at light output loads.

Inductor setting: The step down regulator is optimized for 2.2µH at 2.2MHz and 4.7µH at 1.1MHz

Table 61. Step Down DC/DC Converter parameters

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{IN}	Input voltage	3.0		5.5	V	PIN VSUPPLY_1,VSUPPLY_2, VSUPPLY_3
V_{OUT}	Regulated output voltage	0.6		3.3	V	
V_{OUT_tol}	Output voltage tolerance	-50		+50	mV	output voltage <2.0V
		-100		+100	mV	output voltage >2.0V
I_{LIMIT}	Current limit		800		mA	
R_{PSW}	P-Switch ON resistance			0.5	Ω	V_SUPPLYx=3.0V
R_{NSW}	N-Switch ON resistance			0.5	Ω	V_SUPPLYx=3.0V
I_{load}	Load current	0		500	mA	
f_{SW}	Switching frequency		2.2		MHz	sdX_frequ=0, f_{clk_int} =2.2MHz
			1.1		MHz	sdX_frequ=1, f_{clk_int} =2.2MHz
ηeff	Efficiency		90		%	Iout=100mA, Vout=2.3V, Vsup.=3V
I_{VDD}	Current consumption		250		µA	Operating current without load
			100			Low power mode current
			0.1			Shutdown current
t_{MIN_ON}	Minimum on time		80		ns	
t_{MIN_OFF}	Minimum off time		40		ns	
External Components						
CVSD1-3, CVSD1A	Output capacitor	8.0	10		µF	Ceramic X5R or X7R
CVSUPPLY1-3	Input capacitor		2.2		µF	Ceramic X5R or X7R
			4.7		µF	Ceramic X5R or X7R; CVSUPPLY1 in external controller mode or 1A operating mode
LSD1-SD3	Inductor		2.2		µH	sdX_frequ=0, ± 10% tolerance
			4.7			sdX_frequ=1, ± 10% tolerance
			2.2			SD1 external controller mode; use sd1_freq=1 (1.1Mhz)

Table 62. Step Down DC/DC Bit definitions

Addr:35		Step Down Control1		
		These bits configures the step down converters		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	sd1_psw_on	0	R/W	Only if *sd1_on* = 0, switch on PSW (0.5Ω PMOS)
1	-	0	n/a	
2	-	0	n/a	
3	sd1_nsw_on	0	R/W	Only if *sd1_on* = 0, switch on NSW (0.5Ω NMOS)
4	sd2_psw_on	0	R/W	Only if *sd2_on* = 0, switch on PSW (0.5Ω PMOS)
5	-	0	n/a	
6	-	0	n/a	
7	sd2_nsw_on	0	R/W	Only if *sd2_on* = 0, switch on NSW (0.5Ω NMOS)

Table 63. Step Down DC/DC Bit definitions

Addr:36		Step Down Control2			
		These bits configures the step down converters			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
0	sd3_psw_on	0	R/W	Only if *sd3_on* = 0, switch on PSW (0.5Ω PMOS)	
1	-	0	n/a		
2	-	0	n/a		
3	sd3_nsw_on	0	R/W	Only if *sd3_on* = 0, switch on NSW (0.5Ω NMOS)	
4	sdX_lpo	0	R/W	Step down low power mode:	
				0	Increased current consumption in pulseskip mode
				1	Decreased current consumption in pulseskip mode
5	sd1_dis_pon	0	R/W	Step down pon feature control	
				0	PON feature enabled: 100% duty cycle (pmos always on) if output voltage drops more than 4%. Increased output ripple in that operation.
				1	PON feature disabled: Maximum dutycycle=1-(tmin_off*fsw)
6	sd2_dis_pon	0	R/W	Step down pon feature control	
				0	PON feature enabled: 100% duty cycle (pmos always on) if output voltage drops more than 4%. Increased output ripple in that operation.
				1	PON feature disabled: Maximum dutycycle=1-(tmin_off*fsw)
7	sd3_dis_pon	0	R/W	Step down pon feature control	
				0	PON feature enabled: 100% duty cycle (pmos always on) if output voltage drops more than 4%. Increased output ripple in that operation.
				1	PON feature disabled: Maximum dutycycle=1-(tmin_off*fsw)

Table 64. Step Down DC/DC Bit definitions

Addr:37		Step Down charger control			
		These bits configures the step down converters			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
3	-	0	n/a		
4	sd1_dis_curmin	0	R/W	Step down curmin feature control	
				0	curmin feature enabled: Inductor current regulated to min 170mA. Higher efficiency in low dropout and low output current operation. Higher output ripple and noise.
				1	curmin feature disabled: Decreased efficiency in low dropout mode and at low output current. Small output ripple and noise.
5	sd2_dis_curmin	0	R/W	Step down curmin feature control	
				0	curmin feature enabled: Inductor current regulated to min 170mA. Higher efficiency in low dropout and low output current operation. Higher output ripple and noise.
				1	curmin feature disabled: Decreased efficiency in low dropout mode and at low output current. Small output ripple and noise.
6	sd3_dis_curmin	0	R/W	Step down curmin feature control	
				0	curmin feature enabled: Inductor current regulated to min 170mA. Higher efficiency in low dropout and low output current operation. Higher output ripple and noise.
				1	curmin feature disabled: Decreased efficiency in low dropout mode and at low output current. Small output ripple and noise.

Table 65. Step Down DC/DC Reg Power1 ctrl Bit definitions

Addr:23		Reg Power1 Ctrl			
		These bits control the on/off function of the step down regulator			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
4	sd1_on	ROM	R/W	Switch on/off the step down1 dc/dc converter; it is possible to on/off control DCDC SD1 by CURR3_GPIO3 or CURR4_GPIO4 (see General Purpose Input / Output (CURR1_GPIO1 … CURR4_GPIO4) on page 30)	
				0	Step Down DC/DC 1 off
				1	Step Down DC/DC 1 on
5	sd2_on	ROM	R/W	Switch on/off the step down2 dc/dc converter; it is possible to on/off control DCDC SD2 by CURR3_GPIO3 or CURR4_GPIO4 (see General Purpose Input / Output (CURR1_GPIO1 … CURR4_GPIO4) on page 30)	
				0	Step Down DC/DC 2 off
				1	Step Down DC/DC 2 on

Table 65. Step Down DC/DC Reg Power1 ctrl Bit definitions

Addr:23		Reg Power1 Ctrl			
		These bits control the on/off function of the step down regulator			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
6	sd3_on	ROM	R/W	Switch on/off the step down3 dc/dc converter; it is possible to on/off control DCDC SD3 by CURR3_GPIO3 or CURR4_GPIO4 (see General Purpose Input / Output (CURR1_GPIO1 … CURR4_GPIO4) on page 30)	
				0	Step Down DC/DC 3 off
				1	Step Down DC/DC 3 on

Table 66. Step Down Voltage1 Bit definitions

Addr:00		Step Down Voltage1			
		These bits control the step down regulator voltage, frequency, clk phase			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
5:0	step_down1_v	ROM	R/W	Control the voltage selection for the step down1 DC/DC converter 000000 0.6 V … (LSB=50mV) 111000 – 11111 3.4 V	
6	sd1_frequ	ROM	R/W	Select the step down1 frequency	
				0	f_{clk_int} (1.6MHz to 2.3 MHz)
				1	$f_{clk\_int}/2$ (0.8MHz to 1.15 MHz)
7	sd1_clkinvert	ROM	R/W	Inverts the input clock of the step down1 converter	

Table 67. Step Down Voltage2 Bit definitions

Addr:01		Step Down Voltage2			
		These bits control the step down regulator voltage, frequency, clk phase			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
5:0	step_down2_v	ROM	R/W	Control the voltage selection for the step down2 DC/DC converter 000000 0.6 V … (LSB=50mV) 111000 – 11111 3.4 V	
6	sd2_frequ	ROM	R/W	Select the step down2 frequency	
				0	f_{clk_int} (1.6MHz to 2.3 MHz)
				1	$f_{clk\_int}/2$ (0.8MHz to 1.15 MHz)
7	sd2_clkinvert	ROM	R/W	Inverts the input clock of the step down1 converter	

Table 68. Step Down Voltage3 Bit definitions

Addr:02		Step Down Voltage3			
		These bits control the step down regulator voltage, frequency, clk phase			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
5:0	step_down3_v	ROM	R/W	Control the voltage selection for the step down3 DC/DC converter 000000 0.6 V … (LSB=50mV) 111000 – 11111 3.4 V	
6	sd3_frequ	ROM	R/W	Select the step down3 frequency	
				0	f_{clk_int} (1.6MHz to 2.3 MHz)
				1	$f_{clk\_int}/2$ (0.8MHz to 1.15 MHz)
7	sd3_clkinvert	ROM	R/W	Inverts the input clock of the step down1 converter	

Table 69. Step down1 high current and DVM definitions

Addr:17		Charge Pump Control			
		These bits control the step down high current mode and DVM step size			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
3:2	sd1_dvm_time	ROM	R/W	Time step of DVM voltage change of step down1 If voltage of step down1 (step_down1_v) is changed during operation, voltage is decreased or increased by 25 mV steps with the following time separation between steps:	
				00	0 µsec, immediate change (no DVM)
				01	4 µsec
				10	8 µsec
				11	16 µsec
7:4	sdx_1A_mode	ROM	R/W	Select 1A mode of step down2 (combined operation of SD2 and SD3 with a single coil and up to 1A output current) and/or controller mode of SD1	
				1010	1A mode selected Controlled by SD2 The following pins have to be connected: VSUPPLY2<->VSUPPLY3, LX2<->LX3, PGND2<->PGND3 Stepdown3 is not usable in that mode
				1100	External controller mode. LDO DIG1 and current sink / GPIO CURR1_GPIO1 cannot be used. Set ldo_dig1_on=0, GPIO1Mode=111b (tristate), GPIO1Pulls=00b (no pull-up or pull-down)
				1101	External controller mode SD1, and 1A mode controlled by SD2 The following pins have to be connected: VSUPPLY2<->VSUPPLY3, LX2<->LX3, PGND2<->PGND3 Stepdown3 is not usable in that mode
				all other codes (0000...1001,1011,1110...1111) normal mode	

Table 70. Step Down DC/DC Bit definitions

Addr:133		Step Down Control3			
		Configurate the SD converters to reduce voltage drops on fast transient high current load steps. Double the output capacitor size has to be used!			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
0	sd1_uvlimit	0	R/W	0	Normal operation
				1	Enable SD1 undervoltage limit.
1	sd2_uvlimit	0	R/W	0	Normal operation
				1	Enable SD3 undervoltage limit.
2	sd3_uvlimit	0	R/W	0	Normal operation
				1	Enable SD3 undervoltage limit.

8.11.3 Typical Performance Characteristics

Figure 30. DC/DC step-down Efficiency (sdX_dis_curmin=0, sdX_lpo=0)

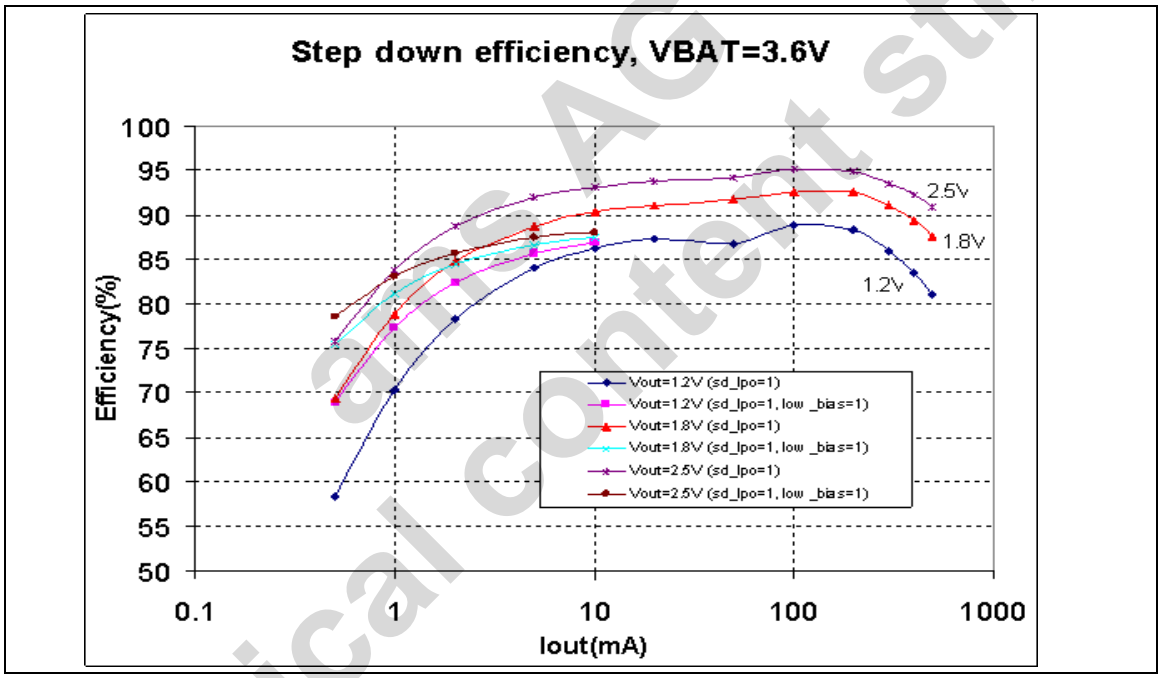
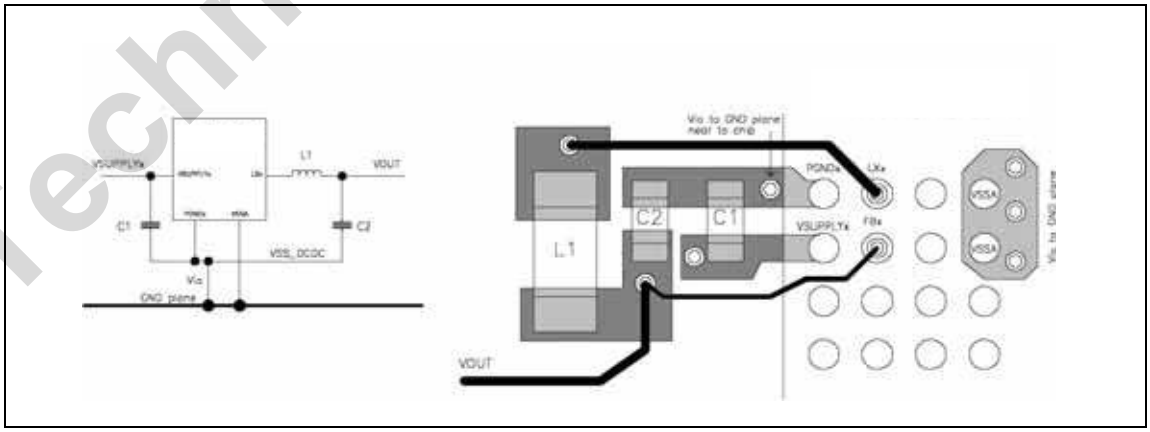


Figure 31. PCB Layout recommendation



8.12 Low Dropout Regulators (LDO)

The low dropout regulators are linear high performance regulators with programmable output voltage.

They are controlled by the following registers:

Table 71. LDO_RF1 voltage bit definitions

Addr:03		LDO_RF1 voltage			
		These bits control the LDO_RF1 voltage and mode			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
4:0	ldo_rf1_v	ROM	R/W	Control the voltage selection for LDO VRF_1 00000 1.85V … (LSB=50mV) 11111 3.40V	
5	rf1_lcurr_en	ROM	R/W	0	current limitation = Ilimit
				1	current limitation Ilimit=Ilimit/2
6	rf1_swprot_en	ROM	R/W	If '1' current limitation is enabled, if RF1-LDO is operating as High side switch	

Table 72. LDO_RF2 voltage bit definitions

Addr:04		LDO_RF2 voltage			
		These bits control the LDO_RF2 voltage and mode			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
4:0	ldo_rf2_v	ROM	R/W	Control the voltage selection for LDO VRF_2 00000 1.85V … (LSB=50mV) 11111 3.40V	
5	rf2_lcurr_en	ROM	R/W	0	current limitation = Ilimit
				1	current limitation Ilimit=Ilimit/2

Table 73. LDO_RF3 voltage bit definitions

Addr:05		LDO_RF3 voltage			
		These bits control the LDO_RF3voltage and mode			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
4:0	ldo_rf3_v	ROM	R/W	Control the voltage selection for LDO VRF_3 00000 1.85V … (LSB=50mV) 11111 3.40V	
5	rf3_lcurr_en	ROM	R/W	0	current limitation = Ilimit
				1	current limitation Ilimit=Ilimit/2
6	rf3_hotplug_en	ROM	R/W	0	normal mode
				1	200mA current limited switch, if bit rf3_sw=1 (rf3_lcurr_en=0)

Table 74. LDO_DIG1 voltage bit definitions

Addr:06		LDO_DIG1 voltage		
		These bits control the LDO_DIG1 voltage		
Bit	**Bit Name**	**Default**	**Access**	**Description**
5:0	ldo_dig1_v	ROM	R/W	Control the voltage selection for LDO DIG_1 (see Table 82)

Table 75. LDO_DIG2 voltage bit definitions

Addr:07		LDO_DIG2 voltage		
		These bits control the LDO_DIG2 voltage		
Bit	**Bit Name**	**Default**	**Access**	**Description**
5:0	ldo_dig2_v	ROM	R/W	Control the voltage selection for LDO DIG_2(see Table 82)

Table 76. LDO_DIG3 voltage bit definitions

Addr:08		LDO_DIG3 voltage		
		These bits control the LDO_DIG3 voltage		
Bit	**Bit Name**	**Default**	**Access**	**Description**
5:0	ldo_dig3_v	ROM	R/W	Control the voltage selection for LDO DIG_3(see Table 82)

Table 77. LDO_DIG4 voltage bit definitions

Addr:09		LDO_DIG4 voltage		
		These bits control the LDO_DIG4 voltage		
Bit	**Bit Name**	**Default**	**Access**	**Description**
5:0	ldo_dig4_v	ROM	R/W	Control the voltage selection for LDO DIG_4(see Table 82)

Table 78. LDOs Reg Power1 ctrl Bit definitions

Addr:23		Reg Power1 Ctrl		
		These bits control the on/off function of the ldo regulator		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	ldo_rf1_on	ROM	R/W	Switch on control of RF1 LDO; Important: Set rf1_sw=0 before setting ldo_rf1_on=1; it is possible to on/off control LDO RF_1 by CURR3_GPIO3 or CURR4_GPIO4 (see General Purpose Input / Output (CURR1_GPIO1 … CURR4_GPIO4) on page 30)
1	ldo_rf2_on	ROM	R/W	Switch on control of RF2 LDO; Important: Set rf2_sw=0 before setting ldo_rf2_on=1; it is possible to on/off control LDO RF_2 by CURR3_GPIO3 or CURR4_GPIO4 (see General Purpose Input / Output (CURR1_GPIO1 … CURR4_GPIO4) on page 30)
2	ldo_dig1_on	ROM	R/W	Switch on control of DIG1 LDO; it is possible to on/off control LDO DIG_1 by CURR3_GPIO3 or CURR4_GPIO4 (see General Purpose Input / Output (CURR1_GPIO1 … CURR4_GPIO4) on page 30)
3	ldo_dig2_on	ROM	R/W	Switch on control of DIG2 LDO. do not set if DCDC SD1 is in external controller mode (if sd1_1A_mode = 1100b). it is possible to on/off control LDO DIG_2 by CURR3_GPIO3 or CURR4_GPIO4(see General Purpose Input / Output (CURR1_GPIO1 … CURR4_GPIO4) on page 30)

Table 79. LDOs Reg Power2ctrl Bit definitions

Addr:30		Reg Power2 Ctrl		
		These bits control the on/off function of the ldo regulator		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	ldo_rf3_on	ROM	R/W	Switch on control of RF3 LDO; Important: Set rf3_sw=0 before setting ldo_rf3_on=1
1	ldo_dig3_on	ROM	R/W	Switch on control of DIG3 LDO; it is possible to on/off control LDO DIG_3 by CURR3_GPIO3 or CURR4_GPIO4 (see General Purpose Input / Output (CURR1_GPIO1 … CURR4_GPIO4) on page 30)'
2	ldo_dig4_on	ROM	R/W	Switch on control of DIG4 LDO
3	rf1_sw	ROM	R/W	If '1' RF1-LDO is operating as High side switch (Ron=1Ω), valid if ldo_rf1_on=0
4	rf2_sw	ROM	R/W	If '1' RF2-LDO is operating as High side switch (Ron=1Ω), valid if ldo_rf2_on=0
7	rf3_sw	ROM	R/W	If '1' RF3-LDO is operating as High side switch (Ron=1Ω), valid if ldo_rf3_on=0

8.12.1 RF LDO's (VRF_1, VRF_2, VRF_3)

These LDO's are designed to supply sensitive analogue circuits like LNA's, Transceivers, VCO's and other critical RF components of cellular radios. Another application is the supply of audio devices or as a reference for AD and DA converters. The design is optimized to deliver the best compromise between quiescent current and regulator performance for battery powered devices.

Stability is guaranteed with ceramic output capacitors of 1µF ±20% (X5R) or 2.2µF +100/-50% (Z5U) for RF2**,** RF3 and 2.2µF ±20% (X5R) or 4.7µF +100/-50% (Z5U) for RF1. The low ESR of these caps ensures low output impedance at high frequencies. Regulation performance is excellent even under low dropout conditions, when the power transistor has to operate in linear mode. Power supply rejection is high enough to suppress the PA-ripple on the battery in TDMA systems at the output. The low noise performance allows direct connection of noise sensitive circuits without additional filtering networks. The low impedance of the power device enables the device to deliver up to I_{OUT} current even at nearly discharged batteries without any decrease of performance.

With vrf2_lcurr_en=0 and vrf3_lcurr_en=0 the regulator VRF_2, VRF_3 can deliver up to 250mA
With vrf1_lcurr_en=0 the regulator VRF_1 can deliver up to 400mA

Figure 32. Analog LDO Block diagram

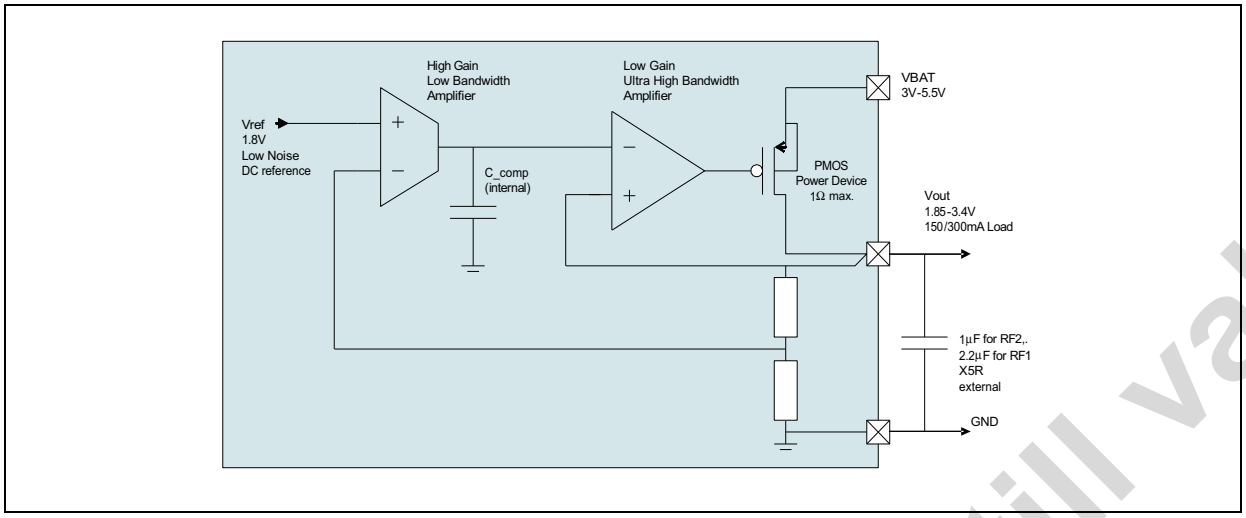


Table 80. Analog LDO (VRF_1, VRF_2, VRF_3) Characteristics, Vx_IN=4V; ILOAD=150mA; Tamb=25ºC; CLOAD =2.2µF (Ceramic); unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Unit	Note
Vx_IN	Supply voltage rage	3		5.5	V	
IOUT	Output current[1]	0		150	mA	VRF_2, rf2_lcurr_en=1 VRF_3, rf3_lcurr_en=1
		0		200		VRF_1, rf1_lcurr_en=1
		0		250		VRF_2, rf2_lcurr_en=0 VRF_3, rf3_lcurr_en=0
		0		400		VRF_1, rf1_lcurr_en=0
R_{ON}	On resistance			0.5	Ω	VRF_1
				1	Ω	VRF_2, VRF_3
PSRR	Power supply rejection ratio	70			dB	f=1kHz
		40				f=100kHz
I_{OFF}	Shut down current			100	nA	
I_{VDD}	Supply current			50	µA	without load
Noise	Output noise			50	μV_{rms}	10Hz < f < 100kHz
t_{start}	Startup time			200	µs	VRF_1,2,3 are set to low current during startup time
V_{out}	Output voltage	1.85		2.85	V	VRFX_IN>3.0V, VRF_1 @ Iout=300mA, VRF_2 and VRF_3 @ Iout=150mA (X=1,2)
		1.85		3.4	V	VRFX_IN>3.55V, VRF_1 @ Iout=300mA, VRF_2 and VRF_3@ Iout=150mA (X=1,2)
V_{out_tol}	Output voltage tolerance	-50		50	mV	
$V_{LineReg}$	Line regulation	-1		1	mV	Static
		-10		10		Transient; Slope: t_r=10µs

Table 80. Analog LDO (VRF_1, VRF_2, VRF_3) Characteristics, Vx_IN=4V; ILOAD=150mA; Tamb=25ºC; CLOAD =2.2µF (Ceramic); unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Unit	Note
$V_{LoadReg}$	Load regulation	-1		1	mV	Static
		-10		10		Transient; Slope: t_r=10µs
$I_{LIMIT\_VRF1\_HCURR}$	Current limitation		800		mA	VRF_1, rf1_lcurr_en=0
$I_{LIMIT\_VRF1\_LCURR}$	Current limitation		400		mA	VRF_1, rf1_lcurr_en=1 and during startup
$I_{LIMIT\_VRF2,3\_L}$	Current limitation VRF_2,3 low current limit		300		mA	rf2_lcurr_en=1, rf3_lcurr_en=1
$I_{LIMIT\_VRF2,3\_H}$	Current limitation VRF_2,3 high current limit		500		mA	rf2_lcurr_en=0, rf3_lcurr_en=0
C_{LOAD_RF1}	Load capacitor	2		5	µF	ceramic only (VRF_1)
$C_{LOAD\_RF2,3\_L}$	Load capacitor	1		5	µF	ceramic only (VRF_2,3) for rf1_lcurr_en=1 and rf2_lcurr_en=1
$C_{LOAD\_RF2,3\_H}$	Load capacitor	2		5	µF	ceramic only (VRF_2,3) for rf1_lcurr_en=0 and rf2_lcurr_en=0

1. Guaranteed by design and verified by laboratory evaluation and characterization; not production tested.

8.12.2 Digital LDO's (VDIG_1, VDIG_2, VDIG_3, VDIG_4)

The Digital LDO's can be used in any medium power system or subsystem where quiescent power consumption of the regulator itself has to be minimized without sacrificing its performance. For its stability a cheap 1µF ceramic capacitor is required. The 5V charge pump will be switched on automatically, if one of the digital LDO's are switched on.

Figure 33. Digital LDO Block diagram

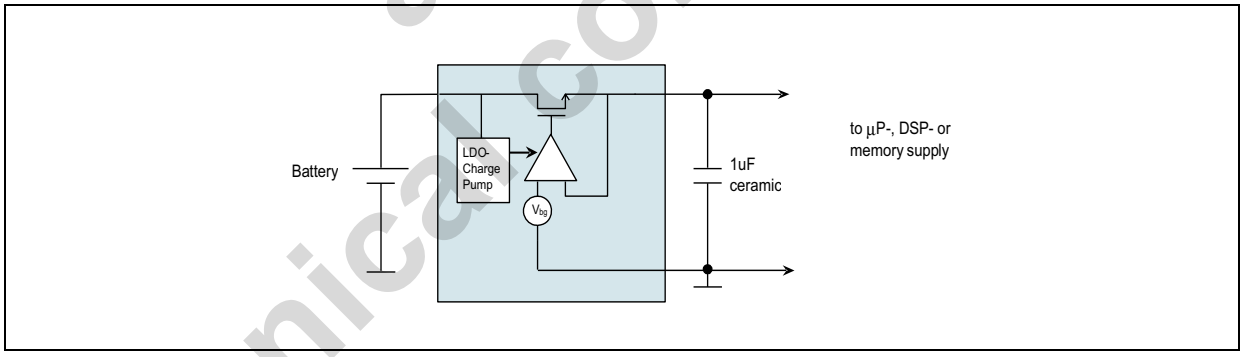


Table 81. Digital LDO (VDIG1, VDIG2, VDIG3, VDIG4) Characteristics,VSUPPLY=4V; ILOAD=200mA; Tamb=25ºC; CLOAD =1µF (Ceramic); unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Unit	Note
VDIGX_IN	Supply voltage range	1		5.5	V	
IOUT	Output current[1]	0		200	mA	Vout<2.2V; VDIGX_IN>Vout+RON*IOUT
		0		100	mA	Vout<2.5V; VDIGX_IN>Vout+RON*IOUT
R_{ON}	On resistance			4	Ω	Vout<2.2V

Table 81. Digital LDO (VDIG1, VDIG2, VDIG3, VDIG4) Characteristics,VSUPPLY=4V; ILOAD=200mA; Tamb=25ºC; CLOAD =1µF (Ceramic); unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Unit	Note
PSRR	Power supply rejection ratio	60			dB	f=1kHz
		30				f=100kHz
I_{OFF}	Shut down current			100	nA	
I_{VDD}	Supply current			20	µA	without load
t_{start}	Startup time			200	µs	
V_{out}	Output voltage	0.75		2.20	V	Vsupply>3.0V, VCP=5.2V, Iout<200mA
				2.5	V	Vsupply>3.0V, VCP=5.2V, Iout<100mA
$V_{out\_tol\_lv}$	Output voltage tolerance	-50		50	mV	Vout<1.85V
$V_{out\_tol\_hv}$	Output voltage tolerance	-60		60	mV	Vout>1.85V
$V_{LineReg}$	Line regulation	-10		10	mV	Static
		-50		50		Transient; Slope: t_r=10µs
$V_{LoadReg}$	Load regulation	-20		20	mV	Static
		-50		50		Transient; Slope: t_r=10µs
I_{LIMIT}	Current limitation		400		mA	

1. Guaranteed by design and verified by laboratory evaluation and characterization; not production tested

Table 82. Digital LDO (VDIG_1.4) Programming voltage table

Code (d)	Code (b)	VOUT(V)	Code (d)	Code (b)	VOUT(V)
0	000000	0.75	22	010110	1.80
1	000001	0.80	23	010111	1.80
2	000010	0.85	24	011000	1.80
3	000011	0.90	25	011001	1.80
4	000100	0.95	26	011010	1.80
5	000101	1.00	27	011011	1.80
6	000110	1.05	28	011100	1.80
7	000111	1.10	29	011101	1.80
8	001000	1.15	30	011110	1.80
9	001001	1.20	31	011111	1.80
10	001010	1.25	32	100000	1.50 (do not use)
11	001011	1.30	33	100001	1.60 (do not use)
12	001100	1.35	34	100010	1.70 (do n0t use)
13	001101	1.40	35	100011	1.80 (do not use)
14	001110	1.45	36	100100	1.90
15	001111	1.50	37	100101	2.00
16	010000	1.55	38	100110	2.10
17	010001	1.60	39	100111	2.20
18	010010	1.65	40	101000	2.30
19	010011	1.70	41	101001	2.40
20	010100	1.75	42	101010	2.50
21	010101	1.80			

Note: Full performance for Vout ≤ 2.20V; max. 100mA output current for Vout ≤ 2.50V; do not use values Vout>2.50V

8.12.3 Low power LDO (V2_5)

The Low power LDO V2_5 is needed to supply the chip core (analog and digital) of the device. It is designed to get the lowest possible power consumption, and still offering reasonable regulation characteristics. The regulator has three supply inputs selecting automatically the higher one. This gives the possibility to supply the chip core either with the battery or with the charger depending on the conditions. Bulk switch comparators are used to avoid any parasitic current flow. To ensure high PSRR and stability, a low-ESR ceramic capacitor of min. 1µF must be connected to the output.

Table 83. Low power LDO (V2_5) Characteristics,VBAT=4V; ILOAD_ext=0; Tamb=25ºC; CLOAD =2.2 µF (Ceramic); unless otherwise specified

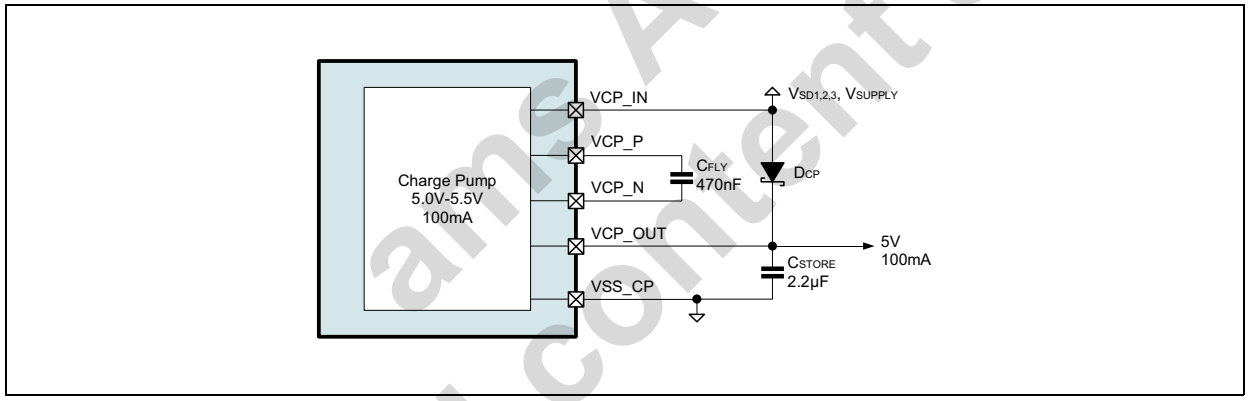
Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{BAT}	Supply voltage rage	2.8		5.5	V	
$V_{CHARGER}$		4		15		
R_{ON}	On resistance			50	Ω	Guaranteed per design
PSRR	Power supply rejection ratio	60			dB	f=1kHz
		40				f=100kHz

Table 83. Low power LDO (V2_5) Characteristics,VBAT=4V; ILOAD_ext=0; Tamb=25ºC; CLOAD =2.2 µF (Ceramic); unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Unit	Note
I_{OFF}	Shut down current			100	nA	
I_{VDD}	Supply current			3	µA	Guaranteed per design, consider chip internal load for measurements.
t_{start}	Startup time			200	µs	
V_{out}	Output voltage	2.4	2.5	2.6	V	
V_{out_tol}	Output voltage tolerance	-50		50	mV	
$V_{LineReg}$	Line regulation	-10		10	mV	Static
		-50		50		Transient; Slope: t_r=10s
$V_{LoadReg}$	Load regulation	-10		10	mV	Static
		-50		50		Transient; Slope: t_r=10s

8.13 5V Charge Pump

Figure 34. 5V Charge Pump Block diagram



The charge pump uses the pad VCP_IN as input, regulates and doubles its voltage with the help of the flying capacitor between CAPP and CAPN to its output VCP_OUT (the output is automatically limited not to exceed VCPOUT). If the bit cp_pulseskip is set, the charge pump operates in pulse skip mode, and only starts cycles if its output voltage is below this level. In this mode the supply current is reduced, but the output ripple is increased.

The charge pump requires the following external components:

Table 84. Charge Pump External Components

Symbol	Parameter	Min	Typ	Min	Unit	Note
C_{FLY}	External flying capacitor	370	470	850	nF	Ceramic X5R or X7R low-ESR capacitor between CAPP and CAPN
C_{STORE}	External storage capacitor	1.76	2.2	2.64	µF	Ceramic X5R or X7R low-ESR capacitor between VCP_OUT and VSS
Dout	Schottky Diode for startup between VCP_IN and VCP_OUT	1			A	Peak current of schottky Diode

Make the connections of the external capacitors as short as possible.

Table 85. Charge Pump Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{CPIN}	Charge Pump input voltage	3.0		5.5	V	
f_{IN}	Switching frequency		1.1		MHz	cp_freq=0, f_{clk_int}=2.2MHz
			0.55		MHz	cp_freq=1, f_{clk_int}=2.2MHz
I_{CPOUT}	Output Current	0.0		100	mA	VCP_IN = 3.2V, Clock = f_{clk_int}/2; cp_pulseskip=0; fin=1.1MHz
V_{CPOUT}	Output Voltage	4.9	5.2	5.6	V	
V_{CPSKIP}	Output Voltage during pulseskip		4.92		V	Use with cp_frequ=1 only
I_{CP_noload}	Supply current without load		2		mA	1.1MHz switching frequency
$I_{CP\_pulseskip}$	Charge pump supply current without load in pulseskip mode		20		µA	cp_pulseskip=1 and cp_frequ=1

Table 86. CP Power1 ctrl Bit definitions

Addr:23		Reg Power1 Ctrl		
		These bits control the on/off function of the ldo regulator		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7	cp_on	ROM	R/W	Switch on of the charge pump block, charge pump is automatically activated if any of the following blocks are active: VDIG_1, VDIG_2, VDIG_3, VDIG_4

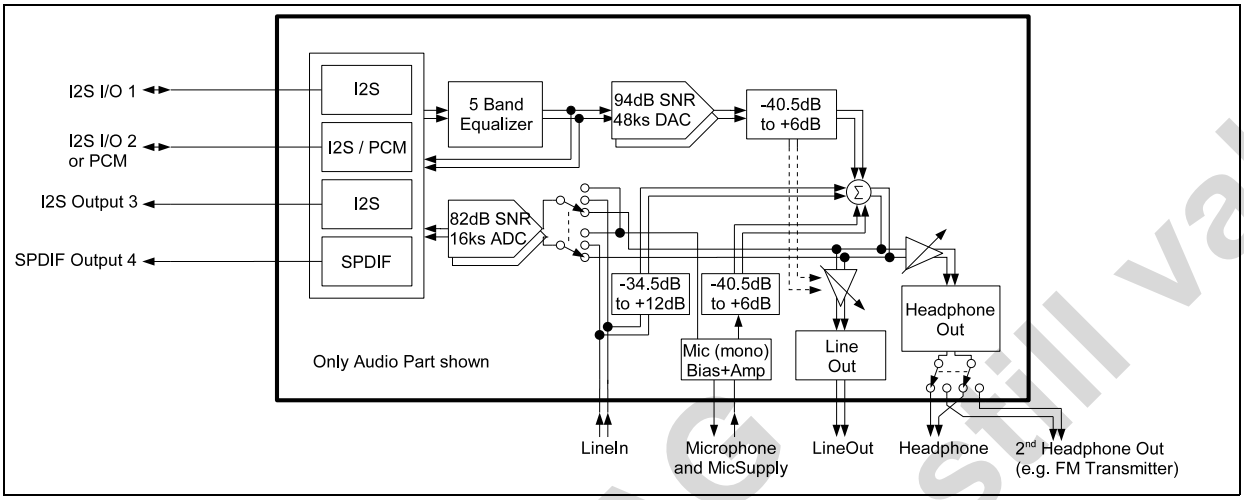
Table 87. Charge Pump Bit definitions

Addr:17		Charge Pump Control			
		These bits control the Charge Pump			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
0	cp_pulseskip	ROM	R/W	Switches on the pulseskip mode of the charge pump	
				0	Normal fixed frequency mode
				1	Pulse skip, low power mode (Set cp_frequ=1 in this mode)
1	cp_freq	ROM	R/W	Defines the clock frequency of the step up dc/dc converter	
				0	f_{clk_int}/2 (0.8 to 1.15 MHz)
				1	f_{clk_int}/4 (0.4 to 0.575 MHz)

9 Detailed Description- Audio Functions

The audio functions consist of all the audio features of AS3658 as shown in the following block diagram:

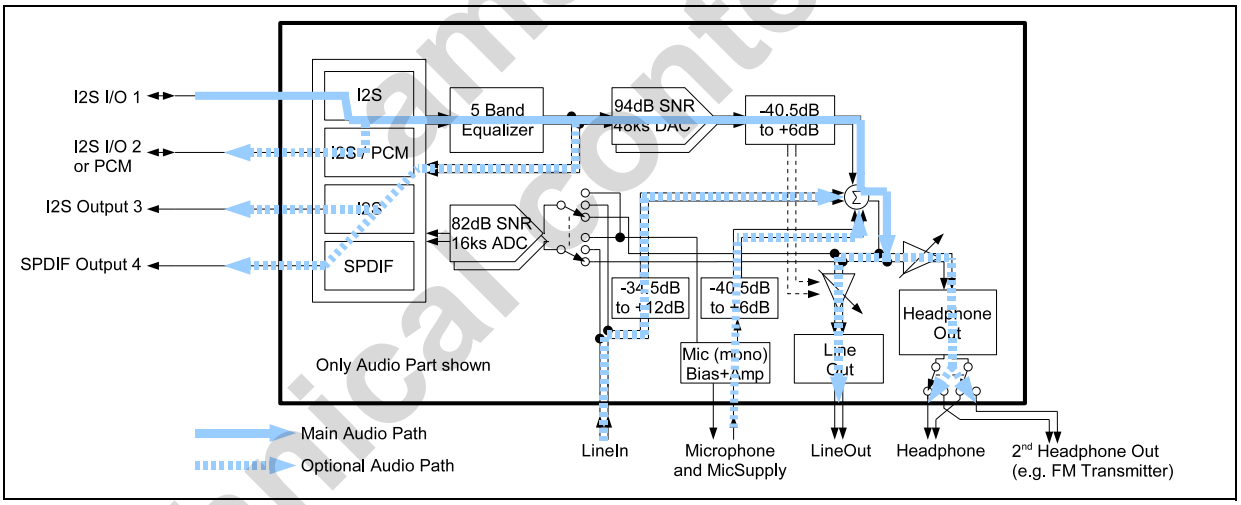
Figure 35. AS3658 *Audio Functions*



9.1 Audio Paths

Following Audio paths are possible (only one configuration is possible at the same time):

Figure 36. AS3658 *I2S I/O 1 or I2S I/O2 Playback*



Note: As the touch screen interface is merged with I2S Output 3 and SPDIF Output 4 either the touch screen interface or I2S Output 3 and SPDIF Output 4 can be used at the same time.

Figure 37. AS3658 *Line In Recording*

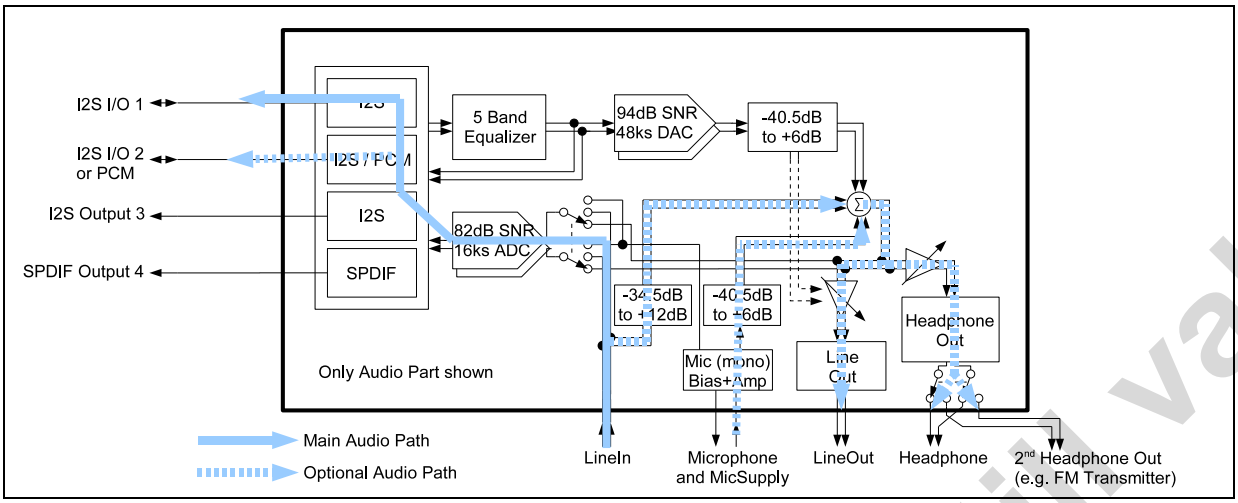
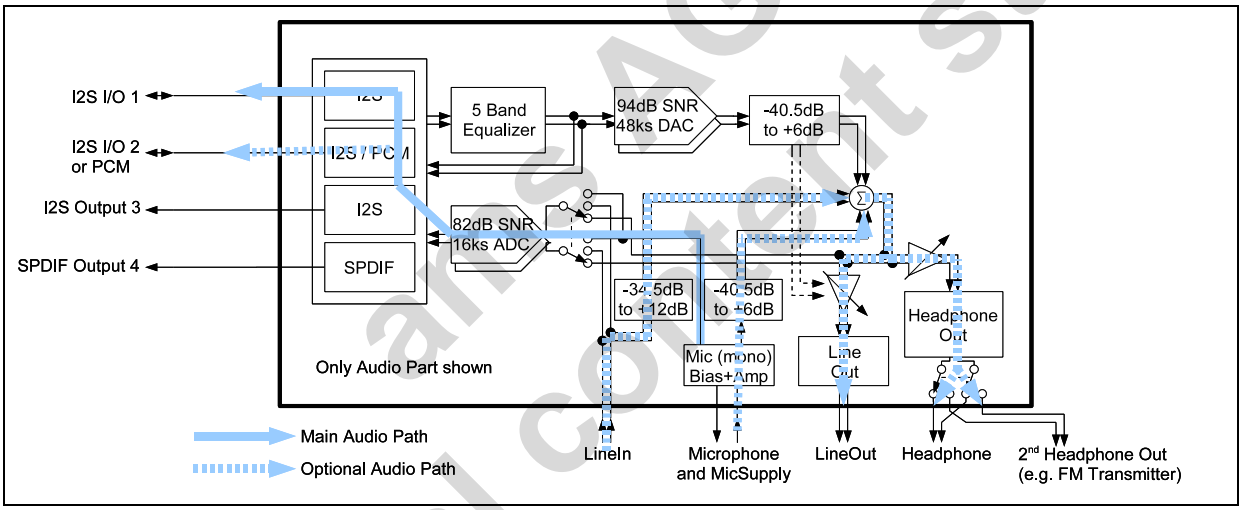


Figure 38. AS3658 *Microphone Recording*



It is also possible to use the Audio ADC and the Audio DAC at the same time. In this case, the sampling frequency of the Audio DAC is either two or four times the sampling rate of the Audio ADC (ADC: max. 16ks / seconds). The equalizer should not be used in this case:

Figure 39. AS3658 *Microphone Recording and I2S I/O Playback (either I2S 1 or I2S 2/PCM)*

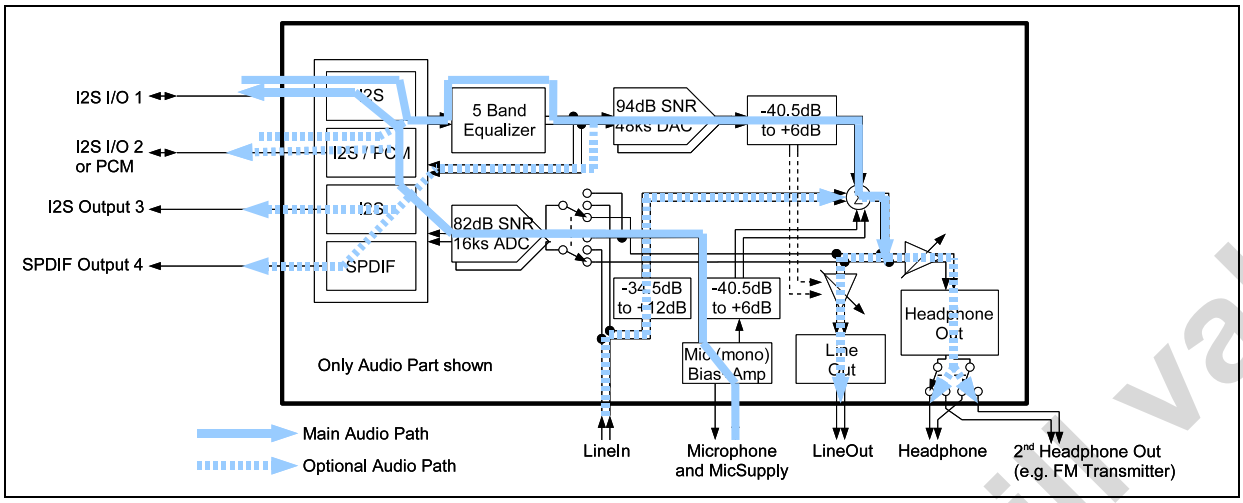
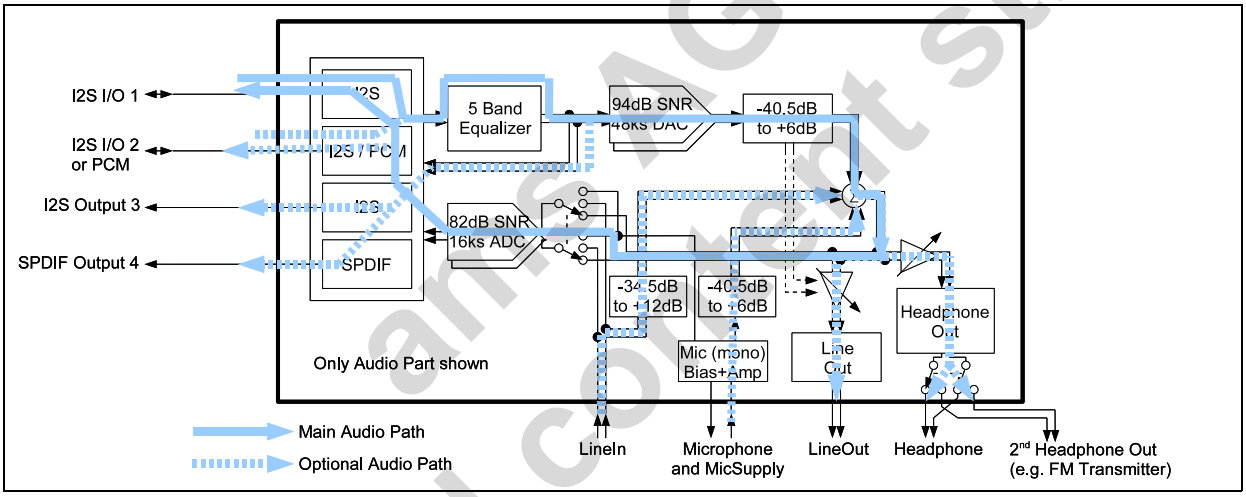


Figure 40. AS3658 *Recording of the Mixed output signal and parallel playback (either I2S 1 or I2S 2/PCM)*



9.2 Common mode voltage generation of HP_CM, LINE_CM

The common mode voltage of the Headphone and Lineout is stored in the C_hpcm and C_linecm capacitor (connected between HP_CM to VSS and LINE_CM to VSS). These capacitor are also responsible for the popless startup, PSRR of the amplifiers and sense path of the GND cancellation circuit.
Startup and PSRR is defined by the value of the external capacitors. The RC limits the maximum achievable PSRR: R=6MΩ typ, C=0.1...1µF:

Table 88. common mode voltage, Audio start-up and PSRR

Capacitor value for C_hpcm and C_linecm	Startup time (typ)	Maximum achievable PSRR	
		@ 1kHz (typ)	@ 100Hz (typ)
µF	msec	dB	dB
0.1	150	76	56
1	1500	90	76

9.3 Audio Setup Registers

Audio LDO has to be switched on first (aud_ldo_on=1), and enables all other functions.

Table 89. AudioSet1 Register

Addr:74		Audio Set1			
		These bits control the Audio functions			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
0	lin_on	0	R/W	0	Line input disabled
				1	Line input enabled
1	dac_on	0	R/W	Switch on control of AUDIO DAC	
				0	DAC disabled
				1	DAC enabled (Switch on, if I2S signal valid only)
2	mix_on	0	R/W	0	Mixer switched off
				1	Mixer switched on
3	gnd_sw_on	0	R/W	0	GND switch off 0V at pin GND_SW
				1	GND switch on Vsupply at pin GND_SW
4	aud_ldo_on	0	R/W	Audio LDO ON control	
				0	Audio LDO off
				1	Audio LDO on
5	mclk_invert	0	R/W	MCLK invert selection	
				0	Change of LRCLK at falling edge of MCLK
				1	Change of LRCLK at rising edge of MCLK
6	mclk256	0	R/W	0	MCLK = LRCLK* 128
				1	MCLK = LRCLK* 256
7	equ_on	0	R/W	0	Equalizer switched off (bypassed)
				1	Equalizer switched on

Table 90. AudioSet2Register

Addr:75		Audio Set2			
		These bits control the Audio functions			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
1,0	ibr_dac<1:0>	00b	R/W	Bias current reduction settings for DAC:	
				00	default
				01	Don't use
				10	Don't use
				11	Don't use
2	dith_on	0	R/W	1	add dither to the audio stream
				0	no dither added
3	I2S_3_on	0	R/W	0	Switch off I2S_3 output
				1	Switch on I2S_3 output

Table 90. AudioSet2Register

Addr:75		Audio Set2			
		These bits control the Audio functions			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
5,4	ibr_hph<1:0>	0	R/W	Bias current reduction settings for headphone output	
				00	0%
				01	17%
				10	34%
				11	50%
6	I2S_select	0	R/W	0	Select I2S_1 input
				1	Select I2S_2 input
7	I2S_mclk_en	0	R/W	0	Generation of the master clock by the internal PLL
				1	Use Pin MCLK_1, MCLK_2 as masterclock input

9.4 ADC, DAC and Digital Audio Input

9.4.1 General

Digital audio data can be fed into the AS3658 via the I2S interface This input data is used by the 18-bit DAC to generate the analog audio signal.

The stage is set to mute by default; If the DAC input is not enabled.

9.4.2 Signal Description

The digital audio interface uses the standard I2S format:

- Left justified
- MSB first
- One additional leading bit

MCLK has to have a fixed ratio of 128 or 256 to LRCLK. With a LRCLK equal to 16, 32, 44.1 or 48kHz, the MCLK can be generated by the on-chip PLL (do not use the internal PLL if there is jitter on the LRCLK1 or 2). For lower sample rates the bit pll_mode has to be set (for sample rates between 8kHz and 12kHz).

The high going edge of MCLK has to have timing separation from LRCLK edges. If the clock generation is so that LRCLK edges are at the same time as MCLK high going edges, the MCLK can be inverted to guarantee a proper DAC function.

This audio input interfaces uses an I2S synchronizer to be able to handle audio sample length of 24bits or less.

Figure 41. I2S Control Diagram

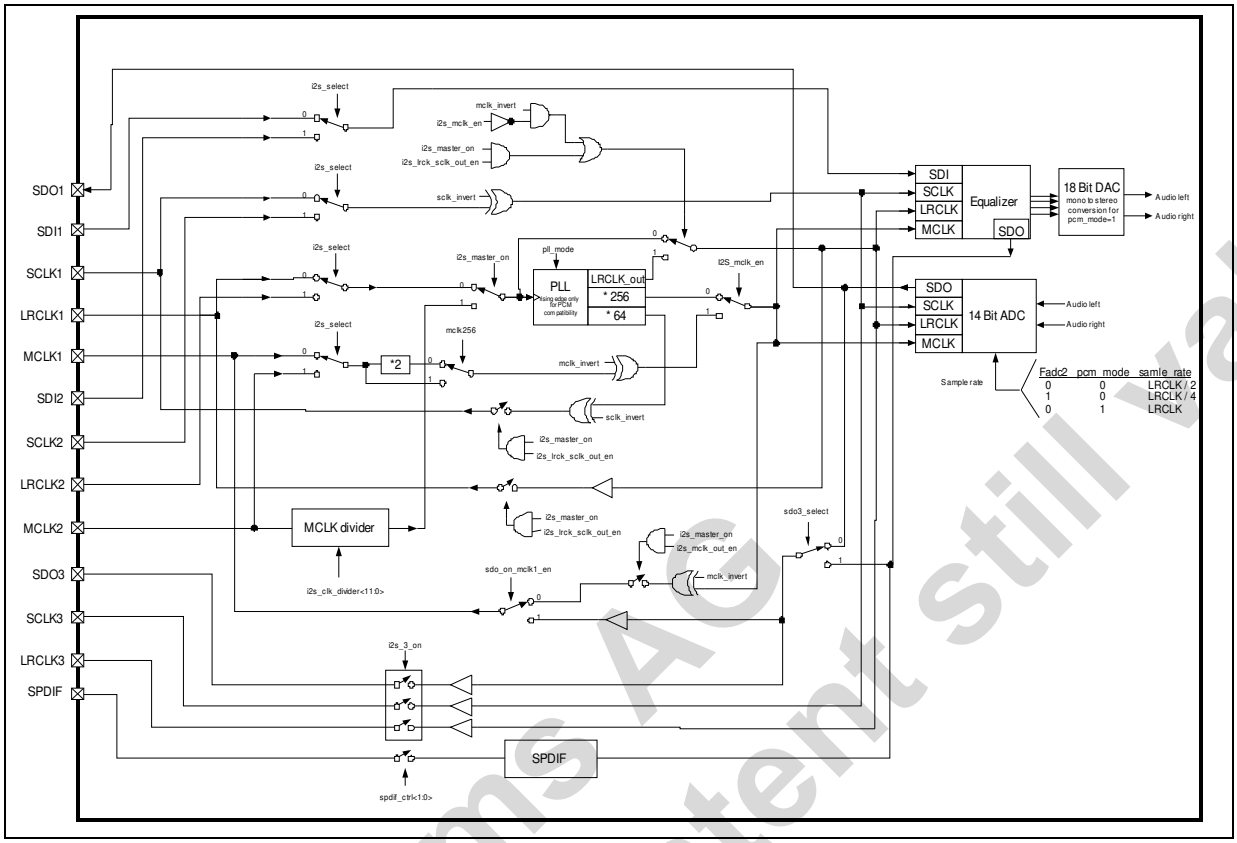


Figure 42. I2S Timing Diagram

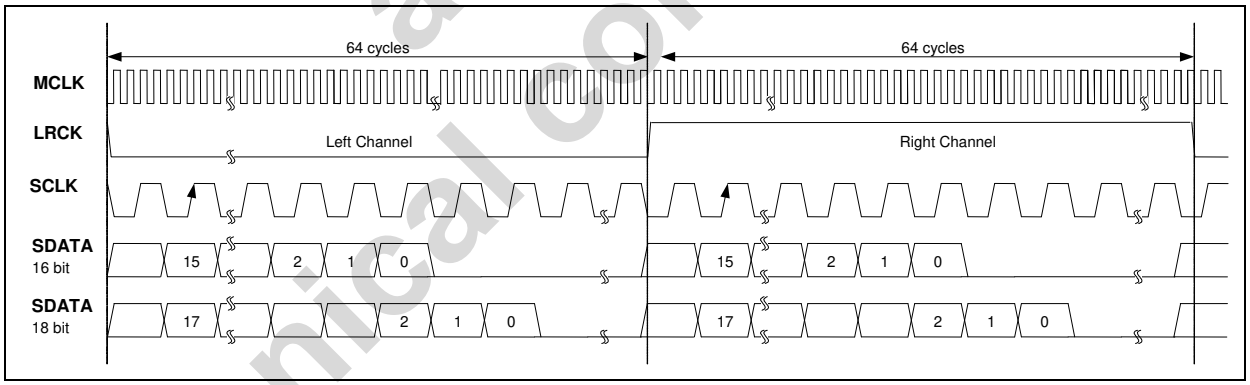


Table 91. PLL,MCLK Settings

I2S_mclk_en	I2S_select	mclk_invert	Description
0	0	0	I2S_1 selected (PLL used) Internal MCLK synchronized to external LRCLK
0	0	1	I2S_1 selected (PLL used) Internal LRCLK used, synchronized to external SDI
0	1	0	I2S_2 selected (PLL used) Internal MCLK synchronized to external LRCLK
0	1	1	I2S_2 selected (PLL used) Internal LRCLK used, synchronized to external SDI

Table 91. PLL,MCLK Settings

I2S_mclk_en	I2S_select	mclk_invert	Description
1	0	0	I2S_1 selected, external MCLK on MCLK_1
1	0	1	I2S_1 selected, external MCLK on MCLK_1 (inverted)
1	1	0	I2S_2 selected, external MCLK on MCLK_2
1	1	1	I2S_2 selected, external MCLK on MCLK_2 (inverted)

9.4.3 Parameter

Table 92. Audio DAC/ADC Parameter

Parameter	Min	Typ	Max	Unit
Analog Performance				
Programmable gain DAC input	-43.43		1.07	dB
Programmable gain ADC input	-34.5		12	dB
Gain step size		1.5		dB
DAC THD+Noise at FS		-85	-75	dB
DAC SN/R (20Hz-20kHz, -60dBFS) A-weighted	90	94		dB
DAC Inter channel Mismatch			0.25	dB
ADC SN/R		82		dB

Table 93. I2S Parameter

I2S Inputs and Outputs VI2S=2.9V		Min	Typ	Max
VIL	SCLKx, LRCLKx, SDIx	-	-	0.42V
VIH	SCLKx, LRCLKx, SDIx	1.02V	-	3.3V
VOL	SDOX,SCLK3,LRCLK3,SPDIF,SCLK1,LRCLK1,MCLK1		0V	
VOH	SDOX,SCLK3,LRCLK3,SPDIF,SCLK1,LRCLK1,MCLK1		VI2S	

Table 94. DAC_L Register

Addr:77		DAC_L			
		These bits control the Audio DAC volume and functions			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
4:0	dal_vol	00000b	R/W	volume settings for left DAC input, adjustable in 32 steps @ 1.5dB	
				00000	-40.5 dB gain
				00001	-39 dB gain
				.....	
				11110	4.5 dB gain
				11111	6 dB gain
5	-	-	-		
6	dac_mute_off	0	R/W	0	DAC input is set to mute
				1	normal operation

Table 95. DAC_R Register

Addr:78		DAC_R			
		These bits control the Audio DAC volume and functions			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
4:0	dar_vol	00000b	R/W	volume settings for right DAC input, adjustable in 32 steps @ 1.5dB	
				00000	-40.5 dB gain
				00001	-39 dB gain
				.....	
				11110	4.5 dB gain
				11111	6 dB gain

Table 96. ADC_L Register

Addr:79		ADC_L			
		These bits control the Audio ADC volume and functions			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
4:0	adl_vol	00000b	R/W	volume settings for left ADC input, adjustable in 32 steps @ 1.5dB	
				00000	-34.5 dB gain
				00001	-33 dB gain
				.....	
				11110	10.5 dB gain
				11111	12 dB gain
5	adc_on	0	R/W	0	ADC disabled
				1	ADC enabled
6	adc_mute_off	0	R/W	0	ADC input is set to mute
				1	normal operation
7	ad_fs2	0	R/W	Divider selection for ADC clock	
				0	ADC sample clock is I2S LRCLK / 2; every ADC sample is sent twice to the I2S output (up-sampling by 2)
				1	ADC sample clock is I2S LRCLK / 4; every ADC sample is sent four times to the I2S output (up-sampling by 4)

Table 97. ADC_R Register

Addr:80		ADC_R			
		These bits control the Audio ADC volume and functions			
Bit	Bit Name	Default	Access	Description	
4:0	adr_vol	00000b	R/W	volume settings for right ADC input, adjustable in 32 steps @ 1.5dB	
				00000	-34.5 dB gain
				00001	-33 dB gain
				.....	
				11110	10.5 dB gain
				11111	12 dB gain
5	adc2dac	0b	R/W	0	normal mode
				1	use ADC output as DAC input (for testing purposes, equalizer is bypassed)
7:6	adcmux	00b	R/W	00	Microphone
				01	Line In
				10	reserved –do not use
				11	Audio Sum (Output of Mixer)

9.5 I2S master mode and PCM Mode

The digital audio interface can also operate in master mode by using I2S1 interface.

The pin MCLK2 is used as clock input in that case. Any input clock between sampling rate and 24MHz may be used as input clock.

In Master Mode operation SCLK1 as output has 32 clock cycles for each sample word.

$$SCLK = [MCLK / 4] = [LRCLK * 256 / 4] = LRCK * 64 \quad (EQ\ 8)$$

Sample Rates

In Master Mode the i2smaster control allows programming various sample rates. The master clock is generated from the MCLK2 input. Sampling frequencies from 8kHz to 48kHz can be selected. For certain division ratios between master clock and sample ratio a certain deviation is system inherent.

$$LRCLK = f_{MCLK\,2} * \frac{1}{2} * \frac{1}{RD + 2}$$

Table 98. PLL,i2s_clk_divider settings

Sample rate	MCLK2 input	Divider	i2s_clk_divider <10:0>	Actual sample rate	Error
kHz	kHz			kHz	%
48,000	12288	126,00	126	48,00	0,00
44,100	12288	137,32	137	44,20	0,23
32,000	12288	190,00	190	32,00	0,00
29,400	12288	206,98	207	29,40	-0,01
24,000	12288	254,00	254	24,00	0,00
22,050	12288	276,64	277	22,02	-0,13
12,000	12288	510,00	510	12,00	0,00

Table 98. PLL,i2s_clk_divider settings

Sample rate	MCLK2 input	Divider	i2s_clk_divider <10:0>	Actual sample rate	Error
kHz	kHz			kHz	%
11,025	12288	555,28	555	11,03	0,05
8,000	12288	766,00	766	8,00	0,00
48,000	12000	123,00	123	48,00	0,00
44,100	12000	134,05	134	44,12	0,04
32,000	12000	185,50	186	31,91	-0,27
29,400	12000	202,08	202	29,41	0,04
24,000	12000	248,00	248	24,00	0,00
22,050	12000	270,11	270	22,06	0,04
12,000	12000	498,00	498	12,00	0,00
11,025	12000	542,22	542	11,03	0,04
8,000	12000	748,00	748	8,00	0,00

Table 99. i2s master control1 Register

Addr:131		I2s master control1		
		This register controls the external clock divider for i2s master mode		
Bit	Bit Name	Default	Access	Description
7:0	i2s_clk_divider<7:0>	00h	R/W	Bit 7:0 of divider for MCLK2 input pin

Table 100. i2s master control2 Register

Addr:132		I2s master control2			
		This register controls the external clock divider and modes for i2s master mode			
Bit	Bit Name	Default	Access	Description	
2:0	i2s_clk_divider<10:8>	000b	R/W		Bit 10:8 of divider for MCLK2 input pin
3	i2s_master_on	0b	R/W	0	i2s master mode disabled
				1	i2s master mode enabled
4	i2s_lrclk_sclk_out_en	0b	R/W	0	LRCLK1 and SCLK1 are used as input (slave mode)
				1	LRCLK1 and SCLK1 are used as output (master mode). Clock input for PLL is MCLK2
5	i2s_mclk_out_en	0b	R/W	0	MCLK1 used as input (slave mode)
				1	MCLK1 used as output for master clock of an external I2S. Clock input for PLL is MCLK2 (MCLK1=256*LRCLK, if bit mclk256=1; MCLK=128*LRCLK, if bit mclk256=0)
6	sdo_on_ mclk1	0b	R/W	0	Normal operation of MCLK1 (input or output according to bit is2_mclk_out_en bit)
				1	MCLK1 used as SDO output (e.g. for audio ADC). May be used as data output (SDO) for I2S_2 port

Table 100. i2s master control2 Register

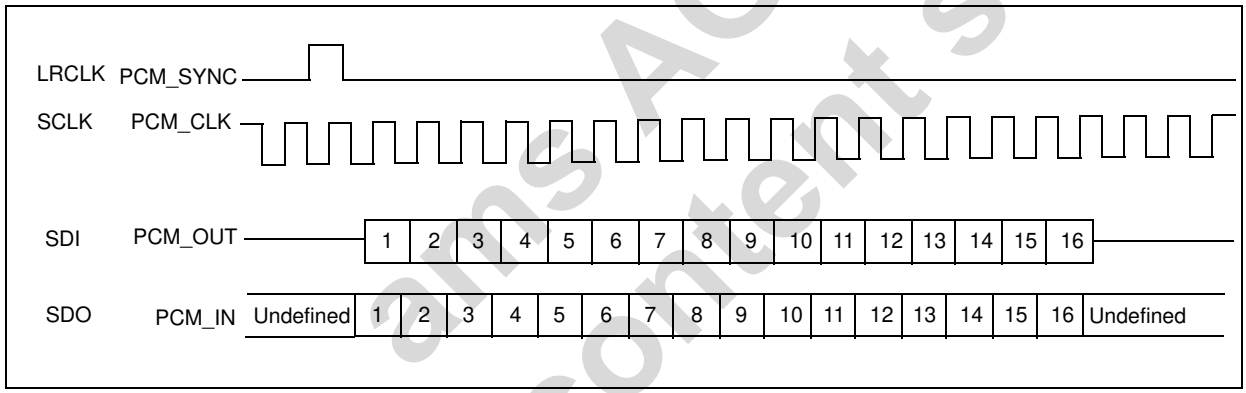
Addr:132		I2s master control2			
		This register controls the external clock divider and modes for i2s master mode			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
7	pcm_mode	0b	R/W	0	Normal I2S mode
				1	PCM mode selected. The following additional settings are necessary to enable PCM mono mode: sclk_invert=1 i2s_mclk_en=0 and mclk_invert=1 (internal PLL used for generation of internal LRCLK)

9.5.1 PCM mode settings

Compatible with BlueCore3-ROM:

Figure 43. Short Frame Sync (shown with 16-bit Sample)

In short Frame Sync the falling edge of PCM_SYNC indicate the start of the PCM word. PCM_Sync is always one clock cycle long.



The following setup on PCM-Master side is needed:

- AS3658 is slave only
- PCM_SYNC is in short frame mode
- PCM_SYNC rate is 8ksamples/s
- PCM_CLK= 512kHz only (64 x PCM_SYNC)
- 16 Bit Linear coding of PCM_OUT and PCM_IN (MSB first, LSB last)
- Mono (single channel) operation only. Only the right channel of the AS3658 is used. The left channel is same as right channel (in the input direction of AS3658) and has to be ignored by PCM master (in output direction of AS3658)

Note: Internally the right channel is copied to the right and left channel.

The following setup of AS3658 is needed:

- Sclk_invert=1
- i2s_mclk_en=0 and mclk_invert=1 (internal PLL used for generation of internal LRCLK)
- pcm_mode=1 and ad_fs2=0 (Necessary to allow unsymmetrical LRCLK and sample rate of 8kHz of ADC)

9.6 Line Input

9.6.1 General

AS3658 includes one stereo single ended inputs.

Figure 44. LineIn Block Diagram

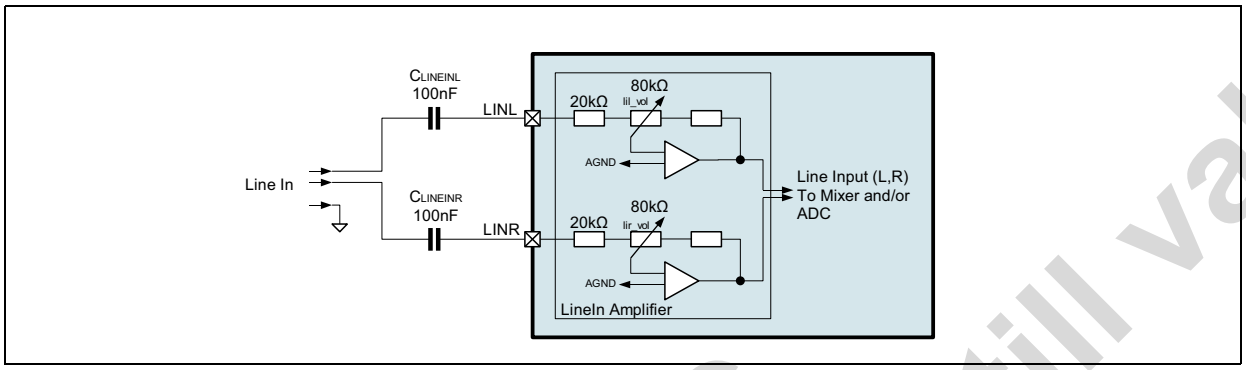


Table 101. Line Inputs Parameter

Parameter	Min	Typ	Max	Unit
Analog Performance				
Rin		50		kΩ

Table 102. LINE_IN_R Register

Addr:85		LINE_IN_R			
		These bits control the LINE_IN volume and functions			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
4:0	lir_vol	00000b	R/W	volume settings for right line input, adjustable in 32 steps @ 1.5dB; gain from line input pin (LIN1R) to mixer input	
				00000	-34.5 dB gain
				00001	-33 dB gain
				.....	
				11110	10.5 dB gain
				11111	12 dB gain
5	mute_off_inr	0	R/W	Control of MUTE switch	
				0	right line input is set to mute
				1	normal operation
7:6		-	-	do not change	

Table 103. LINE_IN_L Register

Addr:86		LINE_IN_L			
		These bits control the LINE_IN volume and functions			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
4:0	lil_vol	00000	R/W	volume settings for right line input, adjustable in 32 steps @ 1.5dB; gain from line input pin (LIN1L) to mixer input	
				00000	-34.5 dB gain
				00001	-33 dB gain
				.....	
				11110	10.5 dB gain
				11111	12 dB gain
5	mute_off_inl	0	R/W	Control of MUTE switch	
				0	left line input is set to mute
				1	normal operation
7:6		00	n/a	do not change	

9.7 Five Band Equalizer

The 5 Band equalizer is build of one low pass, one high pass and 3 band pass filter, and is optimized for 44.1kHz sample frequency:

- Low pass filter: 200Hz (when programming negaitve gain values, this filter changes to a HP filter)
- Band pass filter1: 340Hz / Q=1.0 (when programming negative gain values, this filter changes to a notch filter)
- Band pass filter2: 1100Hz / Q=0.7 (when programming negative gain values, this filter changes to a notch filter)
- Band pass filter3: 3375Hz / Q=1.0 (when programming negative gain values, this filter changes to a notch filter)
- High pass filter: 5940Hz (when pragramming negative gain values, this filter changes to a LP filter)

The Q factors and the cut off frequency of the High and low pass filter are measured at 50% gain and are valid for +6dB amplification of each band.

The attenuation or amplification of each band can be dynamically adjusted by the serial interface. Additional a pre-gain stage can adjust the input level. This gain stage is after the 16 to 24 bit extension and therefore additional gain, which is compensated with the equalizer filter itself (eq_lp_gain, eq_band1,2,3_gain, eq_hp_gain) will not cause clipping:

Figure 45. Equalizer Block Diagram

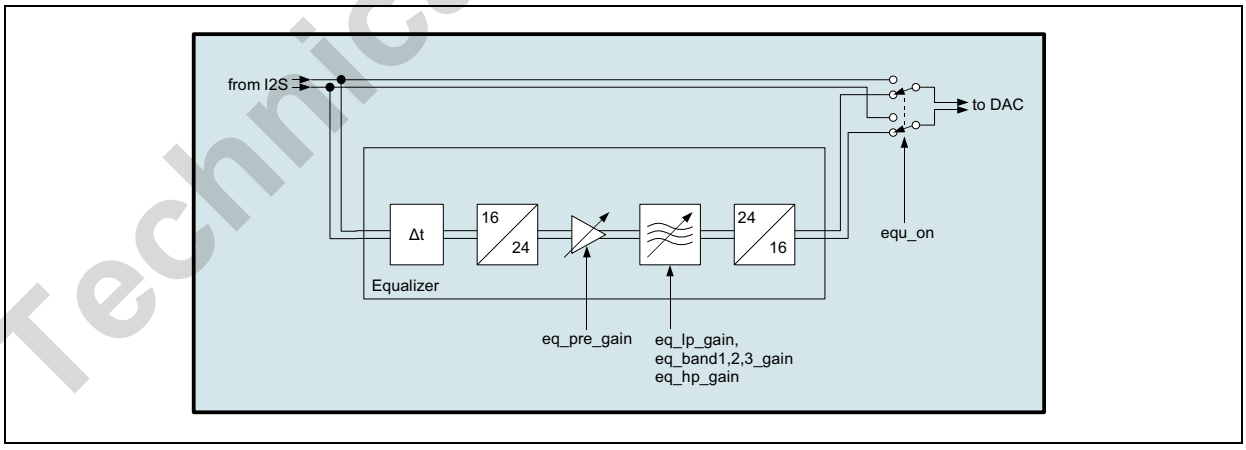


Figure 46. EQ Filter frequency response sum curve

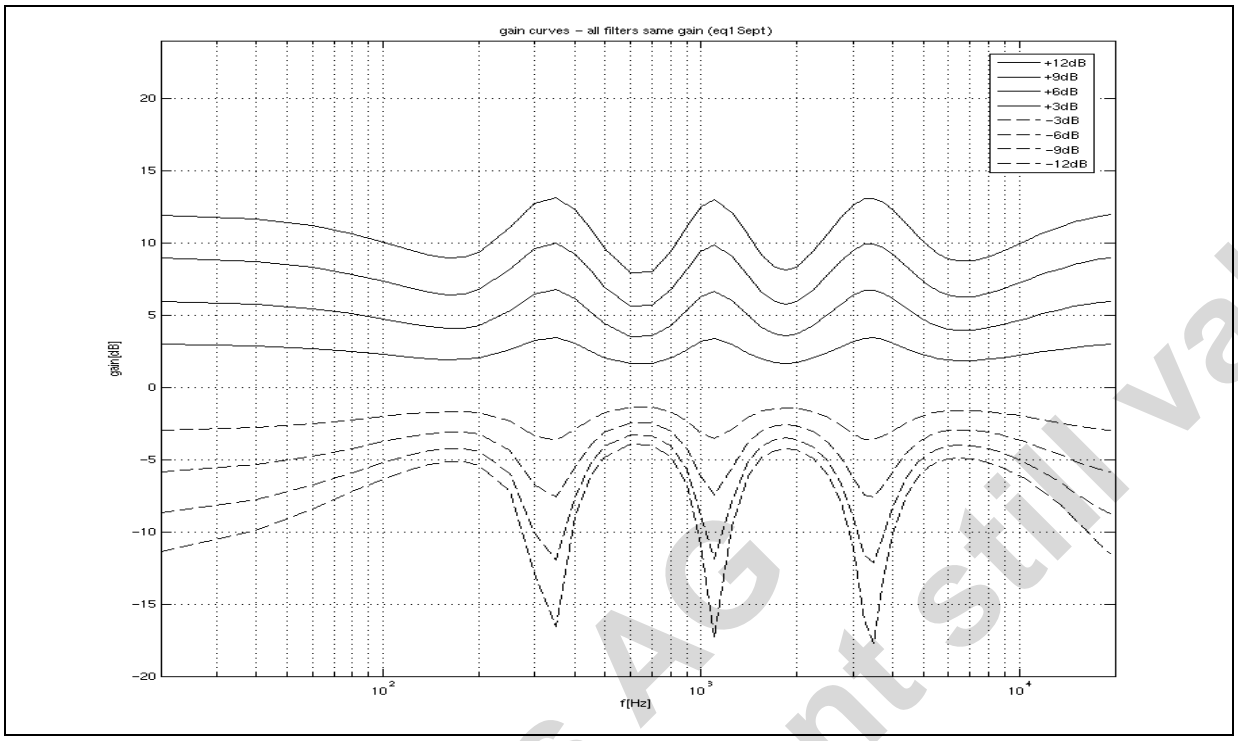


Figure 47. EQ Filter frequency response +12dB/+6dB/+3dB

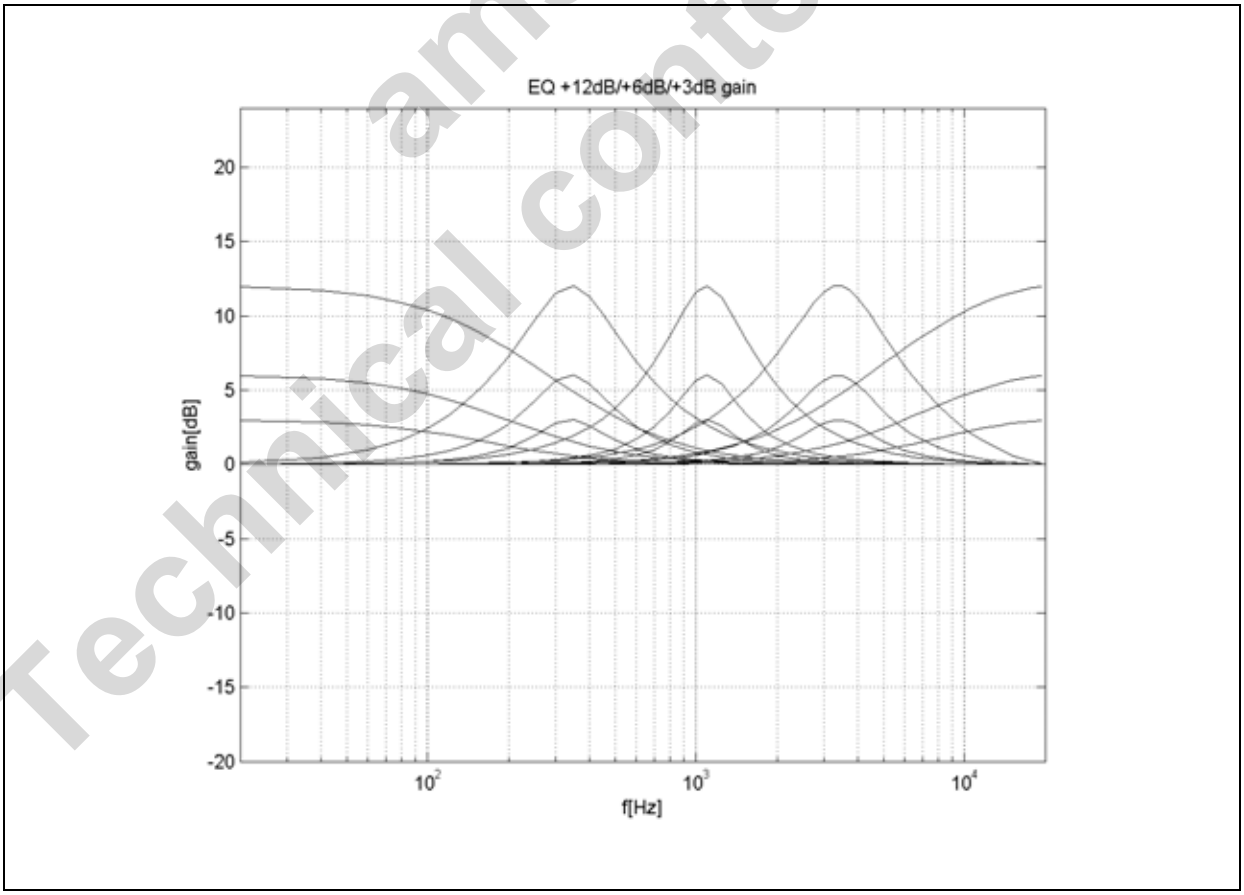
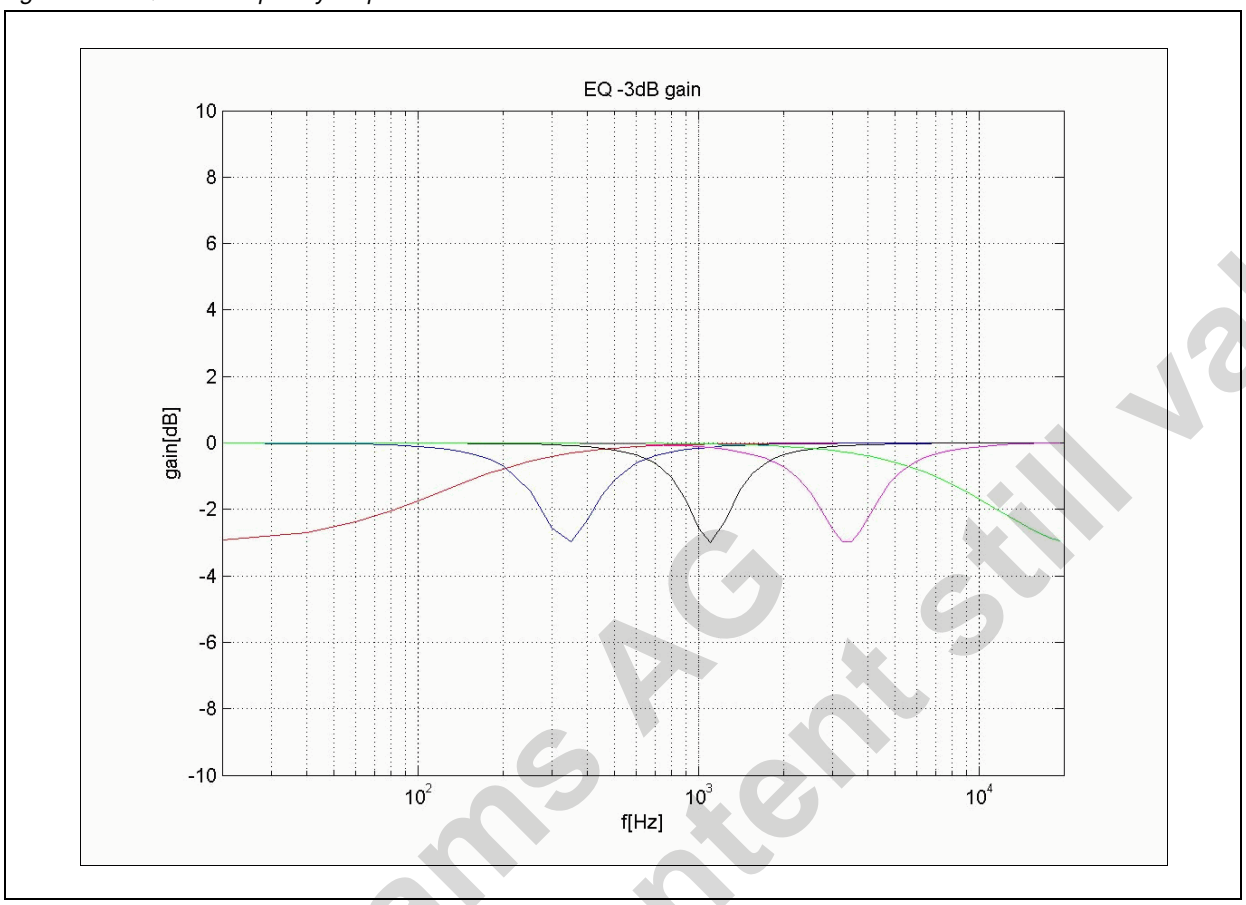


Figure 48. EQ Filter frequency response -3dB



Each band has a range from -12 to +12 dB with each increment equal to ±3dB.

For sample frequencies of the I2S stream different from 44.1kHz, the filter frequencies are shifted (ratiometric).

Table 104. EQ_LP Register

Addr: 90		EQ_LP			
		These bits control the gain of the low pass filter in dB			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
3:0	eq_lp_gain	0000b	R/W	EQ_LP filter gain (-12dB... +12dB)	
				0h	0dB
				1h	3dB
				2h	6dB
				3h	9dB
				4h	12dB
				bh	-3dB
				ch	-6dB
				dh	-9dB
				eh	-12dB

Table 105. EQ_Band1 Register

Addr: 91		EQ_Band1			
		These bits control the gain of the Band pass filter1 in dB			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
3:0	eq_band1_gain	0000b	R/W	EQ_Band1 filter gain (-12dB... +12dB)	
				0h	0dB
				1h	3dB
				2h	6dB
				3h	9dB
				4h	12dB
				bh	-3dB
				ch	-6dB
				dh	-9dB
				eh	-12dB

Table 106. EQ_Band2 Register

Addr: 92		EQ_Band2			
		These bits control the gain of the Band pass filter2 in dB			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
3:0	eq_band2_gain	0000b	R/W	EQ_Band2 filter gain (-12dB... +12dB)	
				0h	0dB
				1h	3dB
				2h	6dB
				3h	9dB
				4h	12dB
				bh	-3dB
				ch	-6dB
				dh	-9dB
				eh	-12dB

Table 107. EQ_Band3 Register

Addr:93		EQ_Band3			
		These bits control the gain of the Band pass filter3 in dB			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
3:0	eq_band3_gain	0000b	R/W	EQ_Band3 filter gain (-12dB... +12dB)	
				0h	0dB
				1h	3dB
				2h	6dB
				3h	9dB
				4h	12dB
				bh	-3dB
				ch	-6dB
				dh	-9dB
				eh	-12dB

Table 108. EQ_HP Register

Addr:94		EQ_HP			
		These bits control the gain of the High pass filter in dB			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
3:0	eq_hp_gain	0000b	R/W	EQ_HP filter gain (-12dB... +12dB)	
				0h	0dB
				1h	3dB
				2h	6dB
				3h	9dB
				4h	12dB
				bh	-3dB
				ch	-6dB
				dh	-9dB
				eh	-12dB

Table 109. EQ_preamp Register

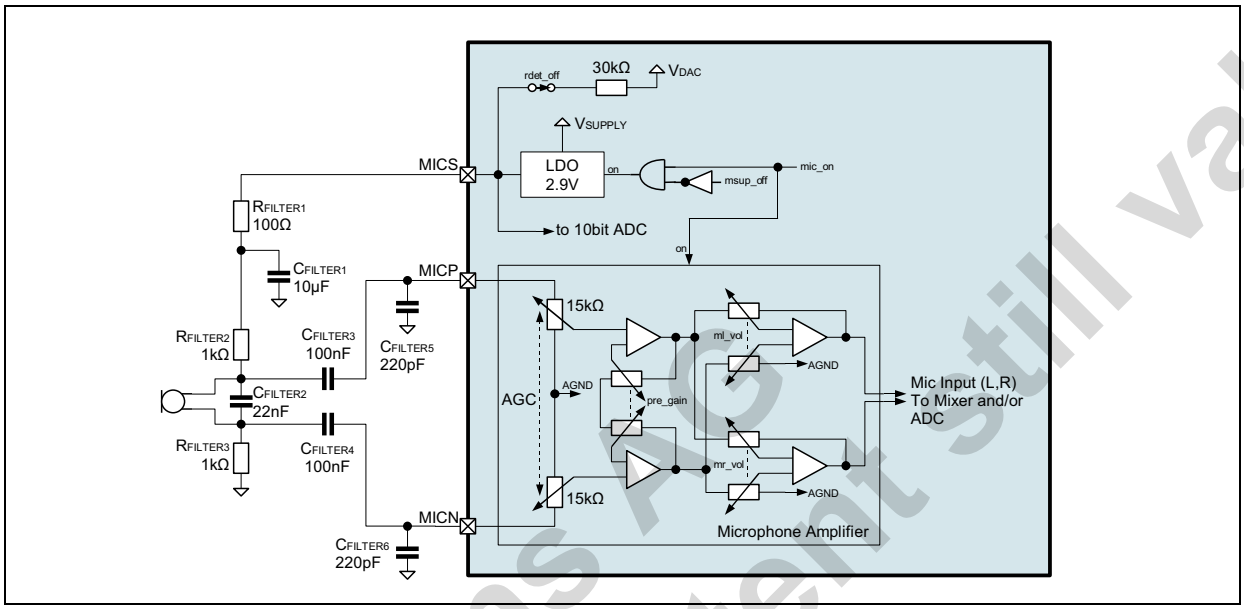
Addr:95		EQ_preamp			
		These bits control the preamplifier of the EQ in dB			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
4:0	eq_pre_gain	00000b	R/W	EQ_vol gain (-12dB ... +12dB with 1.5dB steps)	
				0h	0dB
				01h	-1.5dB
				02h	-3.0dB
				03h	-4.5dB
				04h	-6.0dB
				05h	-7.5dB
				06h	-9.0dB
				07h	-10.5dB
				08h	-12dB
				09h	1.5dB
				bh	3.0dB
				ch	6.0dB
				dh	7.5dB
				eh	9.0dB
				fh	10.5dB
				10h	12dB

9.8 Microphone Input

General

The audio front-end offers one microphone inputs and a low noise microphone voltage supply (microphone bias), voice activation, microphone connect detection and push button remote control.

Figure 49. Microphone Input Block diagram and External Circuit



Gain Stage & Limiter

The integrated pre-amplifier allows 3 preset gain settings. There is also a limiter which attenuates high input signals from e.g. electret microphones signal to 1Vp. The AGC has 15 steps with a dynamic range of about 29dB. The AGC is ON by default but can be disabled by a microphone register bit.

Apart from the microphone pre-amplifier the microphone input signal can further be amplified with 32 @1.5dB programmable logarithmic gain steps and MUTE. All gains and MUTE are independently programmable. The gain can be set from –40.5dB to +6dB.

The stage is set to mute by default. If the microphone input is not enabled, the volume settings are set to their default values. Changing the volume and mute control can only be done after enabling the input.

Supply & Detection

The microphone input generates a supply voltage of 1.5V above AGND. The supply is designed for ≤ 2mA and has a 10mA current limit. In OFF mode the MICS terminal is pulled to AVDD with 30kΩ. A current of typically 50µA generates an interrupt to inform the CPU, that a circuit is connected. When using the MICS terminal as ADC-10 input to monitor external voltage the 30kΩ pull-up can be disabled.

Remote Control

Fast changes of the supply current of typically 500µA are detected as a remote button press, and an interrupt is generated.

Voice Activation

Further a built-in voice activation comparator can actuate an interrupt if microphone input voltage of about 5mVRMS is detected.

Microphone Input Parameter

Table 110. Microphone Inputs Parameter, TA= 25oC unless otherwise mentioned

Symbol	Parameter	Min	Typ	Max	Unit	Note
$V_{MICIN}0$	Input Signal Level		40		mV_{PEAK}	A_{MICPRE} = 28dB; A_{MIC} = 0dB
$V_{MICIN}1$			20		mV_{PEAK}	A_{MICPRE} = 34dB; A_{MIC} = 0dB
$V_{MICIN}2$			10		mV_{PEAK}	A_{MICPRE} = 40dB; A_{MIC} = 0dB
R_{MICIN}	Input Impedance		15		kΩ	MICP, MICN to AGND
MICIN	Input Impedance Tolerance		±15		%	
C_{MICIN}	Input Capacitance		5		pF	
A_{MICPRE}	Microphone Preamplifier Gain		28		dB	Preamplifier has 3 selectable (fixed) gain settings
			34			
			40			
A_{MIC}	Programmable Gain	-40.5		+6	dB	
	Gain Steps		1.5		dB	discrete logarithmic gain steps
	Gain Step Precision		±0.25		dB	
$V_{MICLIMIT}$	Limiter Activation Level		1		V_{PEAK}	
$A_{MICLIMIT}$	Limiter Gain Overdrive		15*2		dB	
t_{ATTACK}	Limiter Attack Time		50		µs/6dB	
t_{DECAY}	Limiter Decay Time		120		ms/6dB	
$A_{MICMUTE}$	Mute Attenuation		100		dB	
V_{MICSUP}	Microphone Supply Voltage		2.9		V	
I_{MICMAX}	Max. Microphone Supply Current		10		mA	microphones nominally need a bias current of 0.5mA-1mA
V_{NOISE}	Microphone Supply Voltage Noise		5		µV	
I_{MICDET}	Microphone Detection Current		50		µA	
I_{REMDET}	Max. Remote Detection Current		500		µA	

Register Description

Table 111. MIC_R Register

Addr:87		MIC_R Right Microphone Input Register Configures the gain from microphone amplifier output			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
4:0	mr_vol	00000b	R/W	volume settings for right microphone input, adjustable in 32 steps @ 1.5dB; gain from microphone amplifier	
				00000	-40.5 dB gain
				00001	-39 dB gain
				.....	
				11110	4.5 dB gain
				11111	6 dB gain
6:5	pre_gain	00	R/W	Sets the gain of the microphone preamplifier	
				00	gain set to 28 dB
				01	gain set to 34 dB
				10	gain set to 40 dB
				11	reserved, do not use
7	mic_agc_off	0	R/W	Control of limiter AGC (automatic gain control). Limits high dynamic range of electret/MEMS microphone (e.g. user shouts or blows into microphone)	
				0	automatic gain control enabled
				1	automatic gain control disabled

Table 112. MIC_L Register

Addr:88		MIC_L Left Microphone Input Register Configures the gain from microphone amplifier output			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
4:0	ml_vol	00000	R/W	volume settings for left microphone input, adjustable in 32 steps @ 1.5dB; gain from microphone amplifier	
				00000	-40.5 dB gain
				00001	-39 dB gain
				.....	
				11110	4.5 dB gain
				11111	6 dB gain
5	rdet_off	0	R/W	Disables the microphone detect function (30kΩ pull-up from MICS to VDAC) to use the terminal as ADC-10 input	
				0	microphone detection enabled
				1	microphone detection disabled
6	mute_off	0	R/W	Control of MUTE	
				0	microphone input set to mute
				1	gain set to 34 dB

Table 112. MIC_L Register

Addr:88		MIC_L			
		Left Microphone Input Register Configures the gain from microphone amplifier output			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
7	msup_off	0	R/W	0	microphone supply on if mic_on=1
				1	microphone supply off

9.9 Audio Output Mixer

9.9.1 General

The mixer stage sums up the audio signals of the following stages

- Microphone Input
- Line Input
- Digital Audio Input (DAC)

The mixing ratios have to be with the volume registers of the corresponding input stages. Please be sure that the input signals of the mixer stage are not higher than 1Vp. If summing up several signals, each individual signal has of course to be accordingly lower. This shall insure that the output signal is also not higher than 1Vp to get a proper signal for the output amplifier.

This stage features an automatic gain control (AGC), which automatically avoids clipping.

9.9.2 Register Description

Table 113. AudioSet_3 Register

Addr:76		Audio_set3 register			
		Configures the mixer inputs and AGC			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
0	pll_mode	0	R/W	Preset of PLL bias for the following sampling frequencies	
				0	16-48kS
				1	8-12kS
1	hp_pulld_en	0	R/W	Controls the pulldown of the HP1 if HP2is enabled and HP2, if HP1 is enabled	
				0	Pulldown disabled if hp_on=1
				1	Pulldown of the not used HP1/2 output enabled, if hp_on=1
2	voxm_on	0	R/W	Switches on the voice recognition	
				0	OFF
				1	ON
3	mic_on	0	R/W	Switches on the microphone amplifier	
				0	OFF
				1	ON

Table 113. AudioSet_3 Register

Addr:76		Audio_set3 register			
		Configures the mixer inputs and AGC			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
4	agc_off	0	R/W	Switches the signal limiter OFF	
				0	automatic gain control for summing stage enabled
				1	automatic gain control for summing stage disabled
5	dacmix_off	0	R/W	Input from DAC to R and L	
				0	ON
				1	OFF
6	micmix_off	0	R/W	Input from microphone to R and L	
				0	ON
				1	OFF
7	linmix_off	0	R/W	Input from line input to R and L	
				0	ON
				1	OFF

9.10 Line Output

9.10.1 General

The line output is designed to provide the audio signal on 600 Ω min.

This output stage has an independent gain regulation for left and right channel with 32 steps @ 1.5dB each. The gain can be set from –40.5dB to +6dB.

9.10.2 No-Pop Function

To avoiding click and pop noise during power-up and shutdown, the output is automatically set to mute when the output stage is disabled. Also the volume settings are set to their default values, and can't be changed, as long the output stage is not enabled.

LINE_CM pin, which needs a 0.1µF... 1µF capacitor outside gets charged on power-up with 1µA to ALVDD/2. After start-up the DC level of the following pins are the same: LOUT_L=LOUT_R=LINE_CM= ALVDD/2. The Start-up time before releasing mute is about 150ms with 0.1µF. To avoid pop-noise 150ms discharging time of LINE_CM after a shutdown, have to be waited before starting up again.

9.10.3 Ground Noise Cancellation

The purpose of the ground cancellation circuit is to compensate noise (ground noise) between different grounds (e.g. the ground where the AS3658 is soldered versus e.g. the ground of a car amplifier (see Figure 50)). This noise between these different grounds can be caused e.g. by a high current devices like a motor-fan. The ground cancellation circuit can be used for line and headphone amplifiers.

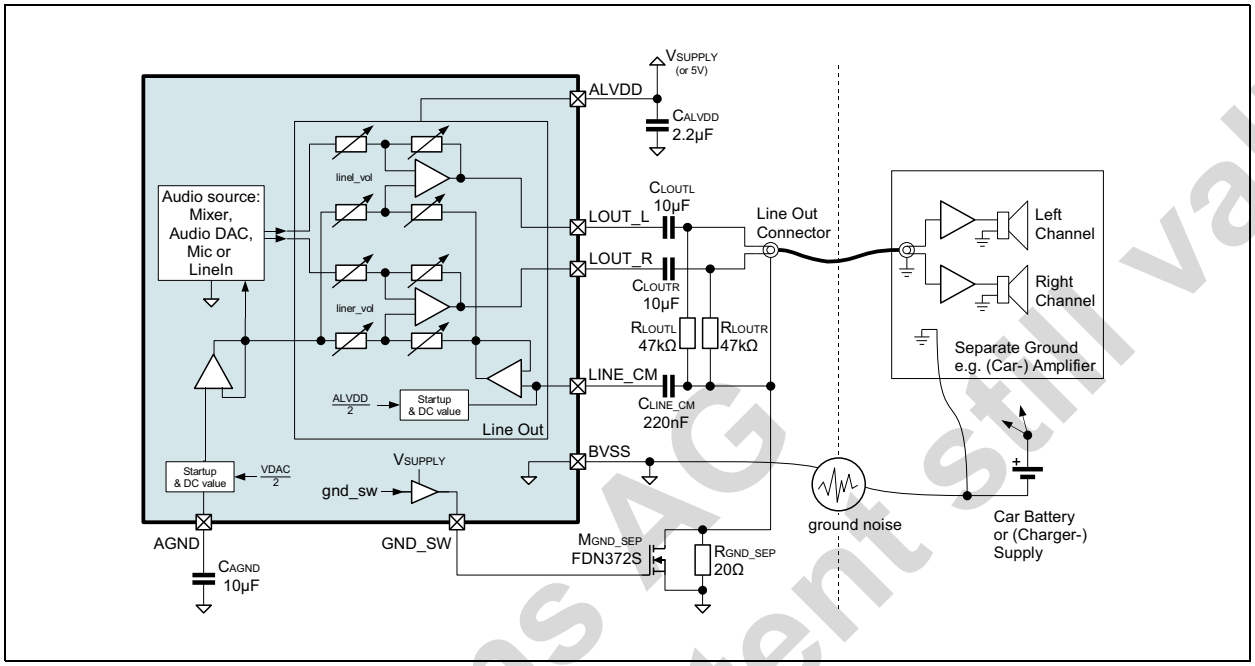
The circuit works as follows:

The ground noise gets added inside the AS3658 to the audio signal (input LINE_CM for the Line Out amplifier or HP_CM for headphone amplifier) in a way that it cancels inside the car amplifier. The sense point is connected with R_{GND_SEP} (20Ω) to the battery ground.

The ground cancellation can be disabled by shorting the 20Ω resistor setting bit gnd_sw to '1'. This bit should be set if e.g. a headphone instead of the car amplifier is connected to the output jack.

Note: A similar cicuit can be used for the headphone amplifier.

Figure 50. Ground Noise Cancellation Application Schematic



9.10.4 Power Save Options

To save power, a reduction of the bias current can be selected.

Table 114. Line Power-Save Options

IBR_LINE	IDD_LINE (typ.)
0	2.2mA
1	1.5mA

9.10.5 Parameter

Table 115. Line out Block Characteristics

Parameter	Min	Typ	Max	Unit
Analog Performance				
R_Load at LOUT_L and LOUT_R single ended	600			Ω
Gain Step Precision (RLmin-max,20Hz-20kHz)		±0.5		dB
SINAD no load, LineIn-> Line out, A-weighted		-97		dB
THD @ 1kHz, no load		-88		dB
THD @ 1kHz, 600Ω		-80		dB
PSRR (200Hz-20kHz)	60	90		dB
IOUT_powerdown	-20		20	µA
Tpower_up (C_LINECM=100nF)		150		ms

Table 115. Line out Block Characteristics

Parameter		Min	Typ	Max	Unit
GND cancellation GND - AUDIO_GND to LOUT_R, LOUT_L no load	100Hz		50		dB
	1kHz		50		
	10kHz		40		

9.10.6 Register Description

To get an interrupt on an over-current event, the corresponding bit in the Interrupt enable register has to be set. All other Line/headphone driver settings are controlled by the following two registers.

Right Line Register

Table 116. LINE_OUT_R Register

Addr:83		LINE_OUT_R			
		These bits control the Line in volume and mode			
Bit	**Bit Name**	**Default**	**Access**		
4:0	liner_vol	00000b	R/W	volume settings for right Line output, adjustable in 32 steps @ 1.5dB	
				00000	-40.5 dB gain
				00001	-39 dB gain
				.....	
				11110	4.5 dB gain
				11111	6 dB gain
5	dac2line_on	0	R/W	0	Line_out amplifier input connected to mixer output
				1	Line_out amplifier input connected to Audio DAC output gain stage (Mixer is bypassed in this mode)
7:6	ibr_line<1:0>	00b	R/W	Bias current reduction settings for line output:	
				00	0%
				01	17%
				10	34%
				11	50%

Left Line Register

Table 117. LINE_OUT_L Register

Addr:84		LINE_OUT_L			
		These bits control the Line in volume and mode			
Bit	**Bit Name**	**Default**	**Access**		
4:0	liner_vol	00000b	R/W	volume settings for left Line output, adjustable in 32 steps @ 1.5dB	
				00000	-40.5 dB gain
				00001	-39 dB gain
				.....	
				11110	4.5 dB gain
				11111	6 dB gain
5	-	0			reserved
6	line_on	0	R/W	0	Line stage not powered
				1	power up Line stage
7	line_mute	0	R/W	0	normal operation
				1	Line output set to mute (mute is on during power-up)

9.11 Headphone Output

The headphone output is designed to provide the audio signal with 2x40mW @ 16Ω or 2x20mW @32Ω, which are typical values for headphones.

This output stage has an independent gain regulation for left and right channel with 32 steps @ 1.5dB each. The gain can be set from –40.5dB to +6dB.

9.11.1 Phantom Ground

HP_CM_PWR pin is the buffered HP_CM output. It can be used to drive the common mode level with a load of 2kΩ. The phantom ground can be switched off to save power if not needed.

9.11.2 No-Pop Function

To avoiding click and pop noise during power-up and shutdown, the output is automatically set to mute when the output stage is disabled. Also the volume settings are set to their default values, and can't be changed, as long the output stage is not enabled.

HP_CM pin, which needs a 100nF to 1µF capacitor outside, gets charged on power-up with 1µA to AVDD/2. After start-up the DC level of the following pins are the same: HPR=HPL=HP_CM=HP_CM_PWR=AVDD/2. The Start-up time before releasing mute is about 150ms. To avoid pop-noise 150ms discharging time of HP_CM after a shutdown, have to be waited before starting up again.

9.11.3 Over-current Protection

This output stage has an over-current protection, which disables the output for 256ms or 512ms. This value can be set in the headphone registers. The over-current protection limit of HPR and HPL pin is about 260mA while HP_CM_PWR pin has a 370mA limit.

9.11.4 Power Save Options

To save power, especially when driving 32 Ω loads, a reduction of the bias current can be selected.

Bias current reduction settings for headphone output:

- 00: 0%
- 01: 17%
- 10: 34%
- 11: 50%

9.11.5 Parameters

Table 118. Power Amplifier Parameter

Parameter		Min	Typ	Max	Unit
Analog Performance					
R_Load at AOUTR and AOUTL single ended		16			Ω
Vout				1.13	Vp
Gain Step Precision (RLmin-max,20Hz-20kHz)			±0.5		dB
SINAD no load, LineIn-> HPH, A-weighted			-97		dB
THD @ 1kHz, no load			-88		dB
THD @ 1kHz, 32Ω, 10mW			-80		dB
THD @ 1kHz, 32Ω, 20mW			-74	-66	dB
THD @ 1kHz, 16Ω, 40mW			-68	-60	dB
Channel Separation (32Ω, dc-coupled)			60		dB
PSRR (200Hz-20kHz)		60	90		dB
Shorted Protection Level			260		mA
Shorted Protection Level of common mode buffer			370		mA
IOUT_powerdown		-20		20	µA
Tpower_up (HP_CM=0.1µF)			150		ms
GND cancellation GND - AUDIO_GND to HP_R, HP_L no load	100Hz		50		dB
	1kHz		50		
	10kHz		40		

9.11.6 Register Description

To get an interrupt on an over-current event, the corresponding bit in the Interrupt enable register has to be set. Changing the bias current or the output driver strength is done via AudioSet2 register. All other headphone driver settings are controlled by the following two registers.

Right Headphone Register

Table 119. HPH_OUT_R Register

Addr:81		HPH_OUT_R			
		These bits control the Right headphone ouput volume and mode			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
4:0	hpr_vol	00000b		volume settings for right headphone output, adjustable in 32 steps @ 1.5dB	
				00000	-40.5 dB gain
				00001	-39 dB gain
				.....	
				11110	4.5 dB gain
				11111	6 dB gain
5	hpcm_off			headphone phantom ground disable	
				0	normal operation
				1	disable common mode buffer
7:6	hp_ovc_to	00h		headphone over current time out: speaker over current time out:	
				00	256 ms
				01	128 ms
				10	512 ms
				11	0 ms

Left Headphone Register

Table 120. HPH_OUT_L Register

Addr:82		HPH_OUT_L			
		These bits control the Left headphone ouput volume and mode			
Bit	**Bit Name**	**Default**	**Access**		
4:0	hpl_vol	00000b		volume settings for left headphone output, adjustable in 32 steps @ 1.5dB	
				00000	-40.5 dB gain
				00001	-39 dB gain
				.....	
				11110	4.5 dB gain
				11111	6 dB gain
5	hp_mux	0	R/W	0	use HPL1, HPR1 as headphone output
				1	use HPL2, HPR2 as headphone output
6	hp_on	0	R/W	0	headphone stage not powered
				1	power up headphone stage
7	hp_mute	0	R/W	0	normal operation
				1	headphone output set to mute (mute is on during power-up)

9.12 SPDIF output

Enables and controls the SPDIF output pin. SPDIF functionality is enabled, if internal masterclock is used (internal PLL), or the external masterclock = 256* LRCLK. (No SPDIF function if external masterclock= 128 *LRCLK)

Table 121. SPDIF Register

Addr:89		SPDIF			
		These bits control the SPDIF output			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
1:0	spdif_cntr	00b	R/W	ISPDIF output ON/OFF control and sample rate status bits	
				00	SPDIF output OFF
				01	SPDIF output ON
				10	reserved (do not use)
				11	reserved (do not use)
2	spdif_invalid	0	R/W		SPDIF sample status bit
				0	sample valid
				1	sample invalid
3	spdif_mclk_inv	0	R/W	SPDIF master clock control bit	
				0	master clock
				1	master clock inverted
4	spdif_copy_ok	0	R/W	SPDIF copy control bit	
				0	copy not permitted
				1	copy permitted
5	sdo3_select	0	R/W	Select source of SDO3 output	
				0	Select adc_output
				1	Select Equalizer output
6	sclk_invert	0	R/W	Invert serial data clock of I2S1 and I2S2	
				0	Normal mode
				1	Invert SCLK1 or SCLK2 input
7	audio_off	0	R/W	switch off audio functionality for low power touchpannel detection	
				0	Normal mode
				1	audio bias switched off to reduce power

10 Detailed Description - System Functions

The system functions consist of the I2C interface, the reset controller, the interrupt controller, startup sequences and programming, the watchdog, internal references, the ON-key detect and the real time clock module.

10.1 I²C Serial Interface

Table 122. I2C SDA,SCL Characteristics

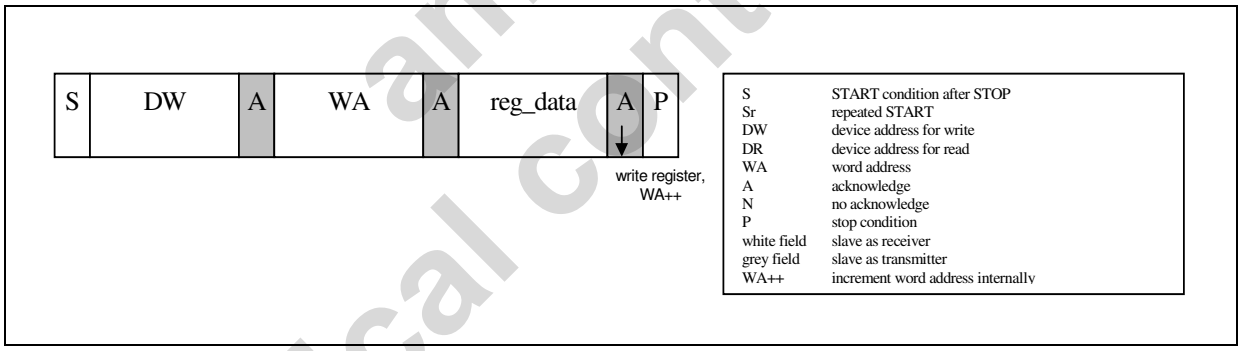
Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{IL}	SCL,SDA Low Level input voltage	-0.3		0.4	V	
V_{IH}	SCL,SDA High Level input voltage	1.3		VSUPPLY	V	

10.1.1 Feature List

- Fast-mode capability (max. SCL-frequency is 400 kHzkHz)
- 7+1-bit addressing mode
- 60h x 8-bit data registers (word address 0x00 - 0x60)
- Write formats: Single-Byte-Write, Page-Write
- Read formats: Current-Address-Read, Random-Read, Sequential-Read
- SDA input delay and SCL spike filtering by integrated RC-components

10.1.2 Transfer Formats

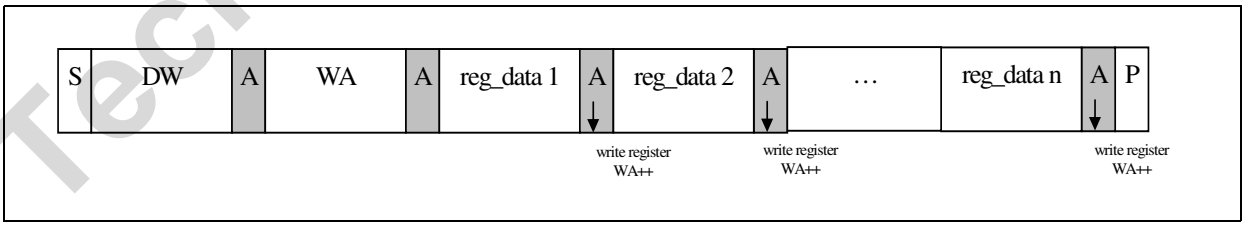
Figure 51. I²C Byte-Write



AS3658 device address write (DW):80h = 10000000b

AS3658 device address read (DR): 81h = 10000001b

Figure 52. I²C Page-Write:



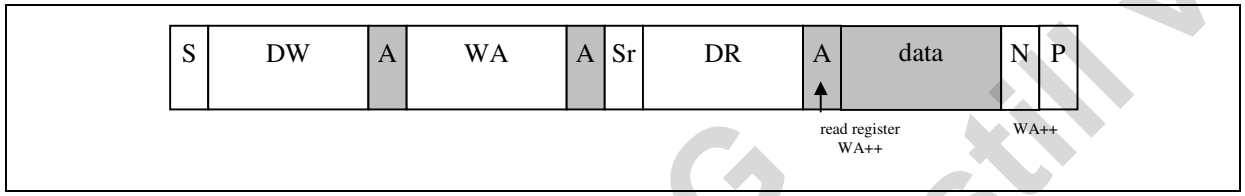
Byte-Write and Page-Write are used to write data to the slave.

The transmission begins with the START condition, which is generated by the master when the bus is in IDLE state (the bus is free). The device-write address is followed by the word address. After the word address any number of data bytes can be send to the slave. The word address is incriminated internally, in order to write subsequent data bytes on subsequent address locations.

For reading data from the slave device, the master has to change the transfer direction. This can be done either with a repeated START condition followed by the device-read address, or simply with a new transmission START followed by the device-read address, when the bus is in IDLE state. The device-read address is always followed by the 1st register byte transmitted from the slave. In Read-Mode any number of subsequent register bytes can be read from the slave. The word address is incriminated internally.

The diagrams below show various read formats available:

Figure 53. I²C Random-Read:

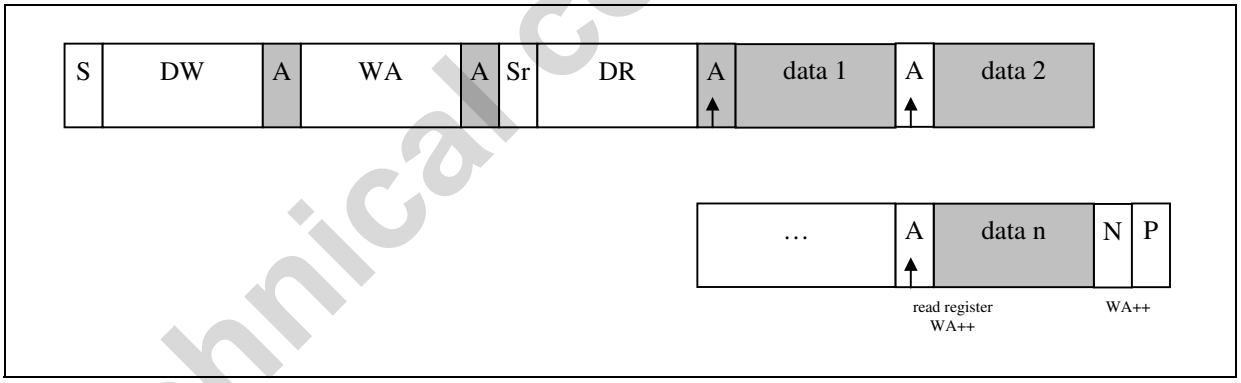


Random-Read and Sequential-Read are combined formats. The repeated START condition is used to change the direction after the data transfer from the master.

The word address transfer is initiated with a START condition issued by the master while the bus is idle. The START condition is followed by the device-write address and the word address.

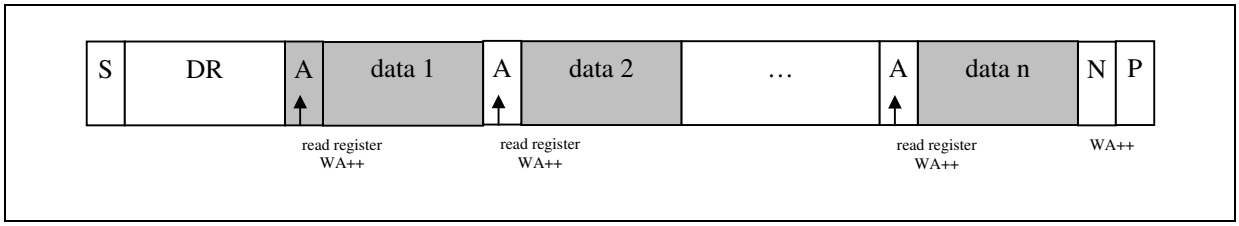
In order to change the data direction a repeated START condition is issued on the 1st SCL pulse after the acknowledge bit of the word address transfer. After the reception of the device-read address, the slave becomes the transmitter. In this state the slave transmits register data located by the previous received word address vector. The master responds to the data byte with a not-acknowledge, and issues a STOP condition on the bus.

Figure 54. I²C Sequential-Read:



Sequential-Read is the extended form of Random-Read, as more than one register-data bytes are transferred subsequently. In difference to the Random-Read, for a sequential read the transferred register-data bytes are responded by an acknowledge from the master. The number of data bytes transferred in one sequence is unlimited (consider the behavior of the word-address counter). To terminate the transmission the master has to send a not-acknowledge following the last data byte and generate the STOP condition subsequently.

Figure 55. I²C Current-Address-Read:



To keep the access time as small as possible, this format allows a read access without the word address transfer in advance to the data transfer. The bus is idle and the master issues a START condition followed by the Device-Read address. Analogous to Random-Read, a single byte transfer is terminated with a not-acknowledge after the 1st register byte. Analogous to Sequential-Read an unlimited number of data bytes can be transferred, where the data bytes has to be responded with an acknowledge from the master. For termination of the transmission the master sends a not-acknowledge following the last data byte and a subsequent STOP condition.

10.2 Reset generator and XON-Key

XRESET is a low active bi-directional pin. An external pull-up to the periphery supply has to be added.

During each reset cycle the following states are controlled by the AS3658:

- Pin XRESET is forced to GND
- Programmable Power-off function
- Programmable Power-on sequence and regulator voltages
- Programmable reset timer
- All registers are set to their default values after power-on, except the reset control- and status-registers.

Note: Programming is controlled by the internal Mask-PROM and the external resistor RPROGRAM

Table 123. XRESET,XON Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{XRESET_IL}	XRESET Low Level input voltage	-0.3		0.4	V	
V_{XRESET_IH}	XRESET High Level input voltage	1.3		VSUPPLY	V	
V_{XON_IL}	XON Low Level input voltage	-0.3		0.3*V2_5		
V_{XON_IH}	XON High Level input	0.7*V2_5		V2_5		
I_{XON_PUP}	XON Pull up current		12		µA	

10.2.1 Reset Conditions

Reset can be activated from 7 different sources:

- Power on (battery or charger insertion)
- Low Battery
- Software forced reset
- Power off mode
- External triggered through the pin RESET
- Overtemperature
- Watchdog

Voltage detection:

There are two types of voltage dependent resets: V_{POR} and V_{XRESET}. V_{POR} monitors the voltage on V2_5 and V_{XRESET} monitors the voltage on VSUPPLY. The linear regulator for V2_5 is always on and uses the voltage VCHARGER, V_{BAT} or V_USB as its source.

The pin RESET is only released if V2_5 is above V_{POR} and VSUPPLY is above $VXRESET_{RISE}$.

Table 124. Reset Levels

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{POR}	Overall power on reset	1.5	2.0	2.3	V	Monitor voltage on V2_5; power on reset for all internal functions
$VXRESET_{RISE}$	Reset level for Vsupply rising		ResVol trise		V	Monitor voltage on Vsupply; rising level
$VXRESET_{FALLING}$	Reset level for Vsupply falling		2.7		V	Monitor voltage on VSupply; falling level
			ResVol tfall		V	if SupResEn=1 only
$VRESET_{MASK}$	Mask time for $VXRESET_{FALLING}$	2.0	2.5	3.0	ms	Duration for V_{BAT}<$VXRESET_{FALLING}$ until a reset cycle is started[1]

1. VRESET signal is debounced with the specified mask time for rising- and falling slope of V_{BAT}.

$VRESET_{FALLING}$ is only accepted if the reset condition is longer than $VRESET_{MASK}$. This guard time is used to avoid a complete reset of the system in case of short drops of V_{BAT}.

Power off:

To put the chip into ultra low power mode, write '1' into xon_enable and '1' into *power_off*. The chip stays in power off mode until the external pin XON is pulled low, the charger is inserted or the level V_{POR} is touched to start a complete reset cycle. The bit *power_off* is automatically cleared by this reset cycle. During *power_off* state all circuits are shut-off except the Low Power LDO (V2_5). Thus the current consumption of AS3658 is reduced to less than 15 µA. The digital part is supplied by V2_5, all other circuits are turned off in this mode, including references and oscillator. Except the reset control registers all other registers are set to their default value after power-on.

Software forced reset

Writing '1' into the register bit force_reset immediately starts a reset cycle. The bit *force_reset* is automatically cleared by this reset.

External triggered reset:

If the pin XRESET is pulled from high to low by an external source (e.g. microprocessor or button) a reset cycle is started as well.

Overtemperature reset:

The reset cycle can be started by overtemperature conditions. (see Protection Functions on page 134)

Watchdog reset:

If the watchdog is armed (register bit *wtdg_on* = 1 and *wtdg_res_on* = 1) and the timer expires it causes a reset. (see Watchdog on page 135).

10.2.2 Reset Control Bits

Table 125. Reset Timer Register

Addr:22		Reset Timer			
		These bits control the reset timer and XON enable register			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
2:0	res_timer	ROM	R/W	Set RES_{TIME}	
				000	RES_{TIME}=10ms
				001	RES_{TIME}=20ms
				010	RES_{TIME}=35ms
				011	RES_{TIME}=50ms
				100	RES_{TIME}=65ms
				101	RES_{TIME}=80ms
				110	RES_{TIME}=95ms
				111	RES_{TIME}=110ms
3	xon_enable	ROM	R/W	This flag enables the XON pad and sets the power on state of the ASIC	
				0	XON pad disabled. Startup of chip; if V_{BAT}>$VRESET_{RISING}$
				1	XON pad enabled. Startup of chip; if V_{BAT}>$VRESET_{RISING}$ and XON=0

Table 126. Reset Control Register

Addr:105		Reset Control		
		These bits control the power off mode and reset timer		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	force_reset	0b	R/W	Setting to ‘1’ starts a complete reset cycle
1	power_off	0b	R/W	Setting to ‘1’ starts a reset cycle, but waits after the Reg_off state for a falling edge on the pin XON or until the charger is detected
2	xon_input	NA	R/W	Read:This flag represents the state of the XON pad directly
				Write: Setting to '1' resets the 5 sec. Onkey reset timer

Table 126. Reset Control Register

Addr:105		Reset Control			
		These bits control the power off mode and reset timer			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
6:3	reset_reason	NA	R	Flags to indicate to the software the reason for the last reset	
				0000	V_{POR} has been reached (battery or charger insertion from scratch)
				0001	$VRESET_{FALLING}$ was reached (battery voltage drop below 2.75V)
				0010	software forced by force_reset
				0011	software forced by power_off and XON was pulled low
				0100	software forced by power_off and charger was detected
				0101	external triggered through the pin RESET
				0110	reset caused by overtemperature T_{140}
				0111	reset caused by watchdog
				1000	reset caused by 5 seconds on press
				1001	reset caused by rtc_alarm register
				1010	reset caused by rtc repeated wakeup
				1011	reset caused by interrupt in standby mode
				1100	reset caused by XON pulled low in standby mode
7	Onkey_reset_5s	1	R/W	0	Reset after 5 seconds ON pressed disabled
				1	Reset after 5 seconds ON pressed enabled

Table 127. Internal references Bit definitions

Addr:59		Internal references Bit definitions			
		These bits control the internal reference mode and internal clk frequency			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
4	standby_mode_on	0	W	Setting to '1' sets the AS3658 into standby mode. All regulators defined in reg.17h "Reg Power1Ctrl" and reg.1Eh "Reg Power2 Ctrl are disabled except those regulators enabled by reg.81h "Reg standby mode". XRESET will be pulled to low. A normal startup of all regulators will be done with any interrupt (has to be enabled before entering standby mode). During this startup, regulators defined by Reg standby mode register are continuously on.	
5	Clk_div2	0	R/W	Divide internal clock oscillator by 2 to reduce quiescent current for low power operation	
				0	Normal mode
				1	Internal clock frequency divided by two. All timings are increased by two. Switching frequency of all DCDC converters are divided by two. Reduced transient performance of DCDC converters.

Table 127. Internal references Bit definitions

Addr:59		Internal references Bit definitions			
		These bits control the internal reference mode and internal clk frequency			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
6	Reg_low_bias_mode	0	R/W	0	Normal mode
				1	The quiescent current of the following regulators is divided by approx. two: SD1, SD2, SD3, RF1, RF2, RF3. The current capability and performance is also reduce in that mode. (E.g. Use this bit only to reduce quiescent current, if system and processor is in a low power mode)

Table 128. Reg standby mode Bit definitions

Addr:129		Reg standby mode			
		These bits control the on/off function of the regulators during standby mode			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
0	ldo_rf1_stby_on	0	R/W	0	RF1 LDO is disabled in standby mode
				1	RF1 LDO is enabled in standby mode
1	ldo_rf2_stby_on	0	R/W	0	RF2 LDO is disabled in standby mode
				1	RF2 LDO is enabled in standby mode
2	ldo_dig1_stby_on	0	R/W	0	DIG1 LDO is disabled in standby mode
				1	DIG1 LDO is enabled in standby mode
3	ldo_dig2_stby_on	0	R/W	0	DIG2 LDO is disabled in standby mode
				1	DIG2 LDO is enabled in standby mode
4	sd1_stby_on	0	R/W	0	Step down 1 is disabled in standby mode
				1	Step down 1 is enabled in standby mode
5	sd2_stby_on	0	R/W	0	Step down 2 is disabled in standby mode
				1	Step down 2 is enabled in standby mode
6	sd3_stby_on	0	R/W	0	Step down 3 is disabled in standby mode
				1	Step down 3 is enabled in standby mode
7	cp_stby_on	0	R/W	0	Charge pump is disabled in standby mode
				1	Charge pump is enabled in standby mode

Table 129. Charger supervision

Addr:14		Fuel Gauge			
		This bit controls first startup out of power on reset			
Bit	Bit Name	Default	Access	Description	
4	auto_shutdown	Boot ROM	R/W	Switch on Power off mode at first startup(e.g. First battery insertion or first charger insertion)	
				0	Startup of all regulators if battery is inserted, charger insertion, onkey pressed or rtc alarm.
				1	Startup of all regulators only if onkey is pressed or rtc alarm (no startup on battery insertion; no startup if charger detected, if no_charging=0). xon_enable has to be set in bootrom. If a charger is detected and the bit no_charging=0 (defined by BootROM) and ch_pwroff_en=0 the AS3658 will start charging without regulators startup (fully autonomous charging). If the bit no_charging=1 and a charger is detected, the regulators are started and the charging can be enabled with software control.

Table 130. Fuel Gauge

Addr:15		Fuel Gauge			
		This bit controls first startup out of power on reset			
Bit	Bit Name	Default	Access	Description	
5	power_off_at_v_suplow	Boot ROM	R/W	Switch on Power off mode if low Vsupply is detected during active or standby mode (Pin XON= high and bit xon_enable=0)	
				0	If low battery is detected, continuously monitor battery voltage and startup if battery voltage is above ResVoltrise
				1	If low battery is detected, enter power off mode

10.2.3 Reset Cycle

During a reset cycle the pin XRESET is forced to low for at least RES_{TIME} and all registers are set to their default values (except the registers marked green in theTable 186 on page 148). During the reset time a normal startup happens (see Startup on page 129), the reset is active until the reset timer (set by register bits *res_timer<2:0>*) expires. Then the voltage on the pin XRESET is pulled high by the external resistor and the whole system is leaving the reset state.

10.2.4 Reset Control: res_con

Reset is internally generated from a power supply supervisor and provided to internal logic as well as externally through the open-drain pad XRESET. At this point, it could be also forced externally from an external power supply supervisor. Additionally Reset can be forced by software.

10.3 Interrupt Controller

The interrupt controller generates an interrupt request for the host controller as soon as one or more of the bits in the *Interrupt* 1…3 register is set by pulling low pin XINT. All the interrupt sources can be enabled in the Interrupt Mask 1…3 register. The Interrupt 1…3 registers are cleared automatically after the host controller has read them. To prevent the AS3658 device from losing an interrupt event, the register that is read is captured before it is transmitted to the host controller via the serial interface. As soon as the transmission of the captured value is complete a logical AND operation with the bit wise inverted captured value is applied to the register to clear all interrupt bits that have already been transmitted. Clearing the read interrupt bits takes 2 clock cycles, a read access to the same register before the clearing process has completed will yield a value of '0'. Note that an interrupt that has been present at the previous read access will be cleared as well in case it occurs again before the clearing process has completed.

During a read access to one of the interrupt registers the XINT pin will be released. As soon as the transferred bits of the interrupt register have been cleared the XINT pin will be pulled low in case a new interrupt has occurred in the meantime. By doing so the interrupt controller will work correctly with host controllers that are edge- and level-sensitive on their interrupt request input. Multiple byte read access is recommended to avoid reading the *Interrupt 1* register over and over again in response to a new interrupt that has occurred in the same register (and thus pulling low pin XINT) before the Interrupt 2,3 register has been read.

Table 131. Interrupt Status 1 Register

Addr:50		Interrupt Status1		
		These bits show the status of the interrupts register is reset at power-on-reset and after each read access		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	chstate_i	NA	R	Bit is set when the following status bits are set or reset: Trickle, CVM, NoBat
1	cheoc_i	NA	R	Bit is set when the EOC status bits are set or reset:
2	charging_tmax_i	NA	R	Bit is set when charge timeout (tricke, CV, CC) has been expired
3	usb_chdet_i	NA	R	Bit is set when the USB_ChDet Bit is set or reset.
4	chdet_i	NA	R	Bit is set when the ChDet Bit is set or reset.
5	Onkey_i	NA	R	Bit is set when status XON bit is set or reset.
6	ovtmp_i	NA	R	Bit is set when the lower temperature threshold $Temp_{110}$ of the temperature sensor is exceeded for longer than $t_{RESMASK}$.
7	Lowsup	NA	R	Bit is set when the main supply voltage VSUPPLY has dropped below $V_{RESFALL}$ for longer than $t_{RESMASK}$.

Table 132. Interrupt Status 2 Register

Addr:51		Interrupt Status2		
		These bits show the status of the interrupts register is reset at power-on-reset and after each read access		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	sd1_lv_i	NA	R	Bit is set when voltage of step down1 drops below low voltage threshold (1msec debounce timer)
1	sd2_lv_i	NA	R	Bit is set when voltage of step down2 drops below low voltage threshold (1msec debounce timer)
2	sd3_lv_i	NA	R	Bit is set when voltage of step down3 drops below low voltage threshold (1msec debounce timer)

Table 132. Interrupt Status 2 Register

Addr:51		Interrupt Status2		
		These bits show the status of the interrupts register is reset at power-on-reset and after each read access		
Bit	**Bit Name**	**Default**	**Access**	**Description**
3	dig1_lv_i	NA	R	Bit is set when voltage of LdoDig1 drops below low voltage threshold (1msec debounce timer)
4	dig2_lv_i	NA	R	Bit is set when voltage of LdoDig2 drops below low voltage threshold (1msec debounce timer)
5	hphcurr_i	NA	R	Bit is set when output stage of headphone amplifier exceeds overcurrent limit.
6	bat_temp_i	NA	R	Bit is set when bit bat_hightemp or bat_lowtemp is set or reset
7	stpup1_i	NA	R	Bit is set when stpup1_oc or stpup1_det is set.

Table 133. Interrupt Status 3 Register

Addr:52		Interrupt Status3		
		These bits show the status of the interrupts register is reset at power-on-reset and after each read access		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	dig3_lv_i	NA	R	Bit is set when voltage of LdoDig3 drops below low voltage threshold (1msec debounce timer)
1	dig4_lv_i	NA	R	Bit is set when voltage of LdoDig4 drops below low voltage threshold (1msec debounce timer)
2	rtc_alarm_i	NA	R	Bit is set by the RTC, if alarm registers=rtc registers
3	rtc_rep_i	NA	R	Bit is set by the RTC every second (Bit irq_min=0) or minute (Bit irq_min=1)
4	mic_con_i	NA	R	Bit is set if a microphone is detected on MIC input
5	mic_rem_i	NA	R	Bit is set, if the microphone supply is increased (remote key press detected) -> measure MICS supply current
6	voxm_i	NA	R	Bit is set, if voice is detected on MIC input
7	tpen_i	NA	R	Bit is set, if the touchpen pendown is detected

Table 134. Interrupt mask 1 Register

Addr:47		Interrupt Mask1			
		These bits mask the interrupt			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
0	chstate_int_mask	1b	R/W	0	Interrupt is enabled
				1	Interrupt is disabled
1	cheoc_int_mask	1b	R/W	0	Interrupt is enabled
				1	Interrupt is disabled

Table 134. Interrupt mask 1 Register

Addr:47		Interrupt Mask1			
		These bits mask the interrupt			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
2	charging_tmax_int_mask	1b	R/W	0	Interrupt is enabled
				1	Interrupt is disabled
3	usb_chdet_int_mask	1b	R/W	0	Interrupt is enabled
				1	Interrupt is disabled
4	chdet_int_mask	1b	R/W	0	Interrupt is enabled
				1	Interrupt is disabled
5	onkey_int_mask	1b	R/W	0	Interrupt is enabled
				1	Interrupt is disabled
6	ovtmp_int_mask	1b	R/W	0	Interrupt is enabled
				1	Interrupt is disabled
7	LowSup_int_mask	1b	R/W	0	Interrupt is enabled
				1	Interrupt is disabled

Table 135. Interrupt mask 2 Register

Addr:48		Interrupt Mask2			
		These bits mask the interrupt			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
0	sd1_lv_int_mask	1b	R/W	0	Interrupt is enabled
				1	Interrupt is disabled
1	sd2_lv_int_mask	1b	R/W	0	Interrupt is enabled
				1	Interrupt is disabled
2	sd3_lv_int_mask	1b	R/W	0	Interrupt is enabled
				1	Interrupt is disabled
3	dig1_lv_int_mask	1b	R/W	0	Interrupt is enabled
				1	Interrupt is disabled
4	dig2_lv_int_mask	1b	R/W	0	Interrupt is enabled
				1	Interrupt is disabled
5	hphcurr_int_mask	1b	R/W	0	Interrupt is enabled
				1	Interrupt is disabled
6	bat_temp_int_mask	1b	R/W	0	Interrupt is enabled
				1	Interrupt is disabled
7	stpup1_int_mask	1b	R/W	0	Interrupt is enabled
				1	Interrupt is disabled

Table 136. Interrupt mask 3 Register

Addr:49		Interrupt Mask3			
		These bits mask the interrupt			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
0	dig3_lv_int_m	1b	R/W	0	Interrupt is enabled
				1	Interrupt is disabled
1	dig4_lv_int_m	1b	R/W	0	Interrupt is enabled
				1	Interrupt is disabled
2	rtc_alarm_int_m	1b	R/W	0	Interrupt is enabled
				1	Interrupt is disabled
3	rtc_rep_int_m	1b	R/W	0	Interrupt is enabled
				1	Interrupt is disabled
4	mic_con_int_m	1b	R/W	0	Interrupt is enabled
				1	Interrupt is disabled
5	mic_rem_int_m	1b	R/W	0	Interrupt is enabled
				1	Interrupt is disabled
6	voxm_intm	1b	R/W	0	Interrupt is enabled
				1	Interrupt is disabled
7	tpen_i_m	1b	R/W	0	Interrupt is enabled
				1	Interrupt is disabled

Table 137. Low voltage status1 Register1

Addr:53		Low voltage status1		
		These bits show the low voltage status of the step down and digital regulators		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	sd1_lv	NA	R	Step down1 low voltage status bit (-10% voltage drop)
1	sd2_lv	NA	R	Step down2 low voltage status bit (-10% voltage drop)
2	sd3_lv	NA	R	Step down3 low voltage status bit (-10% voltage drop)
3	dig1_lv	NA	R	Ldo Dig1 low voltage status bit (-50mV voltage drop)
4	dig2_lv	NA	R	Ldo Dig2 low voltage status bit (-50mV voltage drop)
5	-	-	-	-
6	stpup1_oc	NA	R	Bit is set by analog part, if overcurrent of DCDC StepUp1 occurs for more than 5msec (latched state)
7	stpup1_det	NA	R	Current Detection signal of step up 1

Table 138. Low voltage status2 Register1

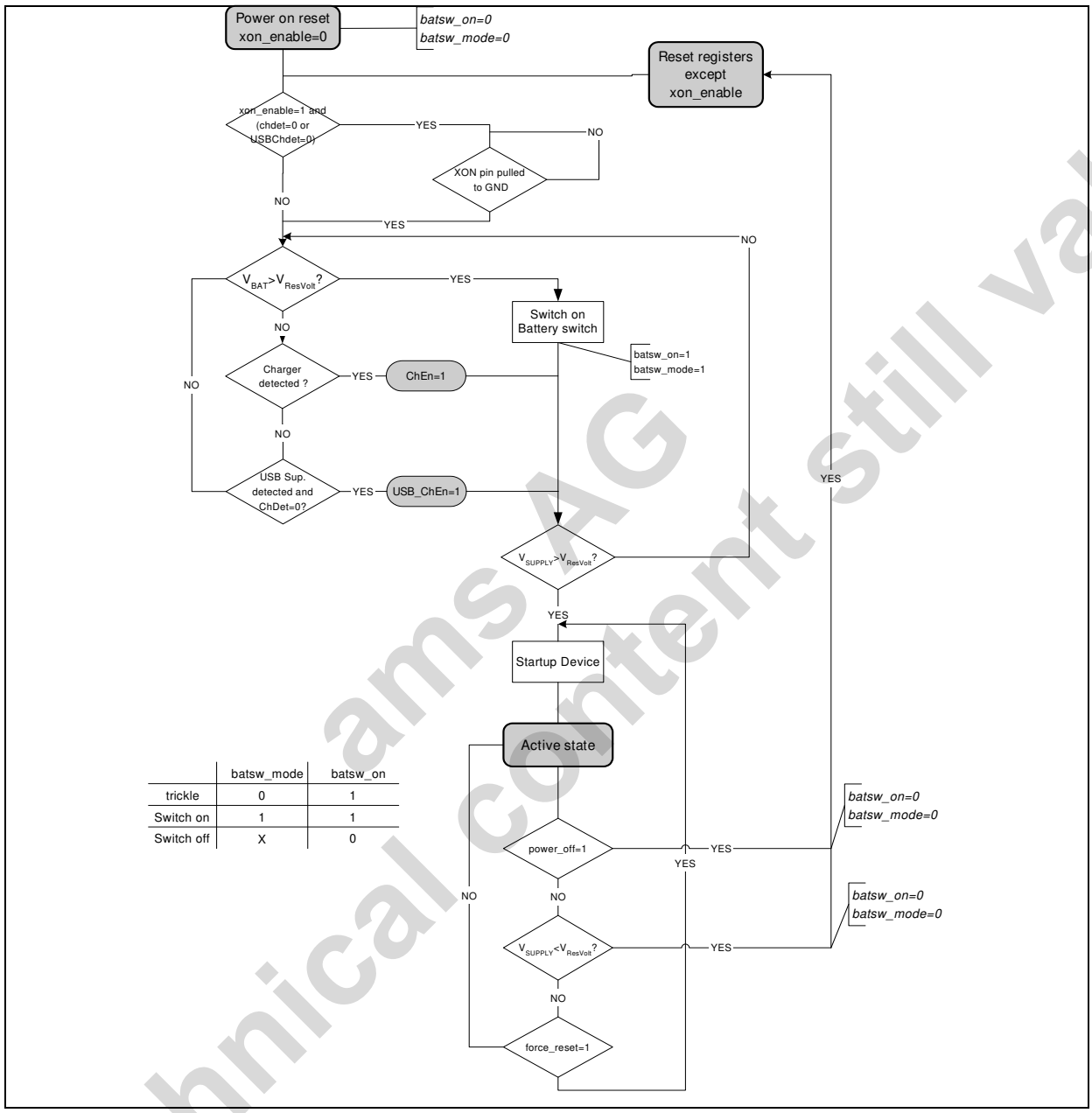
Addr:54		Low voltage status2		
		These bits show the low voltage status of the step down and digital regulators		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	dig3_lv	0b	R	Ldo Dig3 low voltage status bit (-50mV voltage drop)
1	dig4_lv	0b	R	Ldo Dig4 low voltage status bit (-50mV voltage drop)

Table 138. Low voltage status2 Register1

Addr:54		Low voltage status2		
		These bits show the low voltage status of the step down and digital regulators		
Bit	**Bit Name**	**Default**	**Access**	**Description**
2	dcdc_curr1_lv	0b	R	Indicates low voltage on dcdc_curr1
3	dcdc_curr2_lv	0b	R	Indicates low voltage on dcdc_curr2
4	dcdc_curr3_lv	0b	R	Indicates low voltage on dcdc_curr3
5	bat_lowtemp	0b	R	Indicates NTC temperature of battery below 0º
6	bat_hightemp	0b	R	Indicates NTC temperature of batter above 45º (50º)

10.4 Startup

Figure 56. Startup flow chart



10.4.1 Normal Startup

During a normal reset cycle (e.g. after the battery or a charger is inserted; (see Reset generator and XON-Key on page 118)), after V2_5 is above V_{POR} and Vsupply is above $VRESET_{RISE}$ a normal startup happens:

- The external capacitor on CREF is charged to 1.8V
- The 3bit A/D conversion is performed to measure the external resistor value RPROGRAM
- Startup State machine reads out the internal Boot-ROM (address defined by *boot_ctrl*), Start sequence of Step-Down Converter and LDO's controlled by the Boot-ROM
- Reset-Timer is set by the Boot-ROM
- The reset is released when the Reset Timer expires (external pin XRESET)

10.4.2 Startup from Charger

If the voltage on pin VCHARGER is within VSTARTCHARGER, the AS3658 is started (even with VBAT = 0V). This allows the battery to be charged (even from deeply discharged batteries) and finally a normal startup to happen.

Table 139. Charger Startup Conditions

Symbol	Parameter	Min	Typ	Max	unit	Note
VSTARTCHARGER	Voltage on VCHARGER for system to start	4.0	5.0	15	V	on Pin VCHARGER

10.4.3 Programmable Startup Sequences—Boot ROM

The startup- and reset sequences of the device are highly configurable. The configuration of these sequences is defined by the ratio of the internal trimmed bias resistors and RPROGRAM. At the beginning of each reset cycle a 3 bit AD-conversion is performed. The result of this conversion is used to select 1 of 8 possible address-ranges of an internal mask-programmable ROM. The information that is stored in this ROM defines the following parameters:

- Voltage levels for all regulators and step down dcdc converters
- power-on sequence of RF_1, RF_2, DIG_1, DIG_2, SD1, SD2 and SD3
- duration of the reset cycle
- several other configuration bits (e.g. charger)

The following values of $R_{PROGRAM}$ are used to select the 8 possible address ranges (8 different startup voltage / sequences settings can be used):

- 000: open
- 001: 320kΩ
- 010: 160kΩ
- 011: 80kΩ
- 100: 40kΩ
- 101: 20kΩ
- 110: 10kΩ
- 111: 0Ω

Table 140. Boot ROM Bits definitions

Addr:107		Boot_status		
		These bits show the boot status		
Bit	**Bit Name**	**Default**	**Access**	**Description**
2:0	rom_adr	NA	R	Boot-ROM address
3	rom_valid	1	R	If ‘1’ Boot-ROM address is valid

Note: For detailed startup sequences see austriamicrosystems AG document AS3658_BootROM_*.

10.4.4 Additional Startup Settings

Table 141. Boot ROM Bits definitions

Addr:4		LDO_RF2_Voltage			
		These bits defines the startup sequence			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
7	double_reset	ROM	R/W	0	Normal reset pulse
				1	Apply double reset pulse after the normal rest pulse that is define by res_timer. (pulse on XRESET with 2msec high time and 2msec low time
6	slow_startup	ROM	R/W	0	Normal startup of LDOs defined in boot rom with a separation of 1 milliseconds
				1	Startup of all LDOs defined by boot rom with a time separation of 4 milliseconds

10.4.5 Programmable Startup Sequences with fuse registers—Boot OTP

Its possible to program some startup registers, by using the fuse block:

Table 142. ROMF Bit definitions

Addr:196		FUSE4			
		These bits control the startup and are set by factory test			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
7	romf_en	0	R	0	Fusible startup rom disabled
				1	Feasible startup of rom enabled (UniqueID0.UniqueID10) used for startup

Table 143. ROMF Bit definitions

Addr:197		addrf0			
		These bits control the startup and are set by factory test			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
7:0	addrf<7:0>	0	R	Each bit represents a register address of the bootrom table (0....31)	
				0	Use data of ROM table during startup for the according address (0....31)
				1	Use data of fuse register during startup for the according address, starting with data of register romf0 (up to register romf6 max.)

Table 144. ROMF Bit definitions

Addr:198		addrf0			
		These bits control the startup and are set by factory test			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
7:0	addrf<15:8>	0	R	Each bit represents a register address of the bootrom table (0....31)	
				0	Use data of ROM table during startup for the according address (0....31)
				1	Use data of fuse register during startup for the according address, starting with data of register romf0 (up to register romf6 max.)

Table 145. ROMF Bit definitions

Addr:199		addrf2			
		These bits control the startup and are set by factory test			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
7:0	addrf<23:16>	0	R	Each bit represents a register address of the bootrom table (0....31)	
				0	Use data of ROM table during startup for the according address (0....31)
				1	Use data of fuse register during startup for the according address, starting with data of register romf0 (up to register romf6 max.)

Table 146. ROMF Bit definitions

Addr:200		addrf3			
		These bits control the startup and are set by factory test			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
7:0	addrf<31:24>	0	R	Each bit represents a register address of the bootrom table (0....31)	
				0	Use data of ROM table during startup for the according address (0....31)
				1	Use data of fuse register during startup for the according address, starting with data of register romf0 (up to register romf6 max.)

Table 147. ROMF Bit definitions

Addr:201		romf0		
		These bits control the startup and are set by factory test		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	romf0	00h	R	Data for startup register (used for the first “1” in the addrf<31:0> register

Table 148. ROMF Bit definitions

Addr:202		romf1		
		These bits control the startup and are set by factory test		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	romf1	00h	R	Data for startup register (used for the second “1” in the addrf<31:0> register

Table 149. ROMF Bit definitions

Addr:203		romf2		
		These bits control the startup and are set by factory test		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	romf2	00h	R	Data for startup register (used for the third “1” in the addrf<31:0> register

Table 150. ROMF Bit definitions

Addr:204		romf3		
		These bits control the startup and are set by factory test		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	romf3	00h	R	Data for startup register (used for the fourth “1” in the addrf<31:0> register

Table 151. ROMF Bit definitions

Addr:205		romf4		
		These bits control the startup and are set by factory test		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	romf4	00h	R	Data for startup register (used for the fifth “1” in the addrf<31:0> register

Table 152. ROMF Bit definitions

Addr:206		romf5		
		These bits control the startup and are set by factory test		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	romf5	00h	R	Data for startup register (used for the sixth “1” in the addrf<31:0> register

Table 153. ROMF Bit definitions

Addr:207		romf6		
		These bits control the startup and are set by factory test		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	romf6	00h	R	Data for startup register (used for the seventh “1” in the addrf<31:0> register

10.5 Protection Functions

All LDO's, the DCDC step ups and DCDC step downs have an integrated overcurrent protection. An overtemperature protection of the chip is also integrated which can be switched on with the serial interface signal temp_pmc_on (enabled by default; it is not recommended to disable the overtemperture protection). The chip has two signals for the serial interface: ov_temp_110 and ov_temp_140. The flag ov_temp_110 is automatically reset if the overtemperature condition is removed, whereas ov_temp_140 has to be reset by the serial interface with the signal rst_ov_temp_140.

If the flag ov_temp_140 is set, an automatic reset of the complete chip is initiated. The flag ov_temp_140 is not affected by this reset cycle allowing the software to detect the reason for this unexpected shutdown.

Table 154. Overtemperature Detection

Symbol	Parameter	Min	Typ	Max	Unit	Note
T_{110}	ov_temp_110 rising threshold	95	110	125	ºC	
T_{140}	ov_temp_140 rising threshold	125	140	155	ºC	
T_{hyst}	ov_temp_110 and ov_temp_140 hysteresis		5		ºC	

Table 155. Overtermperature detection Bit definition

Addr:106		Overtemperature Control		
		These bits control the startup and are set by factory test		
Bit	Bit Name	Default	Access	Description
0	temp_pmc_on	1	R/W	Switch on / off of temperature supervision; default: on – all other bits are only valid if set to '1' **Leave at 1**, do not disable
1	ov_temp_110	NA	R	Flag that the overtemperature threshold 1 (T_{110}) has been reached
2	ov_temp_140	NA	R	Flag that the overtemperature threshold 2 (T_{140}) has been reached – this flag is not reset by a overtemperature caused reset and has to be reset by rst_ov_temp_140
3	rst_ov_temp_140	0	W	If the overtemperature threshold 2 has been reached, the flag ov_temp_140 is set and a reset cycle is started. ov_temp_140 should be reset by writing 1 and afterward 0 to rst_ov_temp_140

10.5.1 Temperature Supervision

A temperature sensor is implemented to provide over-temperature protection of the chip. It generates two flags linked to the two temperature thresholds (110 degrees, 140 degrees). Both thresholds have an hysteresis to prevent oscillation effects.

First threshold (110 degrees) sets the flag ov_temp_110, signalling the serial interface part and software the 110 degrees overtemperature condition. If enabled (ovtmp_int_mask=0), an interrupt can be send (interrupt 'ovtmp'). Thus software can react and can shutdown power consuming functions to decrease temperature.

The second threshold (140 degrees) initiates a reset cycle and sets ov_temp_140: this sets all regulators into power-down mode and stops charging, and performs the reset cycle of the AS3658.

rst_ov_temp_140 flag

In case of overtemperature and an activated reset (temp_pmc_on=1), the system loses any information about the error which activated the reset state. Therefore, a flag is implemented, which indicates that the reset was caused by overtemperature activation (ov_temp_140 is set). This flag is only resetable by writing '1' to rst_ovtemp_140.

10.6 Watchdog

The purpose of the watchdog is to detect a deadlock of the software. If the watchdog is active, it must receive a continuous trigger signal within a programmable time window. If there is no signal anymore for a certain time period from a defined pad or special serial interface bit, it starts either a complete reset cycle or changes the state of an output pin, which can be used e.g. as an interrupt to the processor.

- The watchdog is highly configurable by the following register bits:
- The complete block can be switched on by wtdg_on = 1 and off by wtdg_on = 0.
- The watchdog time window is defined by the register wtdg_min_timer and wtdg_max_timer.
- The trigger signal can be configured by register wtdg_trigger and wtdg_gpio_input. (Pin CURR1-CURR4 (GPIO1-GPIO4) or register bit)
- If the watchdog expires, the system can start automatically a reset cycle if wtdg_reset_on = 1
- Any of the general purpose input / outputs can be configured to output the watchdog signal. The Watchdog delivers a signal “wtdg_alarm”, which is normal ‘0’ and goes to ‘1’ in the case of a timer-overflow. This signal can be used as e.g. a reset or interrupt for a processor.

Table 156. Watchdog Register definitions

Addr:60		Watchdog control			
		These bits control the watchdog functions			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
0	wtdg_on	0	R/W	Switches on the complete watchdog	
				0	watchdog off
				1	watchdog enabled
1	wtdg_res_on	1	R/W	If the watchdog expires and *wtdg_res_on* = 1 a reset cycle will be started	
2	wtdg_trigger	0	R/W	0	Use the register bit *wtdg_sw_signal* as trigger signal for the watchdog
				1	Use one of the GPIO pins CURR1_GPIO1 … CURR4_GPIO4 as trigger input for the watchdog; the actual pin is selected by setting GPIOXIOSF to 01b(watchdog mode) and GPIOXMode=010b (GPIO digital input) (X=1...4)

Table 157. Watchdog minimum timer definitions

Addr:61		Watchdog_min timer		
		These bits set the watchdog minimum timer		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	Wtdg_min_timer	00h	R/W	Defines the minimum watchdog trigger time (LSB=7.5ms, range: 0 – 1.9s)

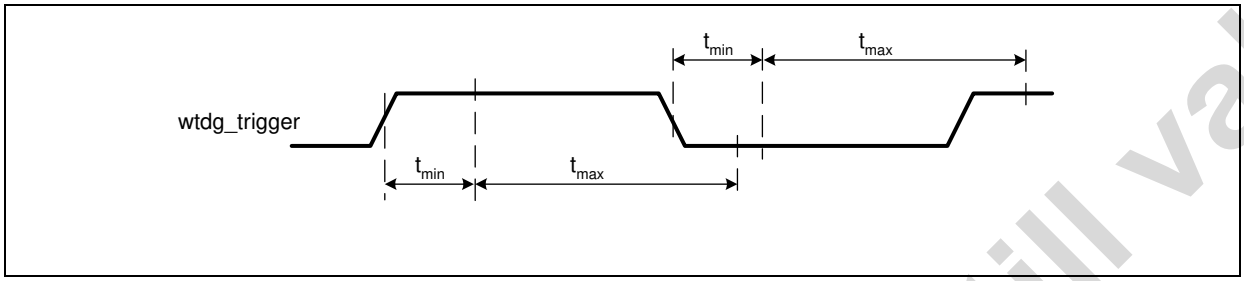
Table 158. Watchdog max timer definitions

Addr:62		Watchdog_max timer		
		These bits set the watchdog maximum timer		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	Wtdg_max_timer	FFh	R/W	Defines the maximum watchdog trigger time (LSB=7.5ms, range: 7.5ms – 1.9s), do not set to (00)h

Table 159. Watchdog software signal definitions

Addr:63		Watchdog software signal		
		This bit sets the watchdog software trigger		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	wtdg_sw_signal	0	R/W	Trigger input by the serial interface if *wtdg_trigger* = 0

Figure 57. Watchdog timing diagram



10.7 General Purpose 10 Bit ADC

Table 160. ADC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Note
Resolution		10			Bit	
Input Voltage Range	Vin	0		1.8	V	
Differential Nonlinearity	DNL		± 0.25		LSB	1LSB 1.76mV (depending on selected channel)
Integral Nonlinearity	INL		± 0.5		LSB	
Input Offset Voltage	Vos		2		LSB	
Input Impedance	Rin	100			MΩ	
Input Capacitance	Cin			9	pF	
Power Supply Current	Idd		500		µA	During conversion only
Power Down Current	Idd		100		nA	
Transient Parameters (25°C)						
Conversion Time	Tc		40		µs	
Clock Frequency	fc		$f_{clk\_int}/8$		kHz	internal CLK frequency/8 Programmable: 0.2 to 0.2875 MHz
Settling time of S&H	ts	1			µs	
ADC_IN1 pull up current		14.25	15	15.75	µA	Pull up current for ADC_IN1, if adc_idc=1111b

Table 161. ADC control Registers bits

Addr:96		ADC_control			
		This register controls the 10 Bit ADC			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
3:0	adc_select	0000b	R/W	Selects an ADC channel	
				0000	ADC1_IN (LSB = 1.76mV)
				0001	ADC2_IN (LSB = 1.76mV)
				0010	V_{BAT} Battery voltage (LSB=5.27mV)
				0011	VCHARGER (LSB=17. 6mV) clamping at 10V
				0100	V_USB Voltage (LSB=5.27mV)
				0101	not used
				0110	temperature sensor: DIE temperature [°C] = adc_result * 0.866 – 274
				0111	ADC test channel – do not use
				1000	check voltage on MICS for remote control or external voltage measurement (LSB=3.52mV)
				1001	VBACK voltage (LSB=3.52mV)
4	adc_slow	0b	R/W	select ADC sampling frequency	
				0	275kHz (conversion time: 60µs)
				1	70kHz (conversion time: 240µs)
5	-	-	-	reserved (do not use)	
6	adc_on	0b	R/W	Writing a 1 into this bit continuously activates the ADC S/H and the input multiplexer. The ADC and the MUX are also activated for a conversion period when start_conversion is set to '1' – useful for high impedance input sources on ADC1_IN or ADC2_IN	
7	start_conversion	0b	R/W	Writing a 1 into this bit starts one ADC conversion.	

Table 162. ADC MSB result register

Addr:97		ADC_MSB result			
		This register shows the MSB result of the ADC conversion			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
0	D3	NA	R	ADC result register	
1	D4	NA	R	ADC result register	
2	D5	NA	R	ADC result register	
3	D6	NA	R	ADC result register	
4	D7	NA	R	ADC result register	
5	D8	NA	R	ADC result register	
6	D9	NA	R	ADC result register	
7	result_not_ready	NA	R	Indicates end of conversion	
				0	result is ready
				1	conversion is running

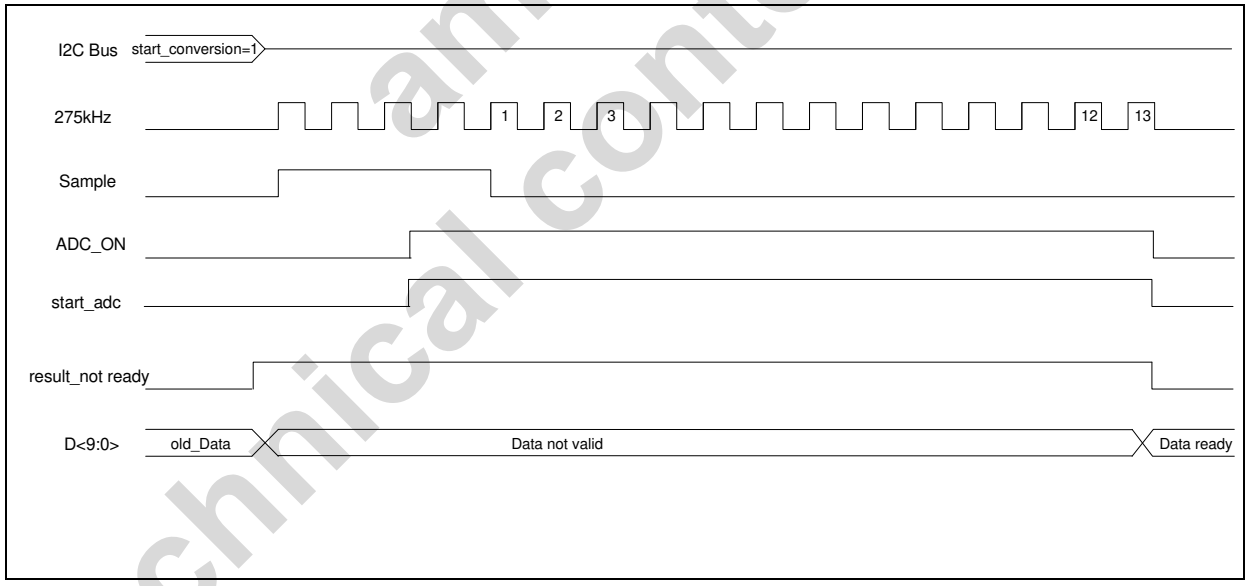
Table 163. ADC LSB result register

Addr:98		ADC_LSB result		
		This register shows the LSB result of the ADC conversion		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	D0	NA	R	ADC result register
1	D1	NA	R	ADC result register
2	D2	NA	R	ADC result register
7:3	-	-	-	reserved (do not use)

Table 164. ADC IDAC register

Addr:46		ADC idac			
		This register controls the current sink on pin ADC_IN1			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
0	adc_idac	000b	R/W		Current source at ADC_IN1 input Set to 0000 if battery temperature supervision is enabled.
				0000	0µA (current sink disabled)
				0001	1µA
				...	
				1111	15 µA

Figure 58. ADC Timing-diagram



10.8 Internal References (V, I, fclk)

The internal reference circuits needs the following external components:

Table 165. Reference External Components

Symbol	Parameter	Min	Typ	Max	Unit	Note
CEXT	External filter capacitor	-10%	100	+10%	nF	Ceramic low-ESR capacitor between CREF and VSS
RBIAS	External bias current set resistor	-1%	220	+1%	kΩ	Bias Current set resistor between RBIAS and VSS

Table 166. References Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Note
VCEXT	Reference Voltage	-1%	1.8	+1%	V	Low noise trimmed voltage reference – connected to Pad CREF; **do not load**
fCLK	Accuracy of Internal reference clock	-10	fCLK	+10	%	Adjustable by serial interface register clk_int

To reduce the current consumption of the chip, the circuit can be set into a special low power mode with the serial interface bit '**low_power_on**'. All specification parameters except the noise parameters are still valid for this mode.

Table 167. Internal references Bit definitions

Addr:59		Internal references Bit definitions			
		These bits control the internal reference mode and internal clk frequency			
Bit	Bit Name	Default	Access		Description
0	low_power_on	0b	R/W	0	Standard mode
				1	Low power mode – all specification except noise parameters are still valid
3:1	clk_int	110b	R/W	Sets the internal CLK frequency fCLK used for fuel gauge, DCDCs, PWM, charge pump. All frequencies, timings and delays in this datasheet are based on 2.2MHz clk_int	
				000b	1.6 MHz
				001b	1.7 MHz
				010b	1.8 MHz
				011b	1.9 MHz
				100b	2.0 MHz
				101b	2.1 MHz
				110b	2.2 MHz (default)
				111b	2.3 MHz

10.8.1 Low Power Mode

Use bit ***low_power_on*** (reg. References Control (see Table 167)) to activate the Low Power Mode. In this mode the on-chip voltage reference and the temperature supervision comparators are operating in pulsed mode. This reduces the quiescent current of the AS3658 by 45uA (typ.). Because of the pulsed function some specifications are not fulfilled in this mode (e.g. increased noise), but still the full functionality is available.

Note: Low power mode can be controlled by the serial interface.

10.9 Real-Time Clock (RTC) Module

The RTC module provides time information to the system. It is implemented as a 6-bit counter that is incremented every second - with the 32kHz oscillator delivering the necessary accurate time base – and is reset to 0 each time the counter value is 60. An additional 24-bit minute counter is incriminated each time the 6-bit counter is reset to 0. Both counters are set to 0 at a power-on-reset. The host controller can set the counter to any value by setting the RTC 1…4 registers.

To prevent ambiguous time information because of the 30-bit value being incremented before all of the 4 registers have been read or written, a 30-bit parallel shadow register is implemented. Every time a write/read access via the serial interface occurs the parallel shadow register is updated with the current value of the 30-bit counter. Any write access to the RTC 1 register will disable the update of the parallel register and set the value of the appropriate byte of the parallel register. Any subsequent write access to the RTC 4 register will transfer the current value of the 30-bit parallel register to the RTC 1…4 registers and the update of the parallel register is enabled again. Similarly, any read access to the RTC 1 register will freeze the current value of the parallel register and submit the appropriate byte to the host controller via the serial interface. Any subsequent read access to the RTC 4 register will enable the update of the parallel register again. This mechanism makes sure that the maximum error of the value that is written to or read from the registers is 1 second.

The startup state after power on reset:RTCSecond=3F, RTCMinute1=FF, RTCMinute2=FF, RTCMinute3=FF
To start the RTC, rtc_mode bits have to be set to a non zero value, and the RTC registers have to be set.
The RTC stops automatically at its highest value (3F,FF,FF,FF) to prevent overrun.

Table 168. RTC Second Register

Addr:64		RTCSecond		
		These bits represents the actual RTC second register register is reset at power-on-reset only		
Bit	**Bit Name**	**Default**	**Access**	**Description**
5:0	RTCSecond	00h	R/W	Bits 5:0 of the 6-bit RTC second counter
7:6	-	-	reserved	

Table 169. RTC Minute1 Register

Addr:65		RTCMinute1		
		These bits represents the actual RTC Minute1 register register is reset at power-on-reset only		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	RTCMinute1	00h	R/W	Bits 7…0 of the 24-bit RTC minute counter

Table 170. RTC Minute2 Register

Addr:66		RTCMinute2		
		These bits represents the actual RTC Minute2 register register is reset at power-on-reset only		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	RTCMinute2	00h	R/W	Bits 15:8 of the 24-bit RTC minute counter

Table 171. RTC Minute3 Register

Addr:67		RTCMinute3		
		These bits represents the actual RTC Minute3 register register is reset at power-on-reset only		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	RTCMinute3	00h	R/W	Bits 23:16 of the 24-bit RTC minute counter

The RTC module includes an alarm function. When the content of the RTC 1…4 registers equals the content of the RTC Alarm 1…4 registers bit RTCAlarm will be set in the Interrupt 1 register. Furthermore the RTC module can generate an interrupt every second (RTC1Sec will be set) and every minute (RTC1min will be set every time the 6-bit second counter is reset to 0). For further details on interrupt generation please refer to Interrupt Controller on page 124.

To avoid ambiguous behavior during write access to the RTC Alarm 1…4 registers any write access to the RTC Alarm 1 register will disable the alarm function; any subsequent write access to the RTC Alarm 4 will enable the alarm function again.

Table 172. RTC Alarm second Register

Addr:68		RTC AlarmSecond		
		These bits set the RTC Alarm Seconds register is reset at power-on-reset only		
Bit	**Bit Name**	**Default**	**Access**	**Description**
5:0	RTCAlarmSecond	3Fh	R/W	Bits 5…0 of 6-bit RTC second alarm value

Table 173. RTC Alarm minute1 Register

Addr:69		RTC AlarmMinute1		
		These bits set the RTC Alarm Minute1 register is reset at power-on-reset only		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	RTCAlarmMinute1	FFh		Bits 7:0 of the 24-bit RTC minute alarm value

Table 174. RTC Alarm minute2 Register

Addr:70		RTC AlarmMinute2		
		These bits set the RTC Alarm Minute2 register is reset at power-on-reset only		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	RTCAlarmMinute2	FFh		Bits 15:8 of the 24-bit RTC minute alarm value

Table 175. RTC Alarm minute3Register

Addr:71		RTC AlarmMinute3		
		These bits set the RTC Alarm Minute3 register is reset at power-on-reset only		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	RTCAlarmMinute3	FFh		Bits 23:16 of the 24-bit RTC minute alarm value

Table 176. RTCT Register

Addr:72		RTCT			
		These bits set the RTC correction and RTC interrupt mode register is reset at power-on-reset only			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
6:0	RTC_TBC<6:0>	0000000	R/W	These bits are used to correct the inaccuracy of the used 32kHz crystal. Correction is done all 8 seconds by removing or adding two clock cycles. Trimming register for RTC, 128 steps @ 7.6ppm	
				100000	- 480.4ppm
				100001	-472.8ppm
				111111	-7.6ppm
				000000	0ppm(default)
				000001	7.6ppm
				011110	472.8ppm
				011111	480.4ppm
7	rtc_irq_mode	0	R/W	0	generate an interrupt every second
				1	generate an interrupt every minute The interrupt has to be enabled by rtc_rep_int_m=0

Table 177. Reset Timer Register

Addr:22		Reset Timer			
		These bits set RTC modes			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
4	rtc_alarm_wakeup_en	ROM	R/W	0	Disables RTC alarm wakeup in power off mode
				1	Enable RTC alarm wakeup in power off mode
5	rtc_rep_wakeup_en	ROM	R/W	0	Disables RTC repeated wakeup in power off mode
				1	Enable RTC repeated wakeup in power off mode
7:6	rtc_mode	ROM	R/W	00	32kHz oscillator off
				01	32kHz oscillator enabled
				10	32kHz oscillator enabled, Pin Q32k enabled
				11	reserved (do not use)

10.10 Touchpen Interface

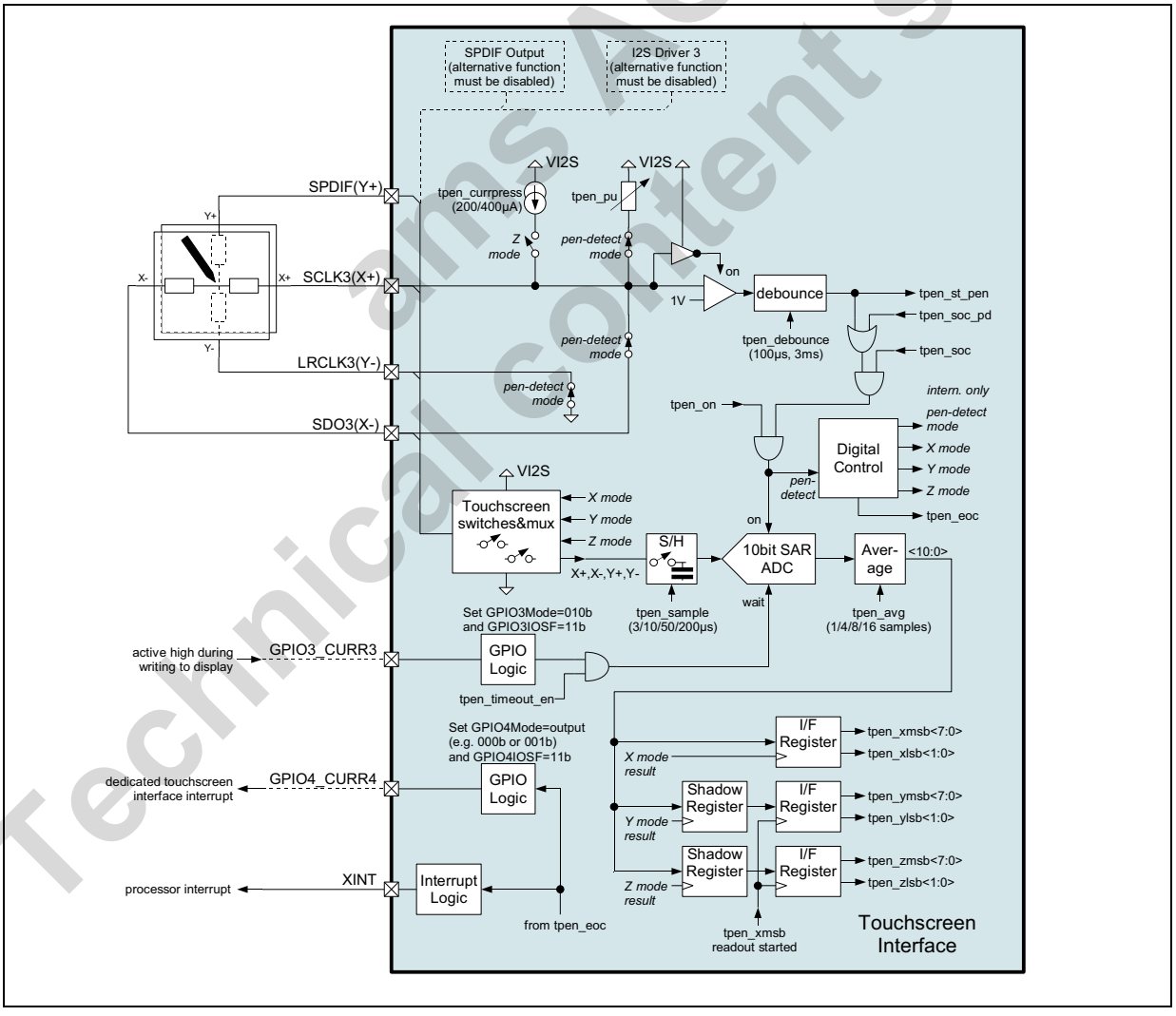
The touchpen interface controls a resistive touchpen. It has the following features:

- Low Power Pen Detect
- Measure pen X,Y position
- Measure pen pressure (Z-position)
- Interrupt, if X,Y,Z data is available; one dedicated output – CURR4_GPIO4 can be configured to be used as touchpen interrupt output and/or standard interrupt output XINT
- The conversion interval can be adjusted
- Up to 16 ADC conversion can be averaged internally
- The sample time of the ADC can be adjusted
- The pin CURR3_GPIO3 can be configured to enable/disable the ADC conversion (useful if the processor updates the LCD to avoid parallel reading of the touchpen position)

The touchpen interface shares the pins with the SPDIF output and the I2S Output 3. If the touchpen interface is used, the SPDIF and the I2S Output 3 cannot be used (and has to be disabled).

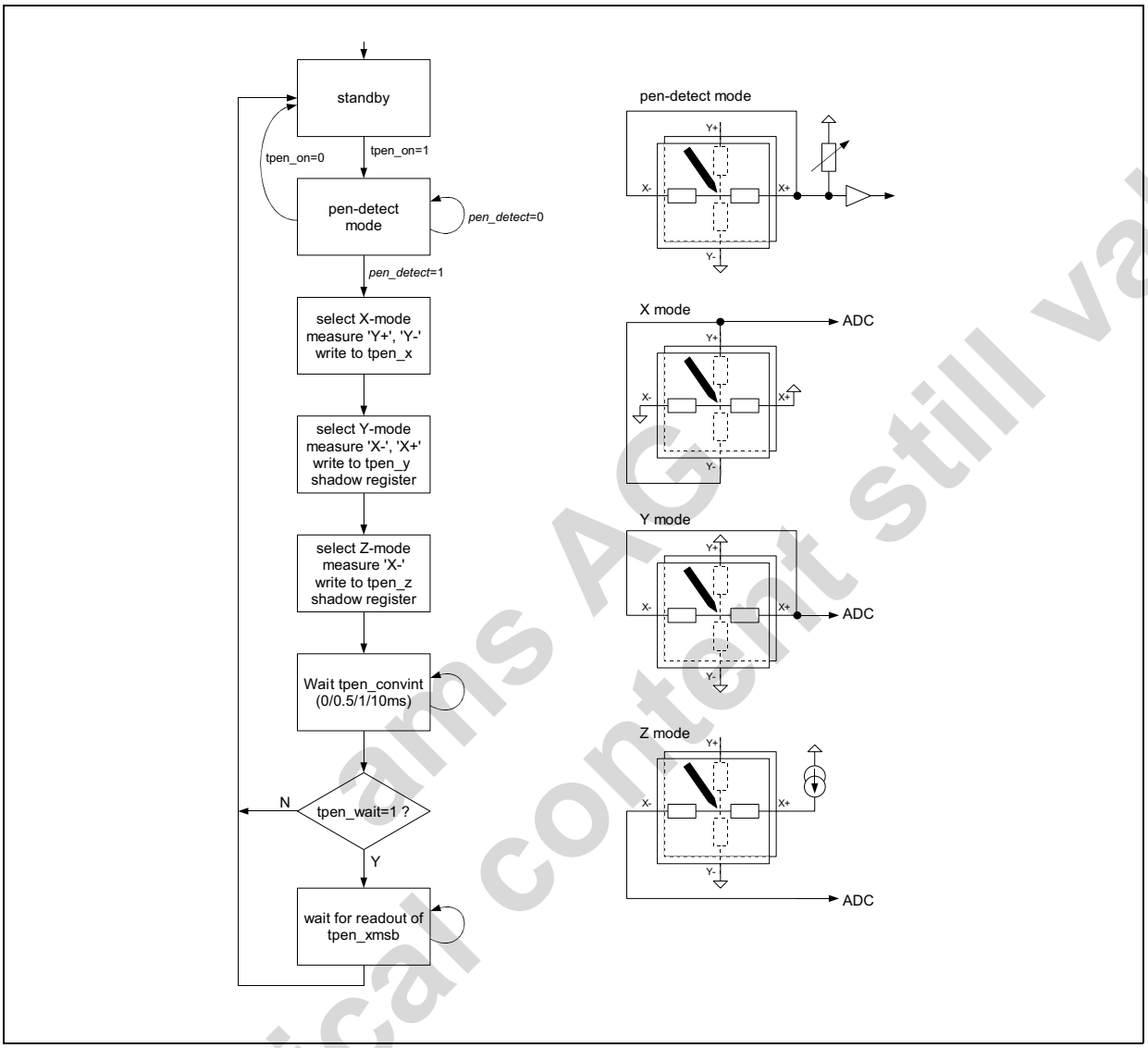
Note: The touchpen interface and the 'General Purpose 10 Bit ADC' can be used at the same time.

Figure 59. Touchpen Block diagram



The touchpen controller is operating according to the following state diagram:

Figure 60. Touchpen State diagram



10.10.1 Software guidelines

1. Setup the configuration registers (tpen – control 1..3) according the hardware
2. Enable receiving of touchpen interrupts (either through XINT or GPIO4_CURR4)
3. Upon receiving of a touchpen interrupt, readout tpen_xmsb, tpen_ymsb (and if required tpen_pressmsb and tpen_xypresslsb) with a **single** I2C **blockread**. This ensured, that the x,y,z is correctly readout and all data belong to one single touchpen x,y,z conversion
4. Perform all the required processing with the data (e.g. accept a pen-down only if the pen is forced onto the touchscreen with a minimum pressure [z-position])

10.10.2 Touchpen Registers

Table 178. Touchpen Register Map

Register Definition	Addr	Default	Content							
Name				b6	b5	b4	b3	b2	b1	b0
tpen_xmsb	108	NA	XD9	XD8	XD7	XD6	XD5	XD4	XD3	XD2
tpen_ymsb	109	NA	YD9	YD8	YD7	YD6	YD5	YD4	YD3	YD2
tpen_pressmsb	110	NA	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2
tpen_xypresslsb	111	NA	PD1	PD0	0	YD1	YD0	0	XD1	XD0
tpen – control 1	112	00h	tpen_st_pen	tpen_eoc	tpen_avg		tpen_soc	tpen_convint		tpen_on
tpen – control 2	113	00h	tpen_socpd	tpen_wait	tpen_curr press	tpen_pu				
tpen – control 3	114	00h					tpen_timeout _en	tpen_debounce	tpen_sample	

Note: The cells marked in color are Read only

Table 179. Touchpannel Result Register Bits

Addr:108		Touchpad_XMSB result		
		X-MSB result register		
Bit	Bit Name	Default	Access	Description
7:0	tpen_xmsb	00000000	R	X – MSB Data

Table 180. Touchpannel Result Register Bits

Addr:109		Touchpad_YMSB result		
		Y-MSB result register		
Bit	Bit Name	Default	Access	Description
7:0	tpen_ymsb	00000000	R	Y – MSB Data

Table 181. Touchpannel Result Register Bits

Addr:110		Touchpad_Pressure result		
		Pressure result register		
Bit	Bit Name	Default	Access	Description
7:0	tpen_pressmsb	00000000	R	Pressure - Data

Table 182. Touchpannel Result Register Bits

Addr:111		Touchpad_XY - LSB result		
		X - MSB result register		
Bit	Bit Name	Default	Access	Description
1:0	tpen_xlsb	00	R	X – LSB Data
4:3	tpen_ylsb	00	R	Y – LSB Data
7:6	tpen_presslsb	00	R	Pressure – LSB Data

Table 183. Touchpannel Control Register Bits

Addr:112		Touchpad – control 1			
		This register controls the different modes of the Touchpad			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
0	tpen_on	0	R/W	Enables Touch Pen Function	
				0	OFF (No wakeup on pen down)
				1	Pen Detect enabled → wakes up Pen Digitizer → Check Pen_Status -> if pen-detect or tpen_soc_pd=1 and tpen_soc=1 then perform X,Y,Z measurements
2:1	tpen_convint	00	R/W	Conversion Interval Timer	
				00	No delay between conversions
				01	every 512 clock periods (0,5 ms) ADC – Averaging limited to max. 4
				10	every 1024 clock periods (1ms) ADC – Averaging limited to max. 8
				11	every 10240 clock periods (10ms)
3	tpen_soc	0	R/W	Start Conversion (x,y, and z conversion)	
				0	No Conversion if pen down detected
				1	Start Conversion if pen down detected or tpen_soc_pd=1 and tpen_on=1 (X, Y and Z-Pressure Measurement)
5:4	tpen_avg	0	R/W	Averaging of x and y measurement	
				00	no averaging
				01	4 measurements (per channel)
				10	8 measurements (per channel)
				11	16 measurements (per channel)
6	tpen_eoc	0	R/W	ADC - End of Conversion bit	
				0	TP in Power down or Conversion ongoing
				1	Valid TP data available (x,y, and pressure) generates an interrupt on GPIO4_CURR4 and/or XINT; the interrupt is released when the readout from the tpen_xmsb is started
7	tpen_st_pen	0	R	Pen status	
				0	penup
				1	pendown

Table 184. Touchpannel Control Register Bits

Addr:113		Touchpad – control 2			
		This register controls the different modes of the Touchpad			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
4:0	tpen_pu	00000	R/W	Internal Resistor used for Pen detection	
				00000	Do not use this Setting
				00001	4kΩ
				00010	8kΩ
				...	
				00100	16kΩ
				...	
				01000	32kΩ
				...	
				10000	64kΩ (most sensitive)
				...	
				11111	~ 2kΩ
5	tpen_currpress	0	R/W	Current used for pressure measurement	
				0	200µA
				1	400µA
6	tpen_wait	0	R/W	0	Do not wait until tpen_xmsb is readout
				1	Start next ADC – conversion after data is read from Register tpen_xmsb
7	tpen_soc_pd	0	R/W	0	Start conversion only if tpen_st_pen is 1 and tpen_soc=1 and tpen_on=1
				1	Measure regardless of pen Status (only if tpen_soc=1 and tpen_on=1)

Table 185. Touchpannel Control Register Bits

Addr:114		Touchpad – control 3			
		This register controls the different modes of the Touchpad			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
0:1	tpen_sample	00	R/W	Sample Time of ADC	
				0	3µs
				1	10µs
				2	50µs
				3	200µs
2	tpen_debounce	0	R/W	0	Pen-down Debounce Time 100µs
				1	Pen-down Debounce Time = 3ms
3	tpen_timeout _en	0	R/W	Enables Timeout Signal (ADC conversion is stopped during tiemeout = 1)	
				0	off
				1	GPIO3_CURR3 can be configured as input for the timeout signal – see block diagram

11 Register map

Table 186. Register Map

Register Definition	Addr	hex	Default	Content							
Name				b7	b6	b5	b4	b3	b2	b1	b0
Step Down Voltage1	0	0h	ROM	sd1_clkinv	sd1_frequ	step_down1_v					
Step Down Voltage2	1	1h	ROM	sd2_clkinv	sd2_frequ	step_down2_v					
Step Down Voltage3	2	2h	ROM	sd3_clkinv	sd3_frequ	step_down3_v					
LDO_RF1 Voltage	3	3h	ROM		rf1_swprot_en	rf1_lcurr_en	ldo_rf1_v				
LDO_RF2 Voltage	4	4h	ROM	double_reset	slow_startup	rf2_lcurr_en	ldo_rf2_v				
LDO_RF3 Voltage	5	5h	ROM		rf3_hotplug_en	rf3_lcurr_en	ldo_rf3_v				
LDO_DIG1 Voltage	6	6h	ROM	ldo_dig1_v							
LDO_DIG2 Voltage	7	7h	ROM	ldo_dig2_v							
LDO_DIG3 Voltage	8	8h	ROM	ldo_dig3_v							
LDO_DIG4 Voltage	9	9h	ROM	ldo_dig4_v							
USB Charger Control	10	Ah	ROM	ext_batsw_en	No_charging	dis_batsw_temp_prot	usb_chgEn	usb_Current			
Charger Control1	11	Bh	ROM	Isolate_bat	ch_det_500ms	charging_tmax	usb_hold_chdet	Auto Resume	CHOVDetEn	Ch_pwroff_en	ChEn
Battery voltage monitor	12	Ch	ROM	FastResEn	SupResEn	ResVoltFall			ResVoltRise		
Charger Config	13	Dh	ROM	ChVoltResume			Vsupply_min		ChVoltEOC		
Charger supervision	14	Eh	ROM	ntc_type	ntc_hyst	ntc_high_temp	auto_shutdown	ch_timeout			
FuelGauge	15	Fh	ROM	ntc_on		power_off_at_vsuplow	CalMod		CalReq	UpdReq	FGEn
Charger Current	16	10h	ROM	ch_voltage			ConstantCurrent			TrickleCurrent	
Charge Pump Control	17	11h	ROM	sdx_1A_mode				sd1_dvm_time		cp_freq	cp_pulseskip
GPIO 1	18	12h	ROM	gpio1_pulls		gpio1_invert	gpio1_iosf		gpio1_mode		
GPIO 2	19	13h	ROM	gpio2_pulls		gpio2_invert	gpio2_iosf		gpio2_mode		
GPIO 3	20	14h	ROM	gpio3_pulls		gpio3_invert	gpio3_iosf		gpio3_mode		
GPIO 4	21	15h	ROM	gpio4_pulls		gpio4_invert	gpio4_iosf		gpio4_mode		

Table 186. Register Map

Register Definition	Addr	hex	Default	Content							
Name				b7	b6	b5	b4	b3	b2	b1	b0
Reset Timer	22	16h	ROM	rtc_mode		rtc_rep_wakeup_en	rtc_alarm_wakeup_en	xon_enable	res_timer		
Reg Power1 Ctrl @ 6 msec	23	17h	ROM	cp_on	sd3_on	sd2_on	sd1_on	ldo_dig2_on	ldo_dig1_on	ldo_rf2_on	ldo_rf1_on
Reg Power1 Ctrl @ 7 msec	24	18h	ROM	cp_on @ 7 msec	sd3_on @ 7 msec	sd2_on @ 7 msec	sd1_on @ 7 msec	ldo_dig2_on @ 7 msec	ldo_dig1_on @ 7 msec	ldo_rf2_on @ 7 msec	ldo_rf1_on @ 7 msec
Reg Power1 Ctrl @ 8 msec	25	19h	ROM	cp_on @ 8 msec	sd3_on @ 8 msec	sd2_on @ 8 msec	sd1_on @ 8 msec	ldo_dig2_on @ 8 msec	ldo_dig1_on @ 8 msec	ldo_rf2_on @ 8 msec	ldo_rf1_on @ 8 msec
Reg Power1 Ctrl @ 9 msec	26	1Ah	ROM	cp_on @ 9 msec	sd3_on @ 9 msec	sd2_on @ 9 msec	sd1_on @ 9 msec	ldo_dig2_on @ 9 msec	ldo_dig1_on @ 9 msec	ldo_rf2_on @ 9 msec	ldo_rf1_on @ 9 msec
Reg Power1 Ctrl @ 10 msec	27	1Bh	ROM	cp_on @10 msec	sd3_on @ 10 msec	sd2_on @ 10 msec	sd1_on @ 10 msec	ldo_dig2_on @ 10 msec	ldo_dig1_on @10 msec	ldo_rf2_on @10 msec	ldo_rf1_on @ 10 msec
Reg Power1 Ctrl @ 11 msec	28	1Ch	ROM	cp_on @ 11 msec	sd3_on @11 msec	sd2_on @ 11 msec	sd1_on @ 11 msec	ldo_dig2_on @ 11 msec	ldo_dig1_on @ 11 msec	ldo_rf2_on @ 11 msec	ldo_rf1_on @ 11 msec
Reg Power1 Ctrl @ 12 msec	29	1Dh	ROM	cp_on @ 12 msec	sd3_on @ 12 msec	sd2_on @ 12 msec	sd1_on @ 12 msec	ldo_dig2_on @ 12 msec	ldo_dig1_on @ 12 msec	ldo_rf2_on @ 12 msec	ldo_rf1_on @ 12 msec
Reg Power2 Ctrl	30	1Eh	ROM	rf3_sw	stpup2_on	stpup1_on	rf2_sw	rf1_sw	ldo_dig4_on	ldo_dig3_on	ldo_rf3
Reg GPIO Ctrl	31	1Fh	ROM	ldo_dig3_gpio	sd3_gpio	sd2_gpio	sd1_gpio	ldo_dig2_gpio	ldo_dig1_gpio	ldo_rf2_gpio	ldo_rf1_gpio
Step Up DC/DC Control	32	20h	00h	stpup2_res		stpup2_freq	stpup2_fb_auto	stpup1_res		stpup1_freq	stpup2_clkinv
Step Up1 DC/DC Control	33	21h	00h	stpup1_oc_timeout	stpup1_shortprot	stpup1_clkinv	stpup1_v				
Step Up2 DC/DC Control	34	22h	00h	stpup2_prot	stpup2_fb		stpup2_v				
Step Down Control1	35	23h	00h	sd2_nsw_on			sd2_psw_on	sd1_nsw_on			sd1_psw_on
Step Down Control2	36	24h	00h	sd3_dis_pon	sd2_dis_pon	sd1_dis_pon	sdX_lpo	sd3_nsw_on			sd3_psw_on
Step down charger control	37	25h	02h		sd3_dis_curmin	sd2_dis_curmin	sd1_dis_curmin		sdc_pass_mode	sdc_pon	sdc_frequ
Backup Battery charger	38	26h	40h		BBCPwrSave	BBCVolt	BBCCur		BBCResOff	BBCMode	
DCDC_CURR1 value	39	27h	00h	dcdc_curr1_current							

Table 186. Register Map

Register Definition	Addr	hex	Default	Content							
Name				b7	b6	b5	b4	b3	b2	b1	b0
DCDC_CURR2 value	40	28h	00h	dcdc_curr2_current							
CURR1 value	41	29h	00h	curr1_current							
CURR2 value	42	2Ah	00h	curr2_current							
CURR3 value	43	2Bh	00h	curr3_current							
CURR4 value	44	2Ch	00h	curr4_current							
DCDC_CURR3 value	45	2Dh	00h	dcdc_curr3_current							
ADC idac	46	2Eh	00h					adc_idac			
Interrupt Mask1	47	2Fh	FFh	LowBat_int_m	ovtmp_int_m	onkey_int_m	chdet_int_m	usb_chdet_int_m	charging_tmax_int_m	cheoc_int_m	chstate_int_m
Interrupt Mask2	48	30h	FFh	stpup1_int_m	bat_temp_m	hphcurr_int_m	dig2_lv_int_m	dig1_lv_int_m	sd3_lv_int_m	sd2_lv_int_m	sd1_lv_int_m
Interrupt Mask3	49	31h	FFh	-	voxm_int_m	mic_rem_int_m	mic_con_int_m	rtc_rep_int_m	rtc_alarm_int_m	dig4_lv_int_m	dig3_lv_int_m
Interrupt Status1	50	32h	NA	LowBat_i	ovtmp_i	onkey_i	chdet_i	usb_chdet_i	charging_tmax_i	cheoc_i	chstate_i
Interrupt Status2	51	33h	NA	stpup1_i	bat_temp_i	hphcurr_i	dig2_lv_i	dig1_lv_i	sd3_lv_i	sd2_lv_i	sd1_lv_i
Interrupt Status3	52	34h	NA	-	voxm_i	mic_rem_i	mic_con_i	rtc_rep_i	rtc_alarm_i	dig4_lv_i	dig3_lv_i
Low voltage Status1	53	35h	NA	stpup1_det	stpup1_oc		dig2_lv	dig1_lv	sd3_lv	sd2_lv	sd1_lv
Low voltage Status2	54	36h	NA		bat_high temp	bat_lowtemp	dcdc_curr3_lv	dcdc_curr2_lv	dcdc_curr1_lv	dig4_lv	dig3_lv
GPIO Signal	55	37h	NA	gpio4_in	gpio3_in	gpio2_in	gpio1_in	gpio4	gpio3	gpio2	gpio1
PWM Frequency Control High Time	56	38h	00h	pwm_h_time							
PWM Frequency Control Low Time	57	39h	00h	pwm_l_time							
CURR control	58	3Ah	00h	pwm_div		dcdc_curr3_ctrl		dcdc_curr2_ctrl		dcdc_curr1_ctrl	
References Control	59	3Bh	0ch		Reg_low_bias_mode	clk_div2	standby_mode_on	clk_int			low_power_on
Watchdog Control	60	3Ch	02h						wtdg_trigger	wtdg_res_on	wtdg_on
Watchdog_min Timer	61	3Dh	00h	wtdg_min_timer							
Watchdog_max Timer	62	3Eh	FFh	wtdg_max_timer							
Watchdog Software Signal	63	3Fh	00h								wtdg_sw_sig

Table 186. Register Map

Register Definition	Addr	hex	Default	Content							
Name				b7	b6	b5	b4	b3	b2	b1	b0
RTCSecond	64	40h	00h	second<7:0>							
RTCMinute1	65	41h	00h	minute<7:0>							
RTCMinute2	66	42h	00h	minute<15:8>							
RTCMinute3	67	43h	00h	minute<23:16>							
RTCAlarmSecond	68	44h	3Fh	alarmsecond<7:0>							
RTCAlarmMinute1	69	45h	FFh	alarmminute<7:0>							
RTCAlarmMinute2	70	46h	FFh	alarmminute<15:8>							
RTCAlarmMinute3	71	47h	FFh	alarmminute<23:16>							
RTCT	72	48h	00h	rtc_irq_mode	rtc_tbc<6:0>						
SRAM	73	49h	00h	sram<7:0>							
Audio Set1	74	4Ah	00h	equ_on	mclk256	mclk_invert	aud_ldo_on	gnd_sw_on	mix_on	dac_on	lin_on
Audio Set2	75	4Bh	00h	I2S_mclk_en	I2S_select	ibr_hph		I2S_3_on	dith_on	ibr_dac	
Audio Set3	76	4Ch	00h	linmix_off	micmix_off	dacmix_off	agc_off	mic_on	voxm_on	hp_pulld_en	pll_mode
DAC_L	77	4Dh	00h		dac_mute_off	dal_vol					
DAC_R	78	4Eh	00h	dar_vol							
ADC_L	79	4Fh	00h	ad_fs2	adc_mut_off	adc_on	adl_vol				
ADC_R	80	50h	00h	adcmux		adc2dac	adr_vol				
HPH out R	81	51h	00h	hp_ovc_to		hpcm_off	hpr_vol				
HPH out L	82	52h	00h	hp_mute	hp_on	hp_mux	hpl_vol				
Line out R	83	53h	00h	ibr_line			liner_vol				
Line out L	84	54h	00h	line_mute	line_on	dac2line_on	linel_vol				
LINE_IN_R	85	55h	00h	mute_mic_sf		mute_off_inr	lir_vol				
LINE_IN_L	86	56h	00h			mute_off_inl	lil_vol				
MIC_R	87	57h	00h	mic_agc_off	pre_gain		mr_vol				
MIC_L	88	58h	00h	msup_off	mute_off_d	rdet_off	ml_vol				
SPDIF	89	59h	00h	audio_off	sclk_invert	sdo3_select	spdif_copy_ok	spdif_mclk_inv	spdif_invalid	spdif_cntr	
EQ_LP	90	5Ah	00h					eq_lp_gain			

Table 186. Register Map

Register Definition	Addr	hex	Default	Content							
Name				b7	b6	b5	b4	b3	b2	b1	b0
EQ_Band1	91	5Bh	00h					eq_band1_gain			
EQ_Band2	92	5Ch	00h					eq_band2_gain			
EQ_Band3	93	5Dh	00h					eq_band3_gain			
EQ_HP	94	5Eh	00h					eq_hp_gain			
EQ_preamp	95	5Fh	00h				eq_ pre_gain				
ADC_control	96	60h	00h	start_conversion	adc_on		adc_slow	adc_select			
ADC_MSB result	97	61h	NA	result_not_ready	D9	D8	D7	D6	D5	D4	D3
ADC_LSB result	98	62h	NA						D2	D1	D0
ChargerStatus	99	63h	NA	ChLinear	NoBat	EOC	CVM	Trickle	Resume	ChAct	ChDet
ChargerStatus_usb	100	64h	NA				ch_overvoltage	batsw_on	batsw_mode	USB_ChAct	USB_ChDet
DeltaCharge$_{MSB}$	101	65h	NA	sign	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}
DeltaCharge$_{LSB}$	102	66h	NA	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
ElapsedTime$_{MSB}$	103	67h	NA	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}
ElapsedTime$_{LSB}$	104	68h	NA	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
Reset Control	105	69h	NA	Onkey_reset_5s	reset_reason				xon_input	power_off	force_reset
Overtemperature Control	106	6Ah	NA					rst_ov_temp_140	ov_temp_140	ov_temp_110	temp_pmc_on
Boot_status	107	6Bh	NA					rom_valid	rom_adr		
tpen_xmsb	108	6Ch	NA	XD9	XD8	XD7	XD6	XD5	XD4	XD3	XD2
tpen_ymsb	109	6Dh	NA	YD9	YD8	YD7	YD6	YD5	YD4	YD3	YD2
tpen_pressmsb	110	6Eh	NA	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2
tpen_xypresslsb	111	6Fh	NA	PD1	PD0	0	YD1	YD0	0	XD1	XD0
tpen – control 1	112	70h	00h	tpen_st_pen	tpen_eoc	tpen_avg		tpen_soc	tpen_convint		tpen_on
tpen – control 2	113	71h	00h	tpen_socpd	tpen_wait	tpen_currpress	tpen_pu				
tpen – control 3	114	72h	00h					tpen_timeout_en	tpen_debounce	tpen_sample	
ASIC ID 1	127	7Fh	NA	1	1	0	0	1	1	0	1
ASIC ID 2	128	80h	NA	0	1	0	1	rev			
Reg_ standby mod	129	81h	00h	cp_stby_on	sd3_stby_on	sd2_stby_on	sd1_stby_on	ldo_dig2_stby_on	ldo_dig1_stby_on	ldo_rf2_stby_on	ldo_rf1_stby_on

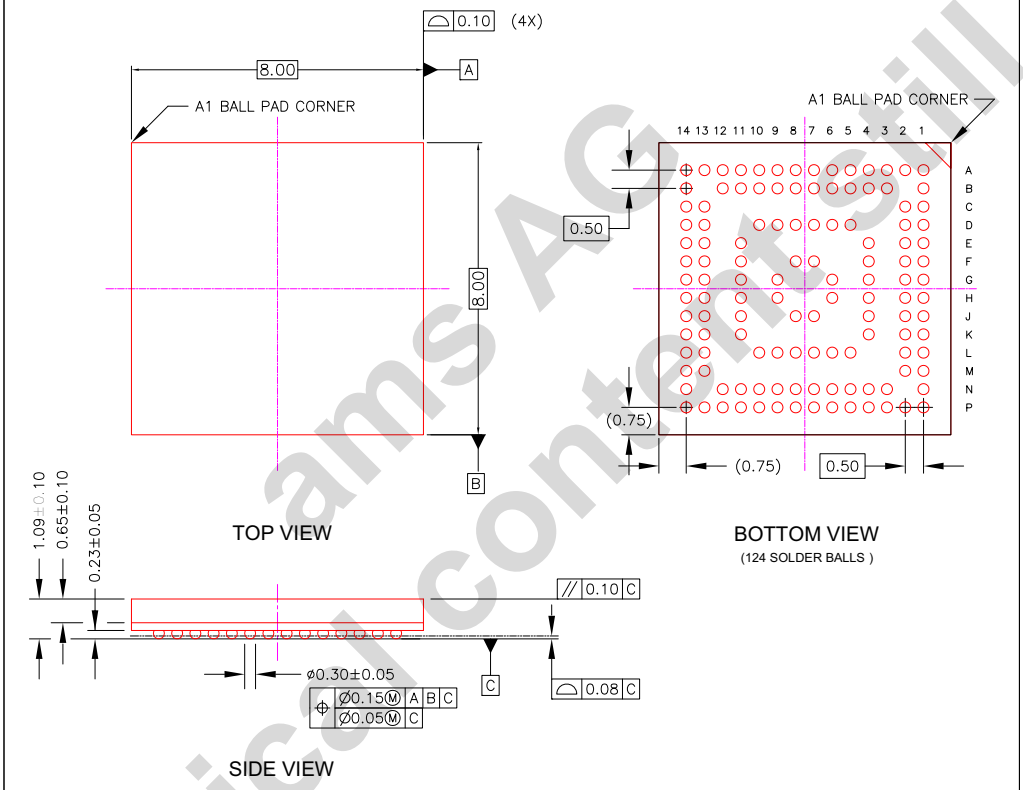
Table 186. Register Map

Register Definition	Addr	hex	Default	Content							
Name				b7	b6	b5	b4	b3	b2	b1	b0
Usb_current_trim	130	82h	00						usb_add_trim_current<2:0>		
i2s master control1	131	83h	00	i2s_clk_divider<7:0>							
i2s master control2	132	84h	00	pcm_mode	sdo_on_mclk1_en	i2s_mclk_out_en	i2s_lrclk_sclk_out_en	i2s_master_on	i2s_clk_divider<10:8>		
step Down Control3	133	85h	00						sd3_uvlimit	sd2_uvlimit	sd1_uvlimit
UniqueID0, addrf0	197	C5h	NA	ID<7:0>, addrf<7:0>							
UniqueID1, addrf1	198	C6h	NA	ID<15:8>, addrf<15:8>							
UniqueID2, addrf2	199	C7h	NA	ID<23:16>, addrf<23:16>							
UniqueID3, addrf3	200	C8h	NA	ID<31:24>, addrf<31:24>							
UniqueID4, romf0	201	C9h	NA	ID<39:32>, romf0							
UniqueID5, romf1	202	CAh	NA	ID<47:40>, romf1							
UniqueID6, romf2	203	CBh	NA	ID<55:48>, romf2							
UniqueID7, romf3	204	CCh	NA	ID<63:56>, romf3							
UniqueID8, romf4	205	CDh	NA	ID<71:64>, romf4							
UniqueID9, romf5	206	CEh	NA	ID<79:72>, romf5							
UniqueID10, romf6	207	CFh	NA	ID<87:80>, romf6							
	Entries marked are read only										
	Entries are not reset in power off mode										

12 Package Drawings and Marking

Figure 61. CTBGA124 8x8 0.5mm pitch

ASE Advanced Semiconductor Engineering Korea, Inc.	PACKAGE OUTLINE	DWG NO.	97SPP01046A
		ISSUE	O
		DATE	OCT.010, 2007



NOTE
1. GENERAL TOLERANCE : ± 0.10

	Dimension & Tolerance ASME Y14.5M	Unit : mm
		Customer : AMS
TITLE : POD for FBGA 8mm X 8mm X 1.09mm, 2L, 0.65CAP, 124BGA, 0.50PITCH, 0.30BALL	COMPANY	***ASE KOREA***
	SHEET	1 OF 2

Figure 62. CTBGA124 Marking

Table 187. Package Code AYWWZZZ

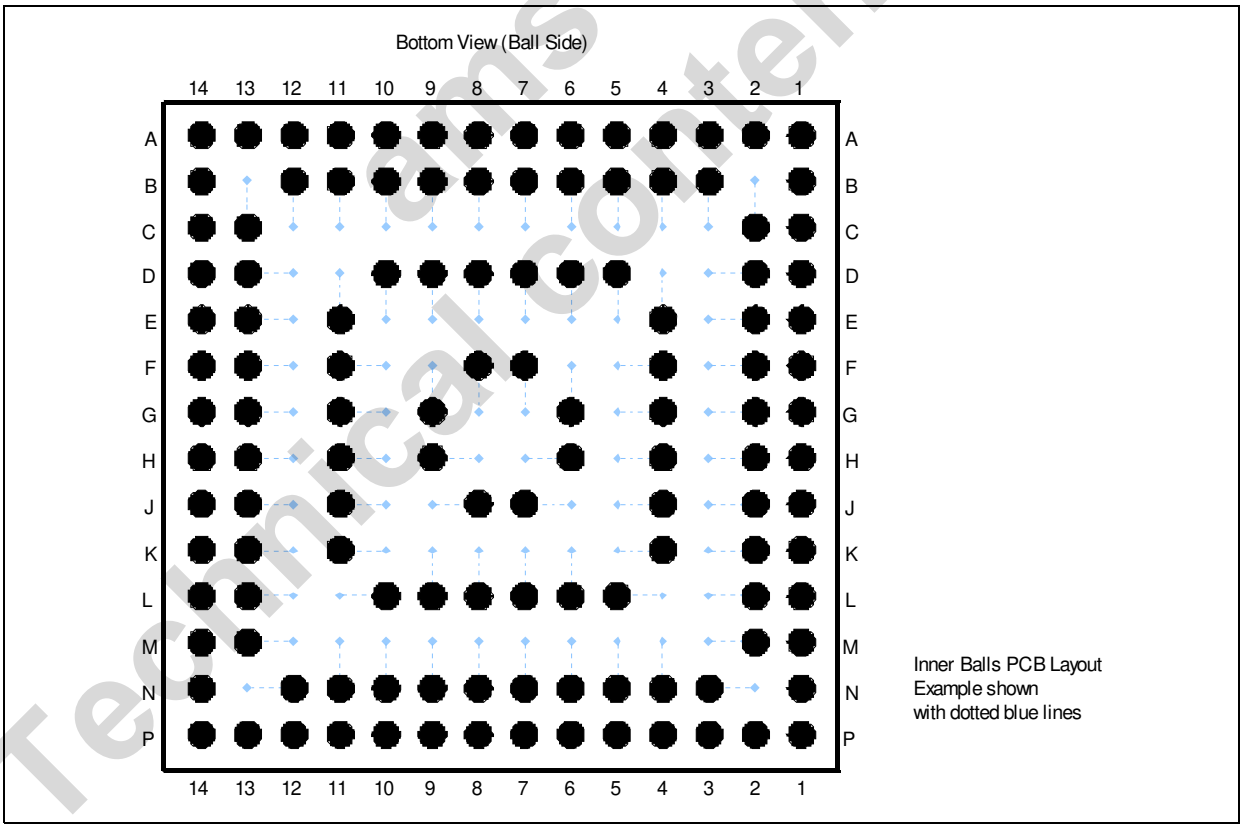
A	Y	WW	ZZZ
B ... for Green	year	working week assembly / packaging	free choice

Table 188. Boot ROM revison

x
B, C, D, E, E1 or F

12.1 Pinout Drawing (Top view) CTBGA 8x8mm

Figure 63. Pinout drawing



13 Ordering Information

The device is available as the standard products listed in Table 189.

Table 189. Ordering Information

Model	Marking	Description	Delivery Form	Package
AS3658B-BCTP	AS3658B	Power and Audio Management Unit for Portable Devices, Boot-ROM Version B	Tape and Reel in Dry Pack	BGA124 8x8mm, 0.5mm pitch
AS3658C-BCTP	AS3658C	Power and Audio Management Unit for Portable Devices, Boot-ROM Version C	Tape and Reel in Dry Pack	BGA124 8x8mm, 0.5mm pitch
AS3658D-BCTP	AS3658D	Power and Audio Management Unit for Portable Devices, Boot-ROM Version D	Tape and Reel in Dry Pack	BGA124 8x8mm, 0.5mm pitch
AS3658E-BCTP	AS3658E	Power and Audio Management Unit for Portable Devices, Boot-ROM Version E	Tape and Reel in Dry Pack	BGA124 8x8mm, 0.5mm pitch
AS3658E1-BCTP	AS3658E1	Power and Audio Management Unit for Portable Devices, Boot-ROM Version E1	Tape and Reel in Dry Pack	BGA124 8x8mm, 0.5mm pitch
AS3658F-BCTP	AS3658F	Power and Audio Management Unit for Portable Devices, Boot-ROM Version F	Tape and Reel in Dry Pack	BGA124 8x8mm, 0.5mm pitch

Description: AS3658x-BCTP

x: Boot-ROM version

B: Teperature Range: Z = -40ºC to 85ºC

CT: Pacakage: CTBGA

P:Delivery Form: Tape and Reel in Dry Pack

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