19-2751; Rev 0; 1/03

MAXIM

+3.3V/+5V, 8-Channel, Cascadable Relay Drivers with Serial/Parallel Interface

General Description

The MAX4820/MAX4821 8-channel relay drivers offer built-in kickback protection and drive +3.3V/+5V non-latching or dual-coil-latching relays. These devices are especially useful when driving +3V relays. Each independent open-drain output features a 2Ω on-resistance and is guaranteed to sink 70mA (min) of load current. Both devices consume less than 50µA (max) quiescent current and have 1µA output off-leakage current.

The MAX4820 features an SPI™-/QSPI™-/MICROWIRE™-compatible serial interface. Input data is shifted into an 8-bit shift register and latched to the outputs when $\overline{CS}$ transitions from low to high. Each data bit in the shift register corresponds to a specific output, allowing independent control of all outputs.

The MAX4821 features a 4-bit (A0, A1, A2, LVL) parallel-input interface. The first three bits (A0, A1, A2) determine the output address, and the fourth bit (LVL) determines whether the selected output is switched on or off. Data is latched to the outputs when $\overline{CS}$ transitions from low to high.

Both devices feature separate set and reset functions that allow the user to turn on or turn off all outputs simultaneously with a single control line. Built-in hysteresis (Schmidt trigger) on all digital inputs allows this device to be used with slow rising and falling signals, such as those from optocouplers or RC power-up initialization circuits. The MAX4820/MAX4821 are available in 20-pin TSSOP and space-saving 20-pin thin QFN packages.

Applications

Central Office

ATE

DSL, ADSL Line Cards

Industrial Equipment

E1/T1 Redundancy

Pin Configurations continued at end of data sheet.

Typical Application Circuits and Functional Diagrams appear at end of data sheet.

SPI and QSPI are trademarks of Motorola, Inc.

MICROWIRE is a trademark of National Semiconductor Corp.

Features

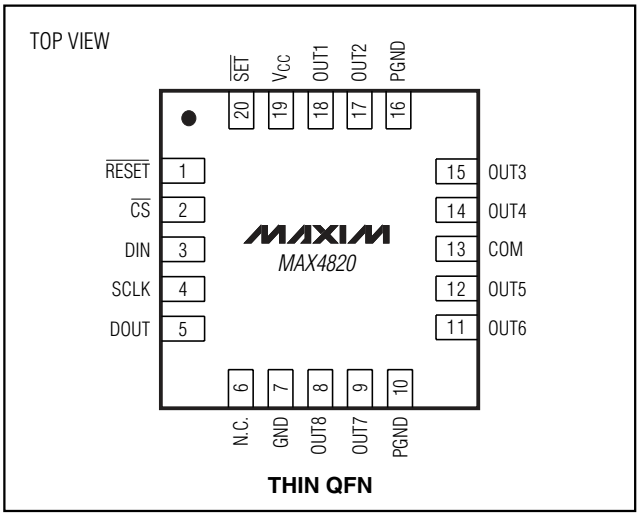
- **8 Independent Output Channels**
- **Built-In Inductive Kickback Protection**
- **Drive +3V and +5V Relays**
- **Guaranteed 70mA (min) Coil Drive Current**
- **$\overline{SET}$ Function to Turn On All Outputs Simultaneously**
- **$\overline{RESET}$ Function to Turn Off All Outputs Simultaneously**
- **SPI-/QSPI-/MICROWIRE-Compatible Serial Interface (MAX4820)**
- **Serial Digital Output for Daisy Chaining (MAX4820)**
- **Parallel Interface (MAX4821)**
- **Low 50µA (max) Quiescent Supply Current**
- **Space-Saving 20-Pin Thin QFN Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX4820ETP*	-40°C to +85°C	20 Thin QFN-EP
MAX4820EUP*	-40°C to +85°C	20 TSSOP
MAX4821ETP*	-40°C to +85°C	20 Thin QFN-EP
MAX4821EUP*	-40°C to +85°C	20 TSSOP

**For maximum heat dissipation, packages have an exposed pad (EP) on the bottom. Solder exposed pad to GND.*

Pin Configurations



+3.3V/+5V, 8-Channel, Cascadable Relay Drivers with Serial/Parallel Interface

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)
V_{CC}, COM.....-0.3V to +6.0V
OUT_.....-0.3V to (V_{COM} + 0.3V)
$\overline{CS}$, SCLK, DIN, $\overline{SET}$, $\overline{RESET}$, A0, A1, A2, LVL.....-0.3V to +6.0V
DOUT.....-0.3V to (V_{CC} + 0.3V)
Continuous OUT_ Current (all outputs turned on).....150mA
Continuous OUT_ Current (single output turned on).....300mA

Continuous Power Dissipation (T_A = +70°C)
20-Lead Thin QFN
(derate 16.9mW/°C above +70°C).....1350mW
θ_{JA}.....59.3°C/W
20-Pin TSSOP
(derate 21.7mW/°C above +70°C).....1739mW
θ_{JA}.....46°C/W
Operating Temperature Range.....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range.....-65°C to +150°C
Soldering Temperature (10s).....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +3V to +5.5V, V_{COM} = V_{CC}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage	V_{CC}			2.3		5.5	V
Quiescent Current	I_Q	$I_{OUT\_}$ = 0, logic inputs = 0 or V_{CC}	V_{CC} = 3.6V		15	50	µA
			V_{CC} = 5.5V		20	70	
Thermal Shutdown					160		°C
Power-On Reset				0.8	1.5	2.2	V
Power-On Reset Hysteresis					140		mV
DIGITAL INPUTS (SCLK, DIN, $\overline{CS}$, LVL, A0, A1, A2, $\overline{RESET}$, $\overline{SET}$)							
Input Logic High Voltage	V_{IH}	V_{CC} = 3.3V		2.0			V
		V_{CC} = 5V		2.4			
Input Logic Low Voltage	V_{IL}	V_{CC} = 3.3V				0.6	V
		V_{CC} = 5V				0.8	
Input Logic Hysteresis	V_{HYST}				150		mV
Input Leakage Currents	I_{LEAK}	Input voltages = 0 or 5.5V		-1.0	0.01	+1.0	µA
C_{IN} Input Capacitance	C_{IN}				5		pF
DIGITAL OUTPUT (DOUT)							
DOUT Low Voltage	V_{OL}	I_{SINK} = 6mA				0.4	V
DOUT High Voltage	V_{OH}	I_{SOURCE} = 0.5mA		V_{CC} - 0.5			V
RELAY OUTPUT DRIVERS (OUT1–OUT8)							
OUT_ Drive Current		V_{CC} = 2.7V		70			mA
		V_{CC} = 4.5V		70			
OUT_ On-Resistance	R_{ON}	V_{CC} = 2.7V			2	6	Ω
OUT_ Voltage	$V_{OUT\_}$	V_{CC} = 3.0V, $I_{OUT\_}$ = 70mA				0.4	V
I_{OUT} Off-Leakage Current	I_{LEAK}	$V_{OUT\_}$ = V_{CC}, all outputs off		-1		+1	µA
Kickback Diode Forward Voltage	V_{FORW}	$I_{OUT\_}$ = 150mA (Note 2)				1.5	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3V to +5.5V, V_{COM} = V_{CC}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SPI TIMING (MAX4821)						
Turn-On Time (OUT_)	t_{ON}	From rising edge of $\overline{CS}$, R_L = 50Ω, C_L = 50pF			1.0	µs
Turn-Off Time (OUT_)	t_{OFF}	From rising edge of $\overline{CS}$, R_L = 50Ω, C_L = 50pF			1.0	µs
SCLK Frequency	f_{SCLK}		0		2.1	MHz
Cycle Time	t_{CH} + t_{CL}		480			ns
$\overline{CS}$ Fall to SCLK Rise Setup	t_{CSS}		240			ns
$\overline{CS}$ Rise to SCLK Hold	t_{CSH}		240			ns
SCLK High Time	t_{CH}		190			ns
SCLK Low Time	t_{CL}		190			ns
Data Setup Time	t_{DS}		100			ns
Data Hold Time	t_{DH}		0			ns
SCLK Fall to DOUT Valid	t_{DO}	50% of SCLK to 10% of DOUT, C_L = 50pF		85	120	ns
Rise Time (DIN, SCLK, $\overline{CS}$, $\overline{SET}$, $\overline{RESET}$)	t_{SCR}	20% of V_{CC} to 70% of V_{CC}, C_L = 50pF			2	µs
Fall Time (DIN, SCLK, $\overline{CS}$, $\overline{RESET}$, $\overline{SET}$)	t_{SCF}	20% of V_{CC} to 70% of V_{CC}, C_L = 50pF			2	µs
$\overline{RESET}$ Min Pulse Width	t_{RW}		70			ns
$\overline{SET}$ Min Pulse Width	t_{SW}		70			ns
PARALLEL TIMING (MAX4820)						
Turn-On Time	t_{ON}	From rising edge of $\overline{CS}$, R_L = 50Ω, C_L = 50pF			1	µs
Turn-Off Time	t_{OFF}	From rising edge of $\overline{CS}$, R_L = 50Ω, C_L = 50pF			1	µs
LVL Setup Time	t_{LS}		100			ns
LVL Hold Time	t_{LH}		0			ns
Address to $\overline{CS}$ Setup Time	t_{AH}		100			ns
Address to $\overline{CS}$ Hold Time	t_{AS}		0			ns
Rise Time (A2, A1, A0, LVL)	t_{SCR}	20% of V_{CC} to 70% of V_{CC}, C_L = 50pF			2	µs
Fall Time (A2, A1, A0, LVL)	t_{SCF}	20% of V_{CC} to 70% of V_{CC}, C_L = 50pF			2	µs
$\overline{RESET}$ Pulse Width	t_{RW}		70			ns
$\overline{SET}$ Pulse Width	t_{SW}		70			ns

Note 1: Specifications at -40°C are guaranteed by design and not production tested.

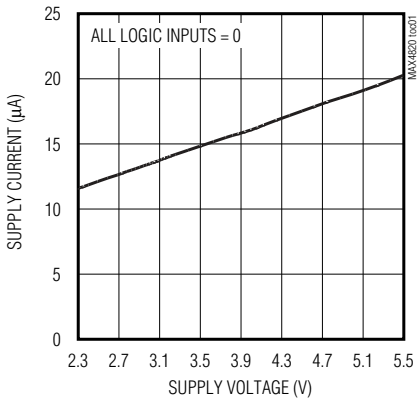
Note 2: After relay turn-off, inductive kickback may momentarily cause the voltage at OUT_ to exceed V_{COM}. This is considered part of normal operation and will not damage the device.

+3.3V/+5V, 8-Channel, Cascadable Relay Drivers with Serial/Parallel Interface

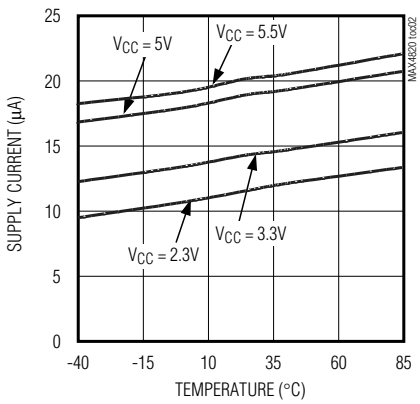
Typical Operating Characteristics

(V_{COM} = V_{CC}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

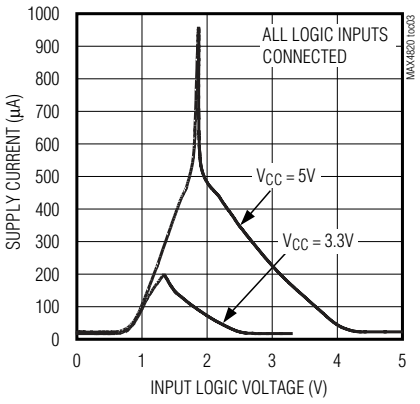
SUPPLY CURRENT vs. SUPPLY VOLTAGE



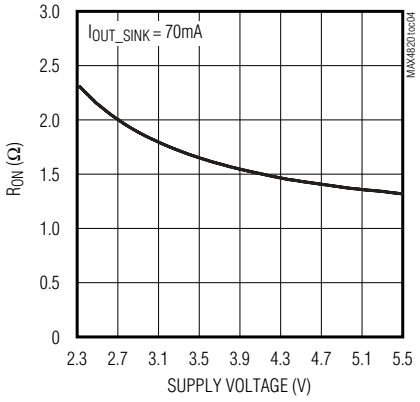
SUPPLY CURRENT vs. TEMPERATURE



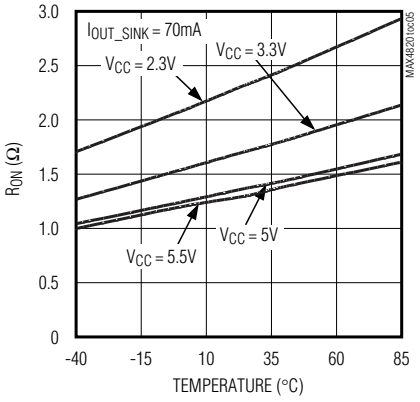
SUPPLY CURRENT vs. INPUT LOGIC VOLTAGE



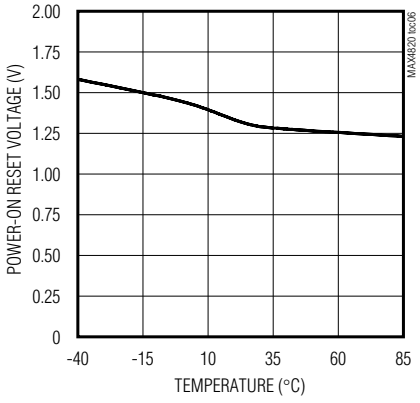
ON-RESISTANCE vs. SUPPLY VOLTAGE



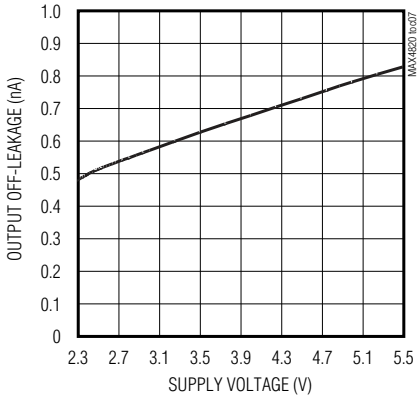
ON-RESISTANCE vs. TEMPERATURE



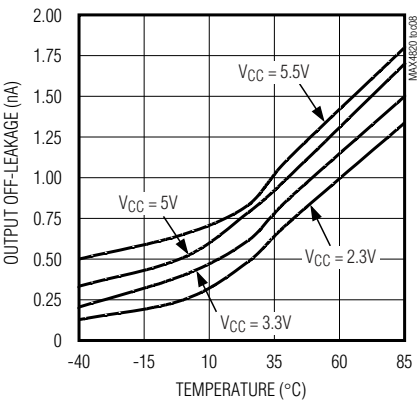
POWER-ON RESET VOLTAGE vs. TEMPERATURE



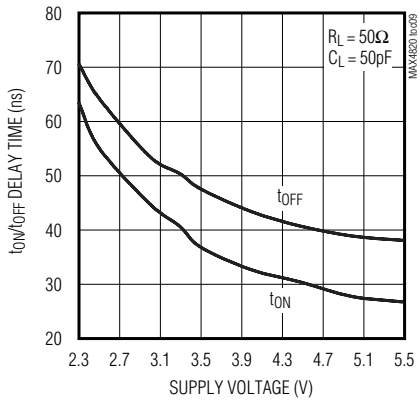
OUTPUT OFF-LEAKAGE CURRENT vs. SUPPLY VOLTAGE



OUTPUT OFF-LEAKAGE CURRENT vs. TEMPERATURE



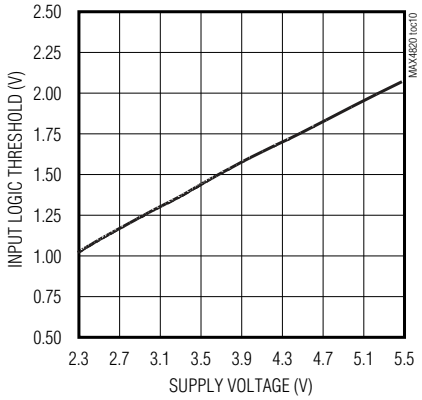
OUT_ TURN-ON/TURN-OFF DELAY TIMES vs. SUPPLY VOLTAGE



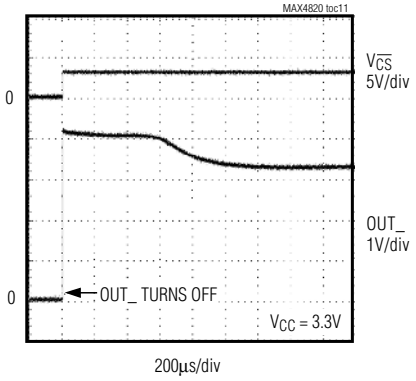
Typical Operating Characteristics (continued)

(V_{COM} = V_{CC}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

INPUT LOGIC THRESHOLD vs. SUPPLY VOLTAGE



BACK EMF CLAMPING WITH STANDARD 3V RELAY



Pin Description

PIN				NAME	FUNCTION
MAX4820		MAX4821			
THIN QFN	TSSOP	THIN QFN	TSSOP		
1	3	1	3	$\overline{RESET}$	Reset Input. Drive $\overline{RESET}$ low to clear all latches and registers (all outputs are turned off). $\overline{RESET}$ overrides all other inputs. If $\overline{RESET}$ and $\overline{SET}$ are pulled low at the same time, then $\overline{RESET}$ takes precedence.
2	4	2	4	$\overline{CS}$	Chip-Select Input. **MAX4820:** Drive $\overline{CS}$ low to select the device. When $\overline{CS}$ is low, data at DIN is clocked into the 8-bit shift register on SCLK's rising edge. Drive $\overline{CS}$ from low to high to latch the data to the registers and activate the appropriate relays. **MAX4821:** Drive $\overline{CS}$ low to select the device and set level on LVL. Drive $\overline{CS}$ from low to high to latch the address and level data to the output.
3	5	—	—	DIN	Serial Data Input
4	6	—	—	SCLK	Serial Clock Input
5	7	—	—	DOUT	Serial Data Output. DOUT is the output of the 8-bit shift register. This output can be used to daisy chain multiple MAX4820s. The data at DOUT appears synchronous to SCLK's falling edge.
6	8	—	—	N.C.	No Connection
7	9	7	9	GND	Ground
8	10	8	10	OUT8	Open-Drain Output 8. Connect OUT8 to the low side of a relay coil. This output is pulled to PGND when activated, but otherwise is high impedance.
9	11	9	11	OUT7	Open-Drain Output 7. Connect OUT7 to the low side of a relay coil. This output is pulled to PGND when activated, but otherwise is high impedance.
10, 16	12, 18	10, 16	12, 18	PGND	Power Ground. PGND is a return for the output sinks. Connect PGND pins together and to GND.
11	13	11	13	OUT6	Open-Drain Output 6. Connect OUT6 to the low side of a relay coil. This output is pulled to PGND when activated, but otherwise is high impedance.

+3.3V/+5V, 8-Channel, Cascadable Relay Drivers with Serial/Parallel Interface

Pin Description (continued)

PIN				NAME	FUNCTION
MAX4820		MAX4821			
THIN QFN	TSSOP	THIN QFN	TSSOP		
12	14	12	14	OUT5	Open-Drain Output 5. Connect OUT5 to the low side of a relay coil. This output is pulled to PGND when activated, but otherwise is high impedance.
13	15	13	15	COM	Common Free-Wheeling Diodes. Connect COM to V_{CC}. COM can also be connected to a separate supply that is higher than V_{CC}. In that case, bypass V_{CC} to GND with a 0.1µF capacitor.
14	16	14	16	OUT4	Open-Drain Output 4. Connect OUT4 to the low side of a relay coil. This output is pulled to PGND when activated, but otherwise is high impedance.
15	17	15	17	OUT3	Open-Drain Output 3. Connect OUT3 to the low side of a relay coil. This output is pulled to PGND when activated, but otherwise is high impedance.
17	19	17	19	OUT2	Open-Drain Output 2. Connect OUT2 to the low side of a relay coil. This output is pulled to PGND when activated, but otherwise is high impedance.
18	20	18	20	OUT1	Open-Drain Output 1. Connect OUT1 to the low side of a relay coil. This output is pulled to PGND when activated, but otherwise is high impedance.
19	1	19	1	V_{CC}	Input Supply Voltage. Bypass V_{CC} to GND with a 0.1µF capacitor.
20	2	20	2	$\overline{SET}$	Set Input. Drive $\overline{SET}$ low to set all latches and registers high (all outputs are turned on). $\overline{SET}$ overrides all parallel and serial control inputs. $\overline{RESET}$ overrides $\overline{SET}$ under all conditions.
—	—	3	5	LVL	Level Input. LVL determines whether the selected address is switched on or off. A logic high on LVL switches on the addressed output. A logic low on LVL switches off the addressed output.
—	—	4	6	A0	Digital Address “0” Input. (See Table 2 for address mapping.)
—	—	5	7	A1	Digital Address “1” Input. (See Table 2 for address mapping.)
—	—	6	8	A2	Digital Address “2” Input. (See Table 2 for address mapping.)
—	—	—	—	EP	Exposed Pad. Solder exposed pad to GND.

Detailed Description

The MAX4820/MAX4821 8-channel relay drivers offer built-in kickback protection and drive +3.3V/+5V non-latching or dual-coil-latching relays. These devices are especially useful when driving +3V relays. Each independent open-drain output features a 2Ω on-resistance and is guaranteed to sink 70mA (min) load current. Both devices consume less than 50µA (max) quiescent current and feature 1µA (min) output off-leakage current.

The MAX4820 features an SPI/QSPI/MICROWIRE-compatible serial interface. Input data is shifted into an 8-bit shift register and latched to the outputs when $\overline{CS}$ transitions from low to high. Each data bit in the shift register corresponds to a specific output, allowing independent control of all outputs.

The MAX4821 features a 4-bit (A0, A1, A2, LVL) parallel input interface. The three bits (A0, A1, A2) determine the output address, and LVL determines whether the selected output is switched on or off. Data is latched to the outputs when $\overline{CS}$ transitions from low to high.

Both devices feature separate set and reset functions that allow the user to turn on or turn off all outputs simultaneously with a single control line. Built-in hysteresis (Schmidt trigger) on all digital inputs allows this device to be used with slow rising and falling signals, such as those from optocouplers or RC power-up initialization circuits. The MAX4820/MAX4821 are available in 20-pin TSSOP and space-saving 20-pin thin QFN packages.

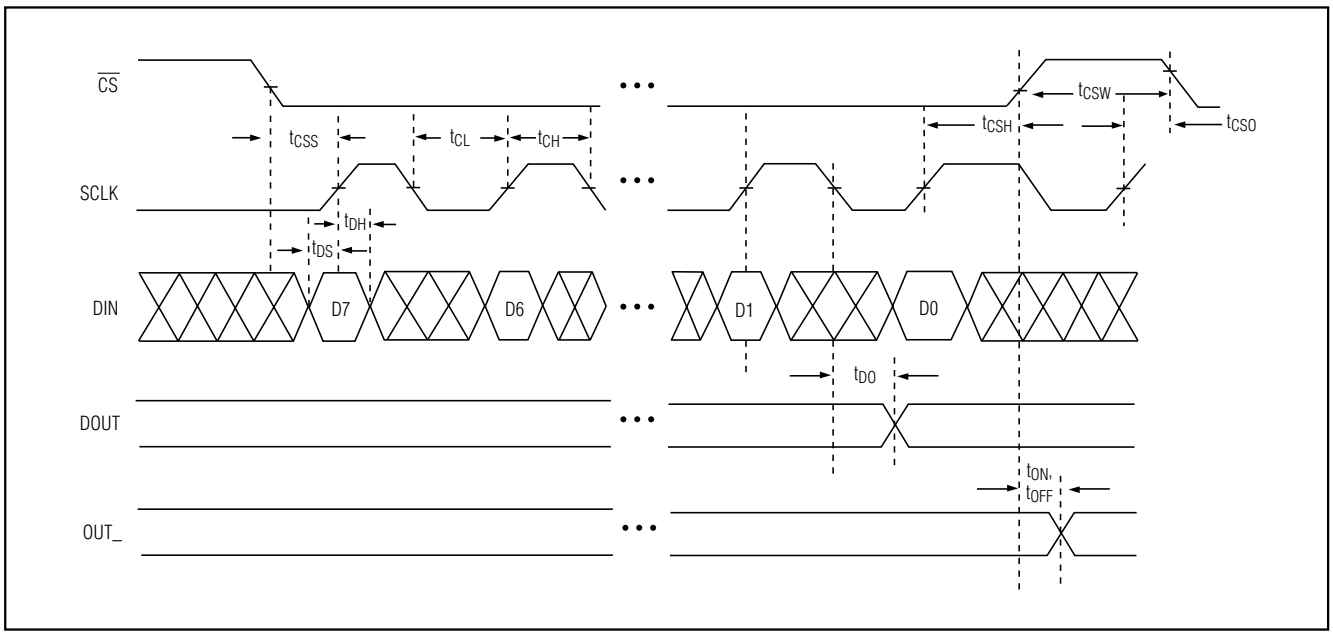


Figure 1. 3-Wire Serial-Interface Timing Diagram (MAX4820 only)

Table 1. Serial Input Address Map (MAX4820 Only)

DIN	D0	D1	D2	D3	D4	D5	D6	D7
OUT_	OUT1	OUT2	OUT3	OUT4	OUT5	OUT6	OUT7	OUT8

Digital Interface

Serial Interface (MAX4820)

The serial interface consists of an 8-bit shift register and parallel latch controlled by SCLK and $\overline{CS}$. The input to the shift register is an 8-bit word. Each data bit controls one of the eight outputs, with the most significant bit (D7) corresponding to OUT8 and the least significant bit (D0) corresponding to OUT1 (see Table 1). When $\overline{CS}$ is low (device is selected), data at DIN is clocked into the shift register synchronously with SCLK's rising edge. Driving $\overline{CS}$ from low to high latches the data in the shift register to the parallel latch.

DOUT is the output of the shift register. Data appears on DOUT synchronously with SCLK's falling edge and is identical to the data at DIN delayed by eight clock cycles. When shifting the input data, D7 is the first bit in and out of the shift register.

While $\overline{CS}$ is low, the switches always remain in their previous state. Drive $\overline{CS}$ high after 8 bits of data have been shifted in to update the output state and inhibit further data from entering the shift register. When $\overline{CS}$ is high, transitions at DIN and SCLK have no effect on the output, and the first input bit (D7) is present at DOUT.

If the number of data bits entered while $\overline{CS}$ is low is greater or less than 8, the shift register contains only the last 8 data bits, regardless of when they were entered.

The 3-wire serial interface is compatible with SPI, QSPI, and MICROWIRE standards. The latch that drives the analog switch is updated on the rising edge of $\overline{CS}$, regardless of SCLK's state.

Parallel Interface (MAX4821)

The parallel interface consists of three address bits (A0, A1, A2) and one level selector bit (LVL). The address bits determine which output is updated, and the level bit determines whether the addressed output is switched on (LVL = high) or off (LVL = low). When $\overline{CS}$ is high, the address and level bits have no effect on the state of the outputs. Driving $\overline{CS}$ from low to high latches the address and level data to the parallel register and updates the state of the outputs. Address data entered after $\overline{CS}$ is pulled low is not reflected in the state of the outputs following the next low-to-high transition on $\overline{CS}$ (Figure 2).

+3.3V/+5V, 8-Channel, Cascadable Relay Drivers with Serial/Parallel Interface

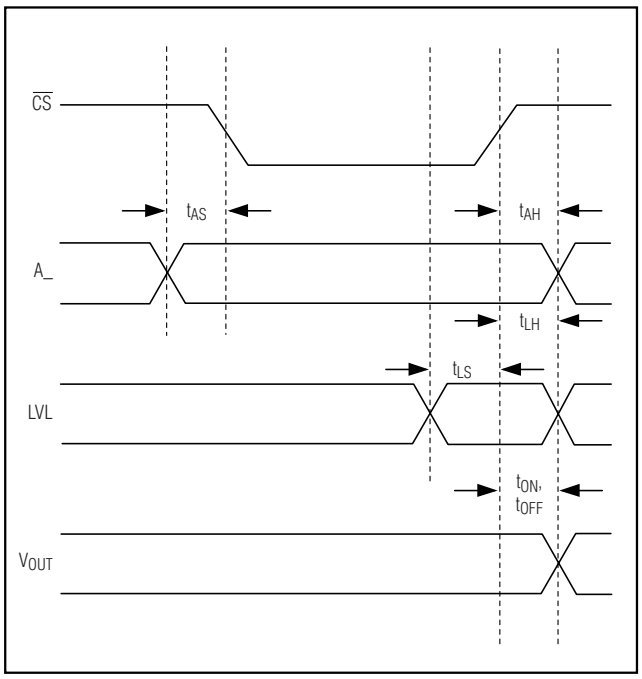


Figure 2. Parallel Interface Timing Diagram (MAX4821 only)

SET/RESET Functions

The MAX4820/MAX4821 feature set and reset inputs that allow the user to simultaneously turn all outputs on or off using a single control line. Drive SET low to set all latches and registers to 1 and turn all outputs on. SET overrides all serial/parallel control inputs. Drive RESET low to clear all latches and registers and turn all outputs off. RESET overrides all other inputs, including SET.

Table 2. Parallel Interface Address Map (MAX4821 Only)

A2	A1	A0	OUTPUT
Low	Low	Low	OUT1
Low	Low	High	OUT2
Low	High	Low	OUT3
Low	High	High	OUT4
High	Low	Low	OUT5
High	Low	High	OUT6
High	High	Low	OUT7
High	High	High	OUT8

Applications Information

Daisy Chaining

The MAX4820 features a digital output, DOUT, that provides a simple way to daisy chain multiple devices. This feature allows the user to drive large banks of relays using only a single serial interface. To daisy chain multiple devices, connect all CS pins together, and connect the DOUT of one device to the DIN of another device (see Figure 3). During operation, a stream of serial data is shifted through all the MAX4820s in series. When CS goes high, all outputs update simultaneously.

The MAX4820 can also be used in a slave configuration that allows the user to address individual devices. Connect all the DIN pins together, and use the CS input to address one device at a time. Drive CS low to select a slave and input the data into the shift register. Drive CS high to latch the data and turn on the appropriate outputs. Typically, in this configuration only one slave is addressed at a time.

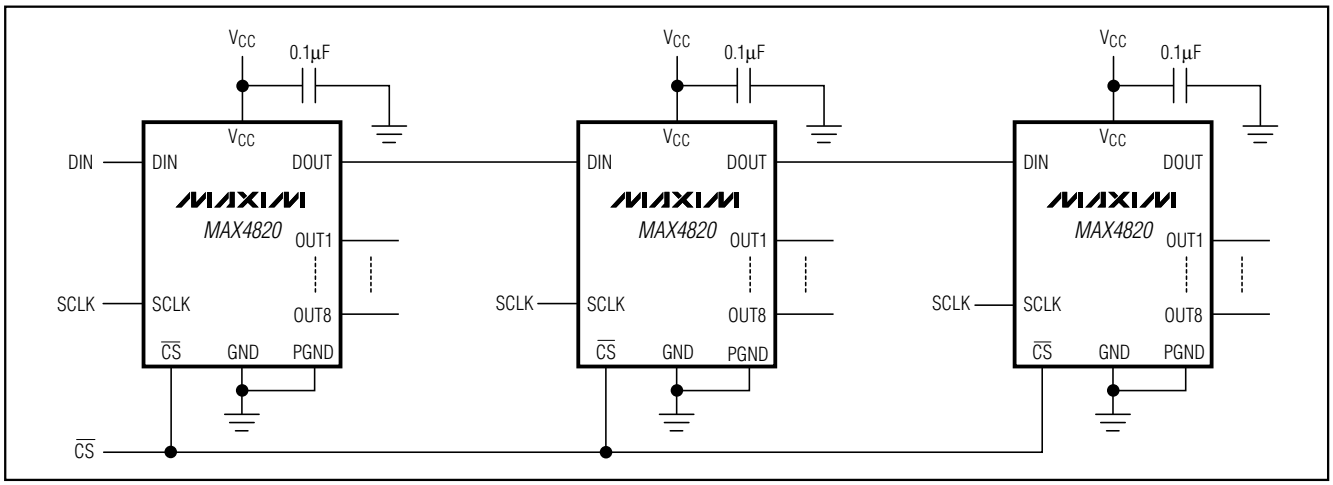


Figure 3. Daisy-Chain Configuration

Inductive Kickback Protection

The MAX4820/MAX4821 feature built-in inductive kickback protection to reduce the voltage spike on OUT_ generated by a relay's coil inductance when the output is suddenly switched off. Internal diodes connected from each output to COM allow the inductor current to flow back to the supply. Connect the common cathode (COM) of the internal protection diodes to V_{CC}.

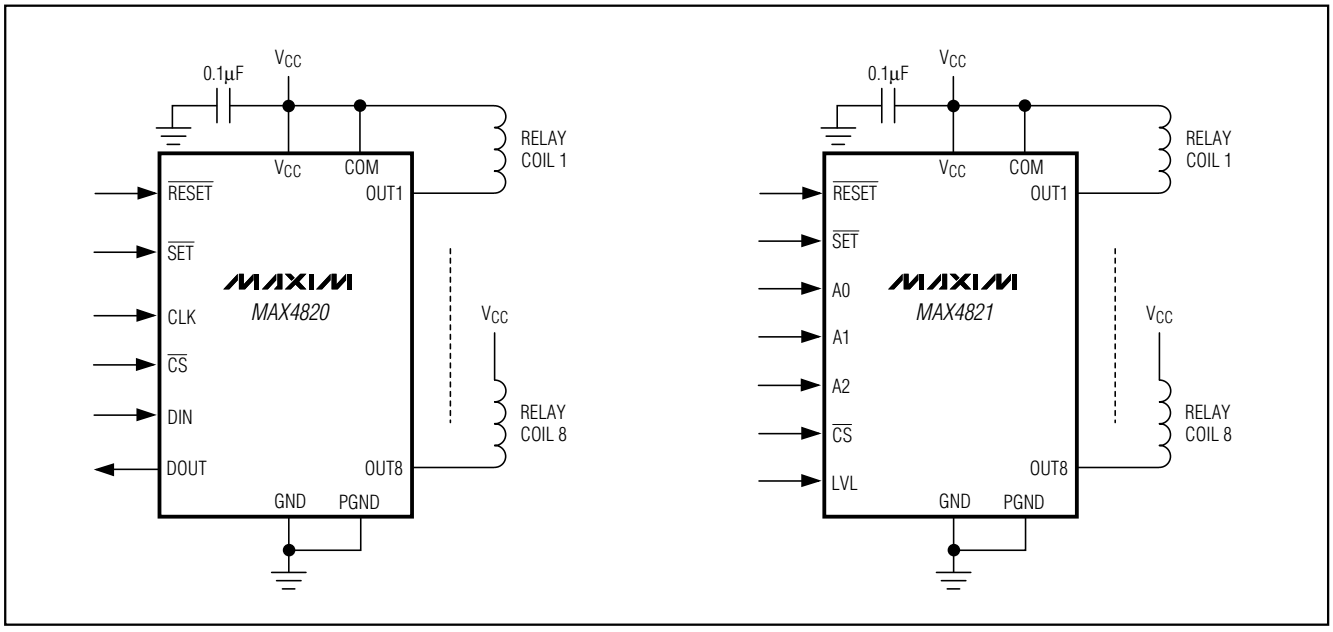
COM also can be connected to a higher voltage than V_{CC} (+6V max) for faster kickback recovery. In this configuration, bypass COM to PGND with a 0.1µF capacitor.

Relay Manufacturers

COMPANY	PHONE	WEBSITE
Aromat Corp.	310-524-9862	www.aromat.com
CP Clare Corp.	978-524-6700	www.crouzet.com
Coto Techonology	401-943-2686	www.cotorelay.com
Deustch Relays, Inc.	516-499-6000	www.deutschrelays.com
Fujitsu Takamisawa	408-745-4900	www.fujitsufta.com
Hella KG Hueck	734-414-0970	www.hella.com

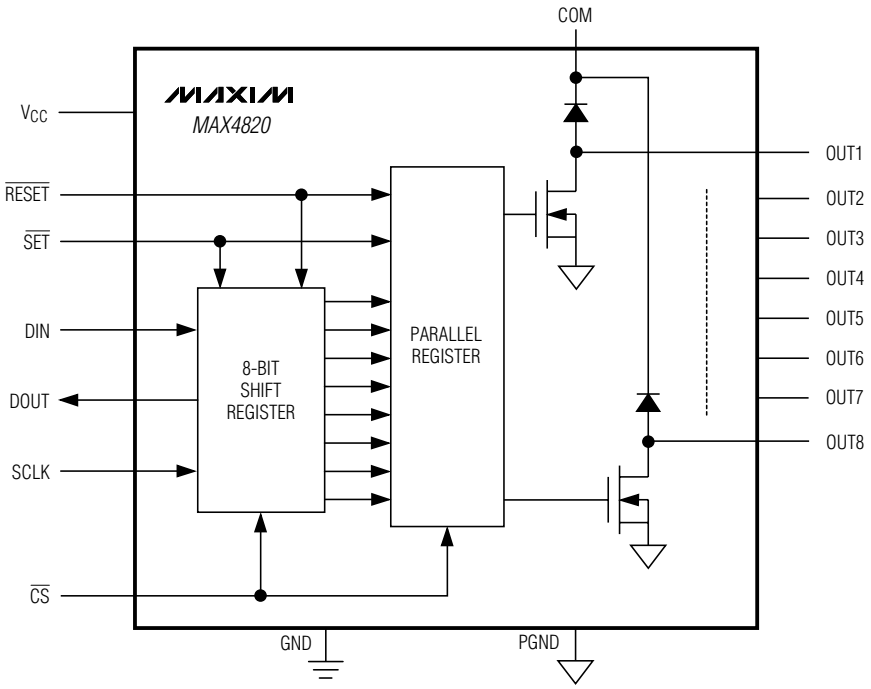
COMPANY	PHONE	WEBSITE
NEC Electronics, Inc.	800-366-9782	www.nec-global.com
Omron Electronics, Inc.	847-843-7900	www.oeiweb.omron.com
Rockwell/Allen-Bradley	414-382-2000	www.ab.com
Siemens Electromechanical Component, Inc.	770-371-3000	www.sec.siemens.com
Teledyne Relays	213-777-0077	www.teledynerelays.com

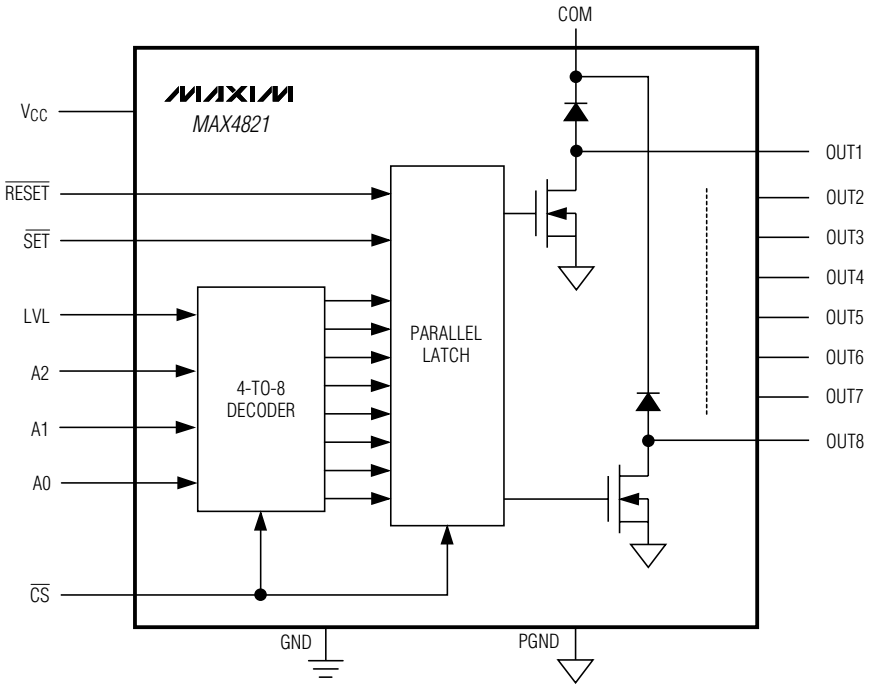
Typical Application Circuits



+3.3V/+5V, 8-Channel, Cascadable Relay Drivers with Serial/Parallel Interface

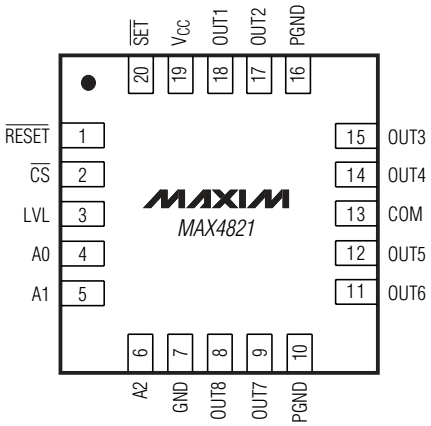
Functional Diagrams



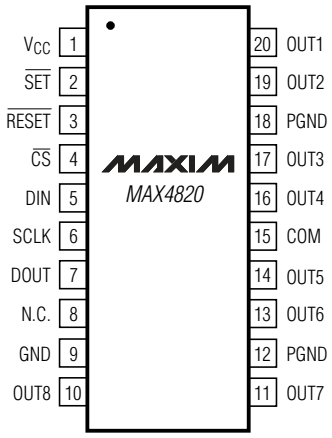


Pin Configurations (continued)

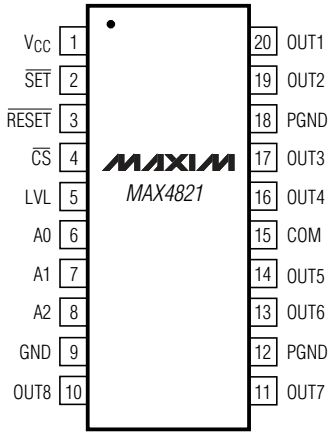
TOP VIEW



THIN QFN



TSSOP



TSSOP

Chip Information

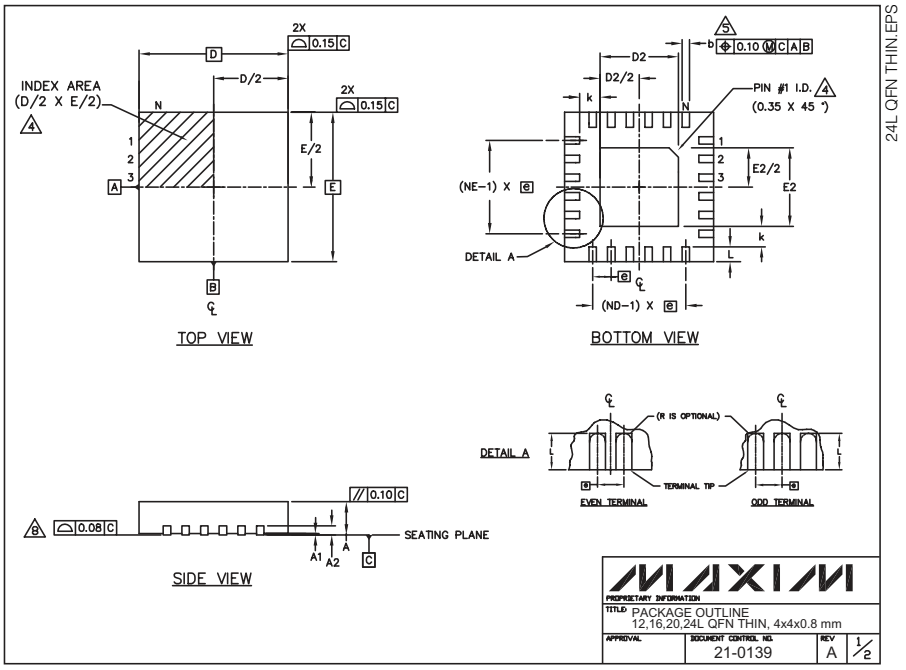
TRANSISTOR COUNT: 1301

PROCESS: BiCMOS

+3.3V/+5V, 8-Channel, Cascadable Relay Drivers with Serial/Parallel Interface

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

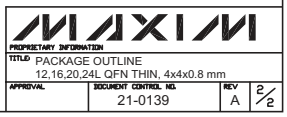


COMMON DIMENSIONS												
PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.		
k	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50
N	12			16			20			24		
ND	3			4			5			6		
NE	3			4			5			6		
Jedec Var.	WGGB			WGGC			WGGD-1			WGGD-2		

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1244-2	1.95	2.10	2.25	1.95	2.10	2.25
T1644-2	1.95	2.10	2.25	1.95	2.10	2.25
T2044-1	1.95	2.10	2.25	1.95	2.10	2.25
T2444-1	2.45	2.60	2.63	2.45	2.60	2.63

NOTES:

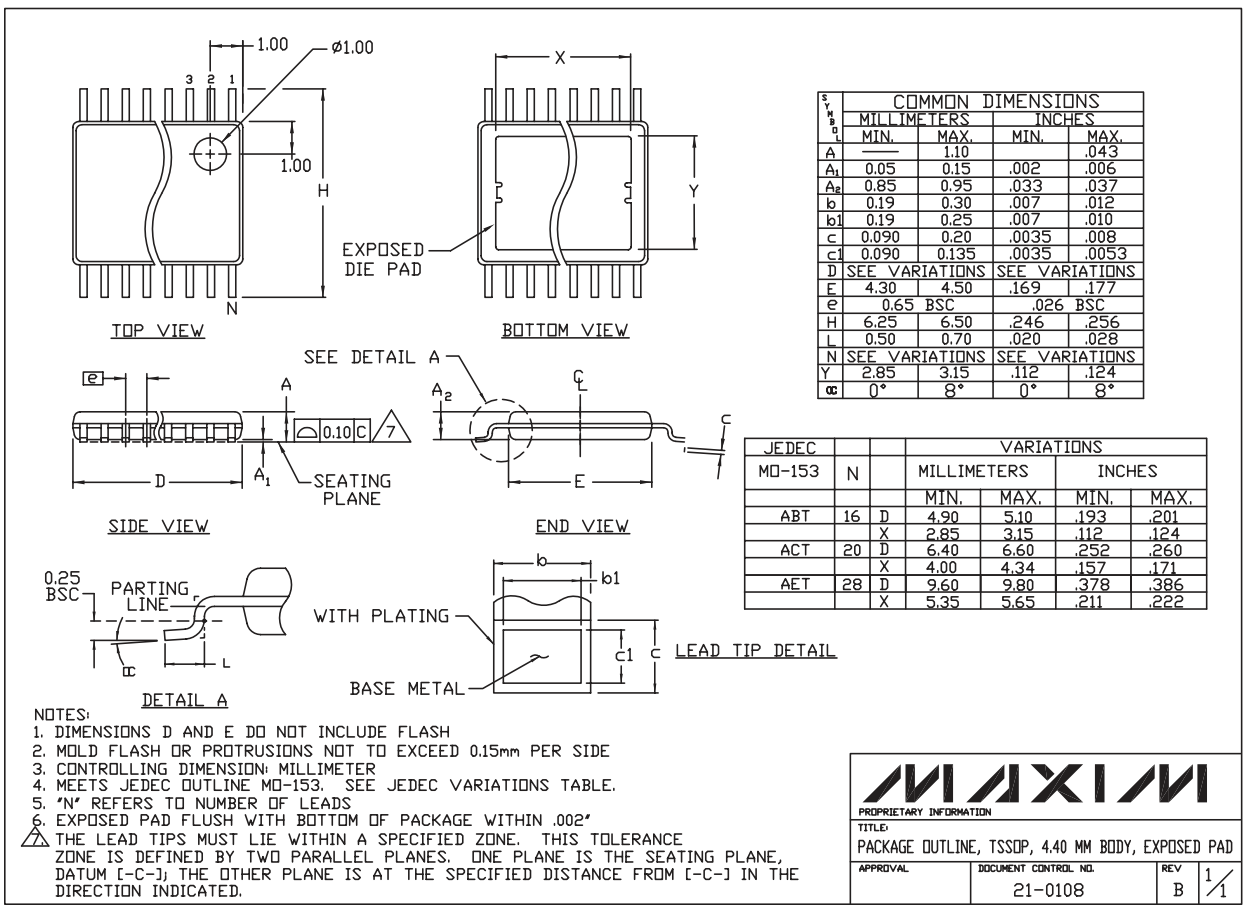
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220.



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

TSSOP, 4.0,EXP PADS.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	———	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b1	0.19	0.25	.007	.010
c	0.090	0.20	.0035	.008
c1	0.090	0.135	.0035	.0053
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.50	.246	.256
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
Y	2.85	3.15	.112	.124
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
ABT	16	D	4.90	5.10	.193	.201
		X	2.85	3.15	.112	.124
ACT	20	D	6.40	6.60	.252	.260
		X	4.00	4.34	.157	.171
AET	28	D	9.60	9.80	.378	.386
		X	5.35	5.65	.211	.222

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE.
5. "N" REFERS TO NUMBER OF LEADS
6. EXPOSED PAD FLUSH WITH BOTTOM OF PACKAGE WITHIN .002"
7. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED.

MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, TSSOP, 4.40 MM BODY, EXPOSED PAD

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0108	B	1/1