AK4958

24bit Stereo CODEC with MIC/SPK/VIDEO-AMP & LDO

GENERAL DESCRIPTION

The AK4958 is a 24-bit stereo CODEC with a microphone, speaker, video amplifiers and LDO. The input circuits include a microphone amplifier and the output circuits include a speaker amplifier. It is suitable for portable application with recording/playback function. A one channel composite In/Out video amplifier is also integrated. The AK4958 is available in a small 32-pin BGA (3.5mm x 3.5mm, 0.5mm pitch: AK4958EG) and a 25-pin CSP (2.2mm x 2.2mm, 0.4mm pitch: AK4958ECB) packages saving mounting area on the board.

FEATURES

1. Recording Functions
- **Analog Input**
  (AK4958EG)
  Stereo Single-ended input with two Selectors
  (AK4958ECB)
  Stereo Single-ended input
- **Microphone Amplifier**
  (+30dB, +25dB, +21dB, +18dB, +15dB, +12dB, +6dB, 0dB)
- **Digital ALC (Automatic Level Control)**
  - Setting Range: +36dB ~ –52.5dB, 0.375dB Step & Mute
  - Motor Noise Reduction Circuit
- **ADC Performance: S/(N+D): 83dB, DR, S/N: 88dB (MIC-Amp=+18dB)**
  S/(N+D): 85dB, DR, S/N: 96dB (MIC-Amp=0dB)
- **Microphone Sensitivity Compensation (with Moving Average Data Output Circuit)**
- **Automatic Wind Noise Reduction Filter**
- **5-Band Notch Filter**
  Include Dynamic Gain Control
- **Stereo Separation Emphasis Circuit**
- **Digital Microphone Interface**

2. Playback Functions
- **Soft Mute**
- **Digital ALC (Automatic Level Control)**
  - Setting Range: +36dB ~ –52.5dB, 0.375dB Step & Mute
- **Digital Volume Control**
  - +6dB ~ –89.5dB, 0.5dB Step & Mute)
- **Stereo Separation Emphasis Circuit**
- **Stereo Line Output**
  - Output Voltage: 1Vrms (AVDD= 3.3V)
  - S/(N+D): 85dB
  - S/N: 92dB
- **Mono Mixing Output**
- **Mono Speaker-Amplifier**
  - S/(N+D): 65dB@150mW, 60dB@250mW,
  - S/N: 90dB
  - BTL Output
  - Output Power: 400mW@8Ω (AVDD=3.3V)
- **Analog Mixing: BEEP Input**
- **Bass Boost Circuit**
- **3-band Dynamic Range Control Circuit**

3. Master Clock:
Reference Clock Input Frequency
(1) MCKI Reference PLL Mode
Frequencies: 11.2896MHz, 12MHz, 13.5MHz, 24MHz, 27MHz (MCKI pin)
(2) BICK Reference PLL Mode
Frequencies: 32fs or 64fs (BICK pin)
(3) External Clock Mode
Frequencies: 256fs, 512fs or 1024fs (MCKI pin)
Output Master Clock Frequency: 64fs/128fs/256fs/512fs
4. Sampling Frequencies
- **MCKI Reference PLL Mode (MCKI pin):**
  8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz
- **BICK Reference PLL Master Mode:**
  8kHz ~ 48kHz
- **EXT Mode:**
  7.35kHz ~ 48kHz (256fs), 7.35kHz ~ 48kHz (512fs), 7.35kHz ~ 13kHz (1024fs)

5. Master/Slave Mode
6. μP I/F:
(AK4958EG)
- **3-wire Serial, I^2C Bus (Ver 1.0, 400kHz Fast-Mode)**

(AK4958ECB)
- **I^2C Bus (Ver 1.0, 400kHz Fast-Mode)**

7. Master/Slave Mode
8. Audio Interface Format: MSB First, 2's complement
- **ADC: 24bit MSB justified, 16/24bit I^2S**
- **DAC: 24bit MSB justified, 16bit LSB justified, 24bit LSB justified, 24bit I^2S**

9. Video Functions
- **One Composite Signal Input**
- **Video Amplifier for Composite Signal Output**
  Gain: (AK4958EG) +6 / +12 / +16.5dB, (AK4958ECB) +12 / +16.5dB
- **Low Pass Filter**

10. Ta = –30 ~ 85°C
11. Power Supply:
(AK4958EG)
- **Analog Power Supply (AVDD): 2.8 ~ 3.6V**
- **Digital Power Supply (DVDD): 1.6 ~ 2.0V**
- **Digital I/O Power Supply (TVDD): 1.6 or DVDD – 0.2 ~ 3.6V**

(AK4958ECB)
- **Analog Power Supply (AVDD): 2.8 ~ 3.6V**
- **Digital & Digital I/O Power Supply (DTVDD): 1.6 ~ 2.0V**

12. Package:
(AK4958EG)
- **32pin BGA (3.5 x 3.5 mm, 0.5mm pitch)**

(AK4958ECB)
- **25pin CSP (2.2 x 2.2 mm, 0.4mm pitch)**

■ Block Diagram

▪ AK4958EG

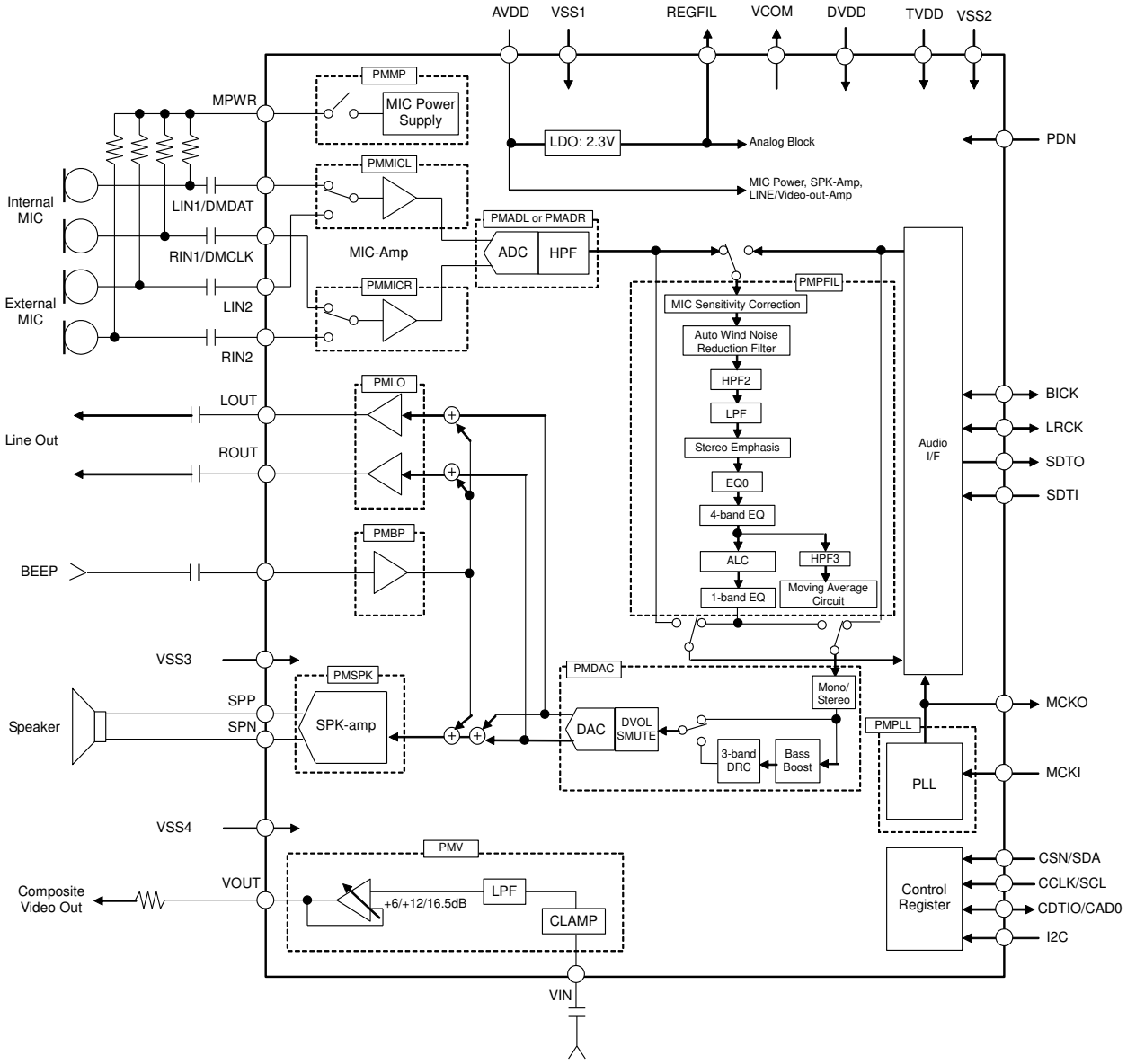


Figure 1. Block Diagram (AK4958EG)

▪ AK4958ECB

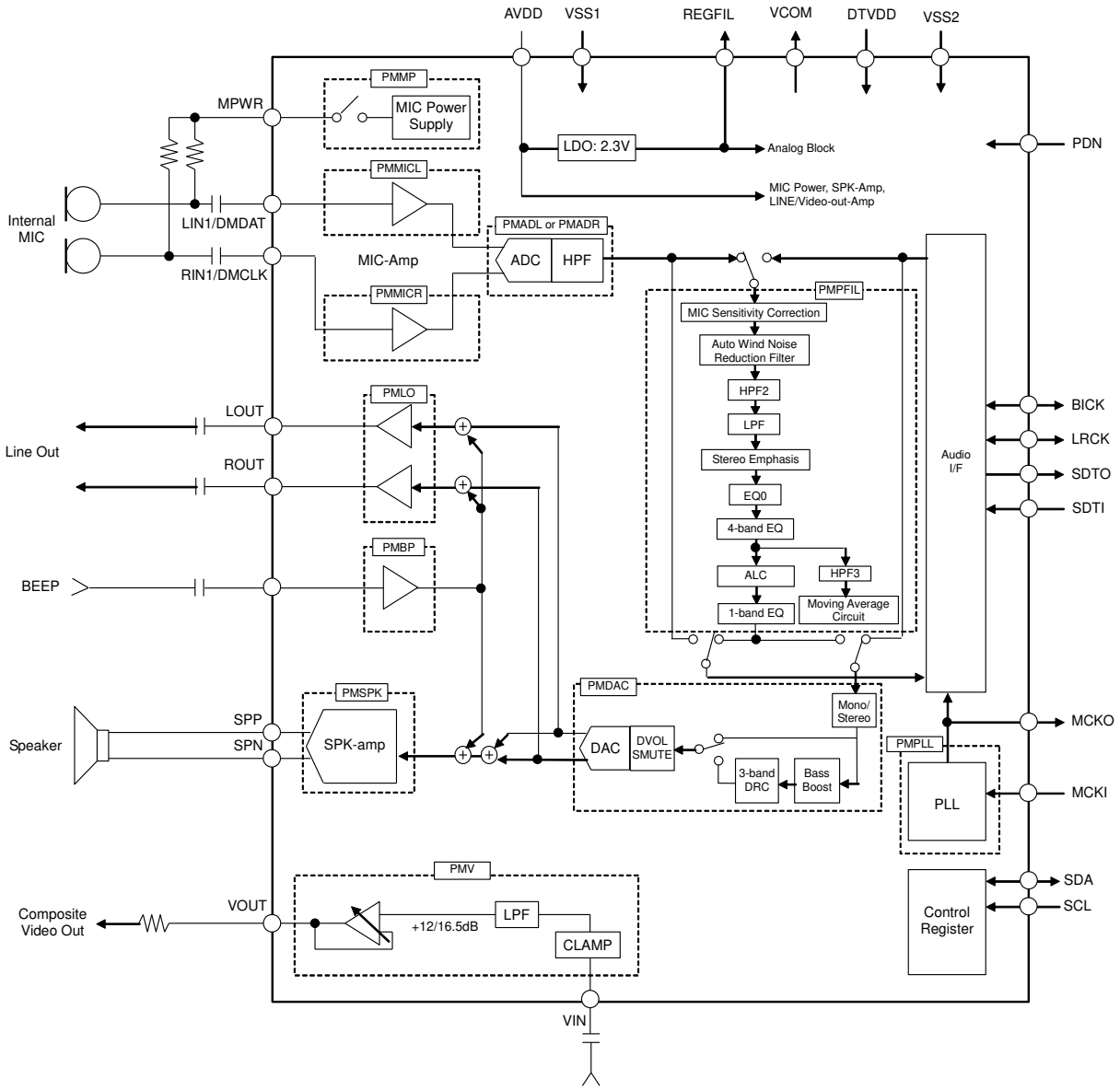


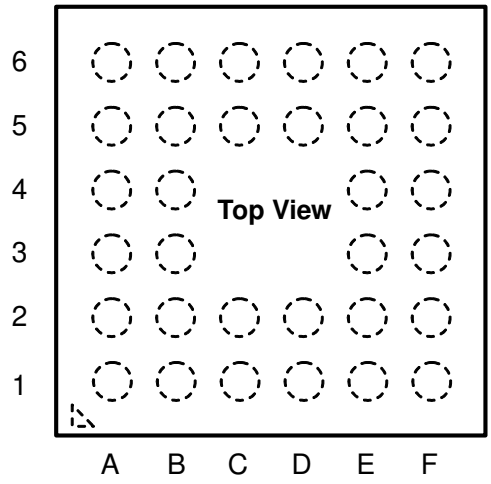
Figure 2. Block Diagram (AK4958ECB)

■ Ordering Guide

AK4958EG	−30 ~ +85°C	32-pin BGA (0.5mm pitch)
AK4958ECB	−30 ~ +85°C	25-pin CSP (0.4mm pitch)
AKD4958EG	Evaluation board for AK4958EG	
AKD4958ECB	Evaluation board for AK4958ECB	

■ Pin Layout

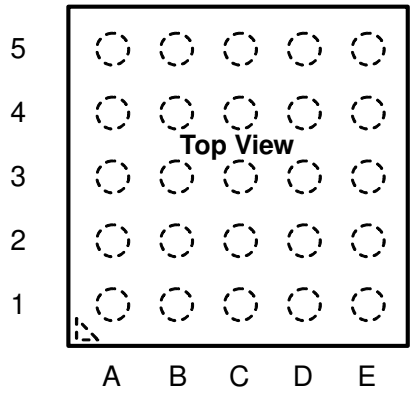
▪ AK4958EG



6	MPWR	ROUT	REGFIL	VCOM	VSS1	VIN
5	RIN2	BEEP	LOUT	AVDD	VOUT	VSS4
4	RIN1 /DMCLK	LIN2			SPP	SPN
3	LIN1 /DMDAT	I2C			VSS2	VSS3
2	CDTIO /CAD0	CSN /SDA	SDTI	MCKO	MCKI	DVDD
1	CCLK /SCL	LRCK	BICK	SDTO	TVDD	PDN
	A	B	C	D	E	F

Top View

▪ AK4958ECB



5	PDN	VSS2	SPP	SPN	VIN
4	MCKO	MCKI	DTVDD	VOUT	VSS1
3	SDTI	SDTO	BEEP	AVDD	VCOM
2	LRCK	BICK	RIN1 /DMCLK	LOUT	REGFIL
1	SCL	SDA	LIN1 /DMDAT	MPWR	ROUT
	A	B	C	D	E

Top View

■ Comparison Table of the AK4958EG and AK4958ECB

Function	AK4958EG	AK4958ECB
Digital I/O Voltage	TVDD = 1.6 or DVDD-0.2 ~ 3.6V	DTVDD = 1.6V ~ 2.0V *Digital Power and Digital Interface Supply share a pin.
Number of VSS Pin	Four pins	Two pins
ADC Input Channel	2 Stereo (LIN1/RIN1, LIN2/RIN2)	1 Stereo (LIN1/RIN1)
Control I/F mode	3-wire / I2C	I2C *Slave address "0010011"
Package	32BGA (3.5 x 3.5mm, 0.5mm pitch)	25CSP (2.2 x 2.2mm, 0.4mm pitch)

PIN/FUNCTION (AK4958EG)

No	Pin Name	I/O	Function
Power Supply			
D5	AVDD	-	Analog Power Supply, 2.8 ~ 3.6V This pin must be connected to VSS1 through a 0.1µF ceramic capacitor.
D6	VCOM	O	Common Voltage Output Bias voltage of ADC inputs and DAC outputs. This pin must be connected to VSS1 through a 2.2µF ±50% capacitor.
E6	VSS1	-	Ground 1
F2	DVDD	-	Digital Power Supply, 1.6 ~ 2.0V This pin must be connected to VSS2 through a 0.1µF ceramic capacitor.
E1	TVDD	-	Digital Interface Supply, 1.6 or DVDD-0.2V ~ 3.6V
C6	REGFIL	O	LDO Voltage Output pin for Analog Logic (typ 2.3V) This pin must be connected to VSS1 through a 2.2µF ±50% capacitor.
E3	VSS2	-	Ground 2
F3	VSS3	-	Ground 3
F5	VSS4	-	Ground 4
Audio Interface			
E2	MCKI	I	Master Clock Input (Note 1)
D2	MCKO	O	Master Clock Output
B1	LRCK	I/O	Channel Clock Pin (Note 1)
C1	BICK	I/O	Audio Serial Data Clock Pin (Note 1)
C2	SDTI	I	Audio Serial Data Input (Note 1)
D1	SDTO	O	Audio Serial Data Output
Control Register Interface			
B2	CSN	I	Chip Select Pin (I2C pin = "L") (Note 1)
	SDA	I/O	Control Data Input/Output (I2C pin = "H") (Note 1)
A1	CCLK	I	Control Data Clock Pin (I2C pin = "L") (Note 1)
	SCL	I	Control Data Clock Pin (I2C pin = "H") (Note 1)
A2	CDTIO	I/O	Control Data Input/Output (I2C pin = "L") (Note 1)
	CAD0	I	Chip Address Select Pin (I2C pin = "H") (Note 1)
B3	I2C	I	Control Mode Select Pin "H": I^2C Bus, "L": 3-wire Serial (Note 1)

Note 1. All input pins except analog input pins (BEEP, LIN1, RIN1, LIN2, RIN2, VIN) must not be allowed to float.

No	Pin Name	I/O	Function
Microphone Block			
3	LIN1	I	Lch Analog Input 1 (DMIC bit = "0")
	DMDAT	I	Digital Microphone Data Input (DMIC bit = "1") (Note 1)
4	RIN1	I	Rch Analog Input 1 (DMIC bit = "0")
	DMCLK	O	Digital Microphone Clock (DMIC bit = "1")
5	LIN2	I	Lch Analog Input 2
6	RIN2	I	Rch Analog Input 2
2	MPWR	O	Microphone Power Supply
MIN Block			
1	BEEP	I	BEEP Signal Input
Lineout Block			
31	LOUT	O	Lch Analog Output
32	ROUT	O	Rch Analog Output
Speaker Block			
21	SPP	O	Speaker Amp Positive Output
22	SPN	O	Speaker Amp Negative Output
Video Block			
25	VIN	I	Composite Video Input
24	VOUT	O	Composite Video Output
Other Functions			
18	PDN	I	Reset & Power-down Pin (Note 1) "L": Reset & Power-down, "H": Normal Operation

Note 1. All input pins except analog input pins (BEEP, LIN1, RIN1, LIN2, RIN2, VIN) must not be allowed to float.

PIN/FUNCTION (AK4958ECB)

No	Pin Name	I/O	Function	
Power Supply				
D3	AVDD	-	Analog Power Supply, 2.8 ~ 3.6V This pin must be connected to VSS1 through a 0.1µF ceramic capacitor.	
E3	VCOM	O	Common Voltage Output Bias voltage of ADC inputs and DAC outputs. This pin must be connected to VSS1 through a 2.2µF ±50% capacitor.	
E4	VSS1	-	Ground 1	
C4	DTVDD	-	Digital Power & Digital Interface Supply, 1.6 ~ 2.0V This pin must be connected to VSS2 through a 0.1µF ceramic capacitor.	
E2	REGFIL	O	LDO Voltage Output pin for Analog Logic (typ 2.3V) This pin must be connected to VSS1 through a 2.2µF ±50% capacitor.	
B5	VSS2	-	Ground 2	
Audio Interface				
B4	MCKI	I	Master Clock Input (Note 2)	
A4	MCKO	O	Master Clock Output	
A2	LRCK	I/O	Channel Clock (Note 2)	
B2	BICK	I/O	Audio Serial Data Clock (Note 2)	
A3	SDTI	I	Audio Serial Data Input (Note 2)	
B3	SDTO	O	Audio Serial Data Output	
Control Register Interface				
B1	SDA	I/O	Control Data Input/Output (Note 2)	
A1	SCL	I	Control Data Clock Pin (Note 2)	
Microphone Block				
C1	LIN1	I	Lch Analog Input 1	(DMIC bit = “0”)
	DMDAT	I	Digital Microphone Data Input	(DMIC bit = “1”) (Note 2)
C2	RIN1	I	Rch Analog Input 1	(DMIC bit = “0”)
	DMCLK	O	Digital Microphone Clock Pin	(DMIC bit = “1”)
D1	MPWR	O	Microphone Power Supply	
BEEP Block				
C3	BEEP	I	BEEP Signal Input	
Lineout Block				
D2	LOUT	O	Lch Analog Output	
E1	ROUT	O	Rch Analog Output	
Speaker Block				
C5	SPP	O	Speaker Amp Positive Output	
D5	SPN	O	Speaker Amp Negative Output	
Video Block				
E5	VIN	I	Composite Video Input	
D4	VOUT	O	Composite Video Output	
Other Functions				
A5	PDN	I	Reset & Power-down Pin “L”: Reset & Power-down, “H”: Normal Operation	

Note 2. All input pins except analog input pins (BEEP, LIN1, RIN1, VIN) must not be allowed to float.

■ Handling of Unused Pin

Unused I/O pins must be processed appropriately as below.

Classification	Pin Name	Setting
Analog	MPWR, SPN, SPP, LOUT, ROUT, BEEP, RIN2, LIN2, VIN, VOUT	These pins must be open.
	LIN1, RIN1	DMIC bit = "0", and these pins must be open.
Digital	MCKO, SDTO	These pins must be open.
	MCKI, SDTI	These pins must be connected to VSS2.
	LRCK, BICK	M/S bit = "0", and these pins must be connected to VSS2.

ABSOLUTE MAXIMUM RATINGS

(AK4958EG: VSS1=VSS2=VSS3=VSS4=0V, AK4958ECB: VSS1=VSS2=0V; Note 3)

Parameter			Symbol	min	max	Unit
Power Supplies (AK4958EG)	Analog		AVDD	–0.3	6.0	V
	Digital		DVDD	–0.3	2.5	V
	Digital I/O		TVDD	–0.3	6.0	
Power Supplies (AK4958ECB)	Analog		AVDD	–0.3	6.0	V
	Digital, Digital I/O		DTVDD	–0.3	2.5	
Input Current, Any Pin Except Supplies			IIN	-	±10	mA
Analog Input Voltage (Note 4)			VINA	–0.3	AVDD+0.3	V
Digital Input Voltage	(AK4958EG, Note 5)		VIND	–0.3	TVDD+0.3	V
	(AK4958ECB, Note 6)		VIND	–0.3	DTVDD+0.3	V
	(Note 8)		VIND	–0.3	6.0	V
Ambient Temperature (powered applied)			Ta	–30	85	°C
Storage Temperature			Tstg	–65	150	°C
Maximum Power Dissipation (Note 8)		AK4958EG	Pd1	-	460	mW
		AK4958ECB	Pd1	-	460	mW

Note 3. All voltages are with respect to ground. VSS1, VSS2, VSS3 and VSS4 must be connected to the same analog ground plane.

Note 4. BEEP, LIN1, RIN1, LIN2, RIN2, VIN, I2C pins

Note 5. PDN, CDTIO, SDTI, LRCK, BICK and MCKI pins

Note 6. PDN, SDTI, LRCK, BICK, MCKI pins

Note 7. CSN/SDA and CCLK/SCL pins

Note 8. This power is the AK4958 internal dissipation that does not include power dissipation of externally connected speakers. The maximum junction temperature is 125°C and θja (Junction to Ambient) is 80°C/W at JESD51-9 (2p2s) for the AK4958EG and 56°C/W for the AK4958ECB. When Pd =460mW and the θja is 80°C/W for the AK4958EG, and 56°C/W for the AK4958ECB, the junction temperature does not exceed 125°C. In this case, the AK4958 will not be damaged by its internal power dissipation. Therefore, the AK4958EG should be used in the condition of θja ≤ 80°C/W, and the AK4958ECB should be used in the condition of θja ≤ 56°C/W.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS (AK4958EG)

(VSS1=VSS2=VSS3=VSS4=0V; Note 3)

Parameter		Symbol	min	typ	max	Unit
Power Supplies (Note 9)	Analog	AVDD	2.8	3.3	3.6	V
	Digital	DVDD	1.6	1.8	2.0	V
	Digital I/O (Note 10)	TVDD	1.6 or DVDD-0.2	1.8	3.6	V

Note 3. All voltages are with respect to ground.

Note 9. The power-up sequence between AVDD, DVDD and TVDD is not critical. The PDN pin must be "L" upon power up, and should be changed to "H" after all power supplies are supplied to avoid an internal circuit error.

Note 10. The minimum value is higher voltage between DVDD-0.2V and 1.6V.

*** When TVDD is powered ON and the PDN pin is "L", AVDD and DVDD can be powered ON/OFF. When the AK4958EG is powered ON from power-down state, the PDN pin must be "H" after all power supplies (AVDD, DVDD and TVDD) are ON.**

RECOMMENDED OPERATING CONDITIONS (AK4958ECB)

(VSS1=VSS2 =0V; Note 3)

Parameter		Symbol	min	typ	max	Unit
Power Supplies (Note 9)	Analog	AVDD	2.8	3.3	3.6	V
	Digital, Digital I/O	DTVDD	1.6	1.8	2.0	V

Note 3. All voltages are with respect to ground.

Note 11. The power-up sequence between AVDD and DTVDD is not critical. The PDN pin must be "L" upon power up, and should be changed to "H" after all power supplies are supplied to avoid an internal circuit error.

*** When DTVDD is powered ON and the PDN pin is "L", AVDD can be powered ON/OFF. When the AK4958ECB is powered ON from power-down state, the PDN pin must be "H" after all power supplies (AVDD and DTVDD) are ON.**

* AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; fs=48kHz, BICK=64fs;Signal Frequency=1kHz; 24bit Data; Measurement Bandwidth =20Hz ~ 20kHz; unless otherwise specified; AK4958EG: AVDD = 3.3V, DVDD = TVDD= 1.8V;VSS1=VSS2=VSS3=VSS4=0V, AK4958ECB: AVDD = 3.3V, DTVDD = 1.8V; VSS1=VSS2=0V)

Parameter			min	typ	max	Unit
Microphone Amplifier: LIN1, RIN1, LIN2, RIN2 pins						
Input Resistance			20	30	42	kΩ
Gain	MGAIN2-0 bits = "000"		-1	0	+1	dB
	MGAIN2-0 bits = "001"		+5	+6	+7	dB
	MGAIN2-0 bits = "010"		+11	+12	+13	dB
	MGAIN2-0 bits = "011"		+14	+15	+16	dB
	MGAIN2-0 bits = "100"		+17	+18	+19	dB
	MGAIN2-0 bits = "101"		+20	+21	+22	dB
	MGAIN2-0 bits = "110"		+24	+25	+26	dB
	MGAIN2-0 bits = "111"		+29	+30	+31	dB
Microphone Power Supply: MPWR pin						
Output Voltage	MICL bit = "0"		2.2	2.4	2.6	V
	MICL bit = "1"		1.8	2.0	2.2	V
Output Noise Level (A-weighted)			-	–108	-	dBV
Load Resistance			0.5	-	-	kΩ
Load Capacitance			-	-	30	pF
PSRR (Sine Wave = 500mVpp, fin = 1kHz)			-	100	-	dB
ADC Analog Input Characteristics AK4958EG: LIN1/RIN1/LIN2/RIN2 pins → ADC (Programmable Filter = OFF) AK4958ECB: LIN1/RIN1 pins → ADC (Programmable Filter = OFF)						
Resolution			-	-	24	Bits
Input Voltage (Note 12)		(Note 13)	-	0.261	-	Vpp
		(Note 14)	1.86	2.07	2.28	Vpp
S/(N+D) (–1dBFS)		(Note 13)	73	83	-	dBFS
		(Note 14)	-	85	-	dBFS
D-Range (–60dBFS, A-weighted)		(Note 13)	78	88	-	dB
		(Note 14)	-	96	-	dB
S/N (A-weighted)		(Note 13)	78	88	-	dB
		(Note 14)	-	96	-	dB
Interchannel Isolation		(Note 13)	75	90	-	dB
		(Note 14)	-	100	-	dB
Interchannel Gain Mismatch		(Note 13)	-	0	0.5	dB
		(Note 14)	-	0	0.5	dB
PSRR (Sine Wave = 500mVpp, fin = 1kHz)			-	80	-	dB

Note 12. Vin = 0.9 x 2.3Vpp (typ) @MGAIN2-0 bits = "000" (0dB)
Note 13. MGAIN2-0 bits = "110" (+18dB)
Note 14. MGAIN2-0 bits = "000" (0dB)

Parameter			min	typ	max	Unit
DAC Characteristics:						
Resolution			-	-	24	Bits
Stereo Line Output Characteristics: DAC → LOUT, ROUT pins, ALC=OFF, DVOL=OVOL =0dB, R_L=10kΩ , PMBP bit = "0", LVCM1-0 bits = "01"						
Output Voltage (Note 15)	(0dBFS)	LVCM0 bit = "0"	-	2.26	-	Vpp
		LVCM0 bit = "1"	-	1.00	-	Vrms
Output Voltage (Note 15)	(–3dBFS)	LVCM0 bit = "0"	1.44	1.60	1.76	Vpp
		LVCM0 bit = "1"	1.82	2.00	2.22	Vpp
S/(N+D) (–3dBFS)			75	85	-	dBFS
S/N (A-weighted)			82	92	-	dB
Interchannel Isolation			85	100	-	dB
Interchannel Gain Mismatch			-	0	0.8	dB
Load Resistance			10	-	-	kΩ
Load Capacitance			-	-	30	pF
PSRR (Sine Wave = 500mVpp, fin = 1kHz)			-	80	-	dB
Speaker-Amp Characteristics: DAC → SPP/SPN pins, ALC=OFF, DVOL=OVOL =0dB, R_L=8Ω, BTL						
Output Voltage (AK4958EG)						
SPKG1-0 bits = "00", –0.5dBFS (Po=150mW)			-	3.18	-	Vpp
SPKG1-0 bits = "01", –0.5dBFS (Po=250mW)			3.20	4.00	4.80	Vpp
SPKG1-0 bits = "10", –0.5dBFS (Po=400mW)			-	1.79	-	Vrms
S/(N+D) (AK4958EG)						
SPKG1-0 bits = "00", –0.5dBFS (Po=150mW)			-	65	-	dB
SPKG1-0 bits = "01", –0.5dBFS (Po=250mW)			20	60	-	dB
SPKG1-0 bits = "10", –0.5dBFS (Po=400mW)			-	20	-	dB
S/N (AK4958EG) SPKG1-0 bits = "01", –0.5dBFS (Po=250mW) (A-weighted)			80	90	-	dB
Output Voltage (AK4958ECB)			-	-	-	
SPKG1-0 bits = "00", –0.7dBFS (Po=150mW)			-	3.18	-	Vpp
SPKG1-0 bits = "01", –0.7dBFS (Po=250mW)			3.20	4.00	4.80	Vpp
SPKG1-0 bits = "10", –0.85dBFS (Po=400mW)			-	1.79	-	Vrms
S/(N+D) (AK4958ECB)						
SPKG1-0 bits = "00", –0.7dBFS (Po=150mW)			-	65	-	dB
SPKG1-0 bits = "01", –0.7dBFS (Po=250mW)			20	60	-	dB
SPKG1-0 bits = "10", –0.85dBFS (Po=400mW)			-	20	-	dB
S/N (AK4958ECB) SPKG1-0 bits = "01", –0.7dBFS (Po=250mW) (A-weighted)			80	90	-	dB
Load Resistance			6.8	-	-	Ω
Load Capacitance			-	-	100	pF
PSRR (Sine Wave = 500mVpp, fin = 1kHz)			-	60	-	dB

Note 15. The output voltage does not track the AVDD.

Parameter			min	typ	max	Unit
BEEP Input: BEEP pin, Internal Resistance Mode (PMBP bit =“1”, BPM bit = “0”, BPVCM bit = “0”, BPLVL3-0 bits = “0000”)						
Input Resistance			46	66	86	kΩ
Maximum Input Voltage (Note 16)			-	-	1.54	Vpp
Gain						
	MIN → LOUT	LVCM1-0 bits = “00”	–1	0	+1	dB
		LVCM1-0 bits = “01”	-	+2.0	-	dB
		LVCM1-0 bits = “10”	-	+2.0	-	dB
		LVCM1-0 bits = “11”	-	+4.0	-	dB
	MIN → SPP/SPN (Note 17)					
		ALC2 bit = “0”, SPKG1-0 bits = “00”	+4.4	+6.4	+8.4	dB
		ALC2 bit = “0”, SPKG1-0 bits = “01”	-	+8.4	-	dB
		ALC2 bit = “0”, SPKG1-0 bits = “10”	-	+11.1	-	dB
		ALC2 bit = “0”, SPKG1-0 bits = “11”	-	+13.1	-	dB
		ALC2 bit = “1”, SPKG1-0 bits = “00”	-	+8.4	-	dB
		ALC2 bit = “1”, SPKG1-0 bits = “01”	-	+10.1	-	dB
		ALC2 bit = “1”, SPKG1-0 bits = “10”	-	+13.1	-	dB
		ALC2 bit = “1”, SPKG1-0 bits = “11”	-	+15.1	-	dB
BEEP Input: BEEP pin, External Resistance mode (PMBP bit =“1”, BPM bit = “1”, BPVCM bit = “0”, BPLVL3-0 bits = “0000”), External Input Resistance= 66kΩ						
Maximum Input Voltage			-	-	1.54	Vpp
Gain (Note 18)						
	BEEP → LOUT	LVCM1-0 bits = “00”	–4.5	0	+4.5	dB
		LVCM1-0 bits = “01”	-	+2.0	-	dB
		LVCM1-0 bits = “10”	-	+2.0	-	dB
		LVCM1-0 bits = “11”	-	+4.0	-	dB
	BEEP → SPP/SPN					
		ALC2 bit = “0”, SPKG1-0 bits = “00”	+1.9	+6.4	+10.9	dB
		ALC2 bit = “0”, SPKG1-0 bits = “01”	-	+8.4	-	dB
		ALC2 bit = “0”, SPKG1-0 bits = “10”	-	+11.1	-	dB
		ALC2 bit = “0”, SPKG1-0 bits = “11”	-	+13.1	-	dB
		ALC2 bit = “1”, SPKG1-0 bits = “00”	-	+8.4	-	dB
		ALC2 bit = “1”, SPKG1-0 bits = “01”	-	+10.4	-	dB
		ALC2 bit = “1”, SPKG1-0 bits = “10”	-	+13.1	-	dB
		ALC2 bit = “1”, SPKG1-0 bits = “11”	-	+15.1	-	dB

Note 16. The maximum value is AVDD Vpp when BPVCM bit = “1”. However, a click noise may occur when the amplitude after BEEP-Amp is 0.5Vpp or more. (set by BPLVL3-0 bits)

Note 17. These are the ideal values with no load resistance. When an 8Ω is connected the value degrades about 0.4dB for the AK4958EG and about 0.2dB for the AK4958ECB.

Note 18. The gain is in inverse proportion to external input resistance.

Parameter		min	typ	max	Unit
Video Signal Input					
External Resistor (Note 20)	R1 (Figure 3)	0.075	-	1.6	kΩ
External Capacitor	C1 (Figure 3)	0.02	0.047	0.2	μF
Maximum Input Voltage: VG1-0 bits = "10" (+12dB)		-	0.6	-	Vpp
Pull Down Current		-	0.125	-	μA
Video Analog Output (Figure 4)					
Output Gain fin =100kHz Sine wave Input (Note 19)	VG1-0 bits = "00", 0.5Vpp Input (AK4958EG)	5.5	6.0	6.5	dB
	VG1-0 bits = "10", 0.5Vpp Input	11.5	12.0	12.5	
	VG1-0 bits = "11", 0.3Vpp Input	16.0	16.5	17.0	
Clamp Level (Note 19)		-	50	100	mV
S/N (Note 21) VG1-0 bits = "10"(+12dB)	BW = 100kH ~ 6MHz, S = 0.35Vpp Input	60	67	-	dB
Maximum Output Voltage (Note 19)	fin =100kHz (Sine wave)	2.54	-	-	Vpp
Secondary Harmonic Distortion VG1-0 bits = "10"(+12dB) fin = 3.58MHz	430mVpp: –20 ~ 100IRE, Sine Wave Input (Flat Field = 100 IRE Burst = –20IRE)	-	–45	–35	dB
Load Resistance		140	150	-	Ω
Load Capacitance	C2 (Figure 4)	-	-	15	pF
	C3 (Figure 4)	-	-	400	pF
PSRR (Note 22) VG1-0 bits = "10"(+12dB)	fin = 10kHz	-	45	-	dB
	fin = 100kHz	-	30	-	dB
LPF for VIN signal : (Note 19)					
Frequency Response (fin = 100kHz, 0.5Vpp, Sine wave Input), C2=15pF, C3=400pF					
	Response at 6.75MHz	–3.0	–0.5	+2.0	dB
	Response at 27MHz	-	–47	–20	
Group Delay	|GD3MHz–GD6MHz|	-	15	100	ns

Note 19. This is a value at measurement point in Figure 4. 0.5Vpp input is the value when VG1-0 bit ="10"(+12dB). Input amplitude is in inverse proportion to the gain. S/N and Secondary Harmonic Distortion values are measured at measuring point 2.

Note 20. PMV bit must be set to "0" if the resistor value exceeds the range from 0.075 to 1.6kΩ in case of the input signal is stopped or the input circuit of the VIN pin is powered down.

Note 21. S/N = 20xlog (Output Voltage[Vpp]/Noise Level[Vrms]). Output Voltage = 0.7 [Vpp].

Note 22. PSRR is applied to AVDD with 500mVpp sine wave when DC level of -20IRE, 0IRE and 100IRE are input to the VIN pin.

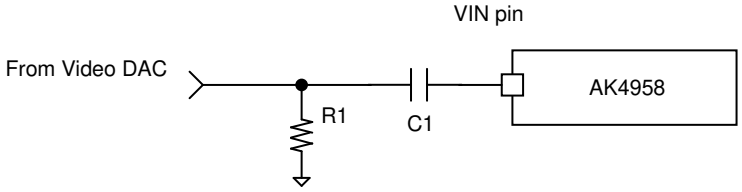


Figure 3. External Resistor of Video Signal Input pin

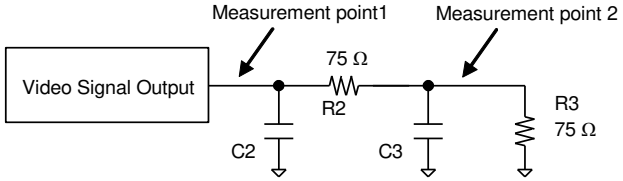


Figure 4. Load Capacitance C2 and C3

Parameter		min	typ	max	Unit
Power Supplies:					
Power Up (PDN pin = "H")					
All Circuit Power-up (Note 23)					
	AVDD	-	10.5	15	mA
	DVDD +TVDD	-	2.8	4.2	mA
MIC + ADC (Note 24)					
	AVDD	-	2.5	-	mA
	DVDD +TVDD	-	0.9	-	mA
DAC + Lineout (Note 25)					
	AVDD	-	2.2	-	mA
	DVDD +TVDD	-	0.7	-	mA
DAC + SPK-Amp (Note 26)					
	AVDD	-	3.3	-	mA
	DVDD +TVDD	-	0.7	-	mA
Video Block (Note 27)					
	AVDD	-	5.3	-	mA
Power Down (PDN pin = "L") (Note 28)					
AVDD+DVDD+TVDD		-	1	5	μA

Note 23. When PMADL=PMADR=PMDAC=PMPFIL=PMLO=PMSPK=PMPLL=MCKO=PMBP=PMMP =PMMICR =PMMICL =M/S =PMV bits = "1", SPK-amp No load, no signals are input to LIN/RIN and BEEP pins, black signal is input to the VIN pin, no output from the LOUT/ROUT pin and "0" data input to the SDTI pin in PLL Master Mode (MCKI=13.5MHz, FS3-0 bits = "1011"). In this case, the output current of the MPWR pin is 0mA. The path settings are, BRDAC= ADCPF = PFSDO bits = "1", PFDAC bit= "0", DACS = DACL bits = "1", and BEEPS = BEEPL bits = "0". MG2-0 bits = "000", HPF = LPF = FIL3 = EQ0 = EQ1~5 = ALC1~2 bits = "0", MONO1-0 bits = "00", DVOL7-0 bits = "C0H", and SMUTE bit = "0".

Note 24. When PMADL = PMADR = PMMICL = PMMICLR bits = "1" and no signals are input to the LIN/RIN pin in EXT Slave Mode (PMPLL=M/S=MCKO bits ="0"). The path setting is ADCPF=PFSDO bits = "0".

Note 25. When PMDAC = PMLO = "1", "0" data input to the SDTI pin, and no output from the LOUT/ROUT pin in EXT Slave Mode (PMPLL=M/S=MCKO bits ="0"). The path settings are BRDAC= PFDAC bit = "0", DACL bit = "1", and DACS =BEEPS =BEEPL bits = "0". MONO1-0 bits = "00", DVOL7-0 bits = "0CH", and SMUTE bit = "0".

Note 26. When PMDAC = PMSPK =SPPSN bits = "1", "0" data input to the SDTI pin, and No load at SPK-amp in EXT Slave Mode (PMPLL=M/S=MCKO bits ="0"). The path settings are MONO1-0 bits= "00", DVOL7-0 bits "C0H", and SMUTE bit = "0".

Note 27. When PMV bit = "1", No-load, and the black signal is input to the VIN pin.

Note 28. Digital input pins (MCKI, LRCK, BICK, SDTI, CSN/SDA, CCLK/SCL, CDTIO/CAD0, I2C pins) are fixed to TVDD (AK4958EG), DTVDD(AK4958ECB) or VSS2, and the I2C pin is fixed to AVDD or VSS.

FILTER CHARACTERISTICS

(Ta =25°C; fs=48kHz; AK4958EG: AVDD=2.8 ~ 3.6V, DVDD = 1.6 ~ 2.0V, TVDD = 1.6 or (DVDD-0.2)~ 3.6V, AK4958ECB: AVDD=2.8 ~ 3.6V, DTVDD = 1.6 ~ 2.0V)

Parameter		Symbol	min	typ	max	Unit
ADC Digital Filter (Decimation LPF):						
Passband (Note 29)	±0.16dB	PB	0	-	18.8	kHz
	–0.66dB		-	21.1	-	kHz
	–1.1dB		-	21.7	-	kHz
	–6.9dB		-	24.1	-	kHz
Stopband (Note 29)		SB	28.4	-	-	kHz
Passband Ripple		PR	-	-	±0.16	dB
Stopband Attenuation		SA	73	-	-	dB
Group Delay (Note 30)		GD	-	17	-	1/fs
Group Delay Distortion		ΔGD	-	0	-	μs
ADC Digital Filter (HPF): HPFC1-0 bits = "00"						
Frequency Response (Note 29)	–3.0dB	FR	-	3.7	-	Hz
	–0.5dB		-	10.9	-	Hz
	–0.1dB		-	23.9	-	Hz
DAC Digital Filter (LPF):						
Passband (Note 29)	±0.05dB	PB	0	-	21.8	kHz
	–6.0dB		-	24	-	kHz
Stopband (Note 29)		SB	26.2	-	-	kHz
Passband Ripple		PR	-	-	±0.05	dB
Stopband Attenuation		SA	54	-	-	dB
Group Delay (Note 30)		GD	-	22	-	1/fs
DAC Digital Filter (LPF) + SCF:						
Frequency Response: 0 ~ 20.0kHz		FR	-	±1.0	-	dB

Note 29. The passband and stopband frequencies scale with fs (sampling frequency). Each response refers to that of 1kHz. For example, it is 0.454 x fs (ADC) when PB=21.7kHz (@–1.1dB).

Note 30. A calculating delay time which is induced by digital filtering. This time is from the input of an analog signal to the setting of 24-bit data of both channels to the ADC output register. For the DAC, this time is from setting the 24-bit data of a channel from the input register to the output of analog signal. For the signal through the programmable filters (1st order HPF + 1st order LPF + 4-band Equalizer + ALC + 1-band Equalizer), the group delay is increased by 4/fs from the value above in both recording and playback modes if there is no phase change by the IIR filter.

DC CHARACTERISTICS

(Ta =25°C; fs=48kHz, AK4958EG: AVDD=2.8 ~ 3.6V, DVDD = 1.6 ~ 2.0V, TVDD = 1.6 or (DVDD-0.2)~ 3.6V; AK4958ECB: AVDD=2.8~3.6V, DTVDD= 1.6~2.0V)

Parameter	Symbol	min	typ	max	Unit
Audio Interface & Serial µP Interface (CDTIO/CAD0, CSN/SDA, CCLK/SCL, I2C, PDN, BICK, LRCK, SDTI, MCKI pins)					
High-Level Input Voltage					
(Except I2C pin, TVDD ≥ 2.2V)	VIH	70%TVDD	-	-	V
(Except I2C pin, TVDD < 2.2V)	VIH	80%TVDD	-	-	V
(I2C pin)	VIH1	70%AVDD	-	-	V
Low-Level Input Voltage					
(Except I2C pin, TVDD ≥ 2.2V)	VIL	-	-	30%TVDD	V
(Except I2C pin, TVDD < 2.2V)	VIL	-	-	20%TVDD	V
(I2C pin)	VIL1	-	-	30%AVDD	V
Input Leakage Current	Iin1	-	-	±10	µA
Audio Interface & Serial µP Interface (CDTIO, SDA MCKO, BICK, LRCK, SDTO pins Output)					
High-Level Output Voltage (Iout = −80µA)	VOH	TVDD−0.2	-	-	V
Low-Level Output Voltage					
(Except SDA pin : Iout = 80µA)	VOL1	-	-	0.2	V
(SDA pin, 2.0V ≤ TVDD ≤ 3.6V: Iout = 3mA)	VOL2	-	-	0.4	V
(SDA pin, 1.6V ≤ TVDD < 2.0V: Iout = 3mA)	VOL2	-	-	20%TVDD	V
Digital Microphone Interface (DMDAT pin Input ; DMIC bit = "1")					
High-Level Input Voltage	VIH2	65%AVDD	-	-	V
Low-Level Input Voltage	VIL2	-	-	35%AVDD	V
Input Leakage Current	Iin2	-	-	±10	µA
Digital Microphone Interface (DMCLK pin Output ; DMIC bit = "1")					
High-Level Output Voltage (Iout=−80µA)	VOH3	AVDD-0.4	-	-	V
Low-Level Output Voltage (Iout= 80µA)	VOL3	-	-	0.4	V

Note 31. TVDD means DTVDD for the AK4958ECB.

Note 32. The external pull-up resistors at the SDA and SCL pins should be connected to the voltage that is TVDD (DTVDD) or more and 6V or less.

SWITCHING CHARACTERISTICS

(Ta =25°C; fs=48kHz; C_L=20pF; AK4958ECB: AVDD=2.8 ~ 3.6V, DVDD = 1.6 ~ 2.0V, TVDD = 1.6 or (DVDD-0.2)~ 3.6V, AK4958ECB: AVDD=2.8 ~ 3.6V, DTVDD = 1.6 ~ 2.0V)

Parameter		Symbol	min	typ	max	Unit
PLL Master Mode (PLL Reference Clock = MCKI pin)						
MCKI Input Timing						
Frequency	PLL3-0 bits = "0100"	fCLK	-	11.2896	27	MHz
	PLL3-0 bits = "0110"	fCLK	-	12	-	MHz
	PLL3-0 bits = "0111"	fCLK	-	24	-	MHz
	PLL3-0 bits = "1100"	fCLK	-	13.5	-	MHz
	PLL3-0 bits = "1101"	fCLK	-	27	-	MHz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	s
Pulse Width High		tCLKH	0.4/fCLK	-	-	s
MCKO Output Timing						
Frequency	PS1-0 bits = "00"	fMCK	-	256fs	-	Hz
	PS1-0 bits = "01"	fMCK	-	128fs	-	Hz
	PS1-0 bits = "10"	fMCK	-	64fs	-	Hz
	PS1-0 bits = "11" (Note 33)	fMCK	-	512fs	-	Hz
Duty Cycle		dMCK	40	50	60	%
LRCK Output Timing						
Frequency		fs	-	Table 6	-	Hz
Duty Cycle		Duty	-	50	-	%
BICK Output Timing						
Period	BCKO bit = "0"	tBCK	-	32fs	-	Hz
	BCKO bit = "1"	tBCK	-	64fs	-	Hz
Duty Cycle		dBCK	-	50	-	%
PLL Slave Mode (PLL Reference Clock = MCKI pin)						
MCKI Input Timing						
Frequency		fCLK	11.2896	-	27	MHz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	s
Pulse Width High		tCLKH	0.4/fCLK	-	-	s
MCKO Output Timing						
Frequency	PS1-0 bits = "00"	fMCK	-	256fs	-	Hz
	PS1-0 bits = "01"	fMCK	-	128fs	-	Hz
	PS1-0 bits = "10"	fMCK	-	64fs	-	Hz
	PS1-0 bits = "11" (Note 33)	fMCK	-	512fs	-	Hz
Duty Cycle		dMCK	40	50	60	%
LRCK Input Timing						
Frequency		fs	-	Table 6	-	Hz
Duty Cycle		Duty	45	-	55	%
BICK Input Timing						
Frequency		tBCK	32fs	-	64fs	Hz
Pulse Width Low		tBCKL	0.4 x tBCK	-	-	s
Pulse Width High		tBCKH	0.4 x tBCK	-	-	s

Note 33. When MCKO=512fs, fs=8, 11.025, 12, 16, 32kHz are not available.

Parameter			Symbol	min	typ	max	Unit
PLL Slave Mode (PLL Reference Clock = BICK pin)							
LRCK Input Timing							
	Frequency	PLL3-0 bits = "0010"	fs	-	fBCK/32	-	Hz
		PLL3-0 bits = "0011"	fs	-	fBCK/64	-	Hz
	Duty		Duty	45	-	55	%
BICK Input Timing							
	Frequency	PLL3-0 bits = "0010"	tBCK	0.2352	-	1.536	MHz
		PLL3-0 bits = "0011"	tBCK	0.4704	-	3.072	MHz
	Pulse Width Low		tBCKL	0.4/tBCK	-	-	s
	Pulse Width High		tBCKH	0.4/tBCK	-	-	s
External Slave Mode							
MCKI Input Timing							
	Frequency	FS1-0 bits = "00"	fCLK	-	256fs	-	Hz
		FS1-0 bits = "01"	fCLK	-	1024fs	-	Hz
		FS1-0 bits = "10" or "11"	fCLK	-	512fs	-	Hz
	Pulse Width Low		tCLKL	0.4/fCLK	-	-	s
	Pulse Width High		tCLKH	0.4/fCLK	-	-	s
LRCK Input Timing							
	Frequency	FS1-0 bits = "00"	fs	7.35	-	48	kHz
		FS1-0 bits = "01"	fs	7.35	-	13	kHz
		FS1-0 bits = "10"	fs	7.35	-	24	kHz
		FS1-0 bits = "00"	fs	7.35	-	48	kHz
	Duty		Duty	45	-	55	%
BICK Input Timing							
	Frequency		tBCK	32fs	-	64fs	Hz
	Pulse Width Low		tBCKL	130	-	-	ns
	Pulse Width High		tBCKH	130	-	-	ns
External Master Mode							
MCKI Input Timing							
	Frequency	256fs (FS1-0 bits = "00")	fCLK	1.8816	-	12.288	MHz
		512fs (FS1-0 bits = "10")	fCLK	3.7632	-	13.312	MHz
		512fs (FS1-0 bits = "11")	fCLK	3.7632	-	24.576	MHz
		1024fs (FS1-0 bits = "01")	fCLK	7.5264	-	13.312	MHz
	Pulse Width Low		tCLKL	0.4/fCLK	-	-	s
	Pulse Width High		tCLKH	0.4/fCLK	-	-	s
LRCK Output Timing							
	Frequency	FS1-0 bits = "00"	fs	-	fCLK/256	-	kHz
		FS1-0 bits = "01"	fs	-	fCLK/1024	-	kHz
		FS1-0 bits = "10" or "11"	fs	-	fCLK/512	-	kHz
	Duty Cycle		Duty	-	50	-	%
BICK Output Timing							
	Frequency	BCKO bit = "0"	tBCK	-	32fs	-	Hz
		BCKO bit = "1"	tBCK	-	64fs	-	Hz
	Duty Cycle		dBCK	-	50	-	%

Parameter	Symbol	min	typ	max	Unit
Audio Interface Timing					
Master Mode					
BICK "↓" to LRCK Edge (Note 34)	tMBLR	–40	-	40	ns
LRCK Edge to SDTO (MSB) (Except I²S mode)	tLRD	–70	-	70	ns
BICK "↓" to SDTO	tBSD	–70	-	70	ns
SDTI Hold Time	tSDH	50	-	-	ns
SDTI Setup Time	tSDS	50	-	-	ns
Slave Mode					
LRCK Edge to BICK "↑" (Note 34)	tLRB	50	-	-	ns
BICK "↑" to LRCK Edge (Note 34)	tBLR	50	-	-	ns
LRCK Edge to SDTO (MSB) (Except I²S mode)	tLRD	-	-	80	ns
BICK "↓" to SDTO	tBSD	-	-	80	ns
SDTI Hold Time	tSDH	50	-	-	ns
SDTI Setup Time	tSDS	50	-	-	ns
Control Interface Timing (3-wire Mode) (Note 35)					
CCLK Period	tCCK	200	-	-	ns
CCLK Pulse Width Low	tCCKL	80	-	-	ns
Pulse Width High	tCCKH	80	-	-	ns
CDTIO Setup Time	tCDS	40	-	-	ns
CDTIO Hold Time	tCDH	40	-	-	ns
CSN "H" Time	tCSW	150	-	-	ns
CSN Edge to CCLK "↑" (Note 36)	tCSS	50	-	-	ns
CCLK "↑" to CSN Edge (Note 36)	tCSH	50	-	-	ns
CCLK "↓" to CDTIO (at Read Command)	tDCD	-	-	70	ns
CSN "↑" to CDTIO (Hi-Z) (at Read Command)(Note 38)	tCCZ	-	-	70	ns
Control Interface Timing (I²C Bus Mode):					
SCL Clock Frequency	fSCL	-	-	400	kHz
Bus Free Time Between Transmissions	tBUF	1.3	-	-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6	-	-	µs
Clock Low Time	tLOW	1.3	-	-	µs
Clock High Time	tHIGH	0.6	-	-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6	-	-	µs
SDA Hold Time from SCL Falling (Note 39)	tHD:DAT	0	-	-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1	-	-	µs
Rise Time of Both SDA and SCL Lines	tR	-	-	0.3	µs
Fall Time of Both SDA and SCL Lines	tF	-	-	0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6	-	-	µs
Capacitive Load on Bus	Cb	-	-	400	pF
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0	-	50	ns

Note 34. BICK rising edge must not occur at the same time as LRCK edge.
Note 35. The AK4958ECB does not support 3-wire Mode.
Note 36. CCLK rising edge must not occur at the same time as CSN edge.
Note 37. I²C-bus is a trademark of NXP B.V.
Note 38. It is the time of 10% potential change of the CDTIO pin when R_L=1kΩ (pull-up or TVDD).
Note 39. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.

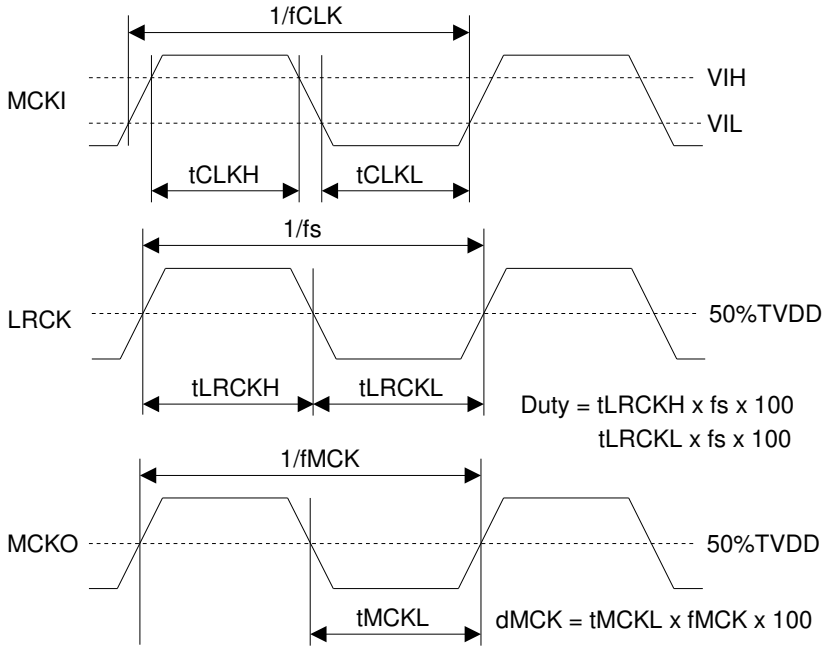
Parameter		Symbol	min	typ	max	Unit
Digital Audio Interface Timing; C_L=100pF						
DMCLK Output Timing						
Period		tSCK	-	1/(64fs)	-	s
Rising Time		tSRise	-	-	10	ns
Falling Time		tSFall	-	-	10	ns
Duty Cycle		dSCK	40	50	60	%
Audio Interface Timing						
DMDAT Setup Time		tDSDS	50	-	-	ns
DMDAT Hold Time		tDSDH	0	-	-	ns
Power-down & Reset Timing						
PDN Accept Pulse Width	(Note 40)	tAPD	200	-	-	ns
PDN Reject Pulse Width	(Note 40)	tRPD	-	-	50	ns
PMADL or PMADR "↑" to SDTO valid	(Note 41)					
ADRST1-0 bits ="00"		tPDV	-	1059	-	1/fs
ADRST1-0 bits ="01"		tPDV	-	267	-	1/fs
ADRST1-0 bits ="10"		tPDV	-	531	-	1/fs
ADRST1-0 bits ="11"		tPDV	-	135	-	1/fs
VCOM Voltage						
Rising Time	(Note 42)	tRVCM	-	0.6	2.0	ms

Note 40. The AK4958 can be reset by the PDN pin = "L". The PDN pin must be held "L" for more than 200ns for a certain reset. The AK4958 is not reset by the "L" pulse less than 50ns.

Note 41. This is the count of LRCK "↑" from the PMADL or PMADR bit = "1".

Note 42. All analog blocks including PLL block are powered up after the VCOM voltage (VCOM pin) rises up. An external capacitor of the VCOM pin is 2.2μF and the REGFIL pin is 2.2μF. The capacitance variation should be ±50%.

■ Timing Diagram



Note 43. MCKO is not available at EXT Master mode.
Figure 5. Clock Timing (PLL/EXT Master mode)

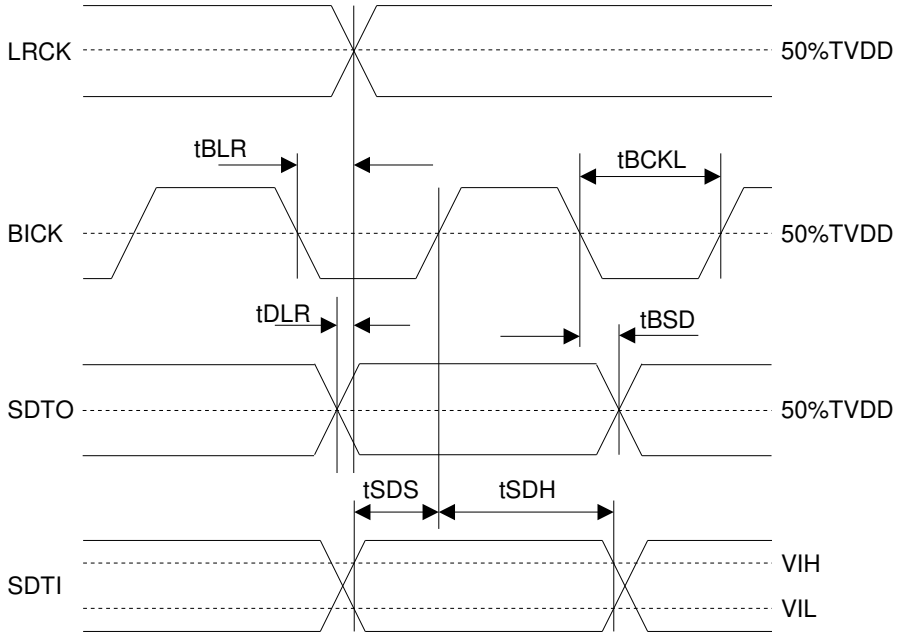


Figure 6. Audio Interface Timing (PLL/EXT Master mode)

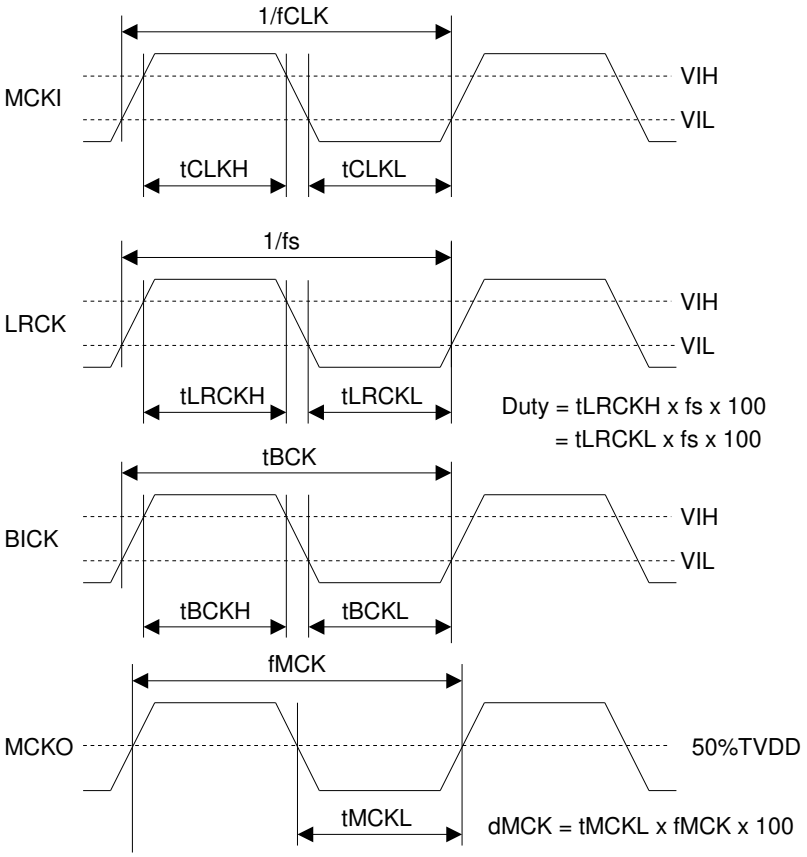


Figure 7. Clock Timing (PLL Slave mode; PLL Reference Clock = MCKI pin)

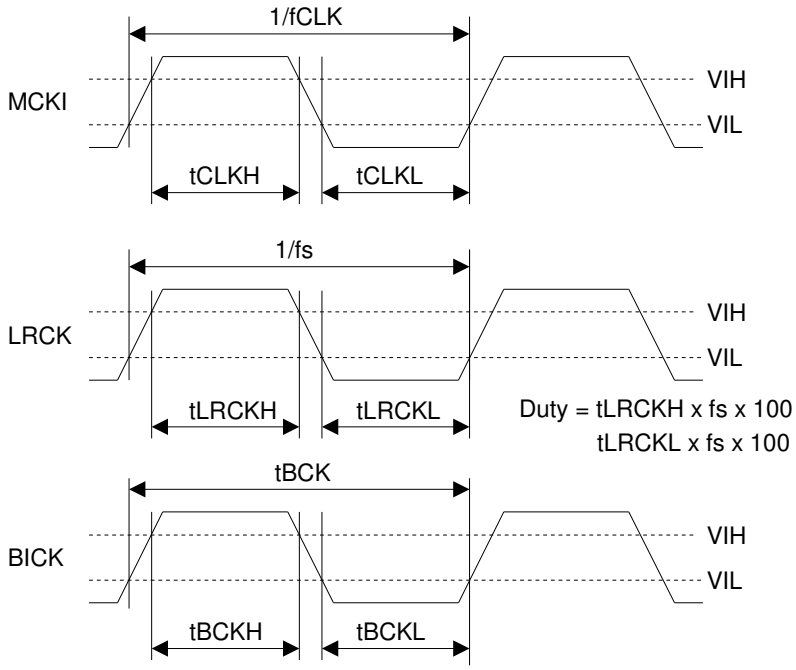


Figure 8. Clock Timing (EXT Slave mode)

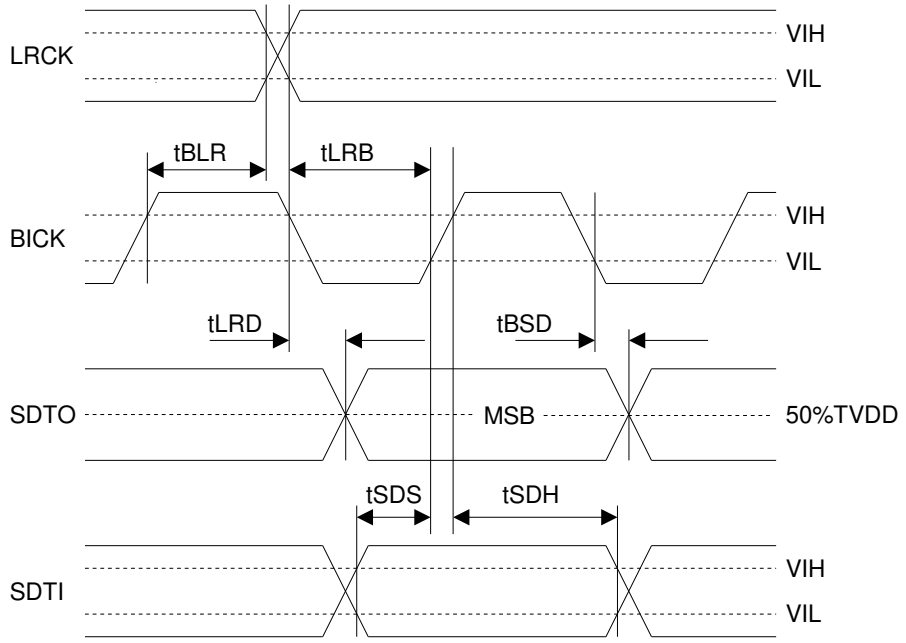


Figure 9. Audio Interface Timing (PLL/EXT Slave mode)

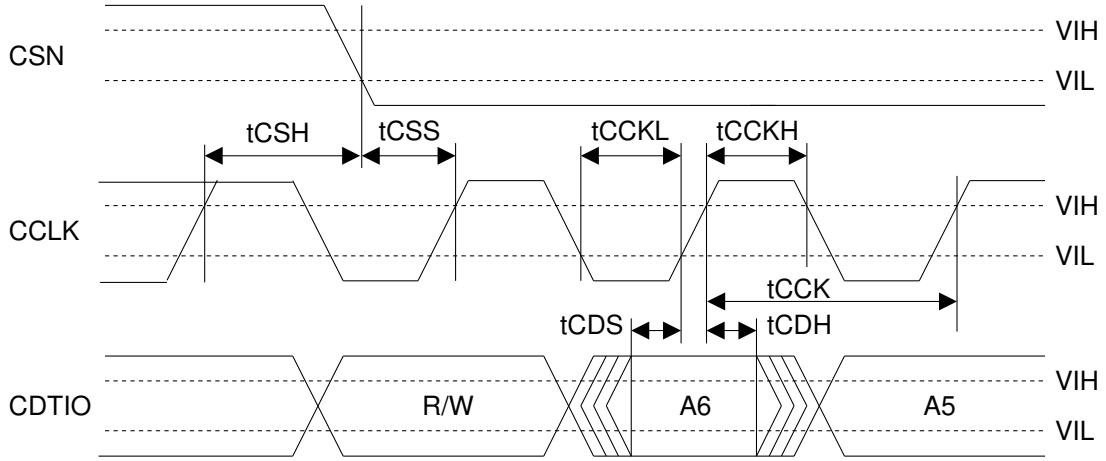


Figure 10. WRITE Command Input Timing

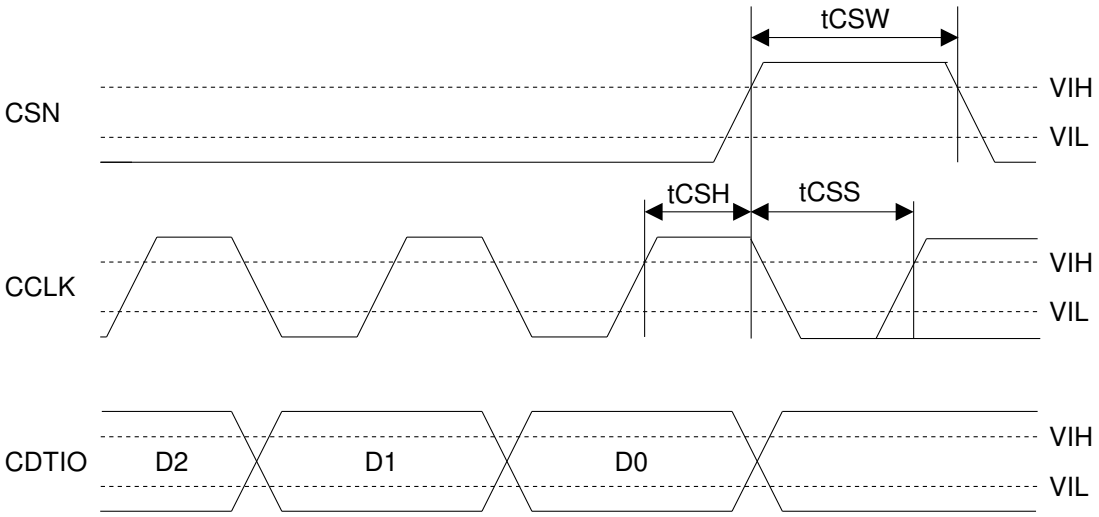


Figure 11. WRITE Data Input Timing

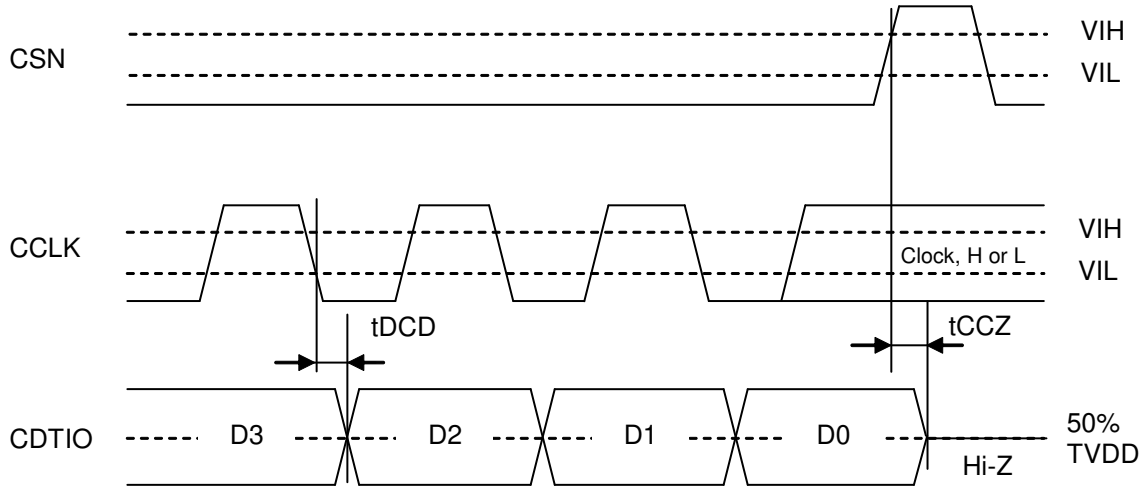


Figure 12. Read Data Output Timing

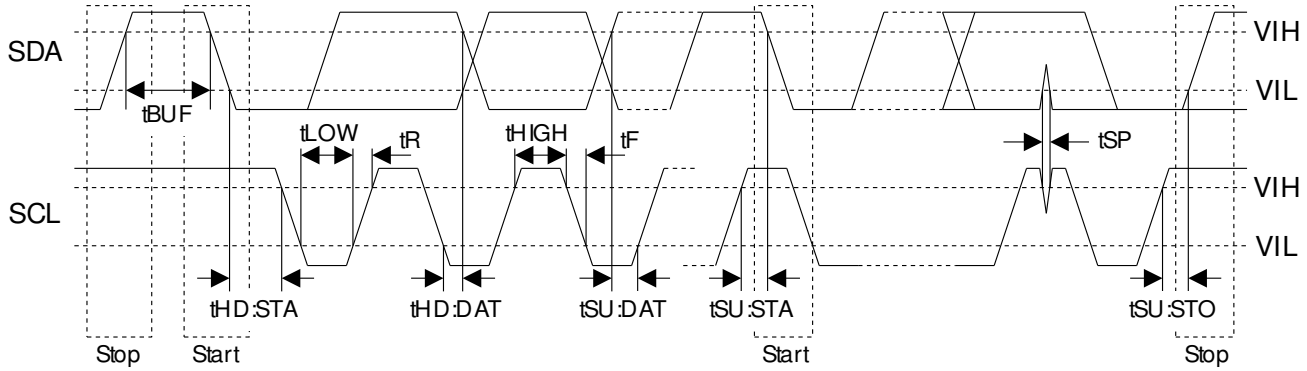
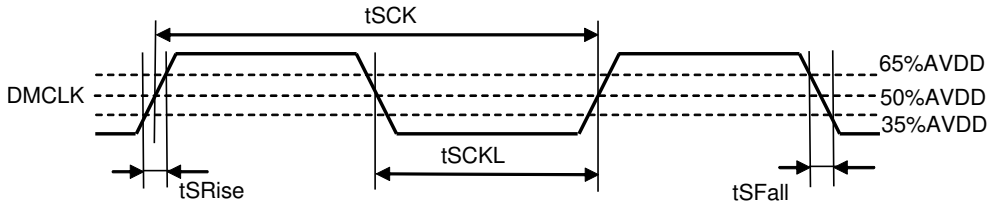


Figure 13. I^{2}C Bus Mode Timing



dSCK = 100 x tSCKL / tSCK

Figure 14. DMCLK Clock Timing

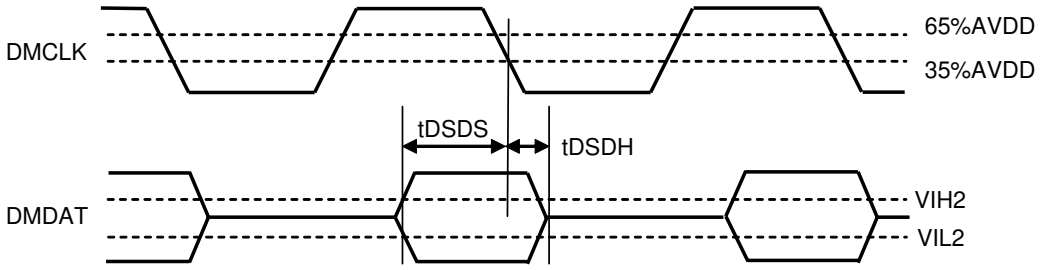


Figure 15. Audio Interface Timing (DCLKP bit = "1")

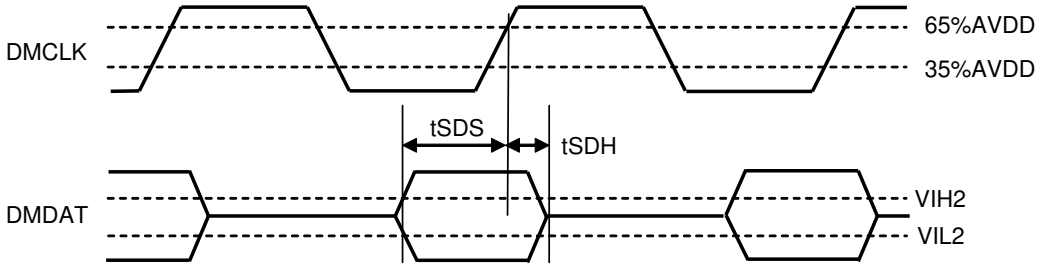


Figure 16. Audio Interface Timing (DCLKP bit = "0")

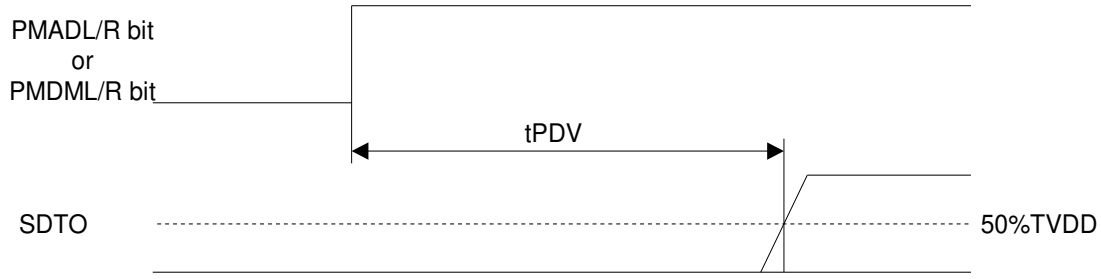


Figure 17. Power Down & Reset Timing 1

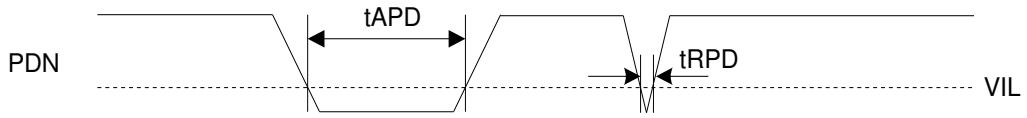


Figure 18. Power Down & Reset Timing 2

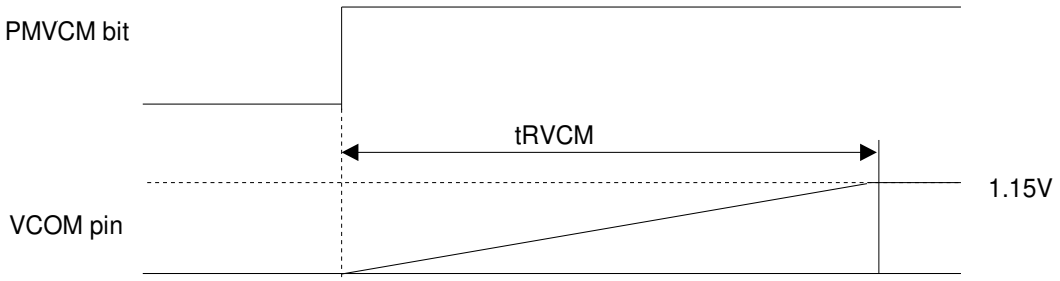


Figure 19. VCOM Rising Timing

OPERATION OVERVIEW

■ System Clock

There are the following five clock modes to interface with external devices (Table 1, Table 2).

Mode	PMPLL bit	M/S bit	PLL3-0 bits	Figure
PLL Master Mode (Note 44)	1	1	Table 4	Figure 20
PLL Slave Mode 1 (PLL Reference Clock: MCKI pin)	1	0	Table 4	Figure 21
PLL Slave Mode 2 (PLL Reference Clock: LRCK or BICK pin)	1	0	Table 4	Figure 22
EXT Slave Mode	0	0	x	Figure 23
EXT Master Mode	0	1	x	Figure 24

Note 44. If M/S bit = "1", PMPLL bit = "0" and MCKO bit = "1" during the setting of PLL Master Mode, the invalid clocks are output from MCKO, BICK and LRCK pins.

Table 1. Clock Mode Setting (x: Don't care)

Mode	MCKO bit	MCKO pin	MCKI pin	BICK pin	LRCK pin
PLL Master Mode	0	L	Selected by PLL3-0 bits	Output (Selected by BCKO bit)	Output (1fs)
	1	Selected by PS1-0 bits			
PLL Slave Mode 1 (PLL Reference Clock: MCKI pin)	0	L	Selected by PLL3-0 bits	Input (≥ 32fs)	Input (1fs)
	1	Selected by PS1-0 bits			
PLL Slave Mode 2 (PLL Reference Clock: BICK pin)	0	L	GND	Input (≥ 32fs)	Input (1fs)
	1	Not Available			
EXT Slave Mode	0	L	Selected by FS3-0 bits	Input (≥ 32fs)	Input (1fs)
	1	Not Available			
EXT Master Mode	0	L	Selected by FS1-0 bits	Output (Selected by BCKO bit)	Output (1fs)
	1	Not Available			

Note 45. When M/S bit = "1" and MCKI is input, LRCK and BICK are output even if PMDAC=PMADL= PMADR bits = "0".

Table 2. Clock pins state in Clock Mode

■ Master Mode/Slave Mode

The M/S bit selects either master or slave mode. M/S bit = "1" selects master mode and "0" selects slave mode. When the AK4958 is in power-down mode (PDN pin = "L") and when exits reset state, the AK4958 is in slave mode. After exiting reset state, the AK4958 goes to master mode by changing M/S bit to "1".

When the AK4958 is in master mode, the LRCK and BICK pins are a floating state until M/S bit becomes "1". The LRCK and BICK pins of the AK4958 must be pulled-down or pulled-up by a resistor (about 100kΩ) externally to avoid the floating state.

M/S bit	Mode	
0	Slave Mode	(default)
1	Master Mode	

Table 3. Select Master/Slave Mode

■ PLL Mode

When PMPLL bit is "1", a fully integrated analog phase locked loop (PLL) circuit generates a clock that is selected by PLL3-0 and FS3-0 bits. The PLL lock times, when the AK4958 is supplied stable clocks after PLL is powered-up (PMPLL bit = "0" → "1") or the sampling frequency is changed, are shown in Table 4.

1) PLL Mode Reference Clock Setting

Mode	PLL3 bit	PLL2 bit	PLL1 bit	PLL0 bit	PLL Reference Clock Input Pin	Input Frequency	PLL Lock Time (max)	
2	0	0	1	0	BICK pin	32fs	2 ms	
3	0	0	1	1	BICK pin	64fs	2 ms	
4	0	1	0	0	MCKI pin	11.2896MHz	5 ms	
6	0	1	1	0	MCKI pin	12MHz	5 ms	
7	0	1	1	1	MCKI pin	24MHz	5 ms	
12	1	1	0	0	MCKI pin	13.5MHz	5 ms	(default)
13	1	1	0	1	MCKI pin	27MHz	5 ms	
Others	Others				N/A			

Table 4. PLL Mode Setting (*fs: Sampling Frequency, N/A: Not Available)

2) Setting of sampling frequency in PLL Mode (PLL reference clock input pin: MCKI pin)
When PLL2 bit is "1" (PLL reference clock input is MCKI pin), the sampling frequency is selected by FS3-0 bits as defined in Table 5.

Mode	FS3 bit	FS2 bit	FS1 bit	FS0 bit	Sampling Frequency (Note 46)	
0	0	0	0	0	8kHz mode	(default)
1	0	0	0	1	12kHz mode	
2	0	0	1	0	16kHz mode	
3	0	0	1	1	24kHz mode	
5	0	1	0	1	11.025kHz mode	
7	0	1	1	1	22.05kHz mode	
10	1	0	1	0	32kHz mode	
11	1	0	1	1	48kHz mode	
15	1	1	1	1	44.1kHz mode	
Others	Others				N/A	

Table 5. Setting of Sampling Frequency at PLL2 bit = "1" and PMPLL bit = "1"
(PLL Reference Clock = MCKI pin), (N/A: Not Available)

Note 46. When the MCKI pin is the PLL reference clock input, the sampling frequency generated by PLL differs from the sampling frequency of mode name in some combinations of MCKI frequency(PLL3-0 bits) and sampling frequency (FS3-0 bits). Refer to Table 6 for the details of sampling frequency. In master mode, LRCK and BICK output frequency correspond to sampling frequencies shown in Table 6. When the BICK pin is the PLL reference clock input, the sampling frequency generated by PLL is the same sampling frequency of mode name.

Input Frequency MCKI[MHz]	Mode Setting by register		Clock Frequency generated by PLL (Note 47)	
	Sampling Frequency Mode (fs mode)	256 * (Sampling Frequency of mode name) [MHz]	Sampling Frequency[kHz]	MCKO at 256fs[MHz]
11.2896	8kHz mode	2.048	8.000000	2.048000
	12kHz mode	3.072	12.000000	3.072000
	16kHz mode	4.096	16.000000	4.096000
	24kHz mode	6.144	24.000000	6.144000
	32kHz mode	8.192	32.000000	8.192000
	48kHz mode	12.288	48.000000	12.288000
	11.025kHz mode	2.8224	11.025000	2.822400
	22.05kHz mode	5.6448	22.050000	5.644800
	44.1kHz mode	11.2896	44.100000	11.289600
12	8kHz mode	2.048	8.000000	2.048000
	12kHz mode	3.072	12.000000	3.072000
	16kHz mode	4.096	16.000000	4.096000
	24kHz mode	6.144	24.000000	6.144000
	32kHz mode	8.192	32.000000	8.192000
	48kHz mode	12.288	48.000000	12.288000
	11.025kHz mode	2.8224	11.024877	2.822368
	22.05kHz mode	5.6448	22.049753	5.644737
	44.1kHz mode	11.2896	44.099507	11.289474
24	8kHz mode	2.048	8.000000	2.048000
	12kHz mode	3.072	12.000000	3.072000
	16kHz mode	4.096	16.000000	4.096000
	24kHz mode	6.144	24.000000	6.144000
	32kHz mode	8.192	32.000000	8.192000
	48kHz mode	12.288	48.000000	12.288000
	11.025kHz mode	2.8224	11.024877	2.822368
	22.05kHz mode	5.6448	22.049753	5.644737
	44.1kHz mode	11.2896	44.099507	11.289474
13.5	8kHz mode	2.048	8.000300	2.048077
	12kHz mode	3.072	12.000451	3.072115
	16kHz mode	4.096	16.000601	4.096154
	24kHz mode	6.144	24.000901	6.144231
	32kHz mode	8.192	32.001202	8.192308
	48kHz mode	12.288	48.001803	12.288462
	11.025kHz mode	2.8224	11.025218	2.822456
	22.05kHz mode	5.6448	22.050436	5.644912
	44.1kHz mode	11.2896	44.100871	11.289823
27	8kHz mode	2.048	8.000300	2.048077
	12kHz mode	3.072	12.000451	3.072115
	16kHz mode	4.096	16.000601	4.096154
	24kHz mode	6.144	24.000901	6.144231
	32kHz mode	8.192	32.001202	8.192308
	48kHz mode	12.288	48.001803	12.288462
	11.025kHz mode	2.8224	11.025218	2.822456
	22.05kHz mode	5.6448	22.050436	5.644912
	44.1kHz mode	11.2896	44.100871	11.289823

Note 47. These values are rounded off to six decimal places.

Table 6. Sampling Frequency and MCKO(256fs) Frequency at PLL mode (Reference clock is MCKI)

3) Setting of sampling frequency in PLL Mode (PLL reference clock input pin: BICK pin)
When PLL2 bit is "0" (PLL reference clock input pin is the BICK pin), the sampling frequency is selected by FS3-2 bits (Table 7).

Mode	FS3 bit	FS2 bit	FS1 bit	FS0 bit	Sampling Frequency Range	
0	0	0	x	x	7.35kHz ≤ fs ≤ 12kHz	(default)
1	0	1	x	x	12kHz < fs ≤ 24kHz	
2	1	0	x	x	24kHz < fs ≤ 48kHz	
Others	Others				N/A	

Table 7. Setting of Sampling Frequency at PLL2 bit = "0" and PMPLL bit = "1" PLL Slave Mode 2 (PLL Reference Clock: BICK pin), (x: Don't care, N/A: Not Available)

■ PLL Unlock State

1) PLL Master Mode (PMPLL bit = "1", M/S bit = "1")

In this mode, LRCK and BICK pins go to "L", and irregular frequency clock is output from the MCKO pin when MCKO bit is "1" before the PLL goes to lock state after PMPLL bit = "0" → "1". If MCKO bit is "0", the MCKO pin outputs "L" (Table 8).

After the PLL is locked, a first period of LRCK and BICK may be invalid clock, but these clocks return to normal state after a period of 1/fs.

The BICK and LRCK pins do not output irregular frequency clocks such as PLL unlock state by setting PMPLL bit to "0". During PMPLL bit = "0", these pins output the same clocks as EXT Master Mode.

PLL State	MCKO pin		BICK pin	LRCK pin
	MCKO bit = "0"	MCKO bit = "1"		
After PMPLL bit "0" → "1"	"L" Output	Invalid	"L" Output	"L" Output
PLL Unlock (except the case above)	"L" Output	Invalid	Invalid	Invalid
PLL Lock	"L" Output	Table 10	Table 11	1fs Output

Table 8. Clock Operation at PLL Master Mode (PMPLL bit = "1", M/S bit = "1")

2) PLL Slave Mode (PMPLL bit = "1", M/S bit = "0")

In this mode, an invalid clock is output from the MCKO pin before the PLL goes to lock state after PMPLL bit = "0" → "1". Then, the clock selected by Table 10 is output from the MCKO pin when PLL is locked. ADC and DAC output invalid data when the PLL is unlocked. The DAC outputs can be muted by setting DACL and DACS bits to "0".

PLL State	MCKO pin	
	MCKO bit = "0"	MCKO bit = "1"
After PMPLL bit "0" → "1"	"L" Output	Invalid
PLL Unlock (except the case above)	"L" Output	Invalid
PLL Lock	"L" Output	Output

Table 9. Clock Operation at PLL Slave Mode (PMPLL bit = "0", M/S bit = "0")

■ PLL Master Mode (PMPLL bit = "1", M/S bit = "1")

When an external clock (11.2896MHz, 12MHz, 13.5MHz, 24MHz or 27MHz) is input to the MCKI pin, the internal PLL circuit generates MCKO, BICK and LRCK clocks. The MCKO output frequency is selected by PS1-0 bits (Table 10) and switched on and off by MCKO bit. The BICK output frequency is selected between 32fs or 64fs, by BCKO bit (Table 11).

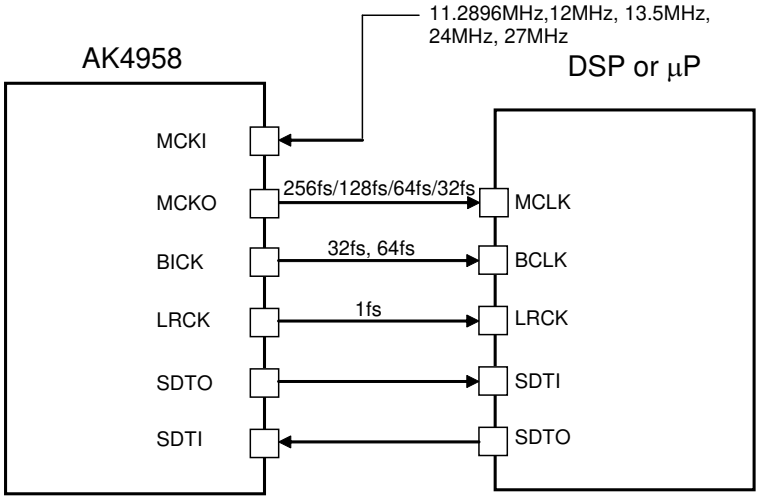


Figure 20. PLL Master Mode

Mode	PS1 bit	PS0 bit	MCKO pin	
0	0	0	256fs	(default)
1	0	1	128fs	
2	1	0	64fs	
3	1	1	512fs (Note 48)	

Note 48. fs=8, 11.025, 12, 16 and 32kHz cannot be used when MCKO = 512fs.

Table 10. MCKO Output Frequency (PLL Mode, MCKO bit = "1")

BCKO bit	BICK Output Frequency	
0	32fs	(default)
1	64fs	

Table 11. BICK Output Frequency at Master Mode

■ PLL Slave Mode (PMPLL bit = "1", M/S bit = "0")

A reference clock of PLL is selected among the input clocks to the MCKI or BICK pins. The required clock for the AK4958 is generated by an internal PLL circuit. Input frequency is selected by PLL3-0 bits (Table 4).

a) PLL reference clock: MCKI pin

The BICK and LRCK inputs must be synchronized with MCKO output. The phase between MCKO and LRCK is not important. The MCKO pin outputs the frequency selected by PS1-0 bits (Table 10) and the output is enabled by MCKO bit. Sampling frequency can be selected by FS3-0 bits (Table 5).

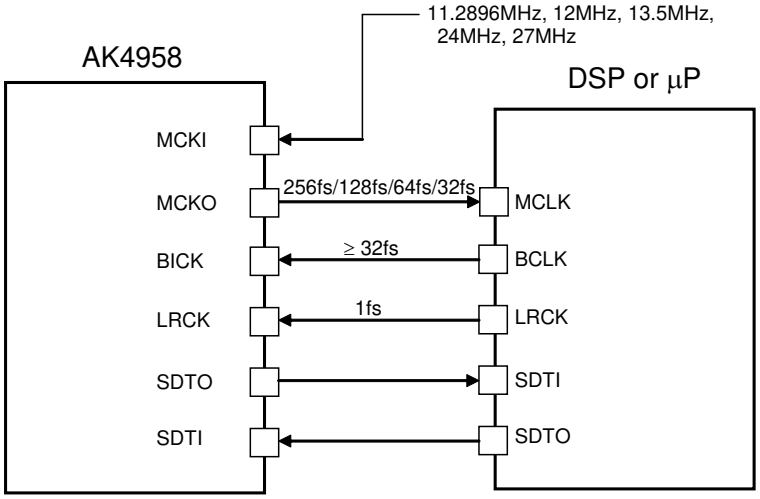


Figure 21. PLL Slave Mode 1 (PLL Reference Clock: MCKI pin)

b) PLL reference clock: BICK pin

The sampling frequency corresponds to a range from 7.35kHz to 48kHz by changing FS3-0 bits (Table 7).

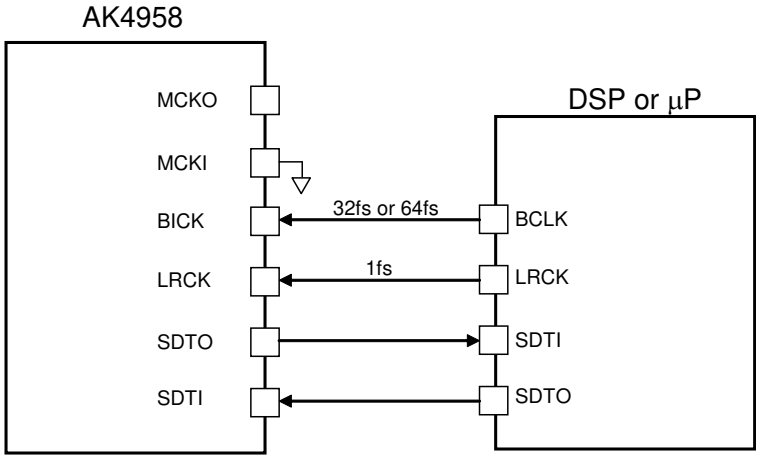


Figure 22. PLL Slave Mode 2 (PLL Reference Clock: BICK pin)

■ EXT Slave Mode (PMPLL bit = "0", M/S bit = "0")

When PMPLL bit is "0", the AK4958 becomes EXT mode. Master clock can be input to the internal ADC and DAC directly from the MCKI pin without internal PLL circuit operation. This mode is compatible with I/F of a normal audio CODEC. The external clocks required to operate this mode are MCKI (256fs, 512fs or 1024fs), LRCK (fs) and BICK (≥32fs). The master clock (MCKI) must be synchronized with LRCK. The phase between these clocks is not important. The input frequency of MCKI is selected by FS1-0 bits (Table 12).

Mode	FS3-2 bits	FS1 bit	FS0 bit	MCKI Input Frequency	Sampling Frequency Range	
0	x	0	0	256fs	7.35kHz ~ 48kHz	(default)
1	x	0	1	1024fs	7.35kHz ~ 13kHz	
2	x	1	0	512fs	7.35kHz ~ 26kHz	
3	x	1	1	512fs	7.35kHz ~ 48kHz	

(x: Don't care)

Table 12. MCKI Frequency at EXT Slave Mode (PMPLL bit = "0", M/S bit = "0")

The S/N of the DAC at low sampling frequencies is worse than at high sampling frequencies due to out-of-band noise. The out-of-band noise can be reduced by using higher frequency of the master clock. The S/N of the DAC output through LOUT/ROUT pins is shown in Table 13.

MCKI	S/N (fs=8kHz, 20kHzLPF + A-weighted)
Mode0: 256fs Mode3: 512fs	80dB
Mode2: 512fs	92dB
Mode1: 1024fs	92dB

Table 13. Relationship between MCKI and S/N of LOUT/ROUT pins

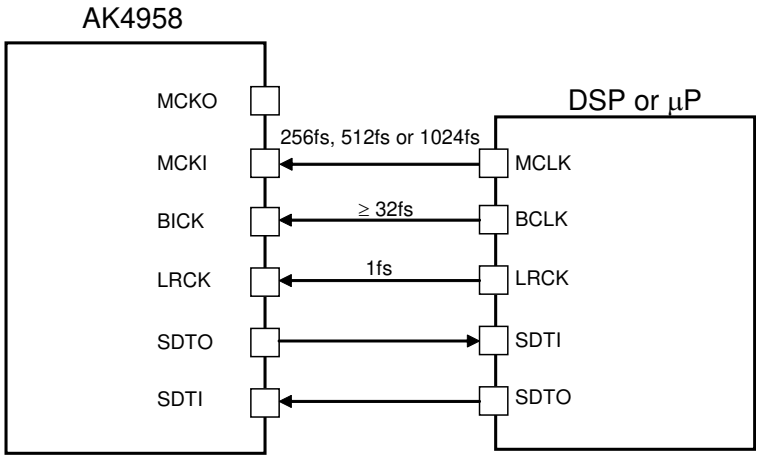


Figure 23. EXT Slave Mode

■ EXT Master Mode (PMPLL bit = “0”, M/S bit = “1”)

The AK4958 becomes EXT Master Mode by setting PMPLL bit = “0” and M/S bit = “1”. Master clock can be input to the internal ADC and DAC directly from the MCKI pin without the internal PLL circuit operation. The external clock required to operate the AK4958 is MCKI (256fs, 512fs or 1024fs). The input frequency of MCKI is selected by FS1-0 bits (Table 14).

Mode	FS3-2 bits	FS1 bit	FS0 bit	MCKI Input Frequency	Sampling Frequency Range	
0	x	0	0	256fs	7.35kHz ~ 48kHz	(default)
1	x	0	1	1024fs	7.35kHz ~ 13kHz	
2	x	1	0	512fs	7.35kHz ~ 26kHz	
3	x	1	1	512fs	7.35kHz ~ 48kHz	

Table 14. MCKI Frequency at EXT Master Mode (PMPLL bit = “0”, M/S bit = “1”) (x: Don’t care)

The S/N of the DAC at low sampling frequencies is worse than at high sampling frequencies due to out-of-band noise. The out-of-band noise can be reduced by using higher frequency of the master clock. The S/N of the DAC output through LOUT/ROUT pins is shown in Table 15.

MCKI	S/N (fs=8kHz, 20kHzLPF + A-weighted)
Mode0: 256fs Mode3: 512fs	80dB
Mode2: 512fs	92dB
Mode1: 1024fs	92dB

Table 15. Relationship between MCKI and S/N of LOUT/ROUT pins

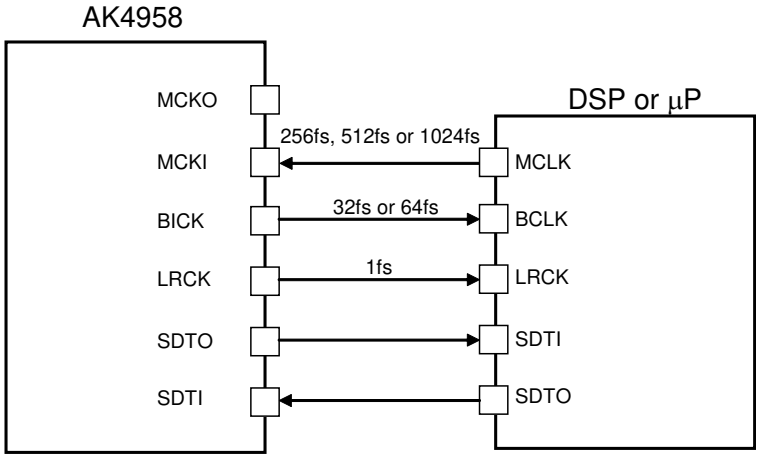


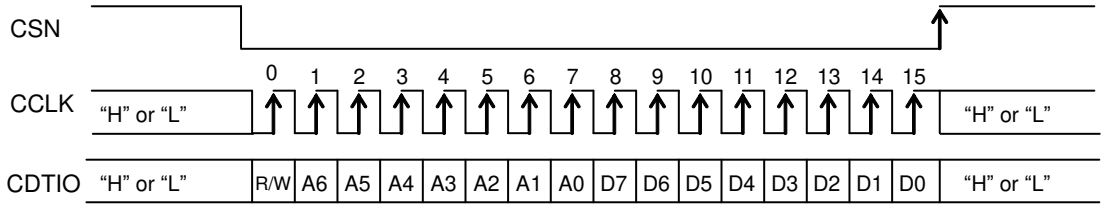
Figure 24. EXT Master Mode

BCKO bit	BICK Output Frequency	
0	32fs	(default)
1	64fs	

Table 16. BICK Output Frequency at Master Mode

■ System Reset

Upon power-up, the AK4958 must be reset by bringing the PDN pin = "L". This reset is released when a dummy command is input after the PDN pin = "H". This ensures that all internal registers reset to their initial value. Dummy command is executed by writing all "0" to the register address 00H. It is recommended to set the PDN pin to "L" before power up the AK4958.



R/W: READ/WRITE ("1": WRITE)
A6-A0: Register Address (00H)
D7-D0: Control data (Input), (00H)

Figure 25. Dummy Command in 3-wire Serial Mode

In I^2C mode, the AK4958 does not return an ACK after receiving a slave address by a dummy command as shown in Figure 26. Therefore, the slave address needs to be sent twice if the I^2C transmitting stops after the first slave address. In the actual case, initializing cycle starts by 16 SCL clocks during the PDN pin = "H" regardless of the SDA line. Executing a write or read command to the other device that is connected to the same I^2C-bus also resets the AK4958.

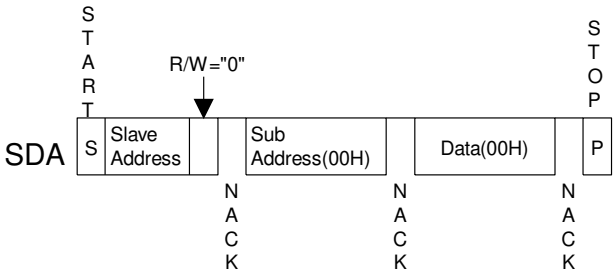


Figure 26. Dummy Command in I^2C-bus Mode

The ADC starts an initialization cycle if the one of PMADL or PMADR is set to "1" when both of the PMADL and PMADR bits are "0". The initialization cycle is set by ADRST1-0 bits (Table 17). During the initialization cycle, the ADC digital data outputs of both channels are forced to "0" in 2's complement. The ADC output reflects the analog input signal after the initialization cycle is finished. When using a digital microphone (PMDML/R bit ="0" → "1"), the initialization cycle is the same as ADC's.

(Note) The initial data of ADC has offset data that depends on microphones and the cut-off frequency of HPF. If this offset is not small, make initialization cycle longer by setting ADRST1-0 bits or do not use the first data of ADC outputs.

	Initialize Cycle				
ADRST1-0 bits	Cycle	fs = 8kHz	fs = 16kHz	fs = 48kHz	
00	1059/fs	132.4ms	66.2ms	22ms	(default)
01	267/fs	33.4ms	16.7ms	5.6ms	
10	531/fs	66.4ms	33.2ms	11.1ms	
11	135/fs	16.9ms	8.4ms	2.8ms	

Table 17. ADC Initialization Cycle

The DAC is initialized by setting PMDAC bit "0" → "1". The initialization cycle is 2/fs. Therefore, the DAC outputs signals after group delay period and 2/fs when power up the device.

(Note) Normally, this group delay period or 2/fs initialization cycle mentioned above is absorbed by power-up time of amplifiers after the DAC (Lineout-amp and SPK-amp).

■ Audio Interface Format

Four types of data formats are available and selected by setting the DIF1-0 bits (Table 18). In all modes, the serial data is MSB first, 2's complement format. Audio interface formats are supported in both master and slave modes. LRCK and BICK are output from the AK4958 in master mode, but must be input to the AK4958 in slave mode. The SDTO is clocked out on the falling edge ("↓") of BICK and the SDTI is latched on the rising edge ("↑") of BICK.

Mode	DIF1 bit	DIF0 bit	SDTO (ADC)	SDTI (DAC)	BICK	Figure	
0	0	0	24bit MSB justified	24bit LSB justified	≥ 48fs	Figure 27	
1	0	1	24bit MSB justified	16bit LSB justified	≥ 32fs	Figure 28	
2	1	0	24bit MSB justified	24bit MSB justified	≥ 48fs	Figure 29	(default)
3	1	1	I^2S Compatible	I^2S Compatible	=32fs or ≥ 48fs	Figure 30	

Table 18. Audio Interface Format

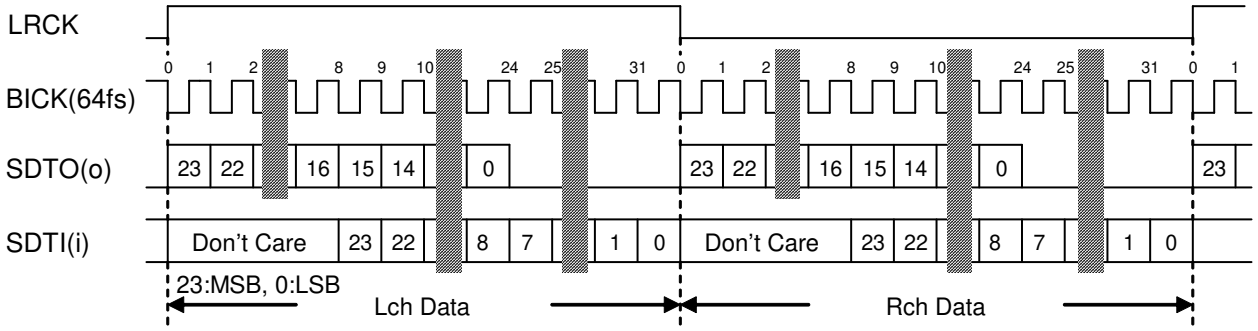


Figure 27. Mode 0 Timing

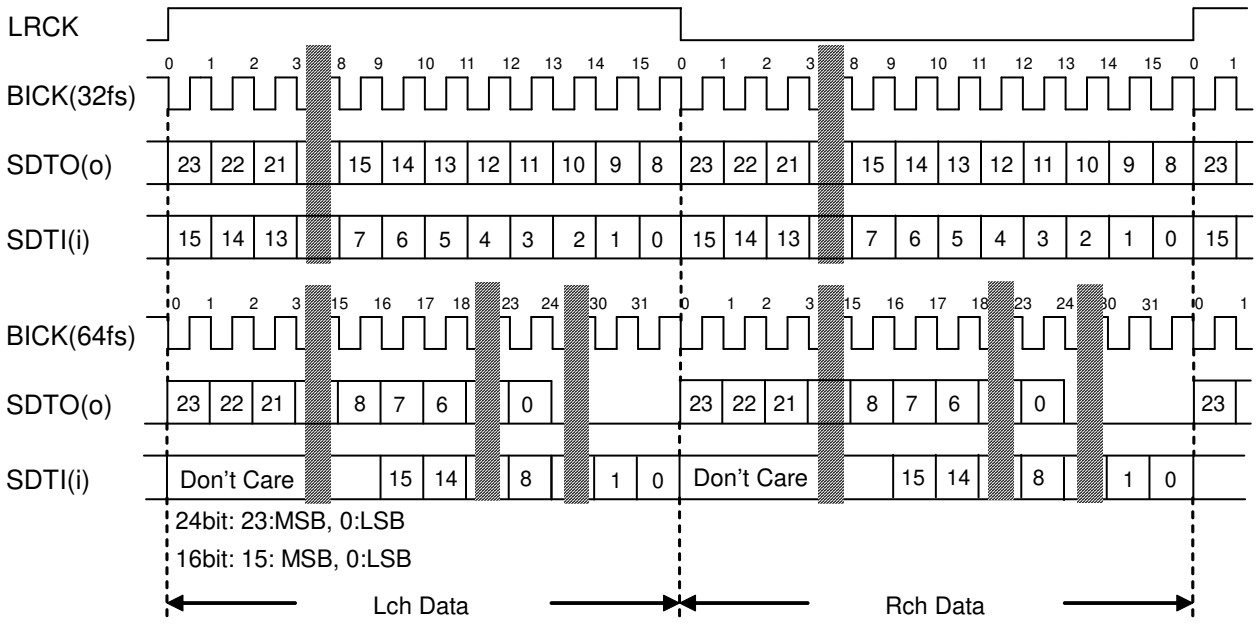


Figure 28. Mode 1 Timing

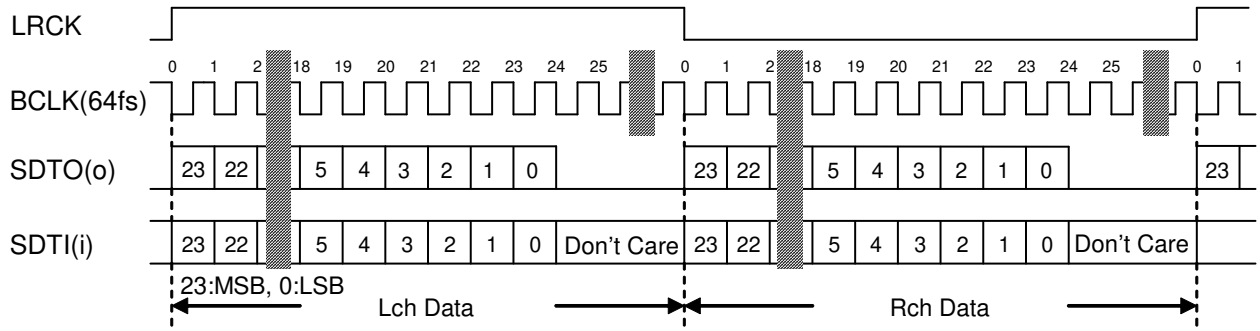


Figure 29. Mode 2 Timing

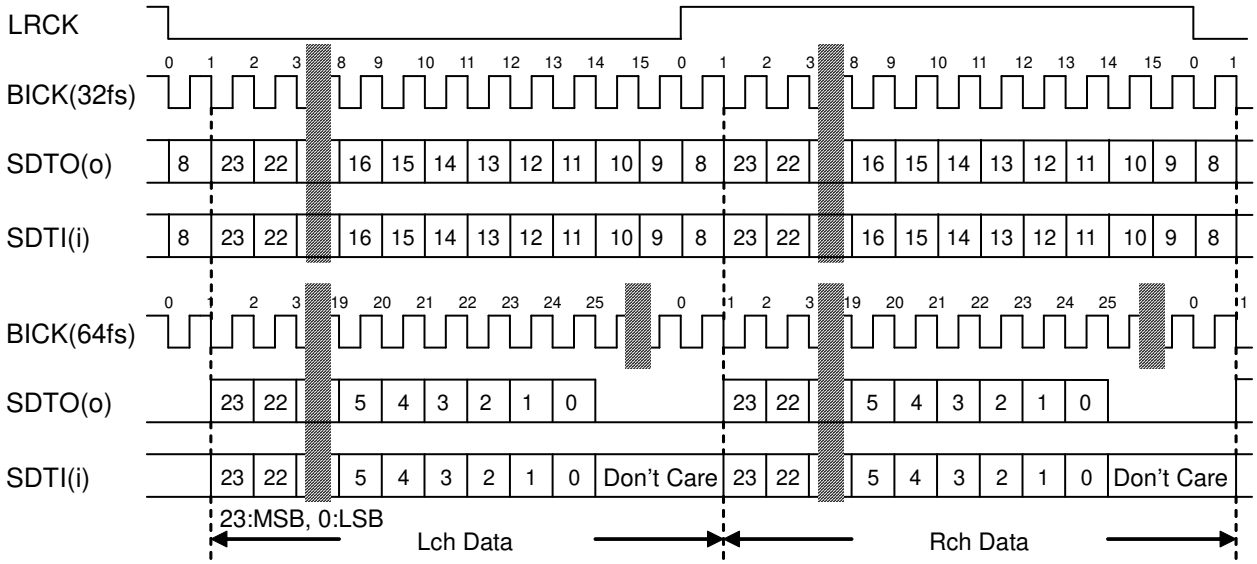


Figure 30. Mode 3 Timing

■ Mono/Stereo Mode

PMADL, PMADR, PMDML and PMDMR bits set mono/stereo ADC operation. When changing ADC operation and analog/digital microphone, PMADL, PMADR, PMDML and PMDMR bits must be set "0" at first. When PMDML or PMDMR bit = "1", PMADL and PMADR bit settings are ignored.

PMADL bit	PMADR bit	ADC Lch data	ADC Rch data	
0	0	All "0"	All "0"	(default)
0	1	Rch Input Signal	Rch Input Signal	
1	0	Lch Input Signal	Lch Input Signal	
1	1	Lch Input Signal	Rch Input Signal	

Table 19. Mono/Stereo ADC operation (Analog Microphone)

PMDML bit	PMDMR bit	ADC Lch data	ADC Rch data	
0	0	All "0"	All "0"	(default)
0	1	Rch Input Signal	Rch Input Signal	
1	0	Lch Input Signal	Lch Input Signal	
1	1	Lch Input Signal	Rch Input Signal	

Table 20. Mono/Stereo ADC operation (Digital Microphone)

■ MIC/LINE Input Selector

The AK4958 has an input selector. INL and INR bits select LIN1/LIN2 and RIN1/RIN2, respectively. When DMIC bit = "1", digital microphone input is selected regardless of INL and INR bits. LIN2 and RIN2 inputs are only for the AK4958EG. The AK4958ECB does not have these pins. Do not write "1" to INL and INR bits of the AK4958ECB.

DMIC bit	INL bit	INR bit	Lch	Rch	
0	0	0	LIN1	RIN1	(default)
	0	1	LIN1	RIN2	
	1	0	LIN2	RIN1	
	1	1	LIN2	RIN2	
1	0	0	Digital Microphone		
	0	1			
	1	0			
	1	1			

Table 21. MIC/Line In Path Select (AK4958EG)

DMIC bit	Lch	Rch	
0	LIN1	RIN1	(default)
1	Digital Microphone		

Table 22. MIC/Line In Path Select (AK4958ECB)

■ Microphone Gain Amplifier

The AK4958 has a gain amplifier for microphone input. It is powered-up by PMMICL/R bit = "1". The gain of MIC-Amp is selected by the MGAIN2-0 bits (Table 23). The typical input impedance is 30kΩ. A click noise may occur if the MIC-Amp gain is changed when both MIC-Amp and ADC (PMADC bit = "1") are powered up.
High frequency characteristics are attenuated when MIC-Amp = +30dB. The attenuation amount of when MIC-Amp = +30dB is 0.5dB at 10kHz frequency and 1.5dB at 20kHz frequency comparing with when MIC-Amp = +18dB.

MGAIN2 bit	MGAIN1 bit	MGAIN0 bit	Input Gain	
0	0	0	0dB	
0	0	1	+6dB	
0	1	0	+12dB	
0	1	1	+15dB	
1	0	0	+18dB	(default)
1	0	1	+21dB	
1	1	0	+25dB	
1	1	1	+30dB	

Table 23. Input Gain (N/A: Not available)

■ Microphone Power

When PMMP bit = "1", the MPWR pin supplies the power for microphones. This output voltage is typically 2.4V @MICL bit ="0", and typically 2.0V@MICL bit = "1". The load resistance is minimum 0.5kΩ In case of using two sets of stereo microphones, the load resistance is minimum 2kΩ for each channel. Any capacitor must not be connected directly to the MPWR pin (Figure 31).

PMMP bit	MPWR pin	
0	Hi-Z	(default)
1	Output	

Table 24. Microphone Power

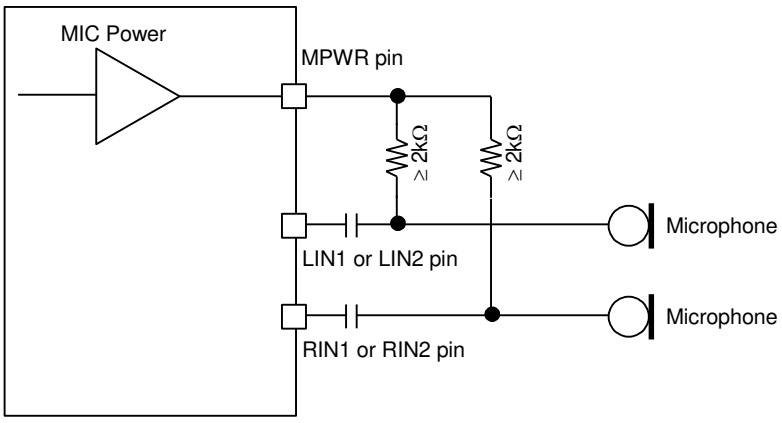


Figure 31. Microphone Block Circuit (When using two channels)

■ Digital Microphone

1. Connection to Digital Microphones

When DMIC bit is set to "1", the LIN1 and RIN1 pins become DMDAT (digital microphone data input) and DMCLK (digital microphone clock supply) pins, respectively. The same voltage as AVDD must be provided to the digital microphone. The Figure 32 and Figure 33 show stereo/mono connection examples. The DMCLK clock is input to a digital microphone from the AK4958. The digital microphone outputs 1bit data, which is generated by ΔΣModulator using DMCLK clock, to the DMDAT pin. PMDML/R bits control power up/down of the digital block (Decimation Filter and Digital Filter). (PMADL/PMADR bits settings do not affect the digital microphone power management. Set PMMP = PMMICL/R bits to "0" when using a digital microphone.) The DCLKE bit controls ON/OFF of the output clock from the DMCLK pin. When the AK4958 is powered down (PDN pin= "L"), the DMCLK and DMDAT pins become floating state. Pull-down resistors must be connected to DMCLK and DMDAT pins externally to avoid this floating state.

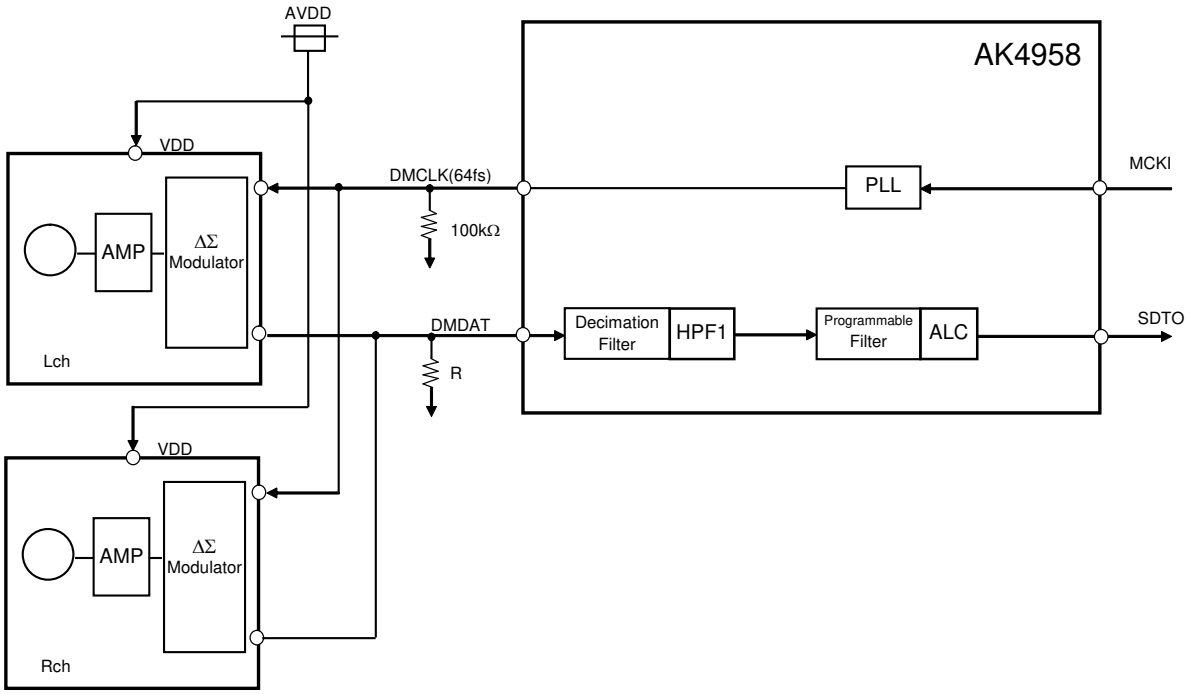


Figure 32. Connection Example of Stereo Digital Microphone

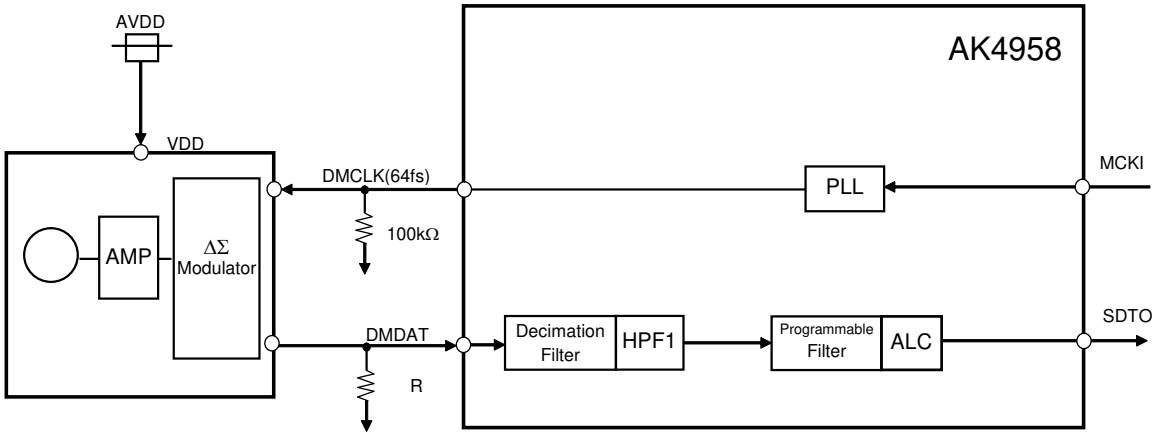


Figure 33. Connection Example of Mono Digital Microphone

2. Interface

The input data channel of the DMDAT pin is set by DCLKP bit. When DCLKP bit = "1", L channel data is input to the decimation filter if DMCLK = "H", and R channel data is input if DMCLK = "L". When DCLKP bit = "0", R channel data is input to the decimation filter while DMCLK pin= "H", and L channel data is input while DMCLK pin= "L". The DMCLK pin only supports 64fs. It outputs "L" when DCLKE bit = "0", and outputs 64fs when DCLKE bit = "1". In this case, necessary clocks must be supplied to the AK4958 for ADC operation. The output data through "the Decimation and Digital Filters" is 24bit full scale when the 1bit data density is 0%~100%.

DCLKP bit	DMCLK pin= "H"	DMCLK pin= "L"	
0	Rch	Lch	(default)
1	Lch	Rch	

Table 25. Data In/Output Timing with Digital Microphone (DCLKP bit = "0")

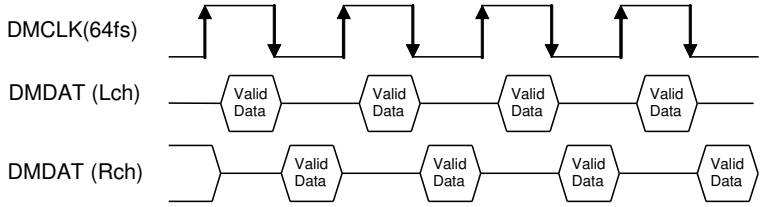


Figure 34. Data In/Output Timing with Digital Microphone (DCLKP bit = "1")

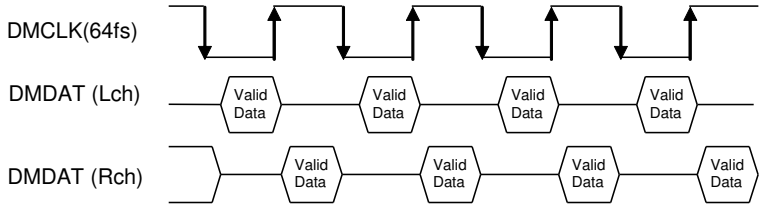
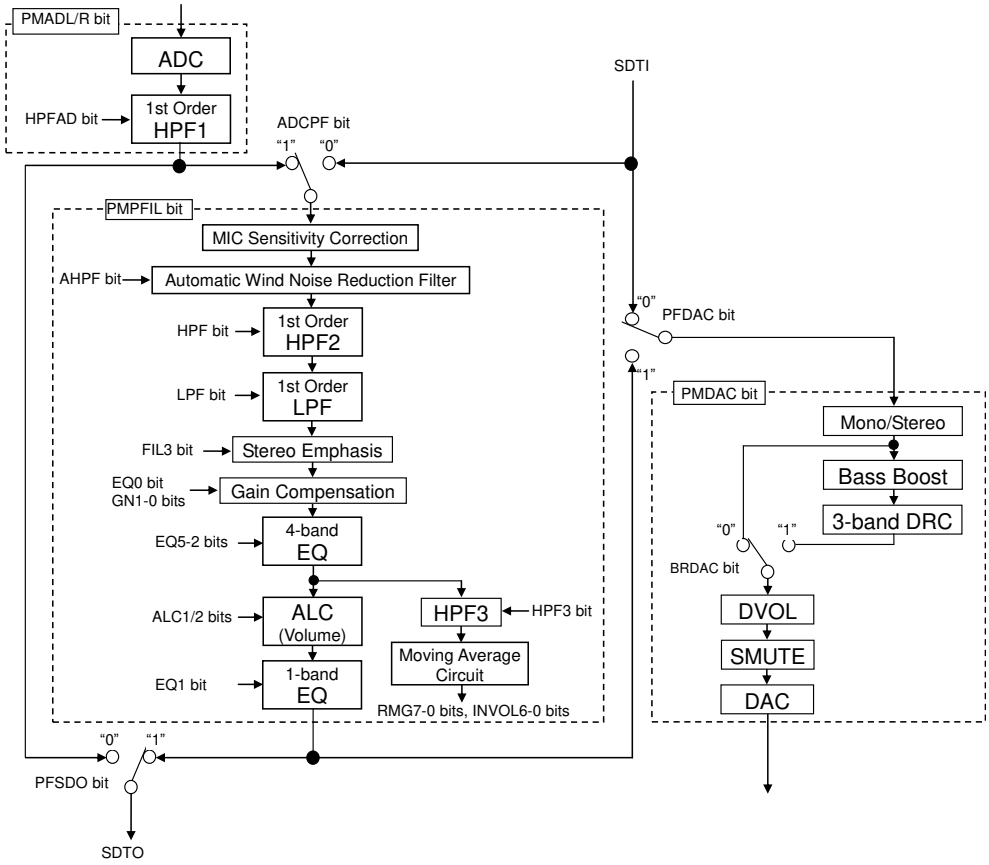


Figure 35. Data In/Output Timing with Digital Microphone (DCLKP bit = "0")

■ Digital Block

The digital block consists of the blocks shown in Figure 36. Recording path and playback path is selected by setting ADCPF bit, PFDAC bit and BRDAC bit. (Figure 37 ~ Figure 40, Table 26)



(1) ADC: Includes the Digital Filter (LPF) for ADC as shown in "FILTER CHRACTERISTICS".
(2) HPF1: High Pass Filter (HPF) for ADC as shown in "Digital HPF1".
(3) Microphone Sensitivity Correction: Microphone volume control between L and R channels. (See "Microphone Sensitivity Correction")
(4) Automatic Wind Noise Reduction Filter: Automatic HPF (See "Automatic Wind Noise Reduction Filter")
(5) HPF2: High Pass Filter. (See "Digital Programmable Filter Circuit")
(6) LPF: Low Pass Filter (See "Digital Programmable Filter Circuit")
(7) Stereo Emphasis: Stereo emphasis Filter. (See "Digital Programmable Filter Circuit")
(8) Gain Compensation: Gain compensation consists of EQ and Gain control. It corrects frequency response after stereo separation emphasis filter. (See "Digital Programmable Filter Circuit")
(9) 4 Band EQ: Applicable for use as Equalizer or Notch Filter. (See "Digital Programmable Filter Circuit")
(10) HPF3: The second order HPF for input level reading function.
(11) Moving Average Circuit. (See "Input Level Reading Function ")
(12) ALC (Volume): Digital Volume with ALC Function. (See "Input Digital Volume" and "ALC Operation")
(13) 1 Band EQ: Applicable for use as Notch Filter (See "Digital Programmable Filter Circuit")
(14) Mono/Stereo Switching: Mono/Stereo lineout outputs select from DAC which described in <Mono Mixing Output> at "Output Digital Volume (Manual Mode)".
(15) Bass Boost: Low frequency enhancement function for speaker output. (See "Bass Boost Circuit")
(16) 3band-DRC: 3-band Dynamic Range Control function (See "3band DRC Operation")
(17) DVOL: Digital volume for playback path (See "Output Digital Volume2")
(18) SMUTE: Soft mute function

Figure 36. Digital Block Path Select

Mode	ADCPF bit	PFDAC bit	PFSDO bit	BRDAC bit	Figure
Recording Mode 1 & Playback Mode 2	1	0	1	0	Figure 37
Recording Mode 2 & Playback Mode 1	0	1	0	1	Figure 38
Recording Mode 2 & Playback Mode 2 (Programmable Filter Bypass Mode: PMPFIL bit = "0")	x	0	0	0	Figure 39
Loopback Mode	1	1	1	1	Figure 40

Table 26. Recording Playback Mode (x: Don't care)

When changing those modes, PMPFIL bit must be "0".

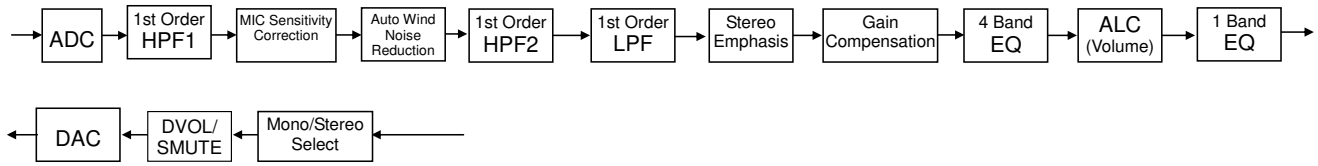


Figure 37. The Path in Recording Mode 1 & Playback Mode 2 (default)

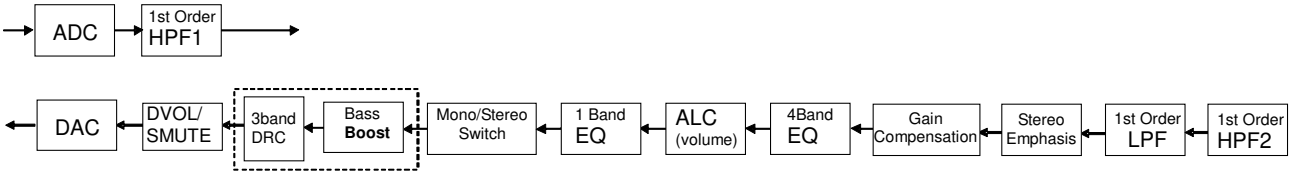


Figure 38. The Path in Recording Mode 2 & Playback Mode 1

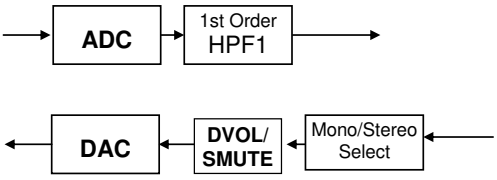


Figure 39. The Path in Recording Mode 2 & Playback Mode 2

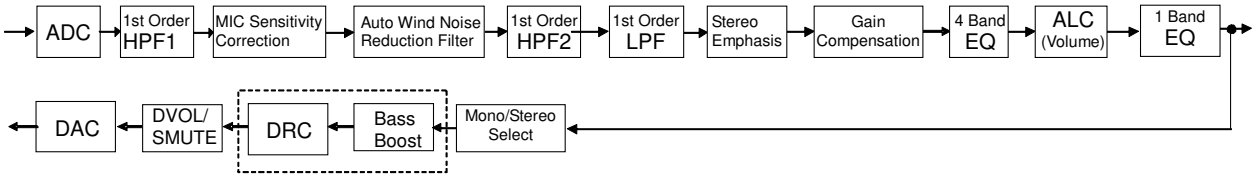


Figure 40. The Path in Loopback Mode

■ Digital HPF1

A digital High Pass Filter (HPF) is integrated for DC offset cancellation of the ADC input. The cut-off frequencies of the HPF1 are set by HPFC1-0 bits (Table 27). It is proportional to the sampling frequency (fs) and the default value is 3.7Hz (@fs = 48kHz). HPFAD bit controls the ON/OFF of the HPF1 (HPF ON is recommended).

HPFC1 bit	HPFC0 bit	fc			
		fs=48kHz	fs=22.05kHz	fs=8kHz	
0	0	3.7Hz	1.7Hz	0.62Hz	(default)
0	1	14.8Hz	6.8Hz	2.47Hz	
1	0	118.4Hz	54.4Hz	19.7Hz	
1	1	236.8Hz	108.8Hz	39.5Hz	

Table 27. HPF1 Cut-off Frequency

■ Microphone Sensitivity Correction

The AK4958 has linear microphone sensitivity correction function controlled by MGL/R7-0 bits.

MGL7-0 bits MGR7-0 bits	MG_DATA	GAIN (dB)	Calculation	
00H	0	Mute	-	
01H	1	-42.144	$20 \log_{10}(MG\_DATA/128)$	(default)
02H	2	-36.124		
:	:	:		
7EH	126	-0.137		
7FH	127	-0.068		
80H	128	0.000		
81H	129	+0.068		
82H	130	+0.135		
:	:	:		
FDH	253	+5.918		
FEH	254	+5.952		
FFH	255	+5.987		

Table 28. Microphone Sensitivity Correction

Example of Microphone Sensitivity Difference Measurement by ALC Input Level Reading Function

Execute the sensitivity difference measurement on L and R channels independently.

<Lch>
Read RMG7-0 bits with an interval of 512/fs (min.) following a start of ALC operation after setting the volume of Lch to 0dB and Rch to Mute (MGL7-0 bits = 80H, MGR7-0 bits = 00H). Adjust the measurement sound source level and Lch volume (MGL7-0 bits) to put the Lch level value of RMG7-0 bits closer to 80H. After the adjustment, take the measurement value of RMG7-0 bits as Lch level.

<Rch>
Read RMG7-0 bits with an interval of 512/fs (min.) following a start of ALC operation after setting the volume of Lch to Mute and Rch to 0dB (MGL7-0 bits = 00H, MGR7-0 bits = 80H). Take the measurement value of RMG7-0 bits as Rch level.

By comparing L and R channel levels by the measurements above, MIC sensitivity difference of L and R channels can be calculated. Correct the Microphone sensitivity by MGL7-0/MGR7-0 bits according to the calculated sensitivity difference. In addition, more accurate measurement is available by limiting measurement band frequency by HPF2, LPF, EQ2~5(Band Pass) (Table 34) and HPF3. The measurement accuracy is also increased by taking an average value of RMG7-0 bits data after several measurements.

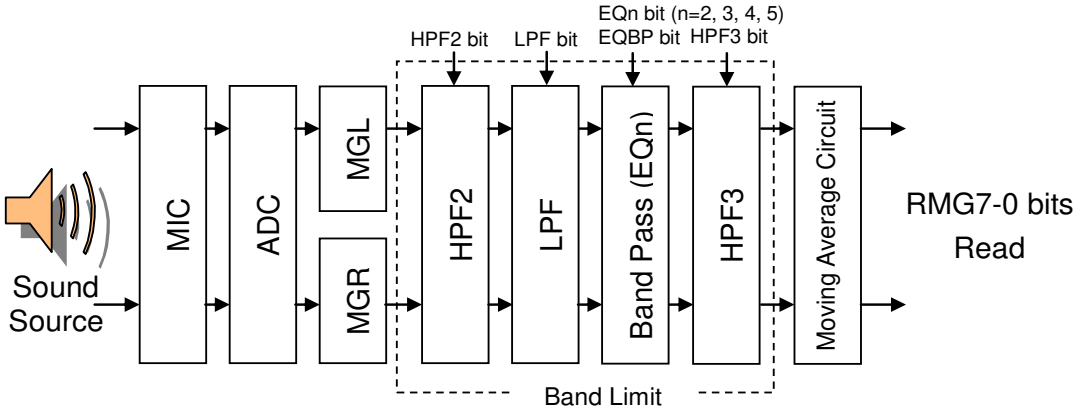


Figure 41. Microphone Sensitivity Measurement Example

RMG7-0 bits	RMG_DATA	Input Level [dB]	Calculation
FFH	255	-54.219	$10 \log_{10}[(2^{-25}) \times (RMG\_DATA-128)]$
FEH	254	-54.254	
:	:	:	
C1H	193	-57.128	
C0H	192	-57.196	
BFH	191	-57.230	$10 \log_{10}[(2^{-26}) \times (RMG\_DATA-64)]$
:	:	:	
81H	129	-60.139	
80H	128	-60.206	
7FH	127	-60.240	$10 \log_{10}[(2^{-27}) \times (RMG\_DATA)]$
:	:	:	
41H	65	-63.149	
40H	64	-63.216	
3FH	63	-63.250	$10 \log_{10}[(2^{-28}) \times (RMG\_DATA+64)]$
:	:	:	
01H	1	-66.159	
00H	0	-66.227	(default)

Table 29. RMG7-0 bits Read Data

■ Automatic Wind Noise Reduction Filter

The AK4958 has an automatic wind noise reduction filter that is controlled by AHPF bit. The automatic wind noise reduction filter is ON when AHPF bit = "1". It attenuates the wind noise when detecting a wind noise and adjusts the attenuation level dynamically. When AHPF bit = "0", the audio data passes this block by 0dB gain. SENC2-0 bits control the wind noise detection sensitivity, and STG1-0 bits control the attenuation level of the maximum attenuation. SENC2-0 bits and STG1-0 bits must be set when AHPF bit = "0" or PMPF bit = "0".

SENC2-0 bits	Sensitivity Level	
000	0.5	Low
001	1.0	⇧
010	1.5	
011	2.0	(default)
100	2.5	
101	3.0	⇩
110	3.5	High
111	4.0	

Table 30. Wind Noise Detection Sensitivity

STG1-0 bits	Attenuation Level		
00	Low	Low	(default)
01	Middle1	⇩	
10	Middle2		
11	High	High	

Table 31. Automatic Wind Noise Reduction Filter

■ Digital Programmable Filter Circuit

(1) High Pass Filter (HPF2)

This is composed 1st order HPF. The coefficient of HPF is set by F1A13-0 bits and F1B13-0 bits. HPF bit controls ON/OFF of the HPF2. When the HPF2 is OFF, the audio data passes this block by 0dB gain. The coefficient must be set when PMPFIL bit = "0" or HPF bit = "0". The HPF2 starts operation 4/fs (max) after when HPF bit=PMPFIL bit= "1" is set.

fs: Sampling Frequency
fc: Cutoff Frequency

Register Setting (Note 49)
HPF: F1A[13:0] bits =A, F1B[13:0] bits =B
(MSB=F1A13, F1B13; LSB=F1A0, F1B0)

$$A = \frac{1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

Transfer Function

$$H(z) = A \frac{1 - z^{-1}}{1 + Bz^{-1}}$$

The cut-off frequency must be set as below.
fc/fs ≥ 0.0001 (fc min = 4.8Hz at 48kHz)

(2) Low Pass Filter (LPF)

This is composed with 1st order LPF. F2A13-0 bits and F2B13-0 bits set the coefficient of LPF. LPF bit controls ON/OFF of the LPF. When the LPF is OFF, the audio data passes this block by 0dB gain. The coefficient must be set when PMPFIL bit = "0" or LPF bit = "0". The LPF starts operation 4/fs (max) after when LPF bit =PMPFIL bit= "1" is set.

fs: Sampling Frequency
fc: Cutoff Frequency

Register Setting (Note 49)
LPF: F2A[13:0] bits =A, F2B[13:0] bits =B
(MSB=F2A13, F2B13; LSB=F2A0, F2B0)

$$A = \frac{1}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

Transfer Function

$$H(z) = A \frac{1 + z^{-1}}{1 + Bz^{-1}}$$

The cut-off frequency must be set as below.
fc/fs ≥ 0.05 (fc min = 2400Hz at 48kHz)

(3) Stereo Separation Emphasis Filter (FIL3)

The FIL3 is used to emphasize the stereo separation of stereo microphone recording data and playback data. F3A13-0 bits and F3B13-0 bits set the filter coefficients of the FIL3. When F3AS bit = "0", the FIL3 performs as a High Pass Filter (HPF), and it performs as a Low Pass Filter (LPF) when F3AS bit = "1". FIL3 bit controls ON/OFF of the FIL3. When the stereo separation emphasis filter is OFF, the audio data passes this block by 0dB gain. The coefficient should be set when FIL3 bit or PMPFIL bit is "0". The FIL3 starts operation 4/fs(max) after when FIL3 bit =PMPFIL bit= "1" is set.

Stereo emphasis method can be selected by STEREO2 bit. STEREO2 bit must not be changed when FIL3 bit = "1".

STEREO2 bit	FIL3 Method	
0	Method 1	(default)
1	Method 2	

Table 32. FIL3 Method Switching

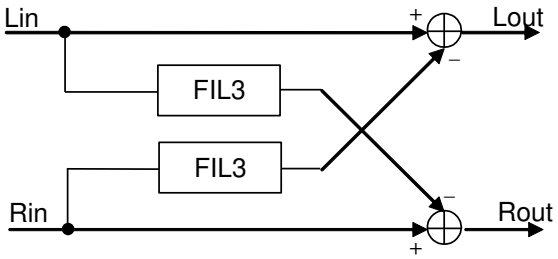


Figure 42. Stereo Emphasis Circuit – Method 1

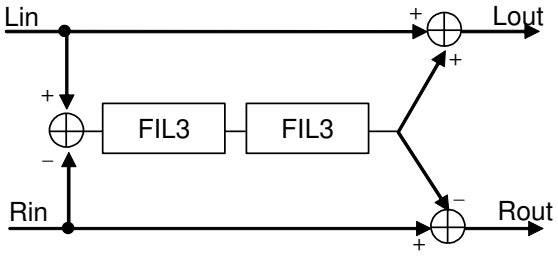


Figure 43. Stereo Emphasis Circuit – Method 2

1) In case of setting FIL3 as HPF

fs: Sampling Frequency
fc: Cutoff Frequency
K: Gain [dB] (0dB ≥ K ≥ −10dB)

Register Setting (Note 49)
FIL3: F3AS bit = "0", F3A[13:0] bits =A, F3B[13:0] bits =B
(MSB=F3A13, F3B13; LSB=F3A0, F3B0)

$$A = 10^{K/20} \times \frac{1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

Transfer Function

$$H(z) = A \frac{1 - z^{-1}}{1 + Bz^{-1}}$$

The cut-off frequency must be set as below.
fc/fs ≥ 0.0001 (fc min = 4.8Hz @fs=48kHz)

2) In case of setting FIL3 as LPF

fs: Sampling Frequency
fc: Cutoff Frequency
K: Gain [dB] (0dB ≥ K ≥ −10dB)

Register Setting (Note 49)
FIL3: F3AS bit = "1", F3A[13:0] bits =A, F3B[13:0] bits =B
(MSB=F3A13, F3B13; LSB= F3A0, F3B0)

$$A = 10^{K/20} \times \frac{1}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

Transfer Function

$$H(z) = A \frac{1 + z^{-1}}{1 + Bz^{-1}}$$

The cut-off frequency must be set as below.
fc/fs ≥ 0.0001 (fc min = 4.8Hz @fs=48kHz)

(4) Gain Compensation (EQ0)

Gain compensation is used to compensate the frequency response and the gain that is changed by the stereo separation emphasis filter. Gain compensation is composed of the Equalizer (EQ0) and the Gain (0dB/+12dB/+24dB). E0A15-0 bits, E0B13-0 bits and E0C15-0 bits set the coefficient of EQ0. GN1-0 bits set the gain (Table 33). EQ0 bit controls ON/OFF of EQ0. When EQ is OFF and the gain is 0dB, the audio data passes this block by 0dB gain. The coefficient should be set when EQ0 bit = "0" or PMPFIL bit = "0". The EQ0 starts operation 4/fs(max) after when EQ0 bit =PMPFIL bit= "1" is set.

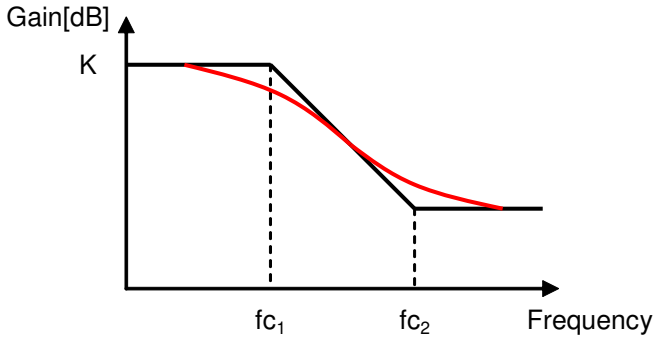
fs: Sampling Frequency
fc_1: Polar Frequency
fc_2: Zero-point Frequency
K: Gain [dB] (Maximum setting is +12dB.)

Register Setting (Note 49)
E0A[15:0] bits =A, E0B[13:0] bits =B, E0C[15:0] bits =C
(MSB=E0A15, E0B13, E0C15; LSB=E0A0, E0B0, E0C0)

$$A = 10^{K/20} \times \frac{1 + 1 / \tan(\pi fc_2/fs)}{1 + 1 / \tan(\pi fc_1/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc_1/fs)}{1 + 1 / \tan(\pi fc_1/fs)}, \quad C = 10^{K/20} \times \frac{1 - 1 / \tan(\pi fc_2/fs)}{1 + 1 / \tan(\pi fc_1/fs)}$$

Transfer Function

$$H(z) = \frac{A + Cz^{-1}}{1 + Bz^{-1}}$$



(Note) Black: Diagrammatic Line, Red: Actual Curve
Figure 44. EQ0 Frequency Response

GN1 bit	GN0 bit	Gain	
0	0	0dB	(default)
0	1	+12dB	
1	x	+24dB	

Table 33. Gain Setting (x: Don't care)

(5) 4-band Equalizer & 1-band Equalizer after ALC

This block can be used as equalizer or Notch Filter. 4-band equalizers (EQ2~EQ5) are switched ON/OFF independently by EQ2, EQ3, EQ4 and EQ5 bits. EQ1 bit controls ON/OFF switching of the equalizer after ALC (EQ1). When the equalizer is OFF, the audio data passes this block by 0dB gain. E1A15-0 bits, E1B15-0 bits and E1C15-0 bits set the coefficient of EQ1. E2A15-0 bits, E2B15-0 bits and E2C15-0 bits set the coefficient of EQ2. E3A15-0 bits, E3B15-0 bits and E3C15-0 bits set the coefficient of EQ3. E4A15-0 bits, E4B15-0 bits and E4C15-0 bits set the coefficient of EQ4. E5A15-0 bits, E5B15-0 bits and E5C15-0 bits set the coefficient of EQ5. The EQx (x=1, 2, 3, 4 or 5) coefficient must be set when EQx bit = "0" or PMPFIL bit = "0". EQx starts operation 4/fs(max) after when EQx = PMPFIL bit = "1" is set.

Each EQ2 ~ 5 blocks have a gain controller (EQ2G ~ EQ5G) independently after the equalizer. EQnG5-0 bits (n = 2~5) setting is reflected by writing "1" to EQCn bit (n = 2~5). EQnG5-0 bits and EQCn bit (n=2~5) can be set during operation (EQn =PMPFIL bit= "1").
When EQBP bit = "1", 4-band equalizer can be used as a band pass filter. (Figure 45)

fs: Sampling Frequency
fo_1 ~ fo_5: Center Frequency
fb_1 ~ fb_5: Band width where the gain is 3dB different from the center frequency
K_1 ~ K_5: Gain ($-1 \le K_n < 3$)

Register Setting (Note 49)
EQ1: E1A[15:0] bits =A_1, E1B[15:0] bits =B_1, E1C[15:0] bits =C_1
EQ2: E2A[15:0] bits =A_2, E2B[15:0] bits =B_2, E2C[15:0] bits =C_2
EQ3: E3A[15:0] bits =A_3, E3B[15:0] bits =B_3, E3C[15:0] bits =C_3
EQ4: E4A[15:0] bits =A_4, E4B[15:0] bits =B_4, E4C[15:0] bits =C_4
EQ5: E5A[15:0] bits =A_5, E5B[15:0] bits =B_5, E5C[15:0] bits =C_5
(MSB=E1A15, E1B15, E1C15, E2A15, E2B15, E2C15, E3A15, E3B15, E3C15, E4A15, E4B15, E4C15, E5A15, E5B15, E5C15 ; LSB= E1A0, E1B0, E1C0, E2A0, E2B0, E2C0, E3A0, E3B0, E3C0, E4A0, E4B0, E4C0, E5A0, E5B0, E5C0)

$$A_n = K_n \times \frac{\tan(\pi fb_n/fs)}{1+\tan(\pi fb_n/fs)}, \quad B_n = \cos(2\pi fo_n/fs) \times \frac{2}{1+\tan(\pi fb_n/fs)}, \quad C_n = -\frac{1-\tan(\pi fb_n/fs)}{1+\tan(\pi fb_n/fs)}$$

(n = 1, 2, 3, 4, 5)

Transfer Function

$$H(z) = \{1 + G_2 \times h_2(z) + G_3 \times h_3(z) + G_4 \times h_4(z) + G_5 \times h_5(z)\} \times \{1 + h_1(z)\}$$

($G_{2,3,4,5}$ = 1 or G)

$$h_n(z) = A_n \frac{1 - z^{-2}}{1 - B_n z^{-1} - C_n z^{-2}}$$

(n = 1, 2, 3, 4, 5)

The center frequency must be set as below.
$0.003 < fo_n / fs < 0.497$

When gain of K is set to "−1", this equalizer becomes a notch filter. When EQ2 ~EQ5 is used as a notch filter, central frequency of a real notch filter deviates from the above-mentioned calculation, if its central frequency of each band is near. The control soft that is attached to the evaluation board has functions that revises a gap of frequency and calculates the coefficient. When its central frequency of each band is near, the central frequency should be revised and confirm the frequency response.

Note 49.
[Translation the filter coefficient calculated by the equations above from real number to binary code (2's complement)]
X = (Real number of filter coefficient calculated by the equations above) x 2^{13}

X should be rounded to integer, and then should be translated to binary code (2's complement).
MSB of each filter coefficient setting register is sine bit.

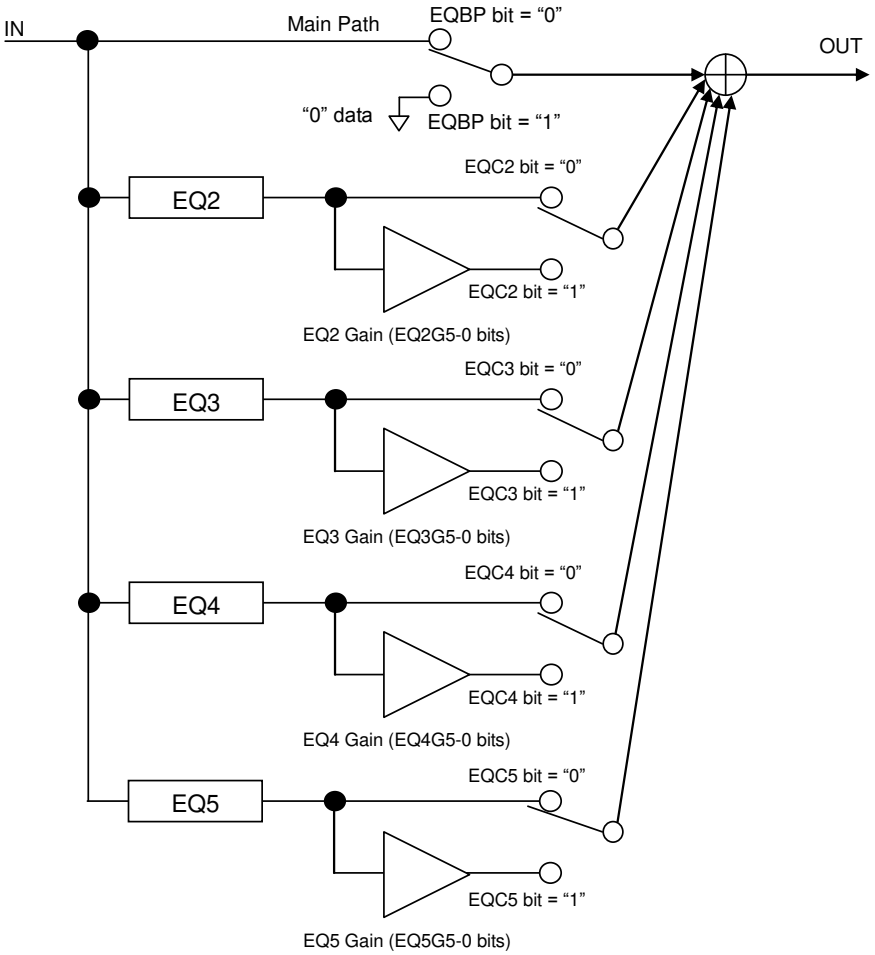


Figure 45. 4-Band EQ Structure

EQBP bit	Main Path の ON/OFF	
0	ON (Audio data)	(default)
1	OFF ("0" data) Microphone sensitivity difference Measurement (Figure 41)	

Table 34. Main Path Switch of the 4-Band Equalizer

EQnG5-0 bits	EQG DATA	Gain [dB]	Formula	
3FH	255	0	$20*\log_{10}$ (EQG_DATA/256)	
3EH	251	-0.17		
3DH	247	-0.31		
:				
02H	11	-27.34		
01H	7	-31.26		
00H	0	MUTE		(default)

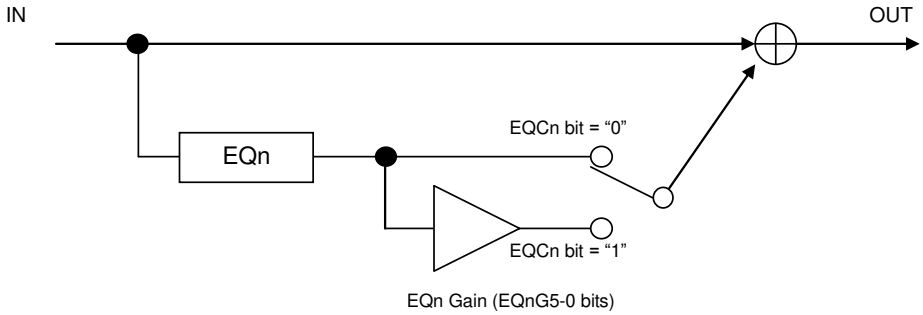
Table 35. EQn Gain Setting (n=2, 3, 4, 5)

EQnT1-0 bits	Transition Time of EQnG5-0 bits = 3FH ~ 00H			
	Setting Value	fs=8kHz	fs=48kHz	
00	256/fs	32ms	5.3ms	(default)
01	2048/fs	256ms	42.7ms	
10	8192/fs	1024ms	170.7ms	
11	16384/fs	2048ms	341.3ms	

Table 36. Transition Time of EQn Gain (n= 2, 3, 4, 5)

Common Gain Sequence Examples

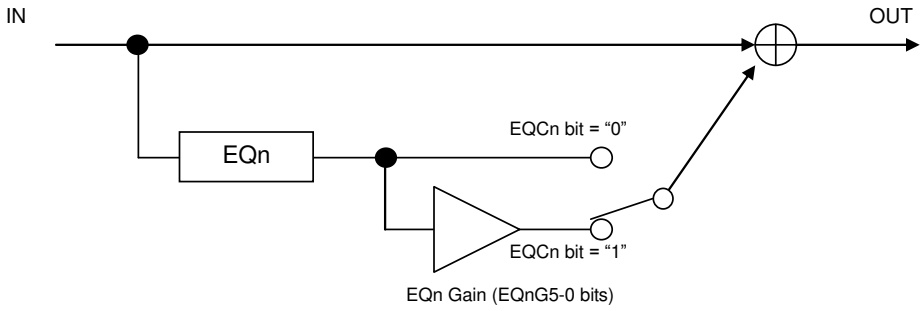
<When noise is generated>



(assuming the noise continues)

(1) Set EQCn bit: "1" → "0" (Path Setting). The gain changes immediately by this setting.
(2) Set EQnT1-0 bits: "xx" → "00" (Transition Time)
(3) Set EQnG5-0 bits: "xxH" → "3FH" (Gain Setting; should be set to 0dB)

<When noise is stopped>



(4) Set EQCn bit: "0" → "1" (Path Setting), EQnT1-0 bits Setting
(Transition Time: It should be set longer when noise is stopped.) (Note 50)
(5) Set EQnG5-0 bits (Gain Setting)
The gain of EQn is changed after a transition time set by EQnT1-0 bits.

Note 50. When changing a path of EQC2-5 by setting EQC2-5 bits "0" → "1", the gain should be transitioned to 0dB before the settings. Otherwise, pop noise may occur on the path change.

■ ALC Input Level Read Function

The input level before ALC can be read in moving average value by INVLO6-0 bits (Table 38). The input level which is read by this function is bigger output between L and R channels after the signals are averaged by moving average circuit following HPF3. The cutoff frequency of the HPF3 is set by HPF3C2-0 bits. The HPF3 is controlled by HPF3 bit. When HPF3 bit = "0", the audio data passes through the HPF3 block by 0dB gain.

Available range of ALC input level reading is from 0 to –95.25dB. INVOL6-0 bits indicate "00H" as 0dB if the input level is more than 0dB, and indicate "7FH" as –95.25dB if the input level is less than –95.25dB.
ALC input level read should be executed with an interval of min. 512/fs after staring ALC operation or changing HPF3 bit "0" → "1". The read input level is a moving average value. The recovery reset level, the limiter detection level and the REF inflection point level are peak levels, so that the input level will degrade by approximately 3dB as compared to these levels.

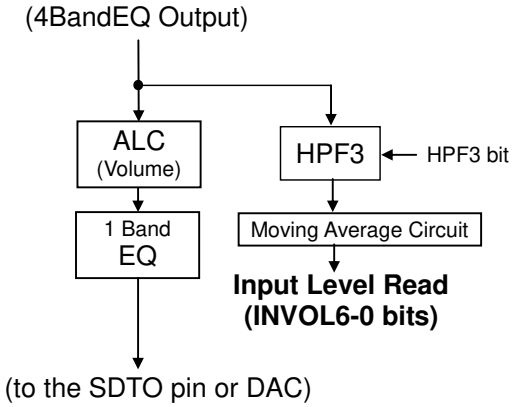


Figure 46. ALC Input Level Read Function

HPF3C2-0 bits	Cutoff Frequency [Hz]			
	fs = 8kHz	fs = 16kHz	fs =48kHz	
000	83	167	500	(default)
001	167	333	1000	
010	250	500	1500	
011	333	667	2000	
100	500	1000	3000	
101	667	1333	4000	

Table 37. HPF3 Cutoff Frequency Setting

INVOL6-0 bits	Input Level [dB]	Step	
7FH	–95.25	1.5dB	
7EH	–94.5		
7DH	–93.75		
7CH	–93		
:	:		
02H	–1.5		
01H	–0.75		
00H	0		(default)

Table 38. ALC Input Level

■ ALC Operation

The ALC (Automatic Level Control) is operated by ALC block. When ADCPF bit is "1", the ALC circuit operates for recording path, and the ALC circuit operates for playback path when ADCPF bit is "0". ALC1 bit controls ON/OFF of ALC operation at recording path, and ALC2 bit controls ON/OFF of ALC operation at playback path.

The ALC block consists of these blocks shown below. The ALC limiter detection level is monitored at the level detection2 block after EQ block. The level detection1 block also monitors clipping detection level (+0.53dBFS).

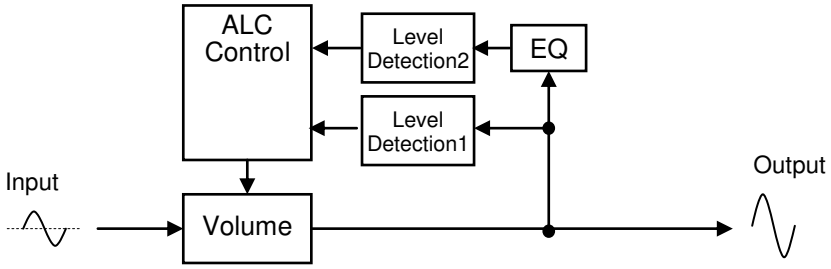


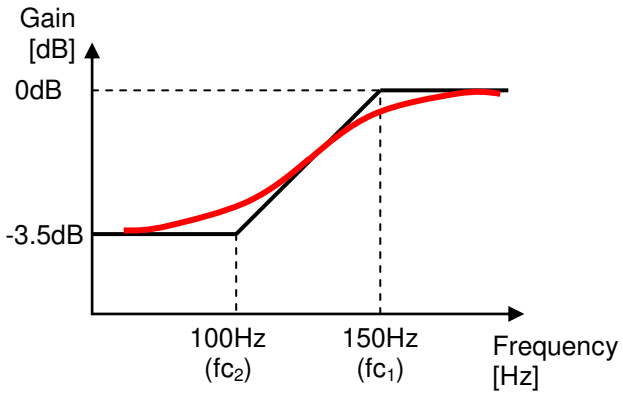
Figure 47. ALC Block

The polar (fc1) and the zero point (fs2) frequencies of EQ block are set by EQFC1-0 bits. Set ALCEQ bits according to the sampling frequency. When ALCEQ bit is OFF (ALCEQ bit = "1"), the level detection is not executed on this block.

EQFC1-0bits	Sampling Frequency Range	Polar Frequency (fc1)	Zero-point Frequency (fc2)	
00	7.35kHz ≤ fs ≤ 12kHz	150Hz @ fs=12kHz	100Hz @ fs=12kHz	
01	12kHz < fs ≤ 24kHz	150Hz @ fs= 24kHz	100Hz @ fs=24kHz	
10	24kHz < fs ≤ 48kHz	150Hz @ fs = 48kHz	100Hz @ fs = 48kHz	(default)

Table 39. ALCEQ Frequency Setting (EQFC1-0 bits)

[ALCEQ: First order zero pole high pass filter]



Note 51. Black: Diagrammatic Line, Red: Actual Curve

Figure 48. ALCEQ Frequency Response (fs = 48kHz)

Note 52. In this section, VOL means IVL and IVR for recording path, OVL and OVR for playback path.
Note 53. In this section, ALC means ALC1 for recording path, ALC2 for playback path.
Note 54. In this section, REF means IREF for recording path, OREF for playback path.

1. ALC Limiter Operation

During ALC limiter operation, when either L or R channel output level exceeds the ALC limiter detection level (Table 40), the VOL value (same value for both L and R) is attenuated automatically by the amount defined by the ALC limiter ATT step (Table 41). (Once this ALC limiter operation is started, attenuation will be repeated sixteen times.)

After completing the attenuate operation, unless ALC bit is changed to "0", the operation repeats when the input signal level exceeds ALC limiter detection level.

LMTH2 bit	LMTH1 bit	LMTH0 bit	ALC Limiter Detection Level	ALC Recovery Counter Reset Level	
0	0	0	ALC Output ≥ −2.5dBFS	−2.5dBFS > ALC Output ≥ −4.1dBFS	(default)
0	0	1	ALC Output ≥ −2.5dBFS	−2.5dBFS > ALC Output ≥ −3.3dBFS	
0	1	0	ALC Output ≥ −4.1dBFS	−4.1dBFS > ALC Output ≥ −6.0dBFS	
0	1	1	ALC Output ≥ −4.1dBFS	−4.1dBFS > ALC Output ≥ −5.0dBFS	
1	0	0	ALC Output ≥ −6.0dBFS	−6.0dBFS > ALC Output ≥ −8.5dBFS	
1	0	1	ALC Output ≥ −6.0dBFS	−6.0dBFS > ALC Output ≥ −7.2dBFS	
1	1	0	ALC Output ≥ −8.5dBFS	−8.5dBFS > ALC Output ≥ −12.0dBFS	
1	1	1	ALC Output ≥ −8.5dBFS	−8.5dBFS > ALC Output ≥ −10.1dBFS	

Table 40. ALC Limiter Detection Level/ Recovery Counter Reset Level

Output	ATT Amount [dB]
+0.53dBFS ≤ Output Level (*)	0.38148
−1.16dBFS ≤ Output Level < +0.53dBFS	0.06812
LM-LEVEL ≤ Output Level < −1.16dBFS	0.02548

Table 41. ALC Limiter ATT Step

When either L or R channel output level exceeds the ALC limiter detection level (Table 40), the VOL value is attenuated automatically by the amount defined by the ALC limiter ATT step (Table 41). This volume change is made on both L and R channels together.

2. ALC Recovery Operation

ALC recovery operation wait for the WTM1-0 bits (Table 42) to be set after completing ALC limiter operation. If the input signal does not exceed "ALC recovery waiting counter reset level" (Table 40) during the wait time, ALC recovery operation is executed. The VOL value is automatically incremented by the setting value of RGAIN2-0 bits (Table 43) up to the set reference level (Table 44) in every sampling. When the VOL value exceeds the reference level (REF value), the VOL values are not increased. The recovery speed gets slower when the VOL peak level exceeds -12dBFS to make the recovery speed for low VOL level faster relatively.

When
"ALC recovery waiting counter reset level ≤ Output Signal < ALC limiter detection level"
during the ALC recovery operation, the waiting timer of ALC recovery operation is reset. When
"ALC recovery waiting counter reset level > Output Signal",
the waiting timer of ALC recovery operation starts.

ALC operations correspond to the impulse noise. When the impulse noise is input, the ALC recovery operation becomes faster than a normal recovery operation. When large noise is input to a microphone instantaneously, the quality of small level in the large noise can be improved by this fast recovery operation. The speed of fast recovery operation is set by RFST1-0 bits (Table 46). Limiter amount of Fast recovery is set by FRATT bit. (Table 47)

WTM1 bit	WTM0 bit		ALC Recovery Cycle			
			8kHz	16kHz	48kHz	
0	0	128/fs	16ms	8ms	2.7ms	(default)
0	1	256/fs	32ms	16ms	5.3ms	
1	0	512/fs	64ms	32ms	10.7ms	
1	1	1024/fs	128ms	64ms	21.3ms	

Table 42. ALC Recovery Operation Waiting Period

RGAIN2 bit	RGAIN1 bit	RGAIN0 bit	GAIN Step [dB]	GAIN Change Timing	
0	0	0	0.00424	1/fs	(default)
0	0	1	0.00212	1/fs	
0	1	0	0.00106	1/fs	
0	1	1	0.00106	2/fs	
1	0	0	0.00106	4/fs	
1	0	1	0.00106	8/fs	
1	1	0	0.00106	16/fs	
1	1	1	0.00106	32/fs	

Table 43. ALC Recovery Gain Step

IREF7-0 bits	GAIN (dB)	Step	
F1H	+36.0	0.375dB	(default)
F0H	+35.625		
EFH	+35.25		
:	:		
E1H	+30.0		
:	:		
92H	+0.375		
91H	0.0		
90H	–0.375		
:	:		
06H	–52.125		
05H	–52.5		
04H~00H	MUTE		

Table 44. Reference Level of ALC Recovery Operation for Recoding

OREF5-0 bits	GAIN (dB)	Step	
3CH	+36.0	1.5dB	(default)
3BH	+34.5		
3AH	+33.0		
:	:		
28H	+6.0		
:	:		
25H	+1.5		
24H	0.0		
23H	–1.5		
:	:		
02H	–51.0		
01H	–52.5		
00H	MUTE		

Table 45. Reference Level of ALC Recovery Operation for Playback

RFST1-0 bits	Fast Recovery Gain Step [dB]	
00	0.0032	(default)
01	0.0042	
10	0.0064	
11	0.0127	

Table 46. Fast Recovery Speed Setting (FRN bit = “0”)

FRATT bit	ATT Amount [dB]	ATT Switch Timing	
0	-0.00106	4/fs	(default)
1	-0.00106	16/fs	

Table 47. Fast Recovery Reference Volume Attenuation Amount

3. The Volume at ALC Operation

The volume value during ALC operation is reflected in VOL7-0 bits. It is possible to check the current volume in 0.75dB step by reading the register value of VOL7-0 bits.

VOL7-0 bits	GAIN [dB]
FFH	+36.0 ≤ Gain
FEH	+35.25 ≤ Gain < +36.0
FCH	+34.5 ≤ Gain < +35.25
FAH	+33.75≤ Gain < +34.5
:	:
A2H	+0.75 ≤ Gain < +1.5
A0H	0.0 ≤ Gain < +0.75
9EH	-0.75 ≤ Gain < 0.0
:	:
12H	-53.25 ≤ Gain < -52.5
10H	-72 ≤ Gain < -53.25
00H	MUTE

Table 48. Value of VOL7-0 bits

4. Example of ALC Setting

Table 49 and Table 50 show the examples of the ALC setting for recording and playback path.

Register Name	Comment	fs=8kHz		fs=48kHz	
		Data	Operation	Data	Operation
LMTH2-0	Limiter detection Level	010	–4.1dBFS	010	–4.1dBFS
FRN	Fast Recovery mode	0	Enable	0	Enable
WTM1-0	Recovery waiting period	01	32ms	11	21.3ms
IREF7-0	Maximum gain at recovery operation	E1H	+30dB	E1H	+30dB
IVL7-0, IVR7-0	Gain of IVOL	E1H	+30dB	E1H	+30dB
RGAIN2-0	Recovery GAIN	000	0.00424dB	011	0.00106dB (2/fs)
RFST1-0	Fast Recovery GAIN	11	0.0127dB	00	0.0032dB
ALCEQN	ALC EQ disable	0	Enable	0	Enable
ALC1	ALC1 enable	1	Enable	1	Enable

Table 49. Example of the ALC Setting (Recording)

Register Name	Comment	fs=8kHz		fs=48kHz	
		Data	Operation	Data	Operation
LMTH2-0	Limiter detection Level	010	–4.1dBFS	010	–4.1dBFS
FRN	Fast Recovery mode	0	Enable	0	Enable
WTM1-0	Recovery waiting period	01	32ms	11	21.3ms
OREF5-0	Maximum gain at recovery operation	28H	+6dB	28H	+6dB
OVL7-0, OVR7-0	Gain of VOL	91H	0dB	91H	0dB
RGAIN2-0	Recovery GAIN	000	0.00424dB	011	0.00106dB (2/fs)
RFST1-0	Fast Recovery GAIN	11	0.0127dB	00	0.0032dB
ALCEQN	ALC EQ disable	0	Enable	0	Enable
ALC2	ALC2 enable	1	Enable	1	Enable

Table 50. Example of the ALC Setting (Playback)

5. Example of registers set-up sequence of ALC Operation

The following registers must not be changed during ALC operation. These bits must be changed after ALC operation is stopped by ALC1 bit = ALC2 bit= "0". ALC output is "0" data until the AK4958 becomes manual mode after writing "0" to ALC1 and ALC2 bits.

LMTH2-0, WTM1-0, RGAIN2-0, IREF7-0, OREF5-0, RFST1-0, EQFC1-0, FRATT, FRN and ALCEQN bits

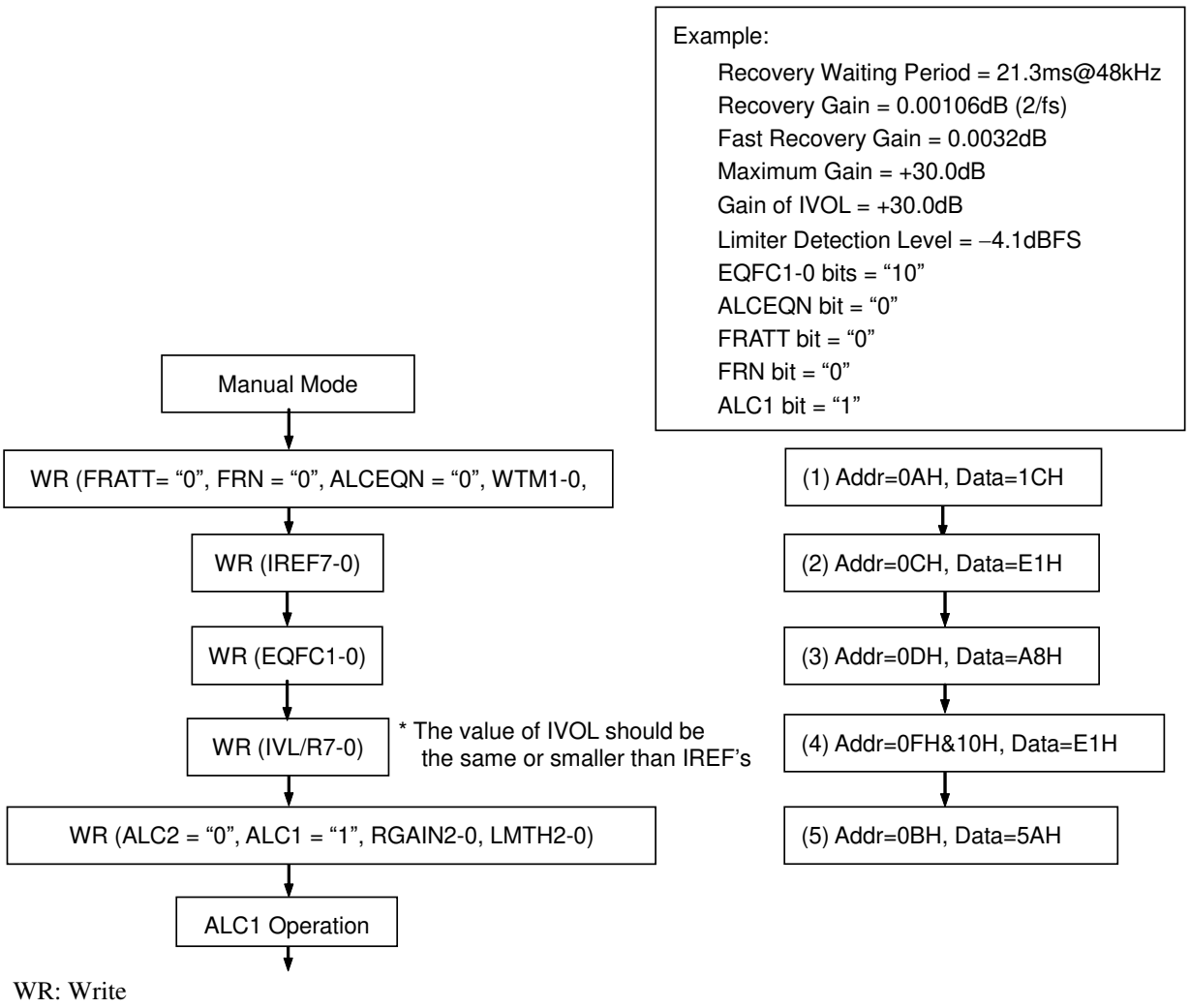


Figure 49. Registers Set-up Sequence at ALC1 Operation (Recording path)

6. ALC REF Inflection Point Setting for Recording

The AK4958 can change the slope of recovery reference value (IREF7-0 bits) on an inflection point set by RF2P2-0 bits at recording ALC (ADC side). RF2SL2-0 bits control the slope of recovery reference value that is after the inflection point. (In the following description, recovery reference values before the inflection point are described as REF1 (set by IREF7-0 bits), and recovery reference values after the inflection point are described as REF2.) ALC bit must be "0" when changing RF2P2-0 bits setting. RF2SL2-0 bits can be set regardless of ALC bit setting. RF2P2-0 bits and RF2SL2-0 bits cannot be used when playback (DAC side) or when REF value < 0dB.

When changing the REF2 slope from "1.0" to any value other than "1.0" (REF2SL2-0 bits = "000" → "xxx"), the output volume changes to REF2 value immediately. When setting the REF2 slope to "1.0" from any value other than "1.0" (REF2SL2-0 bits = "xxx" → "000"), the output volume changes to REF1 value according to the ALC recovery setting.

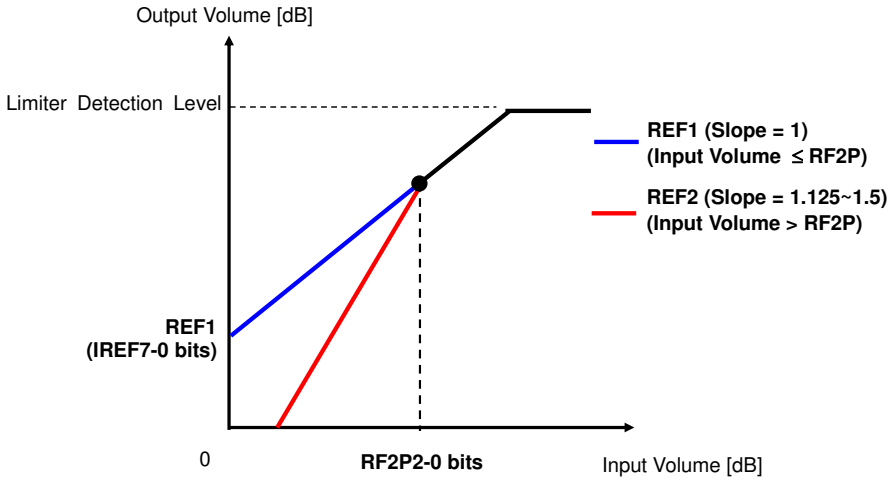


Figure 50. ALC REF Slope when Recording

RF2P2-0 bits	RF2P[dB]	Step	
000	–33	3dB	(default)
001	–36		
010	–39		
011	–42		
100	–45		
101	–48		
110	–51		
111	–54		

Table 51 Inflection Point RF2P Setting

RF2SL2-0 bits	REF2 Slope	
000	1.0	(default)
001	1.125	
010	1.25	
011	1.375	
100	1.5	
Others	N/A	

Table 52 REF2 Inflection Setting (N/A: Not available)

■ Input Digital Volume (Manual Mode)

The input digital volume becomes manual mode when ALC1 bit is set to "0" while ADCPF bit is "1". This mode is used in the cases shown below.

1. After exiting reset state, when setting up the registers for ALC operation (LMTH and etc.)
2. When the registers for ALC operation (Limiter period, Recovery period and etc.) are changed. For example; when the sampling frequency is changed.
3. When IVOL is used as a manual volume control.

IVL7-0 and IVR7-0 bits set the gain of the volume control (Table 53). Lch and Rch volumes are set individually by IVL7-0 and IVR7-0 bits when IVOLC bit = "0". IVL7-0 bits control both Lch and Rch volumes together when IVOLC bit = "1".

This volume has a soft transition function. Therefore no switching noise occurs during the transition. IVTM bit set the transition time (Table 54). When IVTM bit = "1", it takes 944/fs (19.7ms@fs=48kHz) from F1H(+36dB) to 05H(-52.5dB). The volume is muted after transitioned to -72dB in the period set by IVTM bit (236/fs=4.9ms @fs=48kHz) when changing the volume from 05H (-52.5dB) to 00H (MUTE).

IVL7-0 bits IVR7-0 bits	GAIN (dB)	Step	
F1H	+36.0	0.375dB	
F0H	+35.625		
EFH	+35.25		
:	:		
E2H	+30.375		
E1H	+30.0		(default)
E0H	+29.625		
:	:		
92H	+0.375		
91H	0.0		
90H	–0.375		
:	:		
06H	–52.125		
05H	–52.5		
04H~00H	MUTE		

Table 53. Input Digital Volume Setting

IVTM bit	Transition Time of Input/Output Digital Volume IVL/R7-0 OVL/R7-0 bits = "F1H" → "05H"			
	Setting Value	fs=8kHz	fs=48kHz	
0	236/fs	29.5ms	4.9ms	
1	944/fs	118ms	19.7ms	(default)

Table 54. Transition Time of Input/Output Digital Volume

If IVL7-0 or IVR7-0 bits are written during PMPFIL bit = "0", IVOL operation starts with the written values after PMPFIL bit is changed to "1".

■ Output Digital Volume (Manual Mode)

The ALC block becomes output digital volume (manual mode) by setting ALC2 bit to "0" when PMPFIL = PMDAC bits = "1" and ADCPF bit is "0". The output digital volume gain is set by the OVL7-0 bit and the OVR7-0 bit (Table 55). When the OVOLC bit = "1", the OVL7-0 bits control both L and R channel volume levels. When the OVOLC bit = "0", the OVL7-0 bits control L channel volume level and the OVR7-0 bits control R channel volume level. When changing the volumes, zero cross detection is executed on both L and R channels independently. The OVOL value is changed at zero crossing or timeout. The zero crossing timeout period is set by ZTM1-0 bits.
This volume has a soft transition function. Therefore no switching noise occurs during the transition. IVTM bit set the transition time (Table 54). When IVTM bit = "1", it takes 944/fs (19.7ms@fs=48kHz) from F1H(+36dB) to 05H(-52.5dB). The volume is muted after transitioned to -72dB in the period set by IVTM bit (208/fs=4.3ms @fs=48kHz) when changing the volume from 05H (-52.5dB) to 00H (MUTE).

OVL7-0 bits OVR7-0 bits	GAIN [dB]	Step	
F1H	+36.0	0.375dB	
F0H	+35.625		
EFH	+35.25		
:	:		
92H	+0.375		
91H	0.0		(default)
90H	-0.375		
:	:		
06H	-52.125		
05H	-52.5		
04H~00H	MUTE		

Table 55. Output Digital Volume Setting

IVTM bit	Transition Time of Input/Output Digital Volume IVL/R7-0 OVL/R7-0 bits = "F1H" → "05H"			
	Setting Value	fs=8kHz	fs=48kHz	
0	236/fs	29.5ms	4.9ms	
1	944/fs	118ms	19.7ms	(default)

Table 54. Transition Time of Input/Output Digital Volume

<Mono Mixing Output>

Mono mixing outputs are available by setting MONO1-0 bits. Input data from the SDTI pin can be converted to mono signal [(L+R)/2] and are output via LOUT and ROUT pins. (Figure 36)

Set MONO1-0 bits to "11" when using the Bass Boost circuit. Bass boosting is applied to only L channel signal and R channel signal is output without a bass boost if MONO1-0 bits are set to "00" (default). When MONO1-0 bits = "01", L channel signal is output with a bass boost from both channels. When MONO1-0 bits = "10", R channel signal is output with a bass boost from both channels.

MONO1 bit	MONO0 bit	LOUT pin	ROUT pin	
0	0	Lch	Rch	(default)
0	1	Lch	Lch	
1	0	Rch	Rch	
1	1	(Lch+Rch)/2	(Lch+Rch)/2	

Table 56. Output Data Switching of ADC or SDTI Outputs

■ Bass Boost Circuit

The AK4958 has a monaural bass boost circuit for speaker outputs. The monaural mixing signal is bass boosted and output to speakers. The bass boost circuit consists of a HPF, a LPF and three BPF's. It is enabled by setting BSTON bit and PMDAC bit to "1", and boots low band according to the cutoff frequency of the speakers improving the sound quality. The audio data passes this bock by 0dB gain when BSTON bit = "0".
The bass boost circuit automatically boosts bass sound by degrees from the default level. BGN5-0 bits control the bass boost maximum level of the circuit. If the bass boost circuit output exceeds the litter level, boost level is attenuated by the limiter. BGN5-0 bits must be set when BSTON bit = "0" or PMDAC bit = "0"

Set MONO1-0 bits to "11" when using the Bass Boost circuit. Bass boosting is applied to only L channel signal if MONO1-0 bits are set to "00" (default).

BGN5-0 bits	BGN_DATA	Gain	Boost Level	
00H	0	Mute	Not Boost	(default)
01H	1	$20 \log_{10}$ (BGN_DATA/4)	Low ⇩ High	
02H	2			
:	:			
3EH	62			
3FH	63			

Table 57. Bass Boost Level Setting

(1) High Pass Filter (HPF4)

This is composed 1st order HPF. The coefficient of HPF is set by BHA7-0 bits and BHB7-0 bits. The coefficient must be set when BSTON bit = "0" or PMDAC bit = "0". The HPF starts operation in 4/fs(max) after BSTON bit or PMDAC bit= "1" is set.

fs: Sampling frequency
fc: Cut-off frequency

Register setting (Note 55)
HPF4: BHA[7:0] bits =A, BHB[7:0] bits =B
(MSB=BHA7, BHB7; LSB=BHA0, BHB0)

$$A = \frac{1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

Transfer function

$$H(z) = A \frac{1 - z^{-1}}{1 + Bz^{-1}}$$

The cut-off frequency must be set as below.
fc ≥ 250Hz

(2) Low Pass Filter (LPF2)

This is composed with 1st order LPF. BLA7-0 bits and BLB7-0 bits set the coefficient of LPF. The coefficient must be set when BSTON bit = "0" or PMDAC bit = "0". The LPF starts operation in 4/fs (max) after BSTON bit or PMDAC bit= "1" is set.

fs: Sampling frequency
fc: Cut-off frequency

Register setting (Note 55)
LPF: BLA[7:0] bits =A, BLB[7:0] bits =B
(MSB= BLA7, BLB7; LSB=BLA0, BLB0)

$$A = \frac{1}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

Transfer function

$$H(z) = A \frac{1 + z^{-1}}{1 + Bz^{-1}}$$

The cut-off frequency must be set as below.
fc ≥ 500Hz

(3) Band Pass Filter (BPF1, BPF2, BPF3)

This is composed with 2nd order BPF. BB1A7-0, BB1B7-0 and BB1C7-0 bits set the coefficient of BPF1. BB2A7-0, BB2B7-0 and BB2C7-0 bits set the coefficient of BPF2. BB3A7-0, BB3B7-0 and BB3C7-0 bits set the coefficient of BPF3. The coefficient must be set when BSTON bit = "0" or PMDAC bit = "0". BPF1-3 start operation in 4/fs (max) after BSTON and PMDAC bits are set to "1".

fs: Sampling frequency
fo_1 ~ fo_3: Center frequency
fb_1 ~ fb_3: Band width where the gain is 3dB different from center frequency

Register setting
BPF1: BB1A[7:0] bits =A_1(Note 55), BB1B[15:0] bits =B_1, BB1C[15:0] bits =C_1(Note 49)
BPF2: BB2A[7:0] bits =A_2(Note 55), BB2B[15:0] bits =B_2, BB2C[15:0] bits =C_2(Note 49)
BPF3: BB3A[7:0] bits =A_3(Note 55), BB3B[15:0] bits =B_3, BB3C[15:0] bits =C_3(Note 49)
(MSB=BB1A7, BB1B15, BB1C15, BB2A7, BB2B15, BB2C15, BB3A7, BB3B15, BB3C15,
LSB=BB1A0, BB1B0, BB1C0, BB2A0, BB2B0, BB2C0, BB3A0, BB3B0, BB3C0)

$$A_n = 8 \times \frac{\tan(\pi fb_n/fs)}{1+\tan(\pi fb_n/fs)}, \quad B_n = \cos(2\pi fo_n/fs) \times \frac{2}{1+\tan(\pi fb_n/fs)}, \quad C_n = -\frac{1-\tan(\pi fb_n/fs)}{1+\tan(\pi fb_n/fs)}$$

(n =1, 2, 3)

Transfer function

$$H_n(z) = \frac{A_n}{8} \times \frac{1-z^{-2}}{1-B_n z^{-1}-C_n z^{-2}}$$

(n = 1, 2, 3)

The center frequency must be set as below.
$250Hz \le fo_n \le 3000Hz$, $40Hz \le fb_n \le 300Hz$

Note 55.[Translation the filter coefficient calculated by the equations above from real number to binary code (2's complement)]
X=(Real number of filter coefficient calculated by the equations above) x 2^7 (HPF4, LPF2, BPFAn coefficient)
X=(Real number of filter coefficient calculated by the equations above) x 2^{13} (BPFBn, BPFCn coefficient)

X must be rounded to integer, and then should be translated to binary code (2's complement).
MSB of each filter coefficient setting register is sine bit.

Note 56. Coefficient setting examples of each filter are shown below.
Assuming the speaker cutoff frequency = FC,
HPF4 fc = FC/2;
LPF2 fc = FC;
BPF1 fo1 = FC/3, fb1 = 150Hz
BPF2 fo2 = FC*2/3, fb2 = 50Hz
BPF3 fo3 = FC, fb3 = 50Hz

■ 3band DRC Operation

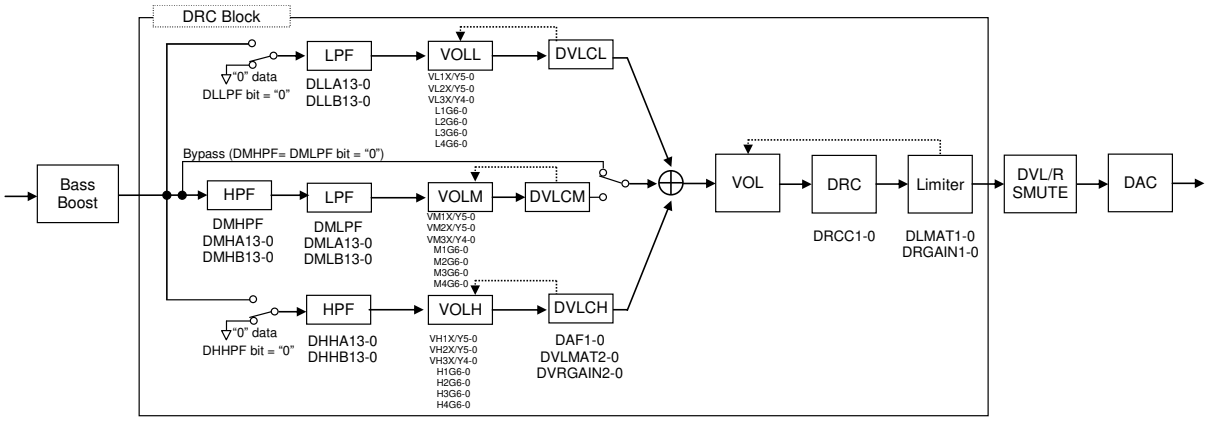


Figure 51. 3band DRC Functions and Signal Path

1. 3band Dynamic Volume Control Block

The AK4958 has a dynamic volume control circuit before DRC bock. The frequency band is divided into three ranges (Low, Middle and High), and this controller is able to control the frequency band independently.

(1) Low Frequency Range

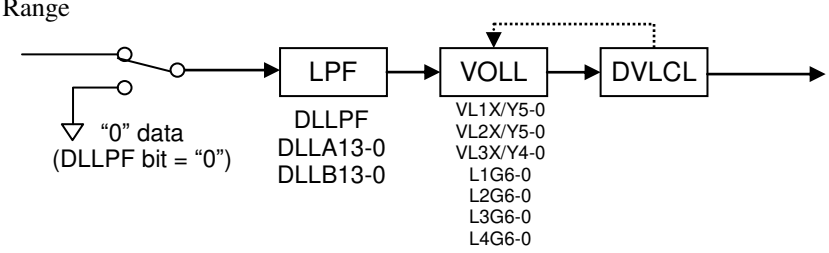


Figure 52. DVLC Functions and Signal Path for Low Frequency Range

(1-1) Low Pass Filter (LPF)

This is composed with 1st order LPF. The coefficient of LPF is set by DLLA13-0 bits and DLLB13-0 bits. When the LPF is OFF, the audio data does not pass this block. The coefficient must be set when DLLPF bit, PMDAC bit or DRC bit = "0". The LPF starts operation in 4/fs (max) after DLLPF bit, DRC bit and PMDAC bit are set to "1".

DLLPF bit	Mode	
0	OFF ("0" data)	(default)
1	ON	

Table 58. DLLPF Operation Switch

fs: Sampling frequency
fc: Cut-off frequency

Register setting
LPF: DLLA[13:0] bits =A, DLLB[13:0] bits =B
(MSB=DLLA13, DLLB13; LSB=DLLA0, DLLB0)

$$A = \frac{1}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

Transfer function

$$H(z) = A \frac{1 + z^{-1}}{1 + Bz^{-1}}$$

The cut-off frequency must be set as below.
fc/fs ≥ 0.002 (fc min = 96Hz at 48kHz)

(1-2) Dynamic Volume Control Curve

The inflection points of the DVLC curve is set by three coordinate values (VL1X5-0, VL1Y5-0, VL2X5-0, VL2Y5-0, VL3X4-0 and VL3Y4-0 bits). The setting of three inflection points are calculated the values of ($X1_L$, $Y1_L$), ($X2_L$, $Y2_L$), ($X3_L$, $Y3_L$) in dB. The inflection points should be set in such a way that VL1X ≤ VL2X ≤ VL3X, VL1Y ≤ VL2Y ≤ VL3Y. And the each slope is set by L1G6-0, L2G6-0, L3G6-0 and L4G6-0 bits. $X4_L$ is fixed full-scale, $Y4_L$ is calculated by the L4G value. The initial value of the DVLC gain is set by the L1G. The inflection points and the slope setting must be made when PMDAC bit = "0" or DRC bit = "0". DVLC starts operation in 4/fs (max) after DRC bit or PMDAC bit is set to "1".

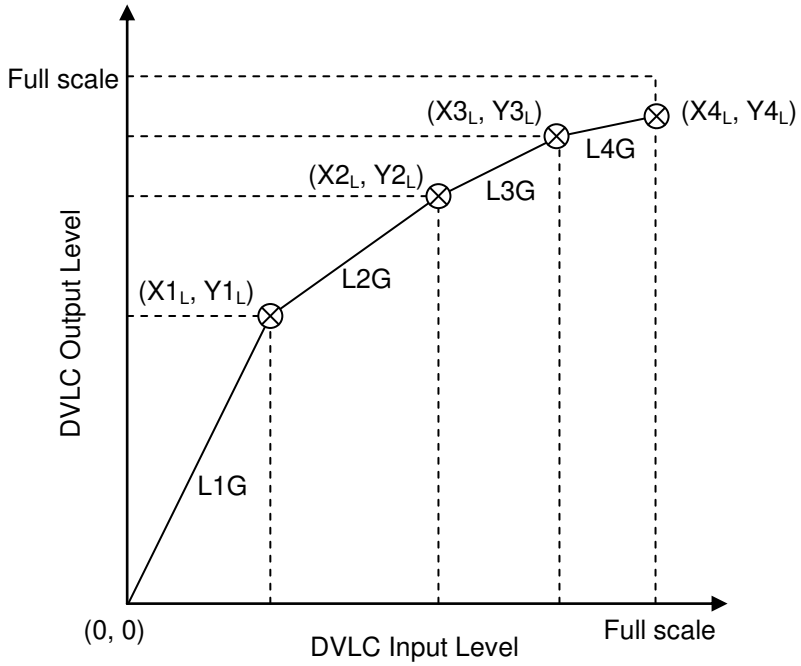


Figure 53. DVLC Curve for Low Frequency Range

VL1X/Y5-0 bits VL2X/Y5-0 bits	Dynamic Volume Control Point [dB]	Step	
00H	0	1.5dB	(default)
01H	−1.5		
:	:		
2EH	−69.0		
2FH	−70.5		
30H	N/A	N/A	
:	:		
3FH	N/A		

Table 59. DVLC Point Setting for X/Y1, X/Y2 for Low Frequency Range (N/A: Not available)

VL3X/Y4-0 bits	Dynamic Volume Control Point [dB]	Step	
00H	0	1.5dB	(default)
01H	–1.5		
02H	–3.0		
:	:		
1EH	–45.0		
1FH	–46.5		

Table 60. DVLC Point Setting for X/Y3 for Low Frequency Range

Slope Setting

$$L1G = \frac{Y1_L}{X1_L} \times 16, \qquad L2G = \frac{(Y2_L - Y1_L)}{(X2_L - X1_L)} \times 16,$$

$$L3G = \frac{(Y3_L - Y2_L)}{(X3_L - X2_L)} \times 16, \quad L4G = \frac{(Y4_L - Y3_L)}{(X4_L - X3_L)} \times 16,$$

The results calculated by the equations above should be rounded off to integer. These integers are the slope data.

L1G6-0 bits, L2G6-0 bits, L3G6-0 bits, L4G6-0 bits	Slope Data	
00H	0	(default)
01H	1	
02H	2	
:	:	
7EH	126	
7FH	127	

Table 61. DVLC Slope Setting for Low Frequency Range

(2) Middle Frequency Range

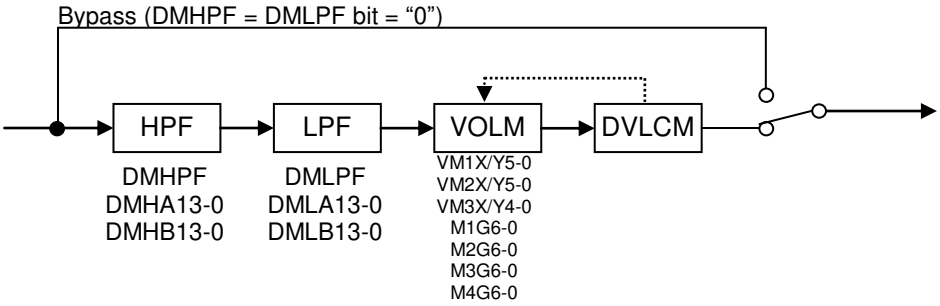


Figure 54. DVLC Functions and Signal Path for Middle Frequency Range

(2-1) High Pass Filter (HPF)

This is composed with 1st order HPF. The coefficient of HPF is set by DMHA13-0 bits and DMHB13-0 bits. HPF bit controls ON/OFF of the HPF. When the HPF is OFF, the audio data passes this block by 0dB gain. The coefficient must be set when DMHPF bit = "0", PMDAC bit = "0" or DRC bit = "0". The HPF starts operation in 4/fs (max) after DMHPF bits = "1", PMDAC bit = "1" or DRC bit = "1" is set.

DMHPF bit	Mode	
0	Bypass	(default)
1	ON	

Table 62. DMHPF Mode Setting

fs: Sampling frequency
fc: Cut-off frequency

Register setting
HPF: DMHA[13:0] bits =A, DMHB[13:0] bits =B
(MSB=DMHA13, DMHB13; LSB=DMHA0, DMHB0)

$$A = \frac{1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

Transfer function

$$H(z) = A \frac{1 - z^{-1}}{1 + Bz^{-1}}$$

The cut-off frequency should be set as below.
fc/fs ≥ 0.0001 (fc min = 4.8Hz at 48kHz)

(2-2) Low Pass Filter (LPF)

This is composed with 1st order LPF. DMLA13-0 bits and DMLB13-0 bits set the coefficient of LPF. DMLPF bit controls ON/OFF of the LPF. When the LPF is OFF, the audio data passes this block by 0dB gain. The coefficient must be set when DMLPF bit = "0", PMDAC bit= "0" or DRC bit = "0". The LPF starts operation in 4/fs (max) after DMLPF bit = "1", PMDAC bit = "1" or DRC bit = "1" is set.

DMLPF bit	Mode	
0	Bypass	(default)
1	ON	

Table 63. DMLPF Mode Setting

fs: Sampling frequency
fc: Cut-off frequency

Register setting
LPF: DMLA[13:0] bits =A, DMLB[13:0] bits =B
(MSB=DMLA13, DMLB13; LSB=DMLA0, DMLB0)

$$A = \frac{1}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

Transfer function

$$H(z) = A \frac{1 + z^{-1}}{1 + Bz^{-1}}$$

The cut-off frequency should be set as below.
fc/fs ≥ 0.05 (fc min = 2400Hz at 48kHz)

(2-3) Dynamic Volume Control Curve

The inflection points of the DVLC curve is set by three coordinate values (VM1X5-0, VM1Y5-0, VM2X5-0, VM2Y5-0, VM3X4-0 and VM3Y4-0 bits). The setting of three inflection points are calculated the values of ($X1_M$, $Y1_M$), ($X2_M$, $Y2_M$), ($X3_M$, $Y3_M$) in dB. The inflection points should be set in such a way that VM1X ≤ VM2X ≤ VM3X, VM1Y ≤ VM2Y ≤ VM3Y. And the each slope is set by M1G6-0, M2G6-0, M3G6-0 and M4G6-0 bits. $X4_M$ is fixed full-scale, $Y4_M$ is calculated by the M4G value. The initial value of the DVLC gain is set by the M1G. When the HPF and LPF is bypass (DMHPF1-0 = DMLPF1-0 bits = "00"), the audio data passes this block by 0dB gain. The inflection points and the slope setting must be made when PMDAC bit = "0" or DRC bit = "0" or HPF and LPF are bypassed (DMHPF = DMLPF bits = "0"). DVLC starts operation in 4/fs (max) after DRC bit or PMDAC bit is set to "1".

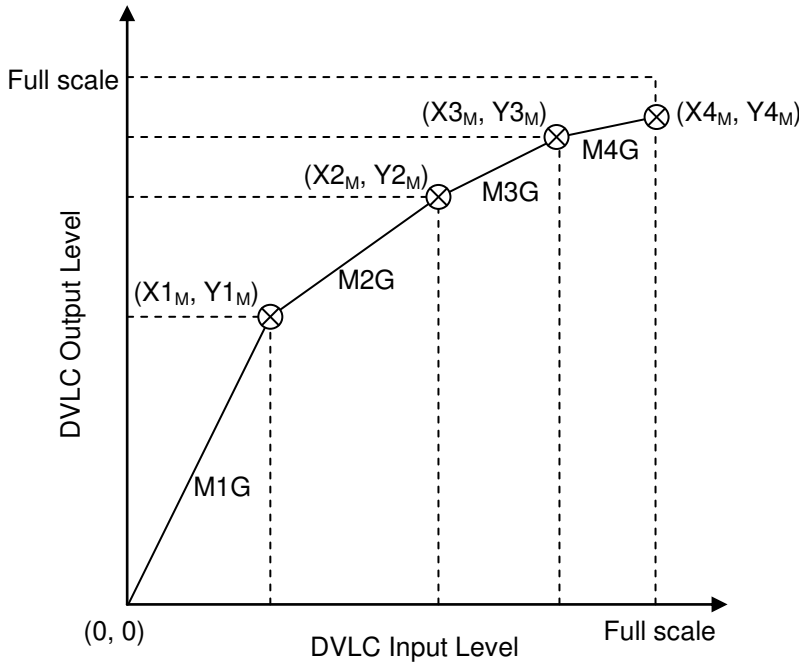


Figure 55. DVLC Curve for Middle Frequency Range

VM1X/Y5-0 bits VM2X/Y5-0 bits	Dynamic Volume Control Point [dB]	Step	
00H	0	1.5dB	(default)
01H	–1.5		
02H	–3.0		
:	:		
2EH	–69.0		
2FH	–70.5		
30H	N/A	N/A	
:	:		
3FH	N/A		

Table 64. DVLC Point Setting for X/Y1, X/Y2 for Middle Frequency Range (N/A: Not available)

VM3X/Y4-0 bits	Dynamic Volume Control Point [dB]	Step	
00H	0	1.5dB	(default)
01H	–1.5		
02H	–3.0		
:	:		
1EH	–45.0		
1FH	–46.5		

Table 65. DVLC Point Setting for X/Y3 for Middle Frequency Range

Slope Setting

$$M1G = \frac{Y1_M}{X1_M} \times 16, \qquad M2G = \frac{(Y2_M - Y1_M)}{(X2_M - X1_M)} \times 16,$$

$$M3G = \frac{(Y3_M - Y2_M)}{(X3_M - X2_M)} \times 16, \quad M4G = \frac{(Y4_M - Y3_M)}{(X4_M - X3_M)} \times 16,$$

The results calculated by the equations above should be rounded off to integer. These integers are the slope data.

M1G6-0 bits, M2G6-0 bits, M3G6-0 bits, M4G6-0 bits	Slope Data	
00H	0	(default)
01H	1	
02H	2	
:	:	
7EH	126	
7FH	127	

Table 66. DVLC Slope Setting for Middle Frequency Range

(3) High Frequency Range

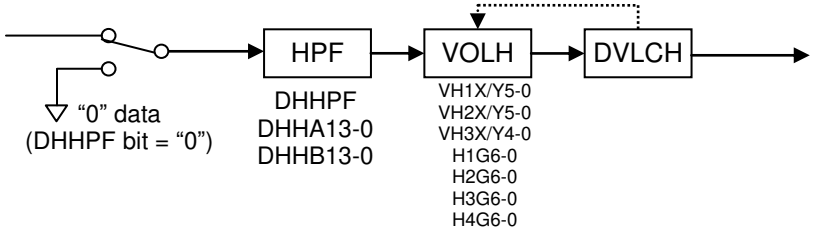


Figure 56. DVLC Functions and Signal Path for High Frequency Range

(3-1) High Pass Filter (HPF)

This is composed with 1st order HPF. The coefficient of HPF is set by DHHA13-0 bits and DHHB13-0 bits. DHHPF1-0 bits control ON/OFF of the HPF. When the HPF is OFF, the audio data does not pass this block. The coefficient must be set when DHHPF bit = "0", PMDAC bit = "0" or DRC bit = "0". The HPF starts operation in 4/fs (max) after DHHPF bit = "1", PMDAC bit = "1" or DRC bit = "1" is set.

DHHPF bit	Mode	
0	OFF ("0" data)	(default)
1	ON	

Table 67. DHHPF Mode Setting

fs: Sampling frequency
fc: Cut-off frequency

Register setting
HPF: DHHA[13:0] bits =A, DHHB[13:0] bits =B
(MSB=DHHA13, DMHB13; LSB=DHHA0, DHHB0)

$$A = \frac{1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

Transfer function (1st order)

$$H(z) = A \frac{1 - z^{-1}}{1 + Bz^{-1}}$$

The cut-off frequency should be set as below.
$fc/fs \geq 0.0001$ (fc min = 4.8Hz at 48kHz)

Note 57. [Translation the filter coefficient calculated by the equations above from real number to binary code (2's complement)]
X=(Real number of filter coefficient calculated by the equations above) x 2^{13}

X must be rounded to integer, and then should be translated to binary code (2's complement).
MSB of each filter coefficient setting register is sine bit.

(3-2) Dynamic Volume Control Curve

The inflection points of the DVLC curve is set by three coordinate values (VH1X5-0, VH1Y5-0, VH2X5-0, VH2Y5-0, VH3X4-0 and VH3Y4-0 bits). The setting of three inflection points are calculated the values of ($X1_H$, $Y1_H$), ($X2_H$, $Y2H_H$), ($X3_H$, $Y3_H$) in dB. The inflection points should be set in such a way that VH1X ≤ VH2X ≤ VH3X, VH1Y ≤ VH2Y ≤ VH3Y. And the each slope is set by H1G6-0, H2G6-0, H3G6-0 and H4G6-0 bits. $X4_H$ is fixed full-scale, $Y4_H$ is calculated by the H4G value. The initial value of the DVLC gain is set by the H1G. The inflection points and the slope setting must be made when PMDAC bit = "0" or DRC bit = "0". DVLC starts operation in 4/fs (max) after DRC bit or PMDAC bit is set to "1".

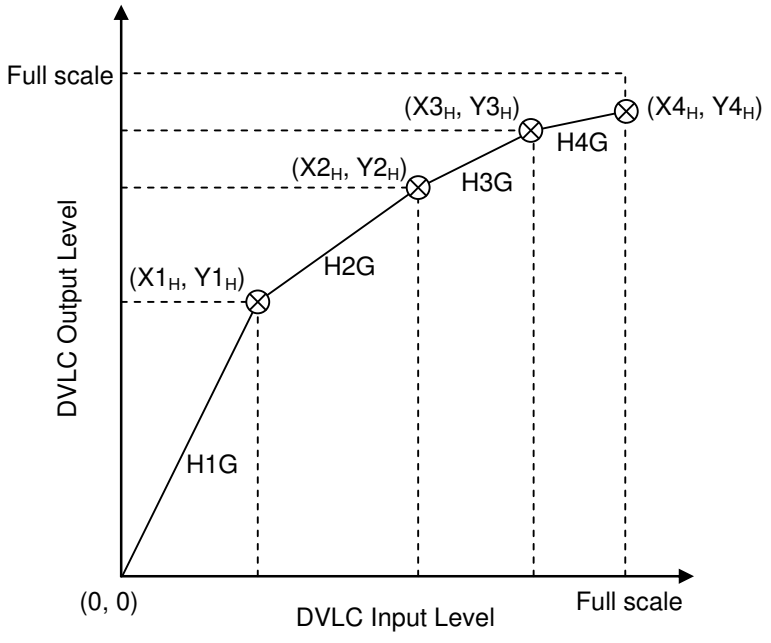


Figure 57. DVLC Curve for High Frequency Range

VH1X/Y5-0 bits VH2X/Y5-0 bits	Dynamic Volume Control Point [dB]	Step	
00H	0	1.5dB	(default)
01H	–1.5		
02H	–3.0		
:	:		
2EH	–69.0		
2FH	–70.5		
30H	N/A	N/A	
:	:		
3FH	N/A		

Table 68. DVLC Point Setting for X/Y1, X/Y2 for High Frequency Range (N/A: Not available)

VH3X/Y4-0 bits	Dynamic Volume Control Point [dB]	Step	
00H	0	1.5dB	(default)
01H	–1.5		
02H	–3.0		
:	:		
1EH	–45.0		
1FH	–46.5		

Table 69. DVLC Point Setting for X/Y3 for High Frequency Range

Slope Setting

$$H1G = \frac{Y1_H}{X1_H} \times 16, \qquad H2G = \frac{(Y2_H - Y1_H)}{(X2_H - X1_H)} \times 16,$$

$$H3G = \frac{(Y3_H - Y2_H)}{(X3_H - X2_H)} \times 16, \quad H4G = \frac{(Y4_H - Y3_H)}{(X4_H - X3_H)} \times 16$$

The results calculated by the equations above should be rounded off to integer. These integers are the slope data.

H1G6-0 bits, H2G6-0 bits, H3G6-0 bits, H4G6-0 bits	Slope Data	
00H	0	(default)
01H	1	
02H	2	
:	:	
7EH	126	
7FH	127	

Table 70. DVLC Slope Setting for High Frequency Range

(4) Dynamic Volume Control

The DVLC automatically controls the volume at the attenuation speed set by DVLMAT2-0 bits (Table 72) or the recovery speed set by DVRGAIN2-0 bits (Table 73) in such a way that the input moving average level set by DAF1-0 bits (Table 71) is reached the output level of the DVLC curve set by each frequency range. DAF1-0 bits, DVLMAT2-0 bits or DVRGAIN2-0 bits must be set when DRC bit or PMDAC bit = "0".

DAF1-0 bits	Moving Average Parameter (Time Constant)				
		fs=8kHz	fs=16kHz	fs=48kHz	
00	256/fs	32ms	16ms	5.3ms	
01	512/fs	64ms	32ms	10.7ms	
10	1024/fs	128ms	64ms	21.3ms	
11	2048/fs	256ms	128ms	42.7ms	(default)

Table 71. DVLC Moving Average Parameter Setting (Time Constant)

DVLMAT2 bit	DVLMAT1 bit	DVLMAT0 bit	ATT Speed			
			8kHz	16kHz	48kHz	
0	0	0	1.1dB/s	2.1dB/s	6.4dB/s	
0	0	1	2.1dB/s	4.2dB/s	12.7dB/s	
0	1	0	4.2dB/s	8.5dB/s	25.4dB/s	
0	1	1	8.5dB/s	17.0dB/s	50.9dB/s	(default)
1	0	0	17.0dB/s	33.9dB/s	101.8dB/s	
1	0	1	33.9dB/s	67.9dB/s	203.6dB/s	
1	1	0	67.9dB/s	135.8dB/s	407.2dB/s	
1	1	1	N/A			

Table 72. DVLC ATT Speed Setting (N/A: Not Available)

DVRGAIN2 bit	DVRGAIN1 bit	DVRGAIN0 bit	Recovery Speed			
			8kHz	16kHz	48kHz	
0	0	0	0.07dB/s	0.13dB/s	0.40dB/s	
0	0	1	0.13dB/s	0.27dB/s	0.80dB/s	
0	1	0	0.27dB/s	0.53dB/s	1.59dB/s	
0	1	1	0.53dB/s	1.06dB/s	3.18dB/s	(default)
1	0	0	1.06dB/s	2.12dB/s	6.36dB/s	
1	0	1	2.12dB/s	4.24dB/s	12.72dB/s	
1	1	0	4.24dB/s	8.48dB/s	25.45dB/s	
1	1	1	N/A			

Table 73. DVLC Recovery Speed Setting (N/A: Not Available)

2. Dynamic Range Control Block

The AK4958 has the dynamic range control (DRC) circuits. The compression level is selected in three levels and set by DRCC1-0 bits (Table 74).

When the DRC is OFF (DRCC1-0 bits = "00"), the audio data passes this block by 0dB gain. However limiter and recovery operation is always ON. The compression level must be set when PMDRC bit = "0" or DRC bit = "0".

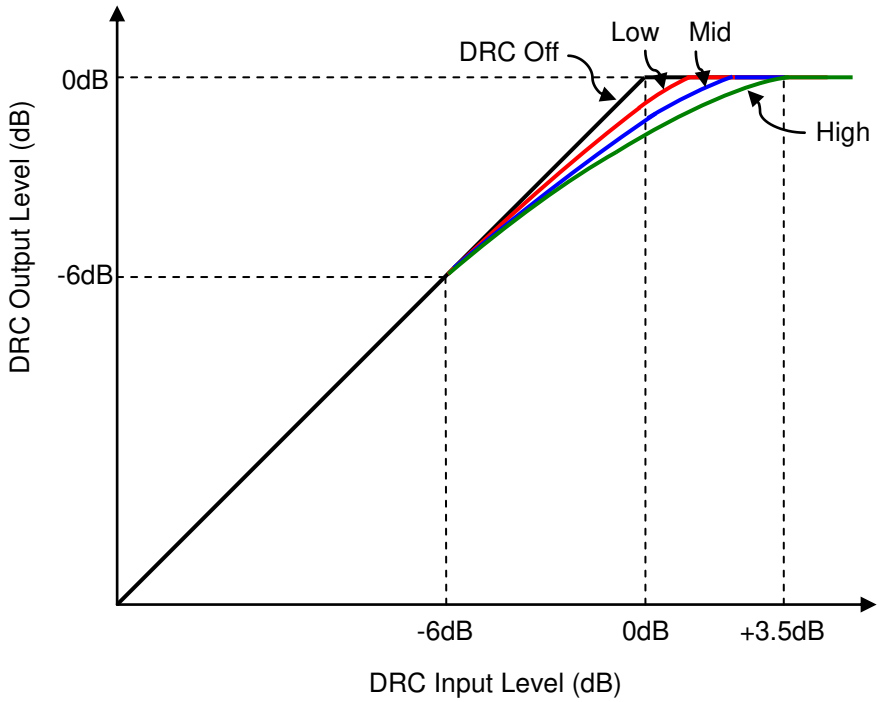


Figure 58. DRC Gain Curve

DRCC1 bit	DRCC0 bit	Compression Level	
0	0	OFF	(default)
0	1	Low	
1	0	Middle	
1	1	High	

Table 74. DRC Compression Level Setting

1. DRC Limiter Operation

During the DRC limiter operation, when the output level of DRC exceeds full-scale, the DRC volume are attenuated automatically with the soft transition in the attenuation speed set by DLMAT2-0 bits (Table 75). DLMAT2-0 bits must be set when DRC bit or PMDAC bit = "0".

DLMAT2 bit	DLMAT1 bit	DLMAT0 bit	ATT Speed			
			8kHz	16kHz	48kHz	
0	0	0	0.1dB/ms	0.3dB/ms	0.8dB/ms	(default)
0	0	1	0.3dB/ms	0.5dB/ms	1.6dB/ms	
0	1	0	0.5dB/ms	1.1dB/ms	3.3dB/ms	
0	1	1	1.1dB/ms	2.2dB/ms	6.5dB/ms	
1	0	0	2.2dB/ms	4.3dB/ms	13.0dB/ms	
1	0	1	4.3dB/ms	8.7dB/ms	26.1dB/ms	
1	1	0	N/A			
1	1	1				

Table 75. DRC ATT Speed Setting (N/A: Not Available)

2. DRC Recovery Operation

During the DRC recovery operation, when the DRC volume reaches 0dB or the output level of DRC exceeds limiter detection level, the DRC volume are set automatically with the soft transition in the recovery speed set by DRGAIN1-0 bits (Table 76). DRGAIN1-0 bits must be set when DRC bit or PMDAC bit = "0".

DRGAIN1 bit	DRGAIN0 bit	Recovery Speed			
		8kHz	16kHz	48kHz	
0	0	1.1dB/s	2.1dB/s	6.4dB/s	(default)
0	1	2.1dB/s	4.2dB/s	12.7dB/s	
1	0	4.2dB/s	8.5dB/s	25.4dB/s	
1	1	8.5dB/s	17.0dB/s	50.9dB/s	

Table 76. DRC Recovery Speed Setting

■ Output Digital Volume 2

The AK4958 has a digital output volume (193 levels, 0.5dB step, Mute). The volume is included in front of a DAC block. The input data of DAC is changed from +6 to –89.5dB or MUTE. The DVOL7-0 bits control both Lch and Rch volume levels together. This volume has soft transition function. In automatic attenuation, the volume is attenuated by soft transition in 194/fs or 776/fs to reduce switching noises. When DVTM bit = "0", it takes 776/fs (16.2ms@fs=48kHz) from 00H (+6dB) to C0H (MUTE).

DVOL7-0 bits	Gain	Step	
00H	+6.0dB	0.5dB	(default)
01H	+5.5dB		
02H	+5.0dB		
:	:		
0CH	0dB		
:			
BEH	–89.0dB		
BFH	–89.5dB		
C0H	Mute (– ∞)		

Table 77. Output Digital Volume2 Setting

DVTM bit	Transition Time between DVOL7-0 bits = 00H and C0H			
	Setting	fs=8kHz	fs=48kHz	
0	776/fs	97ms	16.2ms	(default)
1	194/fs	24.3ms	4ms	

Table 78. Transition Time Setting of Output Digital Volume2

■ Soft Mute

Soft mute operation is performed in the digital domain. When the SMUTE bit is set "1", the output signal is attenuated by -∞ ("0") during the cycle set by DVTM bit. When the SMUTE bit is returned to "0", the mute is cancelled and the output attenuation gradually changes to the value set by DVOL7-0 bits from -∞ during the cycle set by DVTM bit. If the soft mute is cancelled within the cycle set by DVTM bit after starting the operation, the attenuation is discontinued and returned to the level set by DVOL7-0 bits. The soft mute is effective for changing the signal source without stopping the signal transaction.

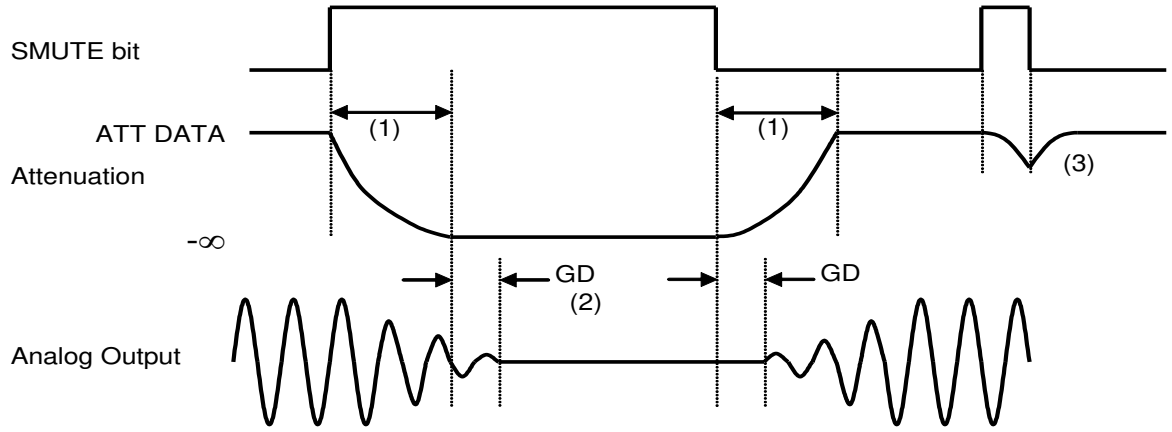


Figure 59. Soft Mute Function

(1) The input signal is attenuated to −∞ ("0") in the cycle set by DVTM bit. When ATT DATA = +6dB (00H), 194/fs = 4ms@ fs=48kHz, DVTM bit= "1".
(2) Analog output corresponding to digital input has group delay (GD).
(3) If soft mute is cancelled before attenuating to −∞, the attenuation is discounted and returned to the level set by DVOL7-0 bits within the same cycle.

■ BEEP Input

When BEEPS bit is set to "1" during PMBP bit= "1", the input signal from the BEEP pin is output to Speaker-Amp. When BEEPL bit is set to "1", the input signal from the BEEP pin is output to the stereo line output amplifier. An external resistor R_i (Figure 61) adjusts the signal level of BEEP input when BPM bit = "1". Table 82 and Table 83 show the typical gain example when R_i = 66kΩ. This gain is in inverse proportion to the R_i value. When BPM bit = "0", the external resistor R_i is not necessary. BPLVL3-0 bits set the gain of BEEP-Amp, and the total gain is defined according to LVCM1-0 and SPKG1-0 bits settings.

BPM bit	BEEP Mode	
0	Internal Resistance Mode	(default)
1	External Resistance Mode	

Table 79. BEEP Mode Setting

1. BEEP-Amp Common Potential

BPVCM bit set the common voltage of BEEP input amplifier. (Table 80)

Note 16. The maximum value is AVDD Vpp when BPVCM bit = "1". However, a click noise may occur when the amplitude after BEEP-Amp is 0.5Vpp or more. (set by BPLVL3-0 bits)

BPVCM bit	BEEP-Amp Common Voltage (typ)	
0	1.15V	(default)
1	1.65V	

Table 80. Common Potential Setting of BEEP-Amp

• Internal Resistance Mode (BPM bits = "0")

Input BEEP gain is controlled by BPLVL3-0 bits (Table 81). In this case an external resistor R_i is not necessary.

BPLVL3 bit	BPLVL2 bit	BPLVL1 bit	BPLVL0 bit	BEEP Gain	
0	0	0	0	0dB	(default)
0	0	0	1	–6dB	
0	0	1	0	–12dB	
0	0	1	1	–18dB	
0	1	0	0	–24dB	
0	1	0	1	–30dB	
0	1	1	0	–33dB	
0	1	1	1	–36dB	
1	0	0	0	–39dB	
1	0	0	1	–42dB	
Other	N/A				

Table 81. BEEP Output Gain Setting when BPM bit = "0" (N/A: Not available)

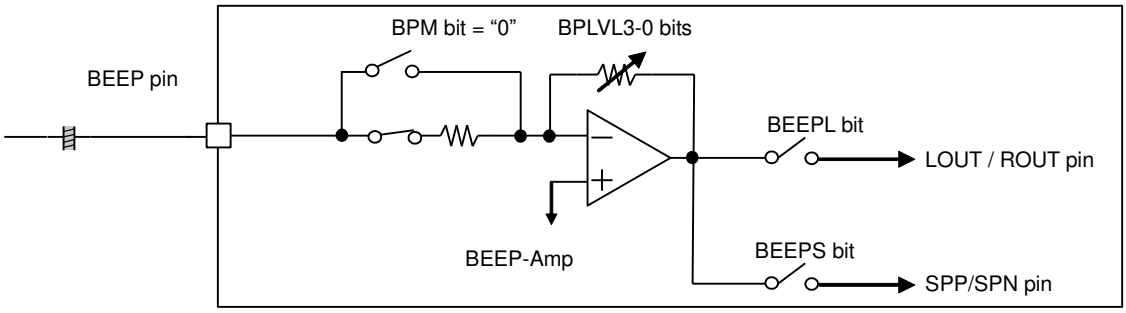


Figure 60. Block Diagram of BEEP pin (BPM bit = "0")

• **External Resistance Mode (BPM bit = "1")**

Gain setting of input BEEP signal is controlled by an external resistor R_i. The gain is in inverse proportion to the R_i value. (Figure 61) Gain setting by BPLVL3-0 bits is not available.

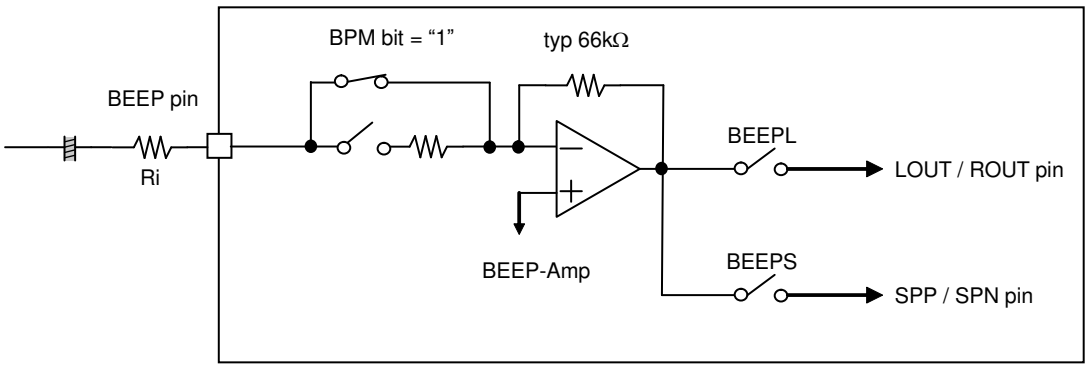


Figure 61. Block Diagram of BEEP pin (BPM bit = "1")

SPKG1-0 bits	BEEP → SPP/SPN Gain		
	ALC2 bit = "0"	ALC2 bit = "1"	
00	+6.4dB	+8.4dB	(default)
01	+8.4dB	+10.4dB	
10	+11.1dB	+13.1dB	
11	+13.1dB	+15.1dB	

Table 82. BEEP → SPK Output Gain

LVCM1-0 bits	AVDD	BEEP → Lineout Gain	Lineout Common Voltage (typ)	
00	2.8 ~ 3.6V	0dB	1.3V	
01	3.0 ~ 3.6V	+2dB	1.5V	(default)
10	2.8 ~ 3.6V	+2dB	1.3V	
11	3.0 ~ 3.6V	+4dB	1.5V	

Table 83. BEEP → Lineout Output Gain

■ Stereo Line Output (LOUT, ROUT pin)

When DACL bit is set to "1", L and R channel signals of DAC are output in single-ended format via LOUT and ROUT pins. When DACL bit is "0", output signals are muted and LOUT and ROUT pins output common voltage. The load impedance is 10kΩ (min.). When the PMLO bit = LOPS bit = "0", the stereo line output enters power-down mode and the output is pulled-down to VSS1 by 100kΩ(typ). When the LOPS bit is "1", stereo line output enters power-save mode. Pop noise at power-up/down can be reduced by changing PMLO bit when LOPS bit = "1". In this case, output signal line should be pulled-down to AVSS by 20kΩ after AC coupled as Figure 63. Rise/Fall time is 300ms (max) when C=1μF and R_L=10kΩ. When PMLO bit = "1" and LOPS bit = "0", stereo line output is in normal operation.

LVCM1-0 bits set the gain of stereo line output.

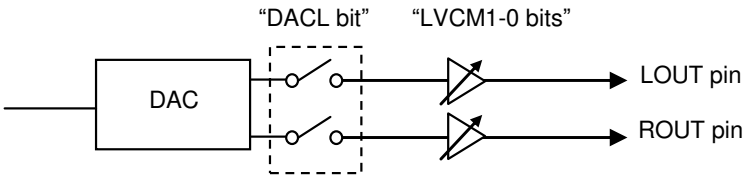


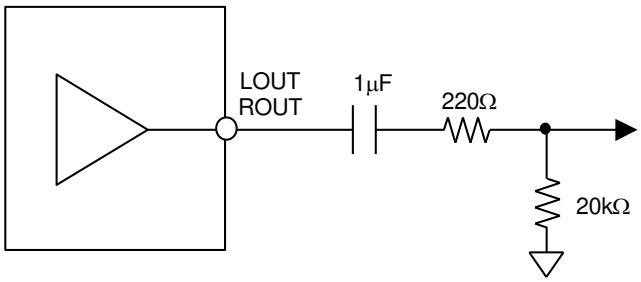
Figure 62. Stereo Line Output

LOPS bit	PMLO bit	Mode	LOUT/ROUT pin	
0	0	Power Down	Pull-down to VSS1	(default)
	1	Normal Operation	Normal Operation	
1	0	Power Save	Fall down to VSS1	
	1	Power Save	Rise up to Common Voltage	

Table 84. Stereo Line Output Mode Select

LVCM1-0 bits	AVDD	Gain	Common Voltage (typ)	Signal Level that may clip	
00	2.8 ~ 3.6V	0dB	1.3V	0dBFS or more	
01	3.0 ~ 3.6V	+2dB	1.5V	−1dBFS or more	(default)
10	2.8 ~ 3.6V	+2dB	1.3V	−2dBFS or more	
11	3.0 ~ 3.6V	+4dB	1.5V	−3dBFS or more	

Table 85. Stereo Lineout Volume Setting



Note 58. If the value of 20kΩ resistance at pop noise reduction circuit is increased, the power-up time of stereo line output is increased but the pop noise level is not decreased. Do not use a resistor less than 20kΩ at the pop noise reduction circuit since the line output drivability is minimum 10kΩ.

Figure 63. External Circuit for Stereo Line Output (in case of using a Pop Noise Reduction Circuit)

[Stereo Line Output Control Sequence (in case of using a Pop Noise Reduction Circuit)]

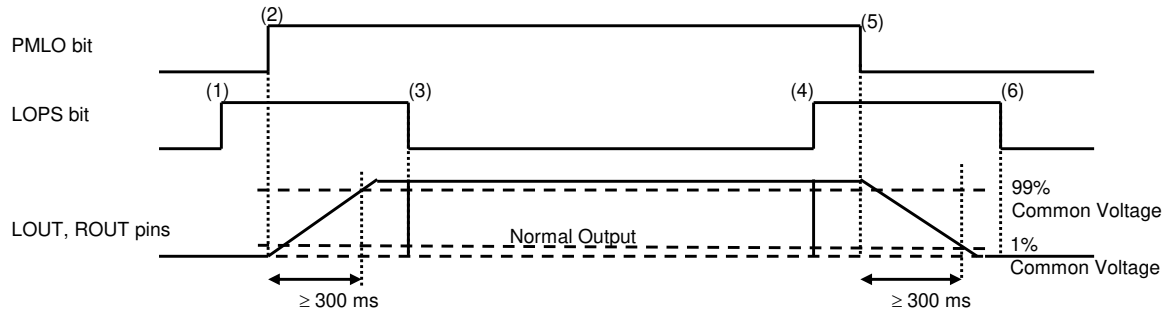


Figure 64. Stereo Line Output Control Sequence (in case of using a Pop Noise Reduction Circuit)

(1) Set LOPS bit = "1". Stereo line output enters power-save mode.
(2) Set PMLO bit = "1". Stereo line output exits power-down mode.
LOUT and ROUT pins rise up to VCOM voltage. Rise time is 200ms (max 300ms) when C=1μF.
(3) Set LOPS bit = "0" after LOUT and ROUT pins rise up. Stereo line output exits power-save mode.
Stereo line output is enabled.
(4) Set LOPS bit = "1". Stereo line output enters power-save mode.
(5) Set PMLO bit = "0". Stereo line output enters power-down mode.
LOUT and ROUT pins fall down to 1% of the common voltage. Fall time is 200ms (max 300ms) at C=1μF.
(6) Set LOPS bit = "0" after LOUT and ROUT pins fall down. Stereo line output exits power-save mode.

■ Speaker Output

The DAC output signal is input to the speaker amplifier as mono signal [(L+R)/2]. The speaker amplifier has mono output as it is BTL (Bridged Transless) capable. The gain and output level are set by SPKG1-0 bits. The output level depends on AVDD and SPKG1-0 bits setting.

SPKG1-0 bits	Gain		
	ALC2 bit = "0"	ALC2 bit = "1"	
00	+6.1dB	+8.1dB	(default)
01	+8.1dB	+10.1dB	
10	+10.1dB	+12.1dB	
11	+12.1dB	+14.1dB	

Table 86. SPK-Amp Gain

SPKG1-0 bits		SPK-Amp Output (DAC Input =0dBFS, AVDD = 3.3V)	
		ALC2 bit = "0"	ALC2 bit = "1" (LMTH2-0 bits = "000")
AK4958EG	00	3.37Vpp	3.17Vpp
	01	4.24Vpp (Note 59)	4.00Vpp
	10	5.78Vpp (Note 59)	5.45Vpp (Note 59)
	11	7.28Vpp (Note 59)	6.33Vpp (Note 59)
AK4958ECB	00	3.44Vpp	3.24Vpp
	01	4.33Vpp (Note 59)	4.08Vpp
	10	5.90Vpp (Note 59)	5.58Vpp (Note 59)
	11	7.43Vpp (Note 59)	7.03Vpp (Note 59)

Note 59. The output level is calculated on the assumption that the signal is not clipped. However, in the actual case, the SPK-Amp output signal is clipped when DAC outputs 0dBFS signal. When SPKG1-0 bits = "10" (ALC2 bit = "0"), ideal output level is 5.78Vpp for the AK4958EG (5.90Vpp for the AK4958ECB). In the actual case, the output level is 1.79Vrms@S/(N+D)=typ. 20dB. The SPK-Amp output level should be kept under 4.0Vpp (AVDD=3.3V) by adjusting digital volume to prevent clipped noise.

Table 87. SPK-Amp Output Level

< Speaker-Amp Control Sequence >

The speaker amplifier is powered-up/down by PMSPK bit. When PMSPK bit is "0", both SPP and SPN pins are in Hi-Z state. When PMSPK bit is "1" and SPPSN bit is "0", the speaker amplifier enters power-save mode. In this mode, the SPP pin is placed in Hi-Z state and the SPN pin outputs AVDD/2 voltage.

When the PMSPK bit is "1" after the PDN pin is changed from "L" to "H", the SPP and SPN pins rise up in power-save mode. In this mode, the SPP pin is placed in a Hi-Z state and the SPN pin goes to AVDD/2 voltage. Because the SPP and SPN pins rise up in power-save mode, pop noise can be reduced. When the AK4958 is powered-down (PMSPK bit = "0"), pop noise can also be reduced by first entering power-save-mode.

PMSPK bit	SPPSN bit	Mode	SPP pin	SPN pin	
0	x	Power-down	Hi-Z	Hi-Z	(default)
1	0	Power-save	Hi-Z	AVDD/2	
	1	Normal Operation	Normal Operation	Normal Operation	

Table 88 Speaker-Amp Mode Setting (x: Don't care)

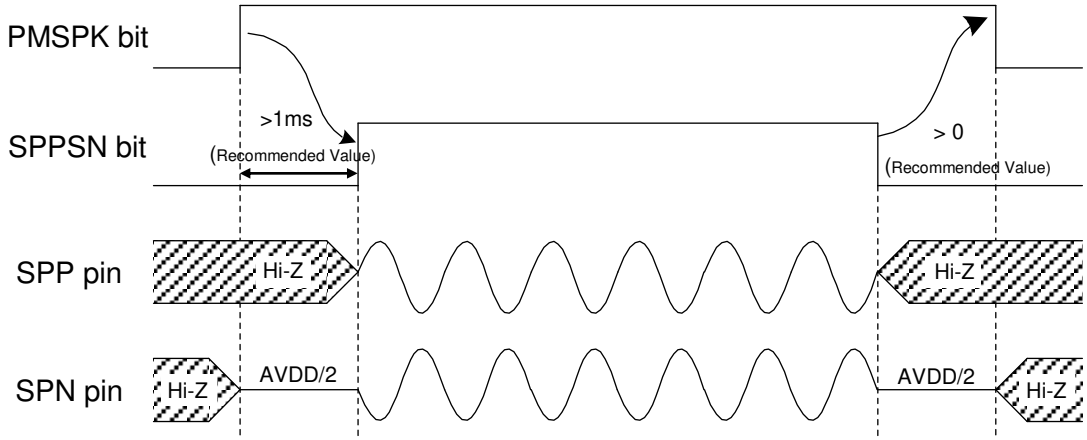


Figure 65. Power-up/Power-down Timing for Speaker-Amp

■ Thermal Shutdown Function

When the internal temperature of the device rises up irregularly (e.g. when output pins are shortened), the speaker amplifier is automatically powered down and then THDET bit becomes "1" (thermal shutdown). The thermal shutdown status can be monitored by reading THDET bit. When the thermal shutdown is executed, all blocks except VCOM and LDO blocks are powered down. These blocks will not return to a normal operation until being reset by the PDN pin. THDET bit becomes "0" by this PDN pin reset.

■ Video Block

The integrated video amplifier has drivability for a load resistance of 150Ω (Figure 66). The AK4958 has a composite input and output. A Low Pass Filter (LPF) and volume are integrated, and VG1-0 bits set the gain (+6/+12/+16.5dB: AK4958EG, +12/+16.5dB: AK4958ECB) (Table 89). The video signal's clamp level is 50mV (typ). The video amplifier power management is controlled by PMV bit. When PMV bit = "0", the VOUT pin outputs 0V. The video inputs must be C-coupled by a capacitor. The video signal source impedance at transmitting side must be in the range of 0.075 ~ 1.6kΩ.

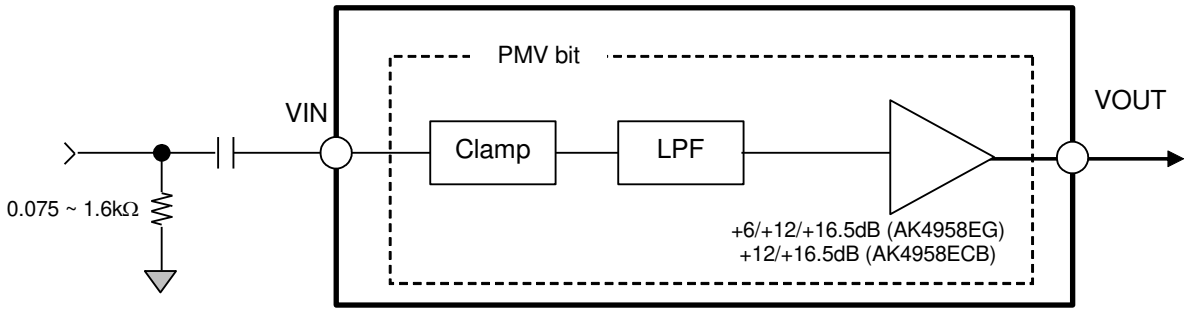


Figure 66. Video Block Diagram

VG1 bit	VG0 bit	GAIN	
0	0	+6dB (AK4958EG) N/A (AK4958ECB)	
0	1	N/A	
1	0	+12dB	(default)
1	1	+16.5dB	

Table 89. Video Signal Gain Setting (N/A: Not available)

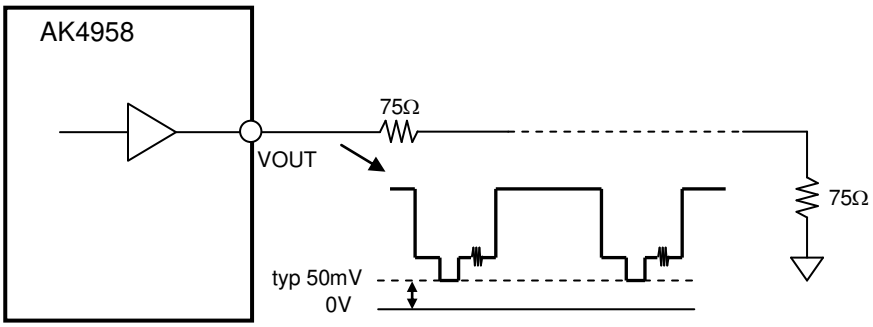


Figure 67. Video Signal Output

■ Regulator Block

The AK4958 integrates a regulator. The 3.3V (typ) power supply voltage from the AVDD pin is converted to 2.3V (typ) by the regulator and supplied to the analog blocks (MIC-Amp, ADC, DAC, BEEP, Video-Amp). The regulator is powered up by PMVCM bit = "1", and powered down by PMVCM = "0". Connect a 2.2μF (± 50%) capacitor to the REGFIL pin to reduce noise on AVDD.

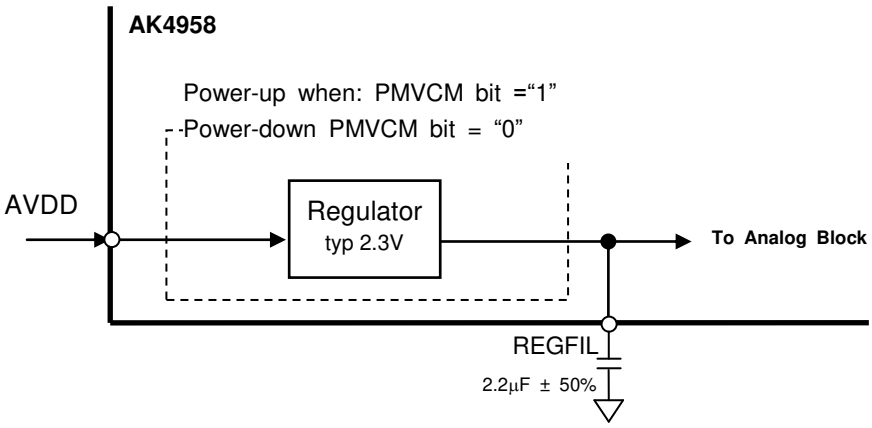


Figure 68 Regulator Block

■ Serial Control Interface

(1) 3-wire Serial Control Mode (Only the AK4958EG supports this interface)

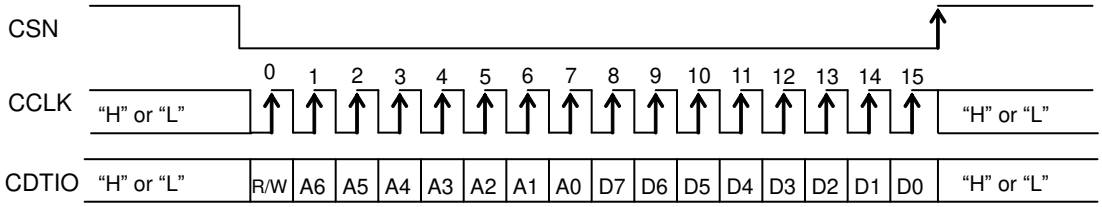
When RBANK bit = "0", Register Map1 (00H ~ 1FH) and Register Map2 (20H~5AH) can be accessed.
When RBANK bit = "1", Register Map1 (00H ~ 1FH) and Register Map3 (20H~60H) can be accessed.
Data read must be executed when READ bit = "1".

1. Data Writing and Reading Modes on Every Address (00H~5AH @ RBANK bit = "0", 00H~60H @ RBANK bit = "1")

One data is written to (read from) one address.

Internal registers may be written by using 3-wire serial interface pins (CSN, CCLK and CDTIO). The data on this interface consists of Read/Write, Register address (MSB first, 7bits) and Control data or Output data (MSB first, 8bits). Address and data is clocked in on the rising edge of CCLK and data is clocked out on the falling edge. Data writings become available on the rising edge of CSN. When reading the data, the CDTIO pin changes to output mode at the falling edge of 8th CCLK and outputs data in D7-D0. However this reading function is available only when READ bit = "1". When READ bit = "0", the CDTIO pin stays as Hi-Z even after the falling edge of 8th CCLK. The data output finishes on the rising edge of CSN. The CDTIO is placed in a Hi-Z state except when outputting the data at read operation mode. Clock speed of CCLK is 5MHz (max). The value of internal registers are initialized by the PDN pin = "L".

Note 60. When RBANK bit = "0", data read is only valid on the addresses in Register Map1 and 2, and data read is only valid on the addresses in Register Map 1 and 3 when RBANK bit = "1". When reading other addresses, the register values are invalid.



R/W: READ/WRITE ("1": WRITE, "0": READ)
A6-A0: Register Address
D7-D0: Control data (Input) at Write Command
Output data (Output) at Read Command

Figure 69. Serial Control Interface Timing 1

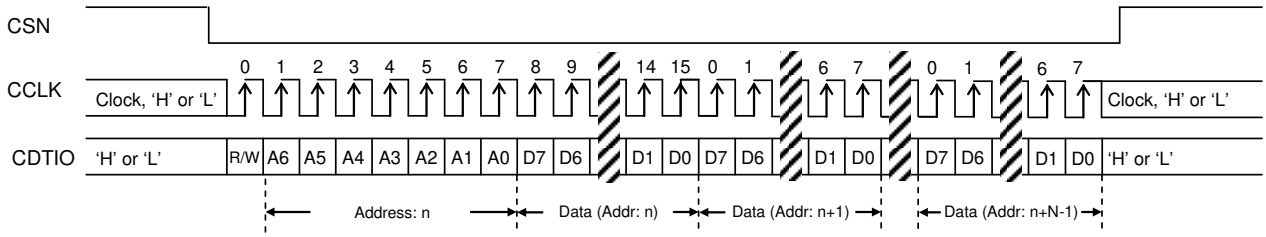
2. Continuous Data Writing Mode

Address is incremented automatically and data is written continuously. This mode does not support reading.
When RBANK bit = "0", the write address is automatically incremented to 00H if the written address reaches 5AH.
When RBANK bit = "1", i the write address is automatically incremented to 00H if the written address reaches 60H.
Writing to the address 0EH, 14H and 18H are ignored.

In this mode, registers are written by 3-wire serial interface pins (CSN, CCLK and CDTIO). The data on the 3-wire serial interface is 8 bit data, consisting of register address (MSB-first, 7bits) and control or output data (MSB-first, 8xN bits)). The receiving data is latched on a rising edge ("↑") of CCLK. The first write data becomes effective between the rising edge ("↑") and the falling edge ("↓") of 16th CCLK. When the micro-processor continues sending CDTIO and CCLK clocks while the CSN pin = "L", the address counter is incremented automatically and writing data becomes effective between the rising edge ("↑") and the falling edge ("↓") of every 8th CCLK. For the last address, writing data becomes effective between the rising edge ("↑") of 8th CCLK and the rising edge ("↑") of CSN. The clock speed of CCLK is 5MHz (max). The internal registers are initialized by the PDN pin = "L".

Even through the writing data does not reach the last address; a write command can be completed when the CSN pin is set to "H".

Note 61. When CSN "↑" was written before "↑" of 8th CCLK in continuous data writing mode, the previous data writing address becomes valid and the writing address is ignored.
Note 62. After 8bits data in the last address became valid, put the CSN pin "H" to complete the write command. If the CDTIO and CCLK inputs are continued when the CSN pin = "L", the data in the next address, which is incremented, is over written.



R/W: READ/WRITE ("1": WRITE, "0": READ)
A6-A0: Register Address
D7-D0: Control data (Input) at Write Command
Output data (Output) at Read Command

Figure 70. Serial Control Interface Timing 2 (Continuous Writing Mode)

(2) I2C-bus Control Mode (AK498EG: I2C pin = “H”)

The AK4958 supports the fast-mode I^2C-bus (max: 400kHz). Pull-up resistors at the SDA and SCL pins must be connected to a voltage in the range from TVDD (DTVDD) or more to 6V or less.
When RBANK bit = “0”, Register Map1 (00H ~ 1FH) and Register Map2 (20H~5AH) can be accessed.
When RBANK bit = “1”, Register Map1 (00H ~ 1FH) and Register Map3 (20H~60H) can be accessed.

(2)-1-1. WRITE Operations

Figure 71 shows the data transfer sequence for the I^2C-bus mode. All commands are preceded by a START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition (Figure 77). After the START condition, a slave address is sent. This address is 7 bits long followed by the eighth bit that is a data direction bit (R/W). For the AK4958EG, the most significant six bits of the slave address are fixed as “001001”. The next bit is device address bit set by the CAD0 pin. This bit identifies the specific device on the bus. For the AK4958ECB, the most significant seven bits of the slave address are fixed as “0010011”. (Figure 72). If the slave address matches that of the AK4958, the AK4958 generates an acknowledge and the operation is executed. The master must generate the acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 78). A R/W bit value of “1” indicates that the read operation is to be executed, and “0” indicates that the write operation is to be executed.

The second byte consists of the control register address of the AK4958. The format is MSB first, and those most significant 1bit is fixed to zero (Figure 73). The data after the second byte contains control data. The format is MSB first, 8bits (Figure 74). The AK4958 generates an acknowledge after each byte is received. Data transfer is always terminated by a STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition (Figure 77).

The AK4958 can perform more than one byte write operation per sequence. After receipt of the third byte the AK4958 generates an acknowledge and awaits the next data. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After receiving each data packet the internal address counter is incremented by one, and the next data is automatically taken into the next address. When RBANK bit = “0”, the address counter will “roll over” to 00H and the previous data will be overwritten if the address exceeds “5AH” of Register Map 2 prior to generating a stop condition. When RBANK bit = “1”, the address counter will “roll over” to 00H and the previous data will be overwritten if the address exceeds “60H” of Register Map 3 prior to generating a stop condition.

The data on the SDA line must remain stable during the HIGH period of the clock. HIGH or LOW state of the data line can only be changed when the clock signal on the SCL line is LOW (Figure 79) except for the START and STOP conditions.

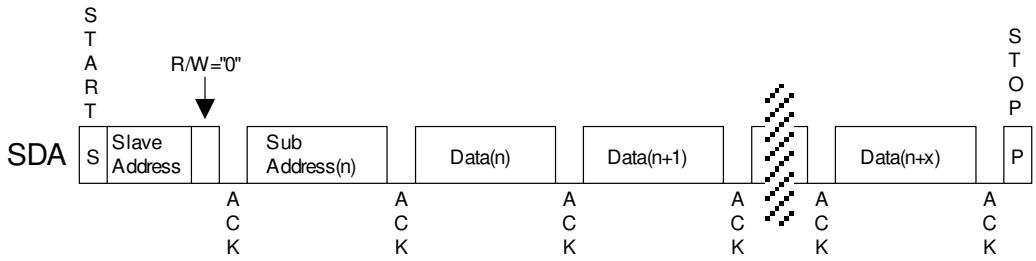


Figure 71. Data Transfer Sequence at I^2C Bus Mode

0	0	1	0	0	1	CAD0	R/W

(AK4958EG)

0	0	1	0	0	1	1	R/W

(AK4958ECB)

Figure 72. The First Byte

0	A6	A5	A4	A3	A2	A1	A0

Figure 73. The Second Byte

D7	D6	D5	D4	D3	D2	D1	D0

Figure 74. The Third Byte

(2)-1-2. READ Operations

Set the R/W bit = "1" for the READ operation of the AK4958. After transmission of data, the master can read the next address's data by generating an acknowledge instead of terminating the write cycle after the receipt of the first data word. After receiving each data packet the internal address counter is incremented by one, and the next data is automatically taken into the next address. When RBANK bit = "0", the address counter will "roll over" to 00H and the data of 00H will be read out if the address exceeds "5AH" of Register map 2 prior to generating a stop condition. When RABNK bit = "1", the address counter will "roll over" to 00H and the data of 00H will be read out if the address exceeds "60H" of Register map 3 prior to generating a stop condition.

Note 63. When RBANK bit = "0", data read is only valid on the addresses 00H to 5AH, and data read is only valid on the addresses 00H to 60H when RBANK bit = "1". When reading other addresses, the register values are invalid.

The AK4958 supports two basic read operations: CURRENT ADDRESS READ and RANDOM ADDRESS READ.

(2)-2-1. CURRENT ADDRESS READ

The AK4958 has an internal address counter that maintains the address of the last accessed word incremented by one. Therefore, if the last access (either a read or write) were to address "n", the next CURRENT READ operation would access data from the address "n+1". After receipt of the slave address with R/W bit "1", the AK4958 generates an acknowledge, transmits 1-byte of data to the address set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge but generates a stop condition instead, the AK4958 ceases the transmission.

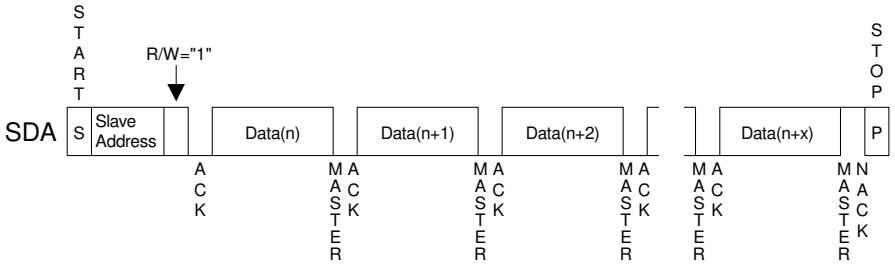


Figure 75. Current Address Read

(2)-2-2. RANDOM ADDRESS READ

The random read operation allows the master to access any memory location at random. Prior to issuing the slave address with the R/W bit "1", the master must first perform a "dummy" write operation. The master issues a start request, a slave address (R/W bit = "0") and then the register address to read. After the register address is acknowledged, the master immediately reissues the start request and the slave address with the R/W bit "1". The AK4958 then generates an acknowledge, 1 byte of data and increments the internal address counter by 1. If the master does not generate an acknowledge but generates a stop condition instead, the AK4958 ceases the transmission.

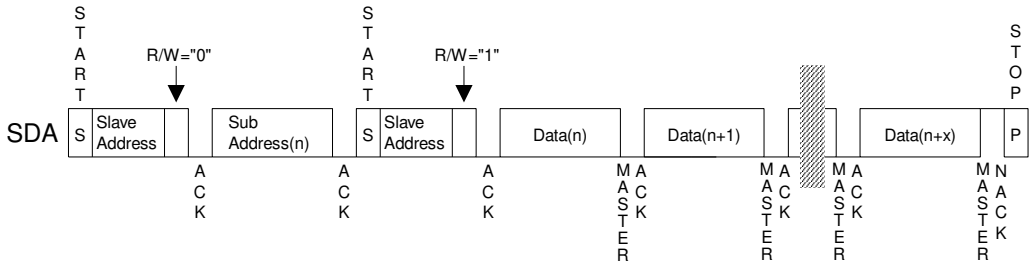


Figure 76. Random Address Read

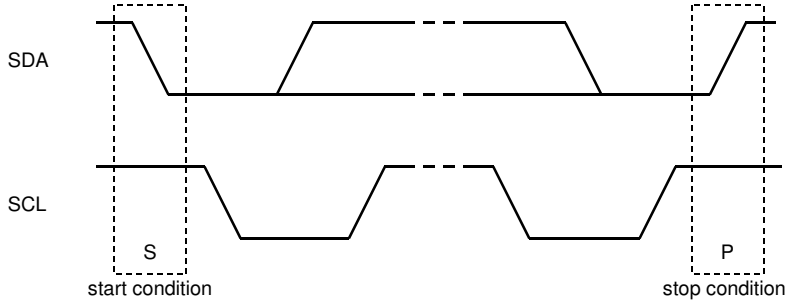


Figure 77. Start Condition and Stop Condition

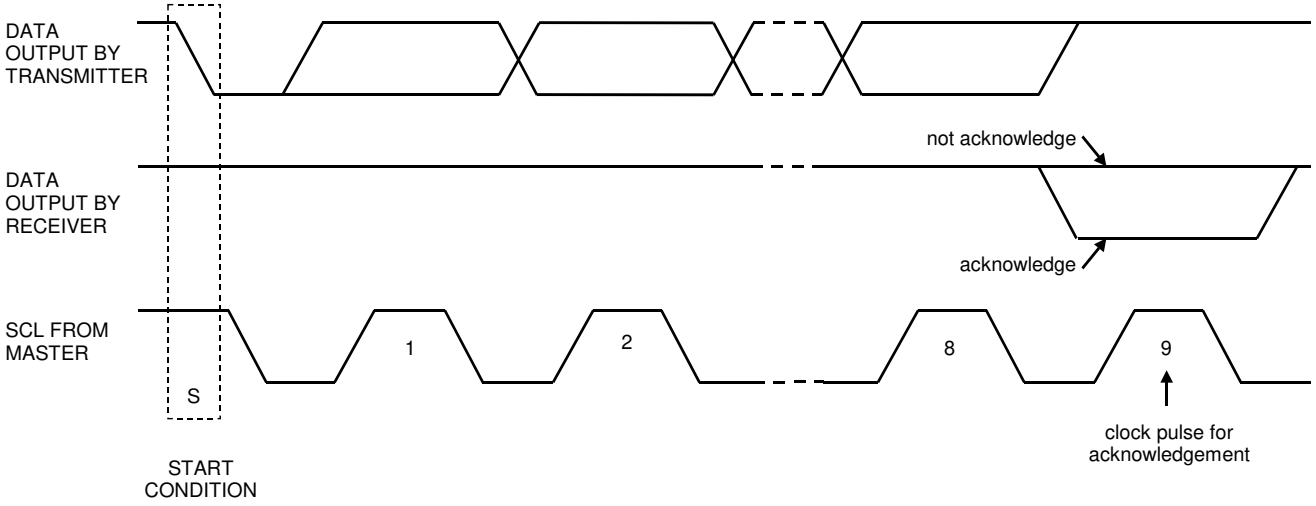


Figure 78. Acknowledge (I^2C Bus)

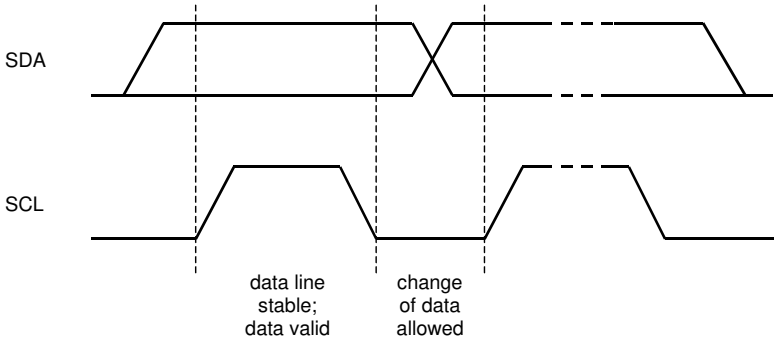


Figure 79. Bit Transfer (I^2C Bus)

■ Register Map 1

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management 1	PMPFIL	PMVCM	PMBP	PMSPK	PMLO	PMDAC	PMADR	PMADL
01H	Power Management 2	PMMICR	PMMICL	0	PMMP	M/S	0	MCKO	PMPLL
02H	Signal Select 1	SPPSN	0	0	MICL	0	MGAIN2	MGAIN1	MGAIN0
03H	Signal Select 2	SPKG1	SPKG0	BEEPS	DACS	0	0	INR (Note 64)	INL (Note 64)
04H	Signal Select 3	MONO1	MONO0	LOPS	DACL	BEEPL	0	LVCM1	LVCM0
05H	Mode Control 1	PLL3	PLL2	PLL1	PLL0	BCKO	0	DIF1	DIF0
06H	Mode Control 2	PS1	PS0	0	0	FS3	FS2	FS1	FS0
07H	Mode Control 3	READ	THDET	SMUTE	0	OVOLC	IVOLC	0	0
08H	Digital MIC	0	0	PMDMR	PMDML	DCLKE	0	DCLKP	DMIC
09H	Timer Select	ADRST1	ADRST0	0	0	0	0	0	DVTM
0AH	ALC Timer Select	FRATT	FRN	ALCEQN	IVTM	WTM1	WTM0	RFST1	RFST0
0BH	ALC Mode Control 1	ALC2	ALC1	RGAIN2	RGAIN1	RGAIN0	LMTH2	LMTH1	LMTH0
0CH	ALC Mode Control 2	IREF7	IREF6	IREF5	IREF4	IREF3	IREF2	IREF1	IREF0
0DH	ALC Mode Control 3	EQFC1	EQFC0	OREF5	OREF4	OREF3	OREF2	OREF1	OREF0
0EH	ALC Volume	VOL7	VOL6	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0
0FH	Lch Input Volume Control	IVL7	IVL6	IVL5	IVL4	IVL3	IVL2	IVL1	IVL0
10H	Rch Input Volume Control	IVR7	IVR6	IVR5	IVR4	IVR3	IVR2	IVR1	IVR0
11H	Lch Output Volume Control	OVL7	OVL6	OVL5	OVL4	OVL3	OVL2	OVL1	OVL0
12H	Rch Output Volume Control	OVR7	OVR6	OVR5	OVR4	OVR3	OVR2	OVR1	OVR0
13H	Digital Volume2 Control	DVOL7	DVOL6	DVOL5	DVOL4	DVOL3	DVOL2	DVOL1	DVOL0
14H	ALC Input Level	0	INVOL6	INVOL5	INVOL4	INVOL3	INVOL2	INVOL1	INVOL0
15H	REF2 Setting	0	RF2SL2	RF2SL1	RF2SL0	0	RF2P2	RF2P1	RF2P0
16H	Lch MIC Gain Setting	MGL7	MGL6	MGL5	MGL4	MGL3	MGL2	MGL1	MGL0
17H	Rch MIC Gain Setting	MGR7	MGR6	MGR5	MGR4	MGR3	MGR2	MGR1	MGR0
18H	MIC Gain Read	RMG7	RMG6	RMG5	RMG4	RMG3	RMG2	RMG1	RMG0
19H	BEEP Control		BPVCM	0	BPM	BPLVL3	BPLVL2	BPLVL1	BPLVL0
1AH	Video Control	0	0	0	0	VG1	VG0	0	PMV
1BH	HPF Filter Control	0	HPF3C2	HPF3C1	HPF3C0	0	HPFC1	HPFC0	HPFAD
1CH	Digital Filter Select 1	HPF3	STEREO2	LPF	HPF	EQ0	GN1	GN0	FIL3
1DH	Digital Filter Mode	0	0	0	0	BRDAC	PFDAC	ADCPF	PFSDO
1EH	Reserved	0	0	0	0	0	0	0	0
1FH	Register map Control	0	0	0	0	0	0	0	RBANK

Note 64. The AK4958ECB does not have these registers and “0”must be written to these addresses.

■ Register Map 2 (RBANK bit = "0")

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
20H	HPF2 Co-efficient 0	F1A7	F1A6	F1A5	F1A4	F1A3	F1A2	F1A1	F1A0
21H	HPF2 Co-efficient 1	0	0	F1A13	F1A12	F1A11	F1A10	F1A9	F1A8
22H	HPF2 Co-efficient 2	F1B7	F1B6	F1B5	F1B4	F1B3	F1B2	F1B1	F1B0
23H	HPF2 Co-efficient 3	0	0	F1B13	F1B12	F1B11	F1B10	F1B9	F1B8
24H	LPF Co-efficient 0	F2A7	F2A6	F2A5	F2A4	F2A3	F2A2	F2A1	F2A0
25H	LPF Co-efficient 1	0	0	F2A13	F2A12	F2A11	F2A10	F2A9	F2A8
26H	LPF Co-efficient 2	F2B7	F2B6	F2B5	F2B4	F2B3	F2B2	F2B1	F2B0
27H	LPF Co-efficient 3	0	0	F2B13	F2B12	F2B11	F2B10	F2B9	F2B8
28H	FIL3 Co-efficient 0	F3A7	F3A6	F3A5	F3A4	F3A3	F3A2	F3A1	F3A0
29H	FIL3 Co-efficient 1	F3AS	0	F3A13	F3A12	F3A11	F3A10	F3A9	F3A8
2AH	FIL3 Co-efficient 2	F3B7	F3B6	F3B5	F3B4	F3B3	F3B2	F3B1	F3B0
2BH	FIL3 Co-efficient 3	0	0	F3B13	F3B12	F3B11	F3B10	F3B9	F3B8
2CH	EQ0 Co-efficient 0	E0A7	E0A6	E0A5	E0A4	E0A3	E0A2	E0A1	E0A0
2DH	EQ0 Co-efficient 1	E0A15	E0A14	E0A13	E0A12	E0A11	E0A10	E0A9	E0A8
2EH	EQ0 Co-efficient 2	E0B7	E0B6	E0B5	E0B4	E0B3	E0B2	E0B1	E0B0
2FH	EQ0 Co-efficient 3	0	0	E0B13	E0B12	E0B11	E0B10	E0B9	E0B8
30H	EQ0 Co-efficient 4	E0C7	E0C6	E0C5	E0C4	E0C3	E0C2	E0C1	E0C0
31H	EQ0 Co-efficient 5	E0C15	E0C14	E0C13	E0C12	E0C11	E0C10	E0C9	E0C8
32H	Digital Filter Select 2	0	0	0	EQ5	EQ4	EQ3	EQ2	EQ1
33H	EQ Common Gain Select	0	0	0	EQC5	EQC4	EQC3	EQC2	EQBP
34H	EQ2 Common Gain Setting	EQ2G5	EQ2G4	EQ2G3	EQ2G2	EQ2G1	EQ2G0	EQ2T1	EQ2T0
35H	EQ3 Common Gain Setting	EQ3G5	EQ3G4	EQ3G3	EQ3G2	EQ3G1	EQ3G0	EQ3T1	EQ3T0
36H	EQ4 Common Gain Setting	EQ4G5	EQ4G4	EQ4G3	EQ4G2	EQ4G1	EQ4G0	EQ4T1	EQ4T0
37H	EQ5 Common Gain Setting	EQ5G5	EQ5G4	EQ5G3	EQ5G2	EQ5G1	EQ5G0	EQ5T1	EQ5T0

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
38H	E1 Co-efficient 0	E1A7	E1A6	E1A5	E1A4	E1A3	E1A2	E1A1	E1A0
39H	E1 Co-efficient 1	E1A15	E1A14	E1A13	E1A12	E1A11	E1A10	E1A9	E1A8
3AH	E1 Co-efficient 2	E1B7	E1B6	E1B5	E1B4	E1B3	E1B2	E1B1	E1B0
3BH	E1 Co-efficient 3	E1B15	E1B14	E1B13	E1B12	E1B11	E1B10	E1B9	E1B8
3CH	E1 Co-efficient 4	E1C7	E1C6	E1C5	E1C4	E1C3	E1C2	E1C1	E1C0
3DH	E1 Co-efficient 5	E1C15	E1C14	E1C13	E1C12	E1C11	E1C10	E1C9	E1C8
3EH	E2 Co-efficient 0	E2A7	E2A6	E2A5	E2A4	E2A3	E2A2	E2A1	E2A0
3FH	E2 Co-efficient 1	E2A15	E2A14	E2A13	E2A12	E2A11	E2A10	E2A9	E2A8
40H	E2 Co-efficient 2	E2B7	E2B6	E2B5	E2B4	E2B3	E2B2	E2B1	E2B0
41H	E2 Co-efficient 3	E2B15	E2B14	E2B13	E2B12	E2B11	E2B10	E2B9	E2B8
42H	E2 Co-efficient 4	E2C7	E2C6	E2C5	E2C4	E2C3	E2C2	E2C1	E2C0
43H	E2 Co-efficient 5	E2C15	E2C14	E2C13	E2C12	E2C11	E2C10	E2C9	E2C8
44H	E3 Co-efficient 0	E3A7	E3A6	E3A5	E3A4	E3A3	E3A2	E3A1	E3A0
45H	E3 Co-efficient 1	E3A15	E3A14	E3A13	E3A12	E3A11	E3A10	E3A9	E3A8
46H	E3 Co-efficient 2	E3B7	E3B6	E3B5	E3B4	E3B3	E3B2	E3B1	E3B0
47H	E3 Co-efficient 3	E3B15	E3B14	E3B13	E3B12	E3B11	E3B10	E3B9	E3B8
48H	E3 Co-efficient 4	E3C7	E3C6	E3C5	E3C4	E3C3	E3C2	E3C1	E3C0
49H	E3 Co-efficient 5	E3C15	E3C14	E3C13	E3C12	E3C11	E3C10	E3C9	E3C8
4AH	E4 Co-efficient 0	E4A7	E4A6	E4A5	E4A4	E4A3	E4A2	E4A1	E4A0
4BH	E4 Co-efficient 1	E4A15	E4A14	E4A13	E4A12	E4A11	E4A10	E4A9	E4A8
4CH	E4 Co-efficient 2	E4B7	E4B6	E4B5	E4B4	E4B3	E4B2	E4B1	E4B0
4DH	E4 Co-efficient 3	E4B15	E4B14	E4B13	E4B12	E4B11	E4B10	E4B9	E4B8
4EH	E4 Co-efficient 4	E4C7	E4C6	E4C5	E4C4	E4C3	E4C2	E4C1	E4C0
4FH	E4 Co-efficient 5	E4C15	E4C14	E4C13	E4C12	E4C11	E4C10	E4C9	E4C8
50H	E5 Co-efficient 0	E5A7	E5A6	E5A5	E5A4	E5A3	E5A2	E5A1	E5A0
51H	E5 Co-efficient 1	E5A15	E5A14	E5A13	E5A12	E5A11	E5A10	E5A9	E5A8
52H	E5 Co-efficient 2	E5B7	E5B6	E5B5	E5B4	E5B3	E5B2	E5B1	E5B0
53H	E5 Co-efficient 3	E5B15	E5B14	E5B13	E5B12	E5B11	E5B10	E5B9	E5B8
54H	E5 Co-efficient 4	E5C7	E5C6	E5C5	E5C4	E5C3	E5C2	E5C1	E5C0
55H	E5 Co-efficient 5	E5C15	E5C14	E5C13	E5C12	E5C11	E5C10	E5C9	E5C8
56H	Auto HPF Control	0	0	AHPF	SENC2	SENC1	SENC0	STG1	STG0
57H	DRC Mode Control	DRC	DLMAT2	DLMAT1	DLMAT0	DRGAIN1	DRGAIN0	DRCC1	DRCC0
58H	DVLC Mode Control	DVRGAIN2	DVRGAIN1	DVRGAIN0	DVLMAT2	DVLMAT1	DVLMAT0	DAF1	DAF0
59H	DVLC Filter Select	0	0	0	0	DLLPF	DMHPF	DMLPF	DHHPF
5AH	Boost Control	BSTON	0	BGN5	BGN4	BGN3	BGN2	BGN1	BGN0

■ Register Map 3 (RBANK bit = "1")

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
20H	DVLCL Curve X1	0	0	VL1X5	VL1X4	VL1X3	VL1X2	VL1X1	VL1X0
21H	DVLCL Curve Y1	0	0	VL1Y5	VL1Y4	VL1Y3	VL1Y2	VL1Y1	VL1Y0
22H	DVLCL Curve X2	0	0	VL2X5	VL2X4	VL2X3	VL2X2	VL2X1	VL2X0
23H	DVLCL Curve Y2	0	0	VL2Y5	VL2Y4	VL2Y3	VL2Y2	VL2Y1	VL2Y0
24H	DVLCL Curve X3	0	0	0	VL3X4	VL3X3	VL3X2	VL3X1	VL3X0
25H	DVLCL Curve Y3	0	0	0	VL3Y4	VL3Y3	VL3Y2	VL3Y1	VL3Y0
26H	DVLCL Slope 1	0	L1G6	L1G5	L1G4	L1G3	L1G2	L1G1	L1G0
27H	DVLCL Slope 2	0	L2G6	L2G5	L2G4	L2G3	L2G2	L2G1	L2G0
28H	DVLCL Slope 3	0	L3G6	L3G5	L3G4	L3G3	L3G2	L3G1	L3G0
29H	DVLCL Slope 4	0	L4G6	L4G5	L4G4	L4G3	L4G2	L4G1	L4G0
2AH	DVLCM Curve X1	0	0	VM1X5	VM1X4	VM1X3	VM1X2	VM1X1	VM1X0
2BH	DVLCM Curve Y1	0	0	VM1Y5	VM1Y4	VM1Y3	VM1Y2	VM1Y1	VM1Y0
2CH	DVLCM Curve X2	0	0	VM2X5	VM2X4	VM2X3	VM2X2	VM2X1	VM2X0
2DH	DVLCM Curve Y2	0	0	VM2Y5	VM2Y4	VM2Y3	VM2Y2	VM2Y1	VM2Y0
2EH	DVLCM Curve X3	0	0	0	VM3X4	VM3X3	VM3X2	VM3X1	VM3X0
2FH	DVLCM Curve Y3	0	0	0	VM3Y4	VM3Y3	VM3Y2	VM3Y1	VM3Y0
30H	DVLCM Slope 1	0	M1G6	M1G5	M1G4	M1G3	M1G2	M1G1	M1G0
31H	DVLCM Slope 2	0	M2G6	M2G5	M2G4	M2G3	M2G2	M2G1	M2G0
32H	DVLCM Slope 3	0	M3G6	M3G5	M3G4	M3G3	M3G2	M3G1	M3G0
33H	DVLCM Slope 4	0	M4G6	M4G5	M4G4	M4G3	M4G2	M4G1	M4G0
34H	DVLCH Curve X1	0	0	VH1X5	VH1X4	VH1X3	VH1X2	VH1X1	VH1X0
35H	DVLCH Curve Y1	0	0	VH1Y5	VH1Y4	VH1Y3	VH1Y2	VH1Y1	VH1Y0
36H	DVLCH Curve X2	0	0	VH2X5	VH2X4	VH2X3	VH2X2	VH2X1	VH2X0
37H	DVLCH Curve Y2	0	0	VH2Y5	VH2Y4	VH2Y3	VH2Y2	VH2Y1	VH2Y0
38H	DVLCH Curve X3	0	0	0	VH3X4	VH3X3	VH3X2	VH3X1	VH3X0
39H	DVLCH Curve Y3	0	0	0	VH3Y4	VH3Y3	VH3Y2	VH3Y1	VH3Y0
3AH	DVLCH Slope 1	0	H1G6	H1G5	H1G4	H1G3	H1G2	H1G1	H1G0
3BH	DVLCH Slope 2	0	H2G6	H2G5	H2G4	H2G3	H2G2	H2G1	H2G0
3CH	DVLCH Slope 3	0	H3G6	H3G5	H3G4	H3G3	H3G2	H3G1	H3G0
3DH	DVLCH Slope 4	0	H4G6	H4G5	H4G4	H4G3	H4G2	H4G1	H4G0
3EH	DVLCL LPF Co-efficient 0	DLLA7	DLLA6	DLLA5	DLLA4	DLLA3	DLLA2	DLLA1	DLLA0
3FH	DVLCL LPF Co-efficient 1	0	0	DLLA13	DLLA12	DLLA11	DLLA10	DLLA9	DLLA8
40H	DVLCL LPF Co-efficient 2	DLLB7	DLLB6	DLLB5	DLLB4	DLLB3	DLLB2	DLLB1	DLLB0
41H	DVLCL LPF Co-efficient 3	0	0	DLLB13	DLLB12	DLLB11	DLLB10	DLLB9	DLLB8
42H	DVLCM HPF Co-efficient 0	DMHA7	DMHA6	DMHA5	DMHA4	DMHA3	DMHA2	DMHA1	DMHA0
43H	DVLCM HPF Co-efficient 1	0	0	DMHA13	DMHA12	DMHA11	DMHA10	DMHA9	DMHA8
44H	DVLCM HPF Co-efficient 2	DMHB7	DMHB6	DMHB5	DMHB4	DMHB3	DMHB2	DMHB1	DMHB0
45H	DVLCM HPF Co-efficient 3	0	0	DMHB13	DMHB12	DMHB11	DMHB10	DMHB9	DMHB8
46H	DVLCM LPF Co-efficient 0	DMLA7	DMLA6	DMLA5	DMLA4	DMLA3	DMLA2	DMLA1	DMLA0
47H	DVLCM LPF Co-efficient 1	0	0	DMLA13	DMLA12	DMLA11	DMLA10	DMLA9	DMLA8
48H	DVLCM LPF Co-efficient 2	DMLB7	DMLB6	DMLB5	DMLB4	DMLB3	DMLB2	DMLB1	DMLB0
49H	DVLCM LPF Co-efficient 3	0	0	DMLB13	DMLB12	DMLB11	DMLB10	DMLB9	DMLB8
4AH	DVLCH HPF Co-efficient 0	DHHA7	DHHA6	DHHA5	DHHA4	DHHA3	DHHA2	DHHA1	DHHA0
4BH	DVLCH HPF Co-efficient 1	0	0	DHHA13	DHHA12	DHHA11	DHHA10	DHHA9	DHHA8
4CH	DVLCH HPF Co-efficient 2	DHHB7	DHHB6	DHHB5	DHHB4	DHHB3	DHHB2	DHHB1	DHHB0
4DH	DVLCH HPF Co-efficient 3	0	0	DHHB13	DHHB12	DHHB11	DHHB10	DHHB9	DHHB8

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
4EH	Boost HPF4 Co-efficient 0	BHA7	BHA6	BHA5	BHA4	BHA3	BHA2	BHA1	BHA0
4FH	Boost HPF4 Co-efficient 1	BHB7	BHB6	BHB5	BHB4	BHB3	BHB2	BHB1	BHB0
50H	Boost LPF2 Co-efficient 0	BLA7	BLA6	BLA5	BLA4	BLA3	BLA2	BLA1	BLA0
51H	Boost LPF2 Co-efficient 1	BLB7	BLB6	BLB5	BLB4	BLB3	BLB2	BLB1	BLB0
52H	Boost BPF1 Co-efficient 0	BB1A7	BB1A6	BB1A5	BB1A4	BB1A3	BB1A2	BB1A1	BB1A0
53H	Boost BPF1 Co-efficient 1	BB1B7	BB1B6	BB1B5	BB1B4	BB1B3	BB1B2	BB1B1	BB1B0
54H	Boost BPF1 Co-efficient 2	BB1B15	BB1B14	BB1B13	BB1B12	BB1B11	BB1B10	BB1B9	BB1B8
55H	Boost BPF1 Co-efficient 3	BB1C7	BB1C6	BB1C5	BB1C4	BB1C3	BB1C2	BB1C1	BB1C0
56H	Boost BPF1 Co-efficient 4	BB1C15	BB1C14	BB1C13	BB1C12	BB1C11	BB1C10	BB1C9	BB1C8
57H	Boost BPF2 Co-efficient 0	BB2A7	BB2A6	BB2A5	BB2A4	BB2A3	BB2A2	BB2A1	BB2A0
58H	Boost BPF2 Co-efficient 1	BB2B7	BB2B6	BB2B5	BB2B4	BB2B3	BB2B2	BB2B1	BB2B0
59H	Boost BPF2 Co-efficient 2	BB2B15	BB2B14	BB2B13	BB2B12	BB2B11	BB2B10	BB2B9	BB2B8
5AH	Boost BPF2 Co-efficient 3	BB2C7	BB2C6	BB2C5	BB2C4	BB2C3	BB2C2	BB2C1	BB2C0
5BH	Boost BPF2 Co-efficient 4	BB2C15	BB2C14	BB2C13	BB2C12	BB2C11	BB2C10	BB2C9	BB2C8
5CH	Boost BPF3 Co-efficient 0	BB3A7	BB3A6	BB3A5	BB3A4	BB3A3	BB3A2	BB3A1	BB3A0
5DH	Boost BPF3 Co-efficient 1	BB3B7	BB3B6	BB3B5	BB3B4	BB3B3	BB3B2	BB3B1	BB3B0
5EH	Boost BPF3 Co-efficient 2	BB3B15	BB3B14	BB3B13	BB3B12	BB3B11	BB3B10	BB3B9	BB3B8
5FH	Boost BPF3 Co-efficient 3	BB3C7	BB3C6	BB3C5	BB3C4	BB3C3	BB3C2	BB3C1	BB3C0
60H	Boost BPF3 Co-efficient 4	BB3C15	BB3C14	BB3C13	BB3C12	BB3C11	BB3C10	BB3C9	BB3C8

Note 65. PDN pin = “L” resets the registers to their default values.

Note 66. The bits defined as 0 must contain a “0” value.

Note 67. Address 0EH, 14H and 18H are a read only register. Writing access to 0EH, 14H and 18H are ignored and does not effect the operation.

■ Register Definitions (Register Map1)

Addr	Register Name	D23	D22	D21	D20	D19	D18	D17	D16
00H	Power Management 1	PMPFIL	PMVCM	PMBP	PMSPK	PMLO	PMDAC	PMADR	PMADL
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

PMADL: ADC Lch Power Management
0: Power-down (default)
1: Power-up
When the PMADL or PMADR bit is changed from "0" to "1", the initialization cycle (1059/fs=21.3ms @48kHz, ADRST1-0 bits = "00") starts. After initializing, digital data of the ADC is output.

PMADR: ADC Rch Power Management
0: Power down (default)
1: Power up
When the PMADL or PMADR bit is changed from "0" to "1", the initialization cycle (1059/fs=21.3ms @48kHz, ADRST1-0 bits = "00") starts. After initializing, digital data of the ADC is output.

PMDAC: DAC Power Management
0: Power-down (default)
1: Power-up

PMLO: Stereo Line Output Power Management
0: Power-down (default)
1: Power-up

PMSPK: Speaker-Amp Power Management
0: Power-down (default)
1: Power-up

PMBP: BEEP Input Power Management
0: Power-down (default)
1: Power-up

PMVCM: VCOM and Regulator (2.3V) Power Management
0: Power down (default)
1: Power up

PMPFIL: Programmable Filter Block Power Management
0: Power down (default)
1: Power up

The AK4958 can be powered down by writing "0" to the address "00H" and PMPLL, PMMICL/R, PMMP, PMDML/R, DMPE, PMV and MCKO bits. In this case, register values are maintained.

Addr	Register Name	D23	D22	D21	D20	D19	D18	D17	D16
01H	Power Management 2	PMMICR	PMMICL	0	PMMP	M/S	0	MCKO	PMPLL
R/W		R/W	R/W	R	R/W	R/W	R	R/W	R/W
Default		0	0	0	0	0	0	0	0

PMPLL: PLL Power Management
0: EXT Mode and Power down (default)
1: PLL Mode and Power up

MCKO: Master Clock Output Enable
0: Disable: MCKO pin = "L" (default)
1: Enable: Output frequency is selected by PS1-0 bits.

M/S: Master / Slave Mode Select
0: Slave Mode (default)
1: Master Mode

PMMP: Microphone Power Management
0: Power down (default)
1: Power up

PMMICL: Microphone Amplifier Lch Power Management
0: Power down (default)
1: Power up

PMMICR: Microphone Amplifier Rch Power Management
0: Power down (default)
1: Power up

Addr	Register Name	D23	D22	D21	D20	D19	D18	D17	D16
02H	Signal Select 1	SPPSN	0	0	MICL	0	MGAIN2	MGAIN1	MGAIN0
R/W		R/W	R	R	R/W	R	R/W	R/W	R/W
Default		0	0	0	0	0	1	0	0

MGAIN2-0: MIC-Amp Gain Control (Table 23)
Default: "100"(+18dB)

MICL: Microphone Power Output Voltage Select
0: typ 2.4 V (default)
1: typ 2.0V

SPPSN: Speaker-Amp Power-Save Mode
0: Power Save Mode (default)
1: Normal Operation
When SPPSN bit is "0", Speaker-Amp is in power-save mode. In this mode, the SPP pin goes to Hi-Z and the SPN pin outputs AVDD/2 voltage. When PMSPK bit = "1", SPPSN bit is enabled. After the PDN pin is set to "L", Speaker-Amp is in power-down mode since PMSPK bit is "0".

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Signal Select 2	SPKG1	SPKG0	BEEPS	DACS	0	0	INR	INL
R/W		R/W	R/W	R/W	R/W	R	R	R/W	R/W
Default		0	0	0	0	0	0	0	0

INL: ADC Lch Input Source Select (AK4958EG Only)
0: LIN1 pin (default)
1: LIN2 pin

INR: ADC Rch Input Source Select (AK4958EG Only)
0: RIN1 pin (default)
1: RIN2 pin

INR and INL bits are only for the AK4958EG. "0"must be written to these addresses for the AK4958ECB.

DACS: Signal Switch Control from DAC to Speaker-Amp
0: OFF (default)
1: ON
When DACS bit is "1", DAC output signal is input to Speaker-Amp.

BEEPS: Signal Switch Control from the BEEP pin to Speaker-Amp
0: OFF (default)
1: ON

SPKG1-0: Speaker-Amp Output Gain Select (Table 86)
Default: "00"(+6.4dB @ ALC2 bit = "0", +8.4dB @ ALC2 bit = "1")

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	Signal Select 3	MONO1	MONO0	LOPS	DACL	BEEPL	0	LVCM1	LVCM0
R/W		R/W	R/W	R/W	R/W	R/W	R	R/W	R/W
Default		0	0	0	0	0	0	0	1

LVCM1-0: Stereo Line Output Gain and Common Voltage Setting (Table 85)
Default: "01"(+2dB)

BEEPL: Signal Switch Control from the BEEP pin to Lineout
0: OFF (default)
1: ON

DACL: DAC Output Signal to Stereo Line Amp Control
0: OFF (default)
1: ON
When PMLO bit = "1", this bit setting is enabled. LOUT and ROUT pins output VSS1 when PMLO bit = "0".

LOPS: Stereo Line Output Power Save
0: Normal Operation (default)
1: Power Save Mode

MONO1-0: LOUT/ROUT Output Signal Mode Select (Table 56)
Default: "00" (LOUT pin = Lch, ROUT pin = Rch)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
05H	Mode Control 1	PLL3	PLL2	PLL1	PLL0	BCKO	0	DIF1	DIF0
R/W		R/W	R/W	R/W	R/W	R/W	R	R/W	R/W
Default		1	1	0	0	0	0	1	0

DIF1-0: Audio Interface Format (Table 18)
Default: "10" (MSB justified)

BCKO: Master Mode BICK Output Frequency Setting (Table 16)
Default: "0"(32fs)

PLL3-0: PLL Reference Clock Select (Table 4)
Default: "1100" (MCKI = 13.5MHz)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
06H	Mode Control 2	PS1	PS0	0	0	FS3	FS2	FS1	FS0
R/W		R/W	R/W	R	R	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

FS3-0: Sampling Frequency (Table 5, Table 7, Table 12, Table 14)

PS1-0: MCKO Frequency Setting (Table 10)
Default: "00" (256fs)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
07H	Mode Control 3	READ	THDET	SMUTE	0	OVOLC	IVOLC	0	0
R/W		R/W	R	R/W	R	R/W	R/W	R	R
Default		0	0	0	0	1	1	0	0

IVOLC: IVOL Control
0: Independent
1: Dependent (default)
When IVOLC bit = "1", IVL7-0 bits control both Lch and Rch volume levels, while register values of IVL7-0 bits are not written to IVR7-0 bits.

OVOLC: Output Digital Volume Control Mode Select
0: Independent
1: Dependent (default)
When OVOLC bit = "1", OVL7-0 bits control both Lch and Rch volume levels, while register values of OVL7-0 bits are not written to OVR7-0 bits.

SMUTE: Soft Mute Control
0: Normal Operation (default)
1: DAC outputs soft-muted

THDET: Thermal Shutdown Detection
0: Thermal Shutdown Off (default)
1: Thermal Shutdown ON

READ: Read Function Enable (Valid only in 3-wire serial control mode)
0: Disable (default)
1: Enable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
08H	Digital MIC	0	0	PMDMR	PMDML	DCLKE	0	DCLKP	DMIC
R/W		R	R	R/W	R/W	R/W	R	R/W	R/W
Default		0	0	0	0	0	0	0	0

DMIC: Digital Microphone Connection Select
0: Analog Microphone (default)
1: Digital Microphone

DCLKP: Data Latching Edge Select
0: Lch data is latched on the DMCLK rising edge (“↑”). (default)
1: Lch data is latched on the DMCLK falling edge (“↓”).

DCLKE: DMCLK pin Output Clock Control
0: “L” Output (default)
1: 64fs Output

PMDML/R: Input Signal Select with Digital Microphone (Table 20)
Default: “00”
ADC digital block is powered-down by PMDML = PMDMR bits = “0” when selecting a digital microphone input (DMIC bit = “1”).

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
09H	Timer Select	ADRST1	ADRST0	0	0	0	0	0	DVTM
R/W		R/W	R/W	R	R	R	R	R	R/W
Default		0	0	0	0	0	0	0	0

DVTM: Digital Volume Soft Transition Time Setting (Table 78)
Default: “0” (776/fs)
This transition time is for when DVOL7-0 bits are changed from 00H to C0H.

ADRST1-0: ADC Initial Cycle Setting (Table 17)
Default: “00” (1059/fs)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0AH	ALC Timer Select	FRATT	FRN	ALCEQN	IVTM	WTM1	WTM0	RFST1	RFST0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	1	0	0	0	1

RFST1-0: ALC Fast Recovery Speed (Table 46)
Default: "01" (Quad Speed)

WTM1-0: ALC Recovery Waiting Period (Table 42)
Default: "00" (128/fs).
A period of recovery operation when any limiter operation does not occur during ALC operation

IVTM: Transition Time of Input/Output Digital Volume (Table 54)
Default: "1" (944/fs)

ALCEQN: ALC EQ Setting
0: ALC EQ On (default)
1: ALC EQ Off

FRN: ALC Fast Recovery Function Enable
0: Enable (default)
1: Disable

RFATT: Fast Recovery Reference Volume Attenuation Amount (Table 47)
0: -0.00106dB (4/fs) (default)
1: -0.00106dB (16/fs)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0BH	ALC Mode Control 1	ALC2	ALC1	RGAIN2	RGAIN1	RGAIN0	LMTH2	LMTH1	LMTH0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

LMTH2-0: ALC Limiter Detection Level / Recovery Counter Reset Level (Table 40)
Default: "000"

RGAIN2-0: ALC Recovery Gain Amount Step (Table 43)
Default: "000" (0.00424dB @ 1/fs)

ALC1: ALC Enable for Recording
0: Recording ALC Disable (default)
1: Recording ALC Enable

ALC2: ALC Enable for Playback
0: Playback ALC Disable (default)
1: Playback ALC Enable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0CH	ALC Mode Control 2	IREF7	IREF6	IREF5	IREF4	IREF3	IREF2	IREF1	IREF0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	1	1	0	0	0	0	1

IREF7-0: Reference Value of ALC Recovery Operation (Recording). 0.375dB step, 242 Level (Table 44)
Default: "E1H" (+30.0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0DH	ALC Mode Control 3	EQFC1	EQFC0	OREF5	OREF4	OREF3	OREF2	OREF1	OREF0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	0	1	0	1	0	0	0

OREF5-0: Reference Value of ALC Recovery Operation (Playback). 0.375dB step, 60 Level (Table 45)
Default: "28H" (+6.0dB)

EQFC1-0: EQ extreme value and Zero point frequency before ALC level detection. (Table 39)
Default: "10" (extreme value =150Hz, Zero point = 100Hz@ fs=48kHz)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0EH	ALC Volume	VOL7	VOL6	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0
R/W		R	R	R	R	R	R	R	R
Default		1	0	0	1	0	0	0	1

VOL7-0: Current ALC volume value, 0.375dB step, 242 Level, Read operation only (Table 48)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0FH	Lch Input Volume Control	IVL7	IVL6	IVL5	IVL4	IVL3	IVL2	IVL1	IVL0
10H	Rch Input Volume Control	IVR7	IVR6	IVR5	IVR4	IVR3	IVR2	IVR1	IVR0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	1	1	0	0	0	0	1

IVL7-0, IVR7-0: Input Digital Volume, 0.375dB step, 242 Level (Table 53)
Default: "E1H" (+30.0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
11H	Lch Output Volume Control	OVL7	OVL6	OVL5	OVL4	OVL3	OVL2	OVL1	OVL0
12H	Rch Output Volume Control	OVR7	OVR6	OVR5	OVR4	OVR3	OVR2	OVR1	OVR0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	0	0	1	0	0	0	1

OVL7-0, OVR7-0: Output Digital Volume (Table 55)
Default: "91H" (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
13H	Digital Volume Control	DVOL7	DVOL6	DVOL5	DVOL4	DVOL3	DVOL2	DVOL1	DVOL0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	1	1	0	0	0

DVOL7-0: Output Digital Volume 2 (Table 77)
Default: "0CH" (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
14H	ALC Input Level	0	INVOL6	INVOL5	INVOL4	INVOL3	INVOL2	INVOL1	INVOL0
R/W		R	R	R	R	R	R	R	R
Default		0	0	0	0	0	0	0	0

INVOL6-0: ALC Input Level Read Function (Table 38)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
15H	ALC REF2 Setting	0	RF2SL2	RF2SL1	RF2SL0	0	RF2P2	RF2P1	RF2P0
R/W		R	R/W	R/W	R/W	R	R/W	R/W	R/W
Default		0	0	0	0	0	0	1	0

RF2P2-0: ALC Input Level Inflection Point (Table 51)
Default: "010" (–39dB)

RF2SL2-0: ALC REF2 Slope Setting (Table 52)
Default: "000" (Slope = 1)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
16H	Lch MIC Gain Setting	MGL7	MGL6	MGL5	MGL4	MGL3	MGL2	MGL1	MGL0
17H	Rch MIC Gain Setting	MGR7	MGR6	MGR5	MGR4	MGR3	MGR2	MGR1	MGR0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

MGL7-0, MGR7-0 bits: Lch Rch Microphone Sensitivity Correction (Table 28)
Default: "80H" (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
18H	MIC Gain Read	RMG7	RMG6	RMG5	MGR4	RMG3	RMG2	RMG1	RMG0
R/W		R	R	R	R	R	R	R	R
Default		0	0	0	0	0	0	0	0

RMG7-0 bits: ALC Input Level Reading Function (Table 29)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
19H	BEEP Control	0	BPVCM	0	BPM	BPLVL3	BPLVL2	BPLVL1	BPLVL0
R/W		R	R/W	R	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

BPLVL3-0: BEEP Output Level Setting (Table 81)
Default: "0000" (0dB)

BPM: BEEP Mode Setting (Table 79)
0: Internal Resistance Mode (default)
1: External Resistance Mode

BPVCM: Common Voltage Setting of MIN Input Amplifier (Table 80)
0: 1.15V (default)
1: 1.65V

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
1AH	Video Control	0	0	0	0	VG1	VG0	0	PMV
R/W		R	R	R	R	R/W	R/W	R	R/W
Default		0	0	0	0	1	0	0	0

PMV: Composite Video Block Power Management
0: Power down (default)
1: Power up

VG1-0: Video Amplifier Gain Select (Table 89)
Default: "10" (+12dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
1BH	HPF Filter Control	0	HPF3C2	HPF3C1	HPF3C0	0	HPFC1	HPFC0	HPFAD
R/W		R	R/W	R/W	R/W	R	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	1

HPFAD: HPF1 Control of ADC
0: OFF
1: ON (default)
When HPFAD bit is "1", the settings of HPFC1-0 bits are enabled. When HPFAD bit is "0", HPFAD block is through (0dB).
When PMADL bit = "1" or PMADR bit = "1", set HPFAD bit to "1".

HPFC1-0: Cut-off Frequency Setting of HPF1 (ADC) (Table 27)
Default: "00" (3.7Hz @ fs = 48kHz)

HPF3C2-0: HPF3 (Before ALC Input Volume Read) Cutoff Frequency Setting (Table 37)
Default: "000" (500Hz)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
1CH	Digital Filter Select 1	HPF3	STEREO2	LPF	HPF	EQ0	GN1	GN0	FIL3
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

FIL3: Stereo Emphasis Filter Control
0: OFF (default)
1: ON
When FIL3 bit = "1", settings of F3A13-0 and F3B13-0 bits are enabled.

GN1-0: Gain Block Gain Setting (Table 33)
Default: "00" (0dB)

EQ0: Gain Correction Filter (EQ0) Control
0: OFF (default)
1: ON
When EQ0 bit = "1", settings of E0A15-0, E0B13-0 and E0C15-0 bits are enabled. When EQ0 bit = "0", the audio data passes this block by 0dB gain.

HPF: HPF2 Coefficient Setting Enable
0: OFF (default)
1: ON
When HPF bit is "1", settings of F1A13-0 and F1B13-0 bits are enabled. When HPF bit is "0", the audio data passes this block by 0dB gain.

LPF: LPF Coefficient Setting Enable
0: OFF (default)
1: ON
When LPF bit is "1", settings of F2A13-0 and F2B13-0 bits are enabled. When LPF bit is "0", the audio data passes this block by 0dB gain.

STEREO2: Stereo Emphasis Method Select
0: Method 1 (Figure 42) (default)
1: Method 2 (Figure 43)

HPF3: HPF3 (Before ALC Input Level Read) Control
0: OFF (default)
1: ON
HPF3C2-0 bits setting is valid when HPF3 bit = "1". The data passes the HPF3 block by 0dB gain when HPF3 bit= "0".

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
1DH	Digital Filter Control	0	0	0	0	BRDAC	PFDAC	ADCPF	PFSDO
R/W		R	R	R	R	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	1	1

PFSDO: SDTO Output Signal Select
0: ADC (+ 1st HPF) Output
1: Programmable Filter / ALC Output (default)

ADCPF: Programmable Filter / ALC Input Signal Select
0: SDTI
1: ADC Output (default)

PFDAC: DAC Input Signal Select
0: SDTI (default)
1: Programmable Filter / ALC Output

BRDAC: DAC Input Signal Select
0: Mono/Stereo Switching Circuit Output (default)
1: Bass Boost/DRC Circuit Output

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
1FH	Register map Control	0	0	0	0	0	0	0	RBANK
R/W		R	R	R	R	R	R	R	R/W
Default		0	0	0	0	0	0	0	0

RBANK: Accessing Register Map Select (after 20H)
0: Register Map 2 (default)
1: Register Map 3

■ Register Definitions (Register Map2: RBANK bit = "0")

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
20H	HPF2 Co-efficient 0	F1A7	F1A6	F1A5	F1A4	F1A3	F1A2	F1A1	F1A0
21H	HPF2 Co-efficient 1	0	0	F1A13	F1A12	F1A11	F1A10	F1A9	F1A8
22H	HPF2 Co-efficient 2	F1B7	F1B6	F1B5	F1B4	F1B3	F1B2	F1B1	F1B0
23H	HPF2 Co-efficient 3	0	0	F1B13	F1B12	F1B11	F1B10	F1B9	F1B8
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		F1A13-0 bits = 0x1FB0, F1B13-0 bits = 0x209F							

F1A13-0, F1B13-0: HPF2 Coefficient (14bit x 2)
Default: F1A13-0 bits = 0x1FB0, F1B13-0 bits = 0x209F
fc = 150Hz@fs=48kHz

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
24H	LPF Co-efficient 0	F2A7	F2A6	F2A5	F2A4	F2A3	F2A2	F2A1	F2A0
25H	LPF Co-efficient 1	0	0	F2A13	F2A12	F2A11	F2A10	F2A9	F2A8
26H	LPF Co-efficient 2	F2B7	F2B6	F2B5	F2B4	F2B3	F2B2	F2B1	F2B0
27H	LPF Co-efficient 3	0	0	F2B13	F2B12	F2B11	F2B10	F2B9	F2B8
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

F2A13-0, F2B13-0: LPF Coefficient (14bit x 2)
Default: "0000H"

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
28H	FIL3 Co-efficient 0	F3A7	F3A6	F3A5	F3A4	F3A3	F3A2	F3A1	F3A0
29H	FIL3 Co-efficient 1	F3AS	0	F3A13	F3A12	F3A11	F3A10	F3A9	F3A8
2AH	FIL3 Co-efficient 2	F3B7	F3B6	F3B5	F3B4	F3B3	F3B2	F3B1	F3B0
2BH	FIL3 Co-efficient 3	0	0	F3B13	F3B12	F3B11	F3B10	F3B9	F3B8
2CH	EQ0 Co-efficient 0	E0A7	E0A6	E0A5	E0A4	E0A3	E0A2	E0A1	E0A0
2DH	EQ0 Co-efficient 1	E0A15	E0A14	E0A13	E0A12	E0A11	E0A10	E0A9	E0A8
2EH	EQ0 Co-efficient 2	E0B7	E0B6	E0B5	E0B4	E0B3	E0B2	E0B1	E0B0
2FH	EQ0 Co-efficient 3	0	0	E0B13	E0B12	E0B11	E0B10	E0B9	E0B8
30H	EQ0 Co-efficient 4	E0C7	E0C6	E0C5	E0C4	E0C3	E0C2	E0C1	E0C0
31H	EQ0 Co-efficient 5	E0C15	E0C14	E0C13	E0C12	E0C11	E0C10	E0C9	E0C8
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

F3A13-0, F3B13-0: Stereo Emphasis FIL3 Coefficient (14bit x 2)
Default: "0000H"

F3AS: Stereo Emphasis FIL3 Select
0: HPF (default)
1: LPF

E0A15-0, E0B13-0, E0C15-C0: Gain Compensation Filter Coefficient (16bit x 2 + 14bit x 1)
Default: "0000H"

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
32H	Digital Filter Select 2	0	0	0	EQ5	EQ4	EQ3	EQ2	EQ1
R/W		R	R	R	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

EQ1: Equalizer 1 Coefficient Setting Enable
0: Disable (default)
1: Enable
When EQ1 bit = "1", settings of E1A15-0, E1B15-0 and E1C15-0 bits are enabled. When EQ1 bit = "0", the audio data passes this block by 0dB gain.

EQ2: Equalizer 2 Coefficient Setting Enable
0: Disable (default)
1: Enable
When EQ2 bit = "1", settings of E2A15-0, E2B15-0 and E2C15-0 bits are enabled. When EQ2 bit = "0", the audio data passes this block by 0dB gain.

EQ3: Equalizer 3 Coefficient Setting Enable
0: Disable (default)
1: Enable
When EQ3 bit = "1", settings of E3A15-0, E3B15-0 and E3C15-0 bits are enabled. When EQ3 bit = "0", the audio data passes this block by 0dB gain.

EQ4: Equalizer 4 Coefficient Setting Enable
0: Disable (default)
1: Enable
When EQ4 bit = "1", settings of E4A15-0, E4B15-0 and E4C15-0 bits are enabled. When EQ4 bit = "0", the audio data passes this block by 0dB gain.

EQ5: Equalizer 5 Coefficient Setting Enable
0: Disable (default)
1: Enable
When EQ5 bit = "1", settings of E5A15-0, E5B15-0 and E5C15-0 bits are enabled. When EQ5 bit = "0". the audio data passes this block by 0dB gain.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
33H	EQ Common Gain Select	0	0	0	EQC5	EQC4	EQC3	EQC2	EQBP
R/W		R	R	R	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

EQBP: Main Path Switch of 4-Band Equalizer (Table 34)
0: ON (Audio data) (default)
1: OFF (“0” data)

EQC2: Equalizer 2 Common Gain Selector
0: Disable (default)
1: Enable
When EQC2 bit = “1”, the common gain setting (EQ2G) is reflected.

EQC3: Equalizer 3 Common Gain Selector
0: Disable (default)
1: Enable
When EQC3 bit = “1”, the common gain setting (EQ3G) is reflected.

EQC4: Equalizer 4 Common Gain Selector
0: Disable (default)
1: Enable
When EQC4 bit = “1”, the common gain setting (EQ4G) is reflected.

EQC5: Equalizer 5 Common Gain Selector
0: Disable (default)
1: Enable
When EQC5 bit = “1”, the common gain setting (EQ5G) is reflected.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
34H	EQ2 Common Gain Setting	EQ2G5	EQ2G4	EQ2G3	EQ2G2	EQ2G1	EQ2G0	EQ2T1	EQ2T0
35H	EQ3 Common Gain Setting	EQ3G5	EQ3G4	EQ3G3	EQ3G2	EQ3G1	EQ3G0	EQ3T1	EQ3T0
36H	EQ4 Common Gain Setting	EQ4G5	EQ4G4	EQ4G3	EQ4G2	EQ4G1	EQ4G0	EQ4T1	EQ4T0
37H	EQ5 Common Gain Setting	EQ5G5	EQ5G4	EQ5G3	EQ5G2	EQ5G1	EQ5G0	EQ5T1	EQ5T0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

EQ2T1-0, EQ3T1-0, EQ4T1-0, EQ5T1-0: Transition Time of EQ2~EQ5 Gain (Table 36)
Default: “00H” (256/fs)

EQ2G5-0, EQ3G5-0, EQ4G5-0, EQ5G5-0: Gain setting of EQ2~EQ5 (Table 35)
Default: “00H” (Mute)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
38H	E1 Co-efficient 0	E1A7	E1A6	E1A5	E1A4	E1A3	E1A2	E1A1	E1A0
39H	E1 Co-efficient 1	E1A15	E1A14	E1A13	E1A12	E1A11	E1A10	E1A9	E1A8
3AH	E1 Co-efficient 2	E1B7	E1B6	E1B5	E1B4	E1B3	E1B2	E1B1	E1B0
3BH	E1 Co-efficient 3	E1B15	E1B14	E1B13	E1B12	E1B11	E1B10	E1B9	E1B8
3CH	E1 Co-efficient 4	E1C7	E1C6	E1C5	E1C4	E1C3	E1C2	E1C1	E1C0
3DH	E1 Co-efficient 5	E1C15	E1C14	E1C13	E1C12	E1C11	E1C10	E1C9	E1C8
3EH	E2 Co-efficient 0	E2A7	E2A6	E2A5	E2A4	E2A3	E2A2	E2A1	E2A0
3FH	E2 Co-efficient 1	E2A15	E2A14	E2A13	E2A12	E2A11	E2A10	E2A9	E2A8
40H	E2 Co-efficient 2	E2B7	E2B6	E2B5	E2B4	E2B3	E2B2	E2B1	E2B0
41H	E2 Co-efficient 3	E2B15	E2B14	E2B13	E2B12	E2B11	E2B10	E2B9	E2B8
42H	E2 Co-efficient 4	E2C7	E2C6	E2C5	E2C4	E2C3	E2C2	E2C1	E2C0
43H	E2 Co-efficient 5	E2C15	E2C14	E2C13	E2C12	E2C11	E2C10	E2C9	E2C8
44H	E3 Co-efficient 0	E3A7	E3A6	E3A5	E3A4	E3A3	E3A2	E3A1	E3A0
45H	E3 Co-efficient 1	E3A15	E3A14	E3A13	E3A12	E3A11	E3A10	E3A9	E3A8
46H	E3 Co-efficient 2	E3B7	E3B6	E3B5	E3B4	E3B3	E3B2	E3B1	E3B0
47H	E3 Co-efficient 3	E3B15	E3B14	E3B13	E3B12	E3B11	E3B10	E3B9	E3B8
48H	E3 Co-efficient 4	E3C7	E3C6	E3C5	E3C4	E3C3	E3C2	E3C1	E3C0
49H	E3 Co-efficient 5	E3C15	E3C14	E3C13	E3C12	E3C11	E3C10	E3C9	E3C8
4AH	E4 Co-efficient 0	E4A7	E4A6	E4A5	E4A4	E4A3	E4A2	E4A1	E4A0
4BH	E4 Co-efficient 1	E4A15	E4A14	E4A13	E4A12	E4A11	E4A10	E4A9	E4A8
4CH	E4 Co-efficient 2	E4B7	E4B6	E4B5	E4B4	E4B3	E4B2	E4B1	E4B0
4DH	E4 Co-efficient 3	E4B15	E4B14	E4B13	E4B12	E4B11	E4B10	E4B9	E4B8
4EH	E4 Co-efficient 4	E4C7	E4C6	E4C5	E4C4	E4C3	E4C2	E4C1	E4C0
4FH	E4 Co-efficient 5	E4C15	E4C14	E4C13	E4C12	E4C11	E4C10	E4C9	E4C8
50H	E5 Co-efficient 0	E5A7	E5A6	E5A5	E5A4	E5A3	E5A2	E5A1	E5A0
51H	E5 Co-efficient 1	E5A15	E5A14	E5A13	E5A12	E5A11	E5A10	E5A9	E5A8
52H	E5 Co-efficient 2	E5B7	E5B6	E5B5	E5B4	E5B3	E5B2	E5B1	E5B0
53H	E5 Co-efficient 3	E5B15	E5B14	E5B13	E5B12	E5B11	E5B10	E5B9	E5B8
54H	E5 Co-efficient 4	E5C7	E5C6	E5C5	E5C4	E5C3	E5C2	E5C1	E5C0
55H	E5 Co-efficient 5	E5C15	E5C14	E5C13	E5C12	E5C11	E5C10	E5C9	E5C8
Default		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		0	0	0	0	0	0	0	0

E1A15-0, E1B15-0, E1C15-0: Equalizer 1 Coefficient (16bit x3)
Default: “0000H”

E2A15-0, E2B15-0, E2C15-0: Equalizer 2 Coefficient (16bit x3)
Default: “0000H”

E3A15-0, E3B15-0, E3C15-0: Equalizer 3 Coefficient (16bit x3)
Default: “0000H”

E4A15-0, E4B15-0, E4C15-0: Equalizer 4 Coefficient (16bit x3)
Default: “0000H”

E5A15-0, E5B15-0, E5C15-0: Equalizer 5 Coefficient (16bit x3)
Default: “0000H”

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
56H	AutoHPF Control	0	0	AHPF	SENC2	SENC1	SENC0	STG1	STG0
R/W		R	R	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	1	1	0	0

STG1-0: Automatic Wind Noise Reduction Filter Maximum Attenuation Level (Table 31)
Default: "00" (Low)

SENC2-0: Wind Noise Detection Sensitivity (Table 30)
Default: "011" (2.0)

AHPF: Automatic Wind Noise Reduction Filter Control
0: OFF (default)
1: ON
When AHPF bit = "1", the automatic wind noise reduction filter is enabled. The audio data passes this block by 0dB gain when AHPF bit = "0".

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
57H	DRC Mode Control	DRC	DLMAT2	DLMAT1	DLMAT0	DRGAIN1	DRGAIN0	DRCC1	DRCC0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

DRCC1-0: DRC Compression Level Setting (Table 74)
Defaut: "00" (Disable)

DRGAIN1-0: DRC Recovery Speed Setting (Table 76)
Default: "00" (6.4dB/s @ fs=48kHz)

DLMAT2-0: DRC Attenuation Speed Setting (Table 75)
Default: "000" (0.8dB/ms @ fs=48kHz)

DRC: DRC Block Control
0: OFF (default)
1: ON
When DRC bit = "1", DRC block is enabled. The audio data passes this block by 0dB gain when DRC bit = "0".

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
58H	DVLC Mode Control	DVRGAIN2	DVRGAIN1	DVRGAIN0	DVLMAT2	DVLMAT1	DVLMAT0	DAF1	DAF0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	1	1	0	1	1	1	1

DAF1-0: DVLC Moving Average Parameter Setting (Table 71)
Default: "11" (2048/fs)

DVLMAT2-0: DVLC Attenuation Speed Setting (Table 72)
Default: "011" (50.9dB/s @ fs=48kHz)

DVRGAIN2-0: DVLC Recovery Speed Setting (Table 73)
Default: "011" (3.18dB/s @ fs=48kHz)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
59H	DVLC Filter Select	0	0	0	0	DLLPF	DMHPF	DMLPF	DHHPF
R/W		R	R	R	R	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

DHHPF: DVLC High Frequency Range HPF Mode (Table 67)
0: OFF ("0" data) (default)
1: ON
When DHHPF bit = "1", settings of DHHA13-0 and DHHB13-0 bits are enabled. When DHHPF bit = "0", the input data of DVLC High Frequency Range HPF becomes "0".

DMLPF1-0: DVLC Middle Frequency Range LPF Mode (Table 63)
0: Bypass (default)
1: ON
When DMLPF bit = "1", settings of DMLA13-0, DMLB13-0 bits are enabled. When DMLPF bit = "0", the audio data passes this block by 0dB gain.

DMHPF1-0: DVLC Middle Frequency Range HPF Mode (Table 62)
0: Bypass (default)
1: ON
When DMHPF bit = "1", settings of DMHA13-0, DMHB13-0 bits are enabled. When DMHPF bit = "0", the audio data passes this block by 0dB gain.

DLLPF1-0: DVLC Low Frequency Range LPF Mode (Table 58)
0: OFF ("0" data) (default)
1: ON
When DLLPF bit = "1", settings of DLLA13-0, DLLB13-0 bits are enabled. When DLLPF bit = "0", the input data of DVLC Low Frequency Range LPF becomes "0".

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
5AH	Boost Control	BSTON	0	BGN5	BGN4	BGN3	BGN2	BGN1	BGN0
R/W		R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

BGN5-0: Boost Level Setting of Bass Boost Block (Table 57)
Default: "00H" (No Boosting)

BSTON: Bass Boost Function Control
0: OFF (default)
1: ON
When BSTON bit = "1", the Bass Boost block is enabled. When BSTON bit = "0", the audio data passes this block by 0dB gain.

■ Register Definitions (Register Map3: RBANK bit = "1")

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
20H	DVLCL Curve X1	0	0	VL1X5	VL1X4	VL1X3	VL1X2	VL1X1	VL1X0
21H	DVLCL Curve Y1	0	0	VL1Y5	VL1Y4	VL1Y3	VL1Y2	VL1Y1	VL1Y0
22H	DVLCL Curve X2	0	0	VL2X5	VL2X4	VL2X3	VL2X2	VL2X1	VL2X0
23H	DVLCL Curve Y2	0	0	VL2Y5	VL2Y4	VL2Y3	VL2Y2	VL2Y1	VL2Y0
24H	DVLCL Curve X3	0	0	0	VL3X4	VL3X3	VL3X2	VL3X1	VL3X0
25H	DVLCL Curve Y3	0	0	0	VL3Y4	VL3Y3	VL3Y2	VL3Y1	VL3Y0
26H	DVLCL Slope 1	0	L1G6	L1G5	L1G4	L1G3	L1G2	L1G1	L1G0
27H	DVLCL Slope 2	0	L2G6	L2G5	L2G4	L2G3	L2G2	L2G1	L2G0
28H	DVLCL Slope 3	0	L3G6	L3G5	L3G4	L3G3	L3G2	L3G1	L3G0
29H	DVLCL Slope 4	0	L4G6	L4G5	L4G4	L4G3	L4G2	L4G1	L4G0
2AH	DVLCM Curve X1	0	0	VM1X5	VM1X4	VM1X3	VM1X2	VM1X1	VM1X0
2BH	DVLCM Curve Y1	0	0	VM1Y5	VM1Y4	VM1Y3	VM1Y2	VM1Y1	VM1Y0
2CH	DVLCM Curve X2	0	0	VM2X5	VM2X4	VM2X3	VM2X2	VM2X1	VM2X0
2DH	DVLCM Curve Y2	0	0	VM2Y5	VM2Y4	VM2Y3	VM2Y2	VM2Y1	VM2Y0
2EH	DVLCM Curve X3	0	0	0	VM3X4	VM3X3	VM3X2	VM3X1	VM3X0
2FH	DVLCM Curve Y3	0	0	0	VM3Y4	VM3Y3	VM3Y2	VM3Y1	VM3Y0
30H	DVLCM Slope 1	0	M1G6	M1G5	M1G4	M1G3	M1G2	M1G1	M1G0
31H	DVLCM Slope 2	0	M2G6	M2G5	M2G4	M2G3	M2G2	M2G1	M2G0
32H	DVLCM Slope 3	0	M3G6	M3G5	M3G4	M3G3	M3G2	M3G1	M3G0
33H	DVLCM Slope 4	0	M4G6	M4G5	M4G4	M4G3	M4G2	M4G1	M4G0
34H	DVLCH Curve X1	0	0	VH1X5	VH1X4	VH1X3	VH1X2	VH1X1	VH1X0
35H	DVLCH Curve Y1	0	0	VH1Y5	VH1Y4	VH1Y3	VH1Y2	VH1Y1	VH1Y0
36H	DVLCH Curve X2	0	0	VH2X5	VH2X4	VH2X3	VH2X2	VH2X1	VH2X0
37H	DVLCH Curve Y2	0	0	VH2Y5	VH2Y4	VH2Y3	VH2Y2	VH2Y1	VH2Y0
38H	DVLCH Curve X3	0	0	0	VH3X4	VH3X3	VH3X2	VH3X1	VH3X0
39H	DVLCH Curve Y3	0	0	0	VH3Y4	VH3Y3	VH3Y2	VH3Y1	VH3Y0
3AH	DVLCH Slope 1	0	H1G6	H1G5	H1G4	H1G3	H1G2	H1G1	H1G0
3BH	DVLCH Slope 2	0	H2G6	H2G5	H2G4	H2G3	H2G2	H2G1	H2G0
3CH	DVLCH Slope 3	0	H3G6	H3G5	H3G4	H3G3	H3G2	H3G1	H3G0
3DH	DVLCH Slope 4	0	H4G6	H4G5	H4G4	H4G3	H4G2	H4G1	H4G0
R/W		0	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

VL1X5-0, VL2X5-0, VL3X4-0: Input Gain Setting of Low Range DVLC Point (Table 59, Table 60)
Default: "00H" (0dB)

VL1Y5-0, VL2Y5-0, VL3Y4-0: Output Gain Setting of Low Range DVLC Point (Table 59, Table 60)
Default: "00H" (0dB)

L1G6-0, L2G6-0, L3G6-0, L4G6-0: Low Range DVLC Slope Setting (Table 61)
Default: "00H"

VM1X5-0, VM2X5-0, VM3X4-0: Input Gain Setting of Middle Range DVLC Point (Table 64, Table 65)
Default: "00H" (0dB)

VM1Y5-0, VM2Y5-0, VM3Y4-0: Output Gain Setting of Middle Range DVLC Point (Table 64, Table 65)
Default: "00H" (0dB)

M1G6-0, M2G6-0, M3G6-0, M4G6-0: Middle Range DVLC Slope Setting (Table 66)
Default: "00H"

VH1X5-0, VH2X5-0, VH3X4-0: Input Gain Setting of High Range DVLC Point (Table 68, Table 69)
Default: "00H" (0dB)

VH1Y5-0, VH2Y5-0, VH3Y4-0: Output Gain Setting of High Range DVLC Point (Table 68, Table 69)
Default: "00H" (0dB)

H1G6-0, H2G6-0, H3G6-0, H4G6-0: High Range DVLC Slope Setting (Table 70)
Default: "00H"

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
3EH	DVLCL LPF Co-efficient 0	DLLA7	DLLA6	DLLA5	DLLA4	DLLA3	DLLA2	DLLA1	DLLA0
3FH	DVLCL LPF Co-efficient 1	0	0	DLLA13	DLLA12	DLLA11	DLLA10	DLLA9	DLLA8
40H	DVLCL LPF Co-efficient 2	DLLB7	DLLB6	DLLB5	DLLB4	DLLB3	DLLB2	DLLB1	DLLB0
41H	DVLCL LPF Co-efficient 3	0	0	DLLB13	DLLB12	DLLB11	DLLB10	DLLB9	DLLB8
42H	DVLCM HPF Co-efficient 0	DMHA7	DMHA6	DMHA5	DMHA4	DMHA3	DMHA2	DMHA1	DMHA0
43H	DVLCM HPF Co-efficient 1	0	0	DMHA13	DMHA12	DMHA11	DMHA10	DMHA9	DMHA8
44H	DVLCM HPF Co-efficient 2	DMHB7	DMHB6	DMHB5	DMHB4	DMHB3	DMHB2	DMHB1	DMHB0
45H	DVLCM HPF Co-efficient 3	0	0	DMHB13	DMHB12	DMHB11	DMHB10	DMHB9	DMHB8
46H	DVLCM LPF Co-efficient 0	DMLA7	DMLA6	DMLA5	DMLA4	DMLA3	DMLA2	DMLA1	DMLA0
47H	DVLCM LPF Co-efficient 1	0	0	DMLA13	DMLA12	DMLA11	DMLA10	DMLA9	DMLA8
48H	DVLCM LPF Co-efficient 2	DMLB7	DMLB6	DMLB5	DMLB4	DMLB3	DMLB2	DMLB1	DMLB0
49H	DVLCM LPF Co-efficient 3	0	0	DMLB13	DMLB12	DMLB11	DMLB10	DMLB9	DMLB8
4AH	DVLCH HPF Co-efficient 0	DHHA7	DHHA6	DHHA5	DHHA4	DHHA3	DHHA2	DHHA1	DHHA0
4BH	DVLCH HPF Co-efficient 1	0	0	DHHA13	DHHA12	DHHA11	DHHA10	DHHA9	DHHA8
4CH	DVLCH HPF Co-efficient 2	DHHB7	DHHB6	DHHB5	DHHB4	DHHB3	DHHB2	DHHB1	DHHB0
4DH	DVLCH HPF Co-efficient 3	0	0	DHHB13	DHHB12	DHHB11	DHHB10	DHHB9	DHHB8
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

DLLA13-0, DLLB13-0: LPF Coefficient of DVLC Low Frequency Range (14bit x 2)
Default: “0000H”

DMHA13-0, DMHB13-0: HPF Coefficient of DVLC Middle Frequency Range (14bit x 2)
Default: “0000H”

DMLA13-0, DMLB13-0: LPF Coefficient of DVLC Middle Frequency Range (14bit x 2)
Default: “0000H”

DHHA13-0, DHHB13-0: HPF Coefficient of DVLC High Frequency Range (14bit x 2)
Default: “0000H”

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
4EH	Boost HPF4 Co-efficient 0	BHA7	BHA6	BHA5	BHA4	BHA3	BHA2	BHA1	BHA0
4FH	Boost HPF4 Co-efficient 1	BHB7	BHB6	BHB5	BHB4	BHB3	BHB2	BHB1	BHB0
50H	Boost LPF2 Co-efficient 0	BLA7	BLA6	BLA5	BLA4	BLA3	BLA2	BLA1	BLA0
51H	Boost LPF2 Co-efficient 1	BLB7	BLB6	BLB5	BLB4	BLB3	BLB2	BLB1	BLB0
52H	Boost BPF1 Co-efficient 0	BB1A7	BB1A6	BB1A5	BB1A4	BB1A3	BB1A2	BB1A1	BB1A0
53H	Boost BPF1 Co-efficient 1	BB1B7	BB1B6	BB1B5	BB1B4	BB1B3	BB1B2	BB1B1	BB1B0
54H	Boost BPF1 Co-efficient 2	BB1B15	BB1B14	BB1B13	BB1B12	BB1B11	BB1B10	BB1B9	BB1B8
55H	Boost BPF1 Co-efficient 3	BB1C7	BB1C6	BB1C5	BB1C4	BB1C3	BB1C2	BB1C1	BB1C0
56H	Boost BPF1 Co-efficient 4	BB1C15	BB1C14	BB1C13	BB1C12	BB1C11	BB1C10	BB1C9	BB1C8
57H	Boost BPF2 Co-efficient 0	BB2A7	BB2A6	BB2A5	BB2A4	BB2A3	BB2A2	BB2A1	BB2A0
58H	Boost BPF2 Co-efficient 1	BB2B7	BB2B6	BB2B5	BB2B4	BB2B3	BB2B2	BB2B1	BB2B0
59H	Boost BPF2 Co-efficient 2	BB2B15	BB2B14	BB2B13	BB2B12	BB2B11	BB2B10	BB2B9	BB2B8
5AH	Boost BPF2 Co-efficient 3	BB2C7	BB2C6	BB2C5	BB2C4	BB2C3	BB2C2	BB2C1	BB2C0
5BH	Boost BPF2 Co-efficient 4	BB2C15	BB2C14	BB2C13	BB2C12	BB2C11	BB2C10	BB2C9	BB2C8
5CH	Boost BPF3 Co-efficient 0	BB3A7	BB3A6	BB3A5	BB3A4	BB3A3	BB3A2	BB3A1	BB3A0
5DH	Boost BPF3 Co-efficient 1	BB3B7	BB3B6	BB3B5	BB3B4	BB3B3	BB3B2	BB3B1	BB3B0
5EH	Boost BPF3 Co-efficient 2	BB3B15	BB3B14	BB3B13	BB3B12	BB3B11	BB3B10	BB3B9	BB3B8
5FH	Boost BPF3 Co-efficient 3	BB3C7	BB3C6	BB3C5	BB3C4	BB3C3	BB3C2	BB3C1	BB3C0
60H	Boost BPF3 Co-efficient 4	BB3C15	BB3C14	BB3C13	BB3C12	BB3C11	BB3C10	BB3C9	BB3C8
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

BHA7-0, BHB7-0: HPF Coefficient of Bass Boost Block (8bit x 2)
Default: "00H"

BLA7-0, BLB7-0: LPF Coefficient of Bass Boost Block (8bit x 2)
Default: "00H"

BB1A7-0, BB1B15-0, BB1C15-0: BPF1 Coefficient of Bass Boost Block (8bit x 1, 16bit x 2)
Default: BB1A7-0 bits = "00H", BB1B15-0, BB1C15-0 bits = "0000H"

BB2A7-0, BB2B15-0, BB2C15-0: BPF2 Coefficient of Bass Boost Block (8bit x 1, 16bit x 2)
Default: BB2A7-0 bits = "00H", BB2B15-0, BB2C15-0 bits = "0000H"

BB3A7-0, BB3B15-0, BB3C15-0: BPF3 Coefficient of Bass Boost Block (8bit x 1, 16bit x 2)
Default: BB3A7-0 bits = "00H", BB3B15-0, BB3C15-0 bits = "0000H"

SYSTEM DESIGN (AK4958EG)

Figure 80 shows the system connection diagram. An evaluation board (AKD4958EG) is available for fast evaluation as well as suggestions for peripheral circuitry.

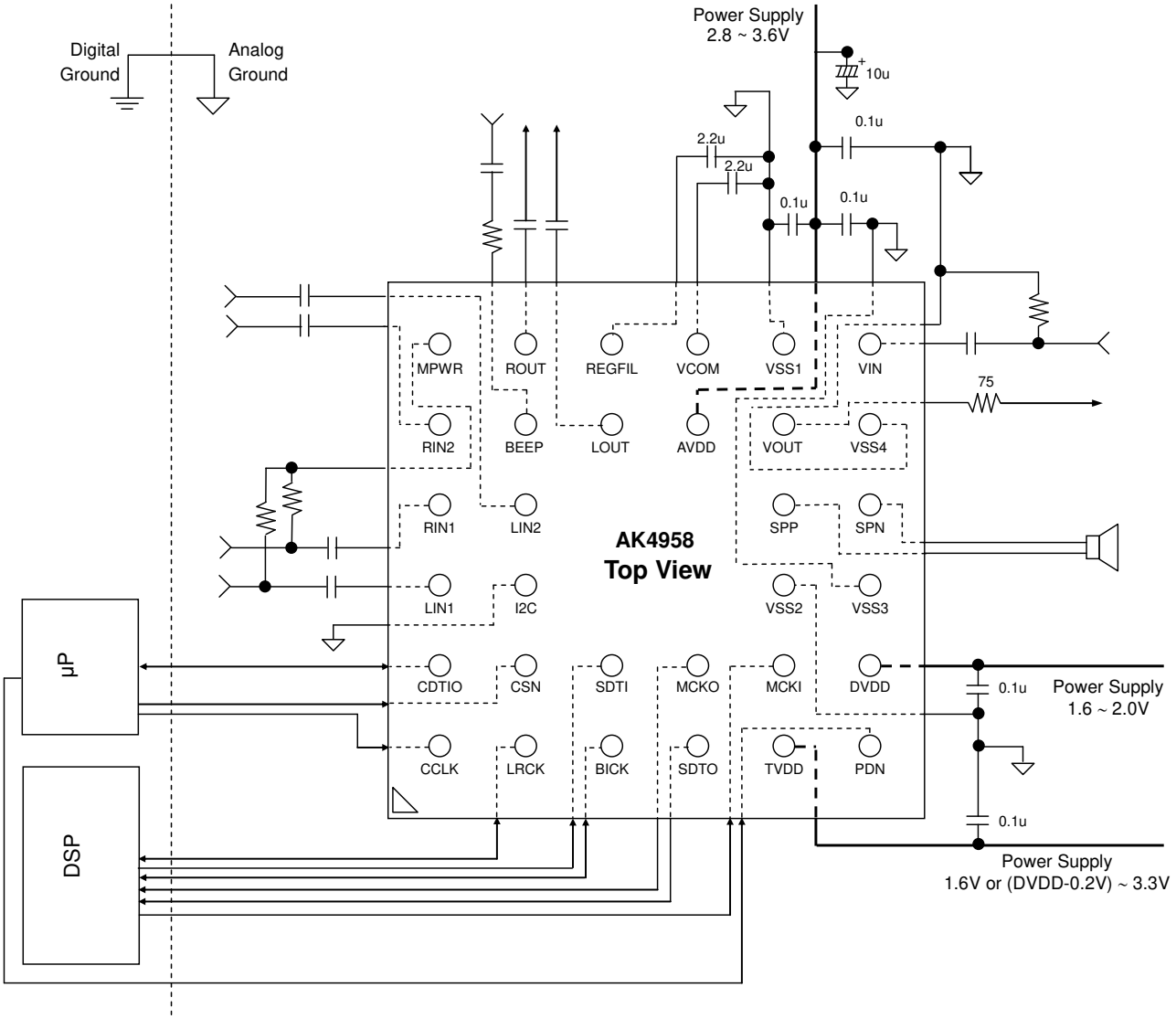


Figure 80. System Connection Diagram (AK4958EG)
(3-wire Serial Mode: I2C pin = "L", BEEP pin External Resistance Mode: BPM bit = "0")

Notes:

- VSS1, VSS2, VSS3 and VSS4 of the AK4958EG must be distributed separately from the ground of external controllers.
- All digital input pins must not be allowed to float.
- When the AK4958EG is used in master mode, LRCK and BICK pins are floating before M/S bit is changed to "1". Therefore, a pull-up or pull-down resistor around 100kΩ must be connected to LRCK and BICK pins of the AK4958EG.
- When the AK4958EG is used in I^2C mode, the I2C pin must be connected to AVDD and the pull-up resistors of the SCL and SDA pins must be connected to the voltage that is TVDD or less and 6V or less.

SYSTEM DESIGN（AK4958ECB）

Figure 81 shows the system connection diagram. An evaluation board (AKD4958ECB) is available for fast evaluation as well as suggestions for peripheral circuitry.

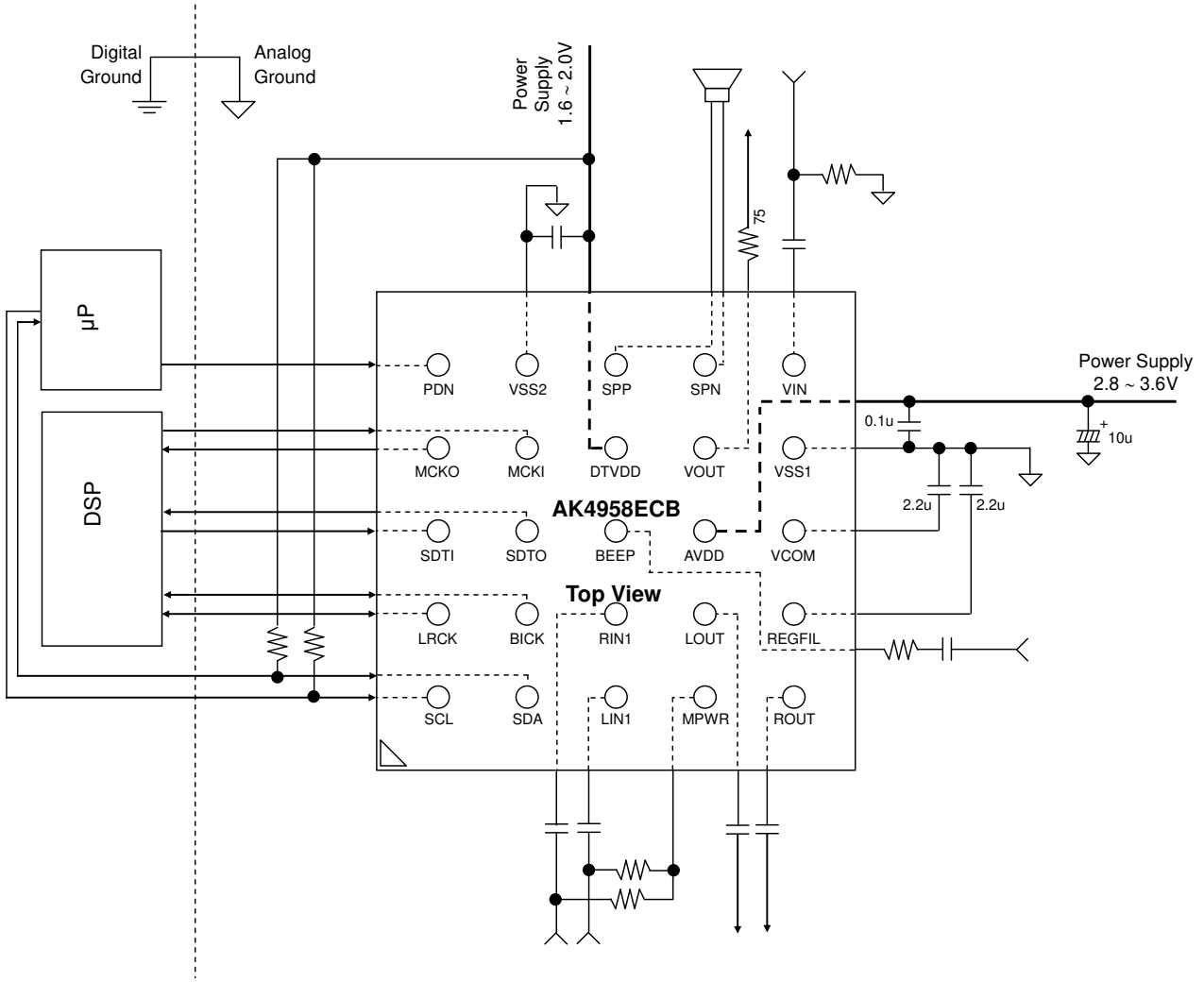


Figure 81. System Connection Diagram (AK4958ECB)
(BEEP pin External Resistance mode; BPM bit = "1")

Notes:
- VSS1 and VSS2 of the AK4958ECB must be distributed separately from the ground of external controllers.
- All digital input pins must not be allowed to float.
- When the AK4958ECB is used in master mode, LRCK and BICK pins are floating before M/S bit is changed to "1". Therefore, a pull-up or pull-down resistor around 100kΩ must be connected to LRCK and BICK pins of the AK4958ECB.

1. Grounding and Power Supply Decoupling

▪ AK4958EG
The AK4958 requires careful attention to power supply and grounding arrangements. If AVDD, DVDD and TVDD are supplied separately, the power-up sequence is not critical. VSS1, VSS2, VSS3 and VSS4 of the AK4958 must be connected to the analog ground plane. System analog ground and digital ground should be wired separately and connected together as close as possible to where the supplies are brought onto the printed circuit board. Decoupling capacitors must be as near to the AK4958 as possible, with the small value ceramic capacitor being the nearest.

▪ AK4958ECB
The AK4958 requires careful attention to power supply and grounding arrangements. The power-up sequence of AVDD and TVDD is not critical. VSS1 and VSS2 of the AK4958 must be connected to the analog ground plane. System analog ground and digital ground should be wired separately and connected together as close as possible to where the supplies are brought onto the printed circuit board. Decoupling capacitors must be as near to the AK4958 as possible, with the small value ceramic capacitor being the nearest.

2. Internal Regulated Voltage Power Supply

REGFIL is a power supply of the analog circuit (typ. 2.3V). A 2.2μF ±50% capacitor attached to the VSS1 pin eliminates the effects of high frequency noise. This capacitor should be placed as near as possible to the AK4958. No load current may be drawn from the REGFIL pin. All digital signals, especially clocks, should be kept away from the REGFIL pin in order to avoid unwanted coupling into the AK4958.

3. Reference Voltage

VCOM is a signal ground of this chip. A 2.2μF ±50% capacitor attached to the VSS1 pin eliminates the effects of high frequency noise. This capacitor should be placed as near as possible to the AK4958. No load current may be drawn from the VCOM pin. All signals, especially clocks, should be kept away from the VCOM pin in order to avoid unwanted coupling into the AK4958. Attention must be paid to the printing pattern and the material of the capacitors to prevent superimposed noises and voltage drops since the VCOM voltage is the reference of many functions.

4. Analog Inputs

The microphone and line inputs support single-ended format. The input signal range scales with nominally at typ. 2.07Vpp (@ MGAIN = 0dB), centered around the internal signal ground (typ. 1.15V). Usually the input signal is AC coupled with a capacitor. The cut-off frequency is $fc = 1/(2\pi RC)$.

5. Analog Outputs

The input data format for the DAC is 2's complement. The output voltage is a positive full scale for 7FFFFFH (@24bit) and a negative full scale for 800000H (@24bit). The ideal output is VCOM voltage for 000000H (@24bit data). The common voltage of stereo lineout is typically 1.0Vrms (AVDD=3.3V) centered on 1.5V (typ) (@LVCM0 bit = "1"). The speaker outputs are centered on AVDD/2 (typ).

CONTROL SEQUENCE

■ Clock Set Up

When ADC, DAC, Programmable Filter Bass boost circuit or DRC block is powered-up, the clocks must be supplied.

1. PLL Master Mode

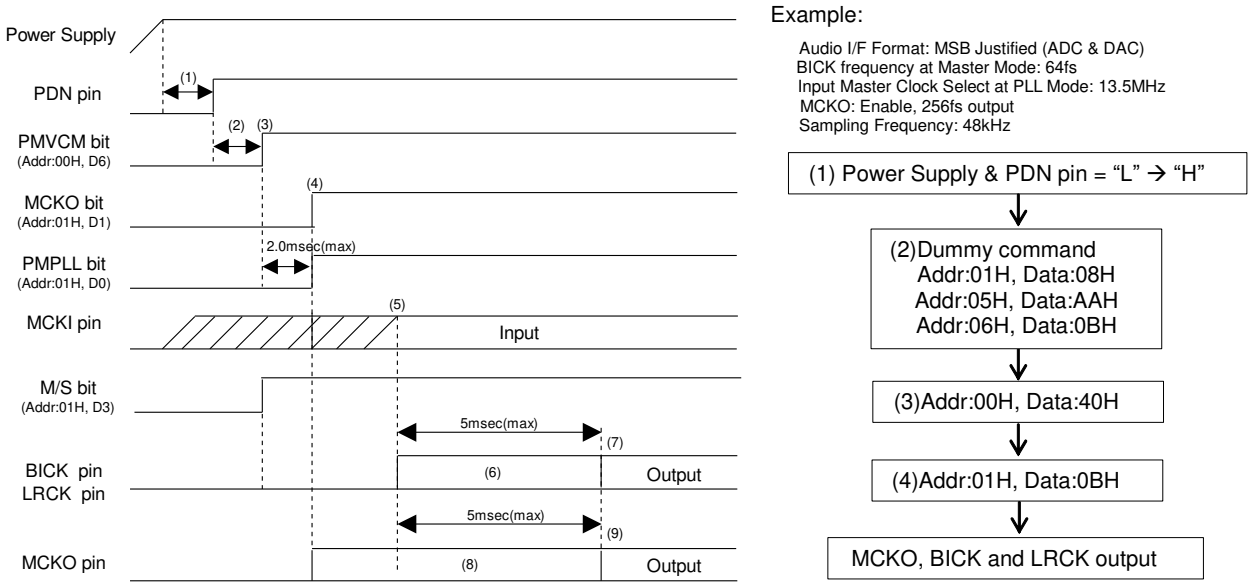


Figure 82. Clock Set Up Sequence (1)

<Sequence>

(1) After Power Up: PDN pin "L" → "H"
"L" time of 200ns or more is needed to reset the AK4958.

(2) After Dummy Command input, M/S, DIF1-0, BCKO, PLL3-0, FS3-0 and PS1-0 bits must be set during this period.

(3) Power Up VCOM and Regulator: PMVCM bit = "0" → "1"
VCOM and Regulator must first be powered-up before the other block operates. Power up time is 0.6ms (typ.), 2.0ms (max) when the capacitance of an external capacitor for the VCOM and the REGFIL pin is 2.2μF ±50% each.

(4) In case of using MCKO output: MCKO bit = "1"
In case of not using MCKO output: MCKO bit = "0"

(5) PLL starts after PMPLL bit changes from "0" to "1" and MCKI is supplied from an external source, and PLL lock time is 5ms (max)

(6) BICK pin outputs "H" and LRCK pin outputs "L" during this period.

(7) The AK4958 starts to output the LRCK and BICK clocks after the PLL became stable. Then normal operation starts.

(8) An invalid frequency is output from the MCKO pin during this period if MCKO bit = "1".

(9) A normal clock is output from the MCKO pin after the PLL is locked if MCKO bit = "1".

2. PLL Slave Mode (BICK pin)

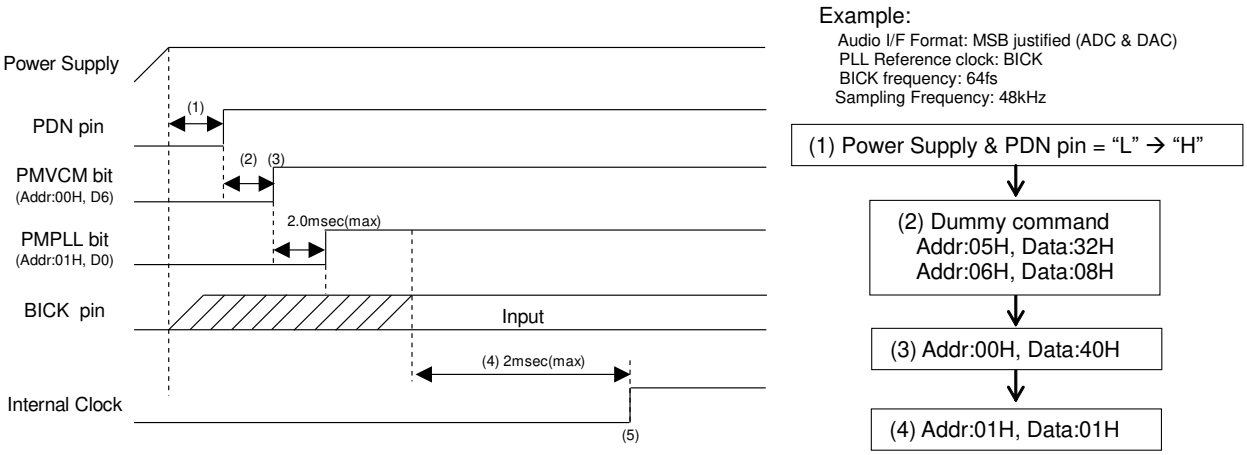


Figure 83. Clock Set Up Sequence (2)

<Sequence>

(1) After Power Up: PDN pin "L" → "H"
"L" time of 200ns or more is needed to reset the AK4958.

(2) After Dummy Command input, DIF1-0, PLL3-0, and FS3-0 bits must be set during this period.

(3) Power Up VCOM and Regulator: PMVCM bit = "0" → "1"
VCOM and Regulator must first be powered-up before the other block operates. Power up time is 0.6ms (ty.), 2.0ms (max) when the capacitance of an external capacitor for the VCOM and the REGFIL pin is 2.2μF ±50% each.

(4) PLL starts after the PMPLL bit changes from "0" to "1" and PLL reference clock (BICK pin) is supplied. PLL lock time is 2ms (max) when BICK is a PLL reference clock.

(5) Normal operation starts after that the PLL is locked.

3. PLL Slave Mode (MCKI pin)

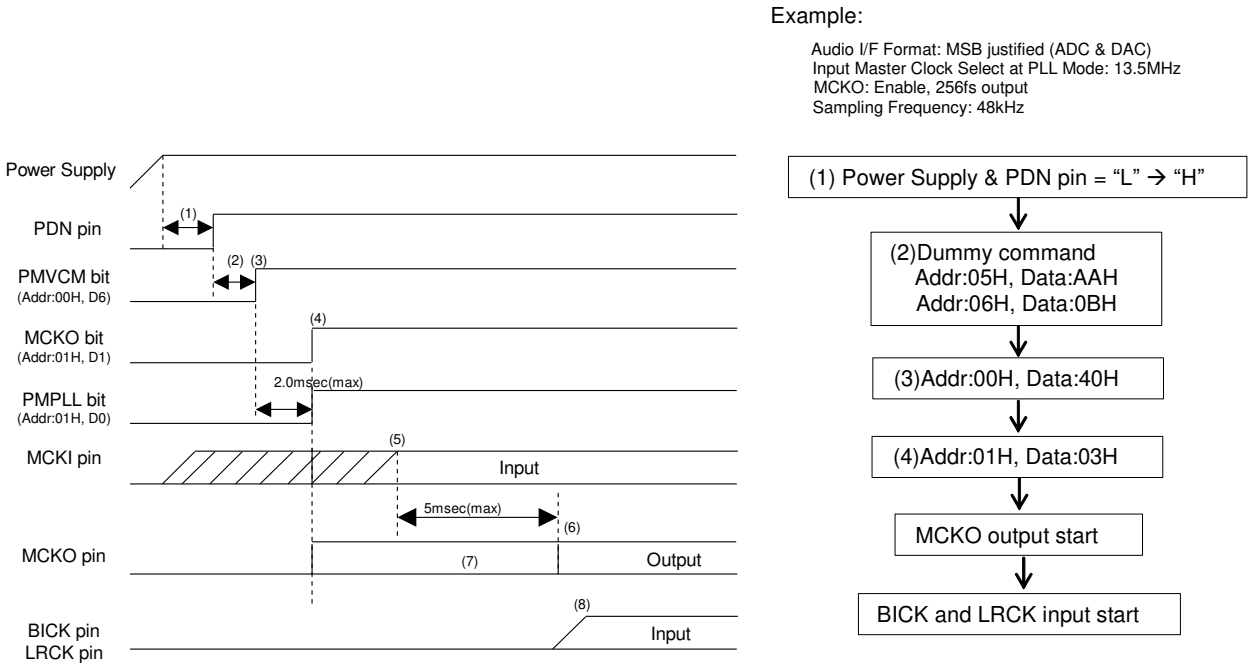


Figure 84. Clock Set Up Sequence (3)

<Sequence>

(1) After Power Up: PDN pin "L" → "H"
"L" time of 200ns or more is needed to reset the AK4958.
(2) After Dummy Command input, DIF1-0, PLL3-0, FS3-0 and PS1-0 bits must be set during this period.
(3) Power Up VCOM and Regulator: PMVCM bit = "0" → "1"
VCOM and Regulator must first be powered-up before the other block operates. Power up time is 0.6ms (typ.), 2.0ms (max) when the capacitance of an external capacitor for the VCOM pin and the REGFIL pin is 2.2μF ±50% each.
(4) Enable MCKO output: MCKO bit = "1"
(5) PLL starts after that the PMPLL bit changes from "0" to "1" and PLL reference clock (MCKI pin) is supplied. PLL lock time is 5ms (max).
(6) A normal clock is output from MCKO after PLL is locked.
(7) An invalid frequency is output from MCKO during this period.
(8) BICK and LRCK clocks must be synchronized with MCKO clock.

4. EXT Slave Mode

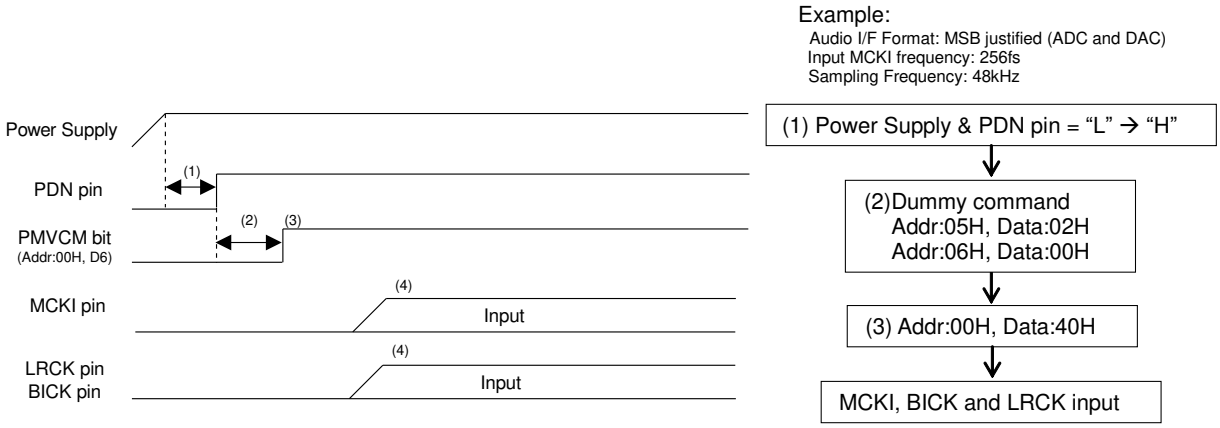


Figure 85. Clock Set Up Sequence (4)

<Sequence>

(1) After Power Up: PDN pin "L" → "H"
"L" time of 200ns or more is needed to reset the AK4958.

(2) After Dummy Command input, DIF1-0 and FS3-0 bits must be set during this period.

(3) Power Up VCOM and Regulator: PMVCM bit = "0" → "1"
VCOM and Regulator must first be powered-up before the other block operates. Power up time is 0.6ms (typ.), 2.0ms (max) when the capacitance of an external capacitor for the VCOM and the REGFIL pin is 2.2μF ±50% each.

(4) Normal operation starts after the MCKI, LRCK and BICK are supplied.

5. EXT Master Mode

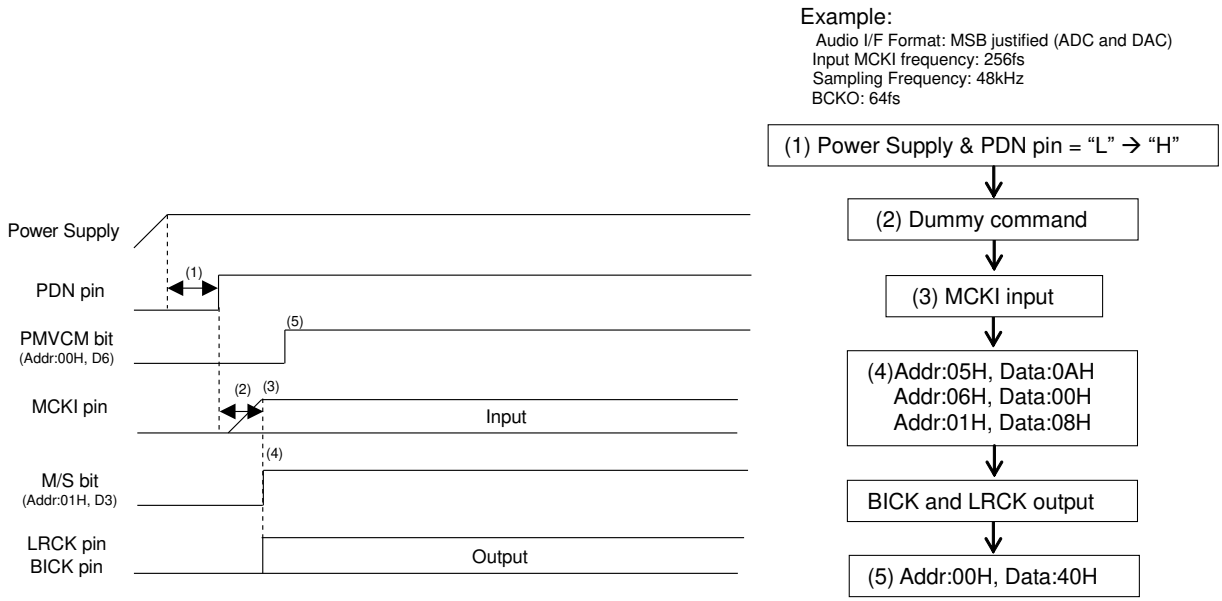


Figure 86. Clock Set Up Sequence (5)

<Sequence>

(1) After Power Up: PDN pin "L" → "H"
"L" time of 200ns or more is needed to reset the AK4958.
(2) Dummy Command must be input during this period.
(3) MCKI is supplied.
(4) After DIF1-0, BCKO and FS3-0 bits are set. M/S bit should be set to "1". Then LRCK and BICK are output.
(5) Power Up VCOM and Regulator: PMVCM bit = "0" → "1"
VCOM and Regulator must first be powered-up before the other block operates. Power up time is 0.6ms (typ.) 2.0ms (max) when both capacitances of an external capacitor for the VCOM and REGFIL pins are 2.2μF ±50% each.

■ Microphone Input Recording (Stereo)

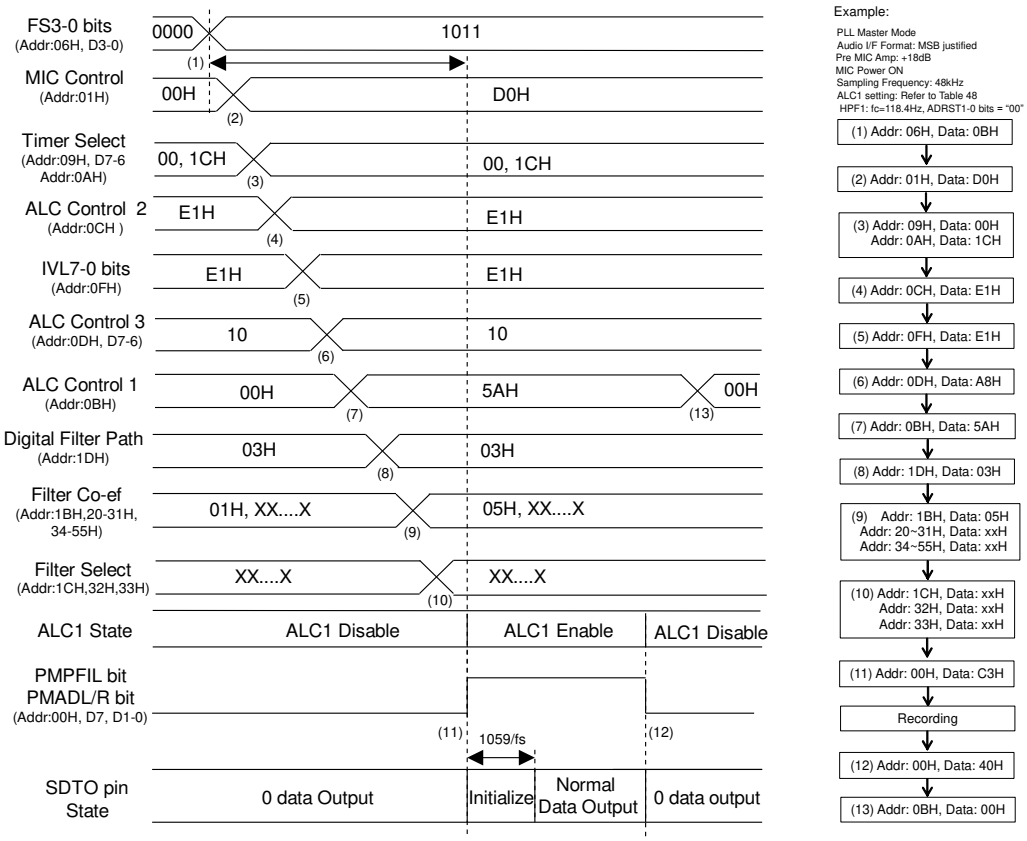


Figure 87. Microphone Input Recording Sequence

<Sequence>

This sequence is an example of ALC1 setting at fs= 48kHz. For changing the parameter of ALC, please refer to Table 49. At first, clocks should be supplied according to "Clock Set Up" sequence.

(1) Set up a sampling frequency (FS3-0 bits). When the AK4958 is in PLL mode, Microphone, ADC and Programmable Filter of (11) must be powered-up in consideration of PLL lock time after a sampling frequency is changed.
(2) Set up Microphone Amp and Microphone Power. (Addr = 01H)
(3) Set up ALC1 Timer, ADRST1-0 bits (Addr = 09H, 0AH)
(4) Set up IREF value at ALC1 (Addtr = 0CH)
(5) Set up IVOL value at ALC1 operation start (Addr = 0FH)
(6) Set up EQFC1-0 bits (Addr =0DH)
(7) Set up LMTH2-0, RGAIN2-0 and ALC1 bits (Addr = 0BH)
(8) Set up Programmable Filter Path: PFSDO bit = ADCPF bit = "1" (Addr = 1DH)
(9) Set up Coefficient Programmable Filter (Addr: 20H ~ 31H, 34H ~ 55H)
(10) Programmable Filter ON/OFF Setting (Addr: 1CH, 32H, 33H)
(11) Power Up ADC and Programmable Filter: PMADL = PMADR =PMPFIL bits = "0" → "1"
The initialization cycle time of ADC is 1059/fs=22ms @ fs=48kHz, ADRST1-0 bit = "00". ADC outputs "0" data during the initialization cycle. After the ALC1 bit is set to "1", the ALC1 operation starts from IVOL value of (5).
(12) Power Down ADC and Programmable Filter: PMADL = PMADR = PMPFIL bits = "1" → "0"
(13) ALC Disable: ALC1 bit = "1" → "0"

■ Digital Microphone Input (Stereo)

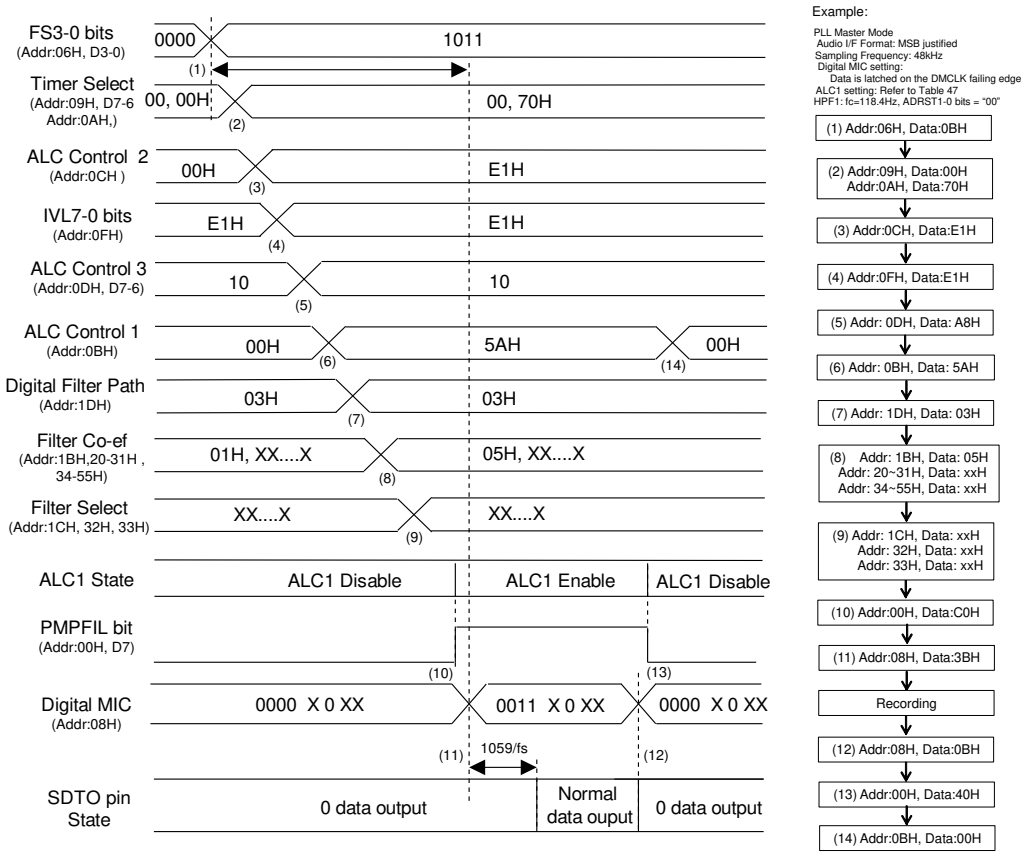


Figure 88. Digital Microphone Input Recording Sequence

<Sequence>

This sequence is an example of ALC1 setting at fs=48kHz. For changing the parameter of ALC, please refer to Table 49. At first, clocks should be supplied according to "Clock Set Up" sequence.

(1) Set up a sampling frequency (FS3-0 bits). When the AK4958 is PLL mode, Digital Microphone of (11) and Programmable Filter of (10) must be powered-up in consideration of PLL lock time after a sampling frequency is changed.
(2) Set up ALC1 Timer and ADRST1-0 bits (Addr = 09H, 0AH)
(3) Set up IREF value for ALC1 (Addtr = 0CH)
(4) Set up IVOL value at ALC1 operation start (Addr = 0FH)
(5) Set up RGAIN1-0 bits (Addr =0DH)
(6) Set up LMTH2-0 and ALC1 bits (Addr = 0BH)
(7) Set up Programmable Filter Path: PFSDO bit = ADCPF bit = "1" (Addr = 1DH)
(8) Set up Coefficient of Programmable Filter (Addr:1EH ~ 25H, 32H ~ 4FH)
(9) Set up Programmable Filter ON/OFF
(10) Power Up Programmable Filter: PMPFIL bit = "0" → "1"
(11) Set Up & Power Up Digital Microphone: PMDMR = PMDML bits = "0" → "1"
The initialization cycle time of ADC is 1059/fs=22ms@ fs=48kHz, ADRST1-0 bit = "00". ADC outputs "0" data during initialization cycle. After the ALC1 bit is set to "1", the ALC1 operation starts from IVOL value of (4).
(12) Power Down Digital Microphone: PMDMR =PMDML bits = "1" → "0"
(13) Power Down Programmable Filter: PMPFIL bit = "1" → "0"
(14) ALC1 Disable: ALC1 bit = "1" → "0"

■ Speaker-Amp Output

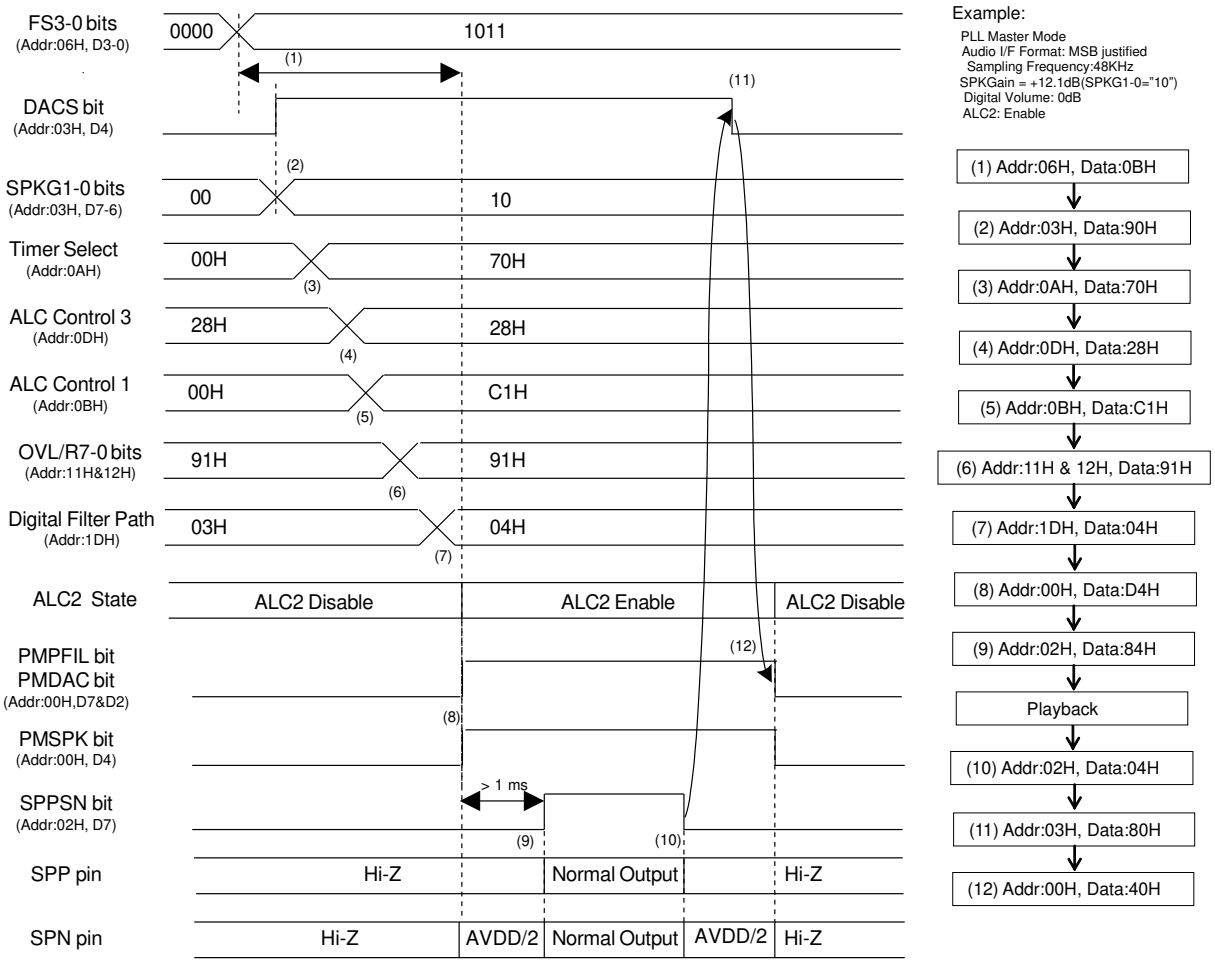


Figure 89. Speaker-Amp Output Sequence

<Sequence>

At first, clocks must be supplied according to "Clock Set Up" sequence.

(1) Set up a sampling frequency (FS3-0 bits). When the AK4957 is in PLL mode, DAC and Speaker-Amp of (9) must be powered-up in consideration of PLL lock time after a sampling frequency is changed.
(2) Set up the path of DAC → SPK-Amp: DACS bit = "0" → "1",
SPK-Amp gain setting: SPKG1-0 bits = "00" → "01"
(3) Set up Timer Select for ALC2 (Addr = 0AH)
(4) Set up OREF value of ALC2 and RGAIN1-0 bits (Addr = 0DH)
(5) Set up LMTH2-0 and ALC2 bits (Addr = 0BH)
(6) Set up the output digital volume. (Addr = 11H, 12H)
Set up OVOL value at ALC2 operation start. When OVOLC bit is "1" (default), OVL7-0 bits (Address: 11H) set the volume of both channels. When ALC2 bit is "0", it could be digital volume control.
(7) Set up Programmable Filter Path (PFDAC, ADCPF, PFSDO bits) (Addr = 1DH)
(8) Power up DAC, Programmable Filter and Speaker Amp: PMDAC = PMPFIL = PMSPK bits = "0" → "1"
(9) Exit the power-save mode of Speaker-Amp: SPPSN bit = "0" → "1"
(10) Enter Speaker-Amp Power Save Mode: SPPSN bit = "1" → "0"
(11) Disable the path of DAC → SPK-Amp: DACS bit = "1" → "0"
(12) Power down DAC, Programmable Filter and speaker: PMDAC = PMPFIL = PMSPK bits = "1" → "0"

■ Beep Signal Output from Speaker-Amp

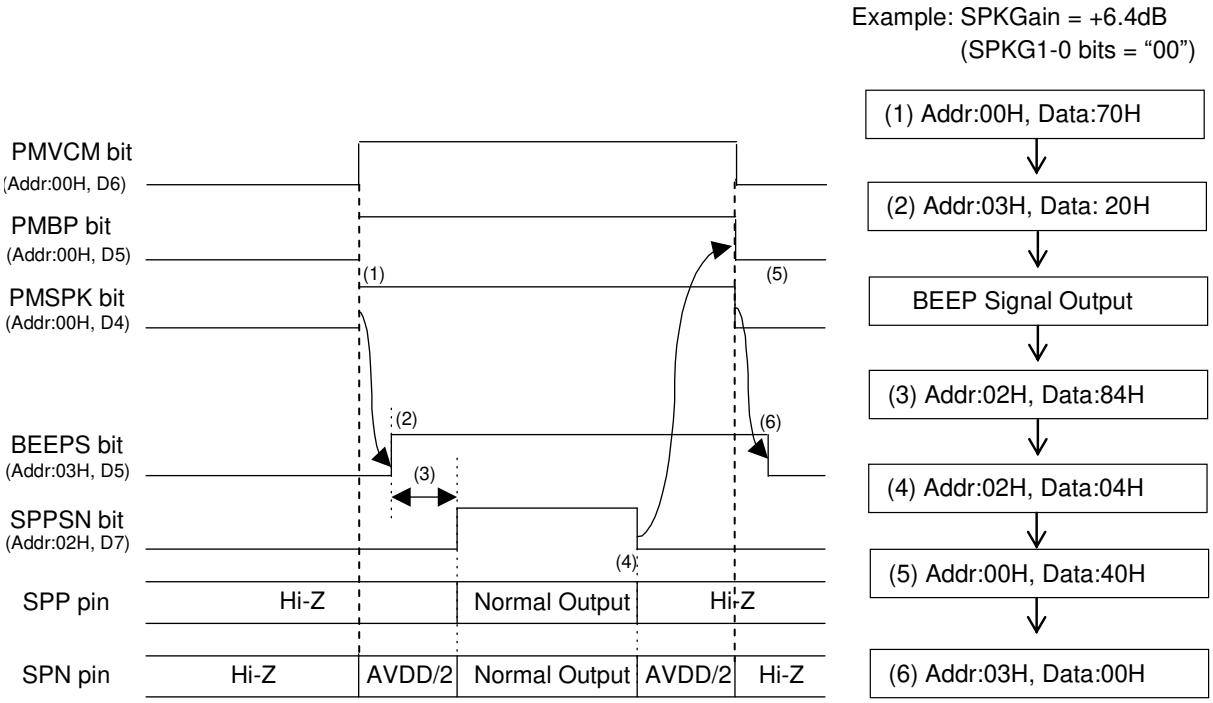


Figure 90. "BEEP-Amp → Speaker-Amp" Output Sequence

<Sequence>
Clock input is not necessary when the AK4958 is operating only on the path of "BEEP-Amp" → "SPK-Amp".

(1) Power up VCOM, MIN-Amp and Speaker: PMVCM = PMBP = PMSPK bits = "0" → "1"
(2) Set up the path of BEEP → SPK-Amp: BEEPS bit = "0" → "1"
(3) Exit the power save mode of Speaker-Amp: SPPSN bit = "0" → "1"
Period (3) should be set according to the time constant of a capacitor and a resistor that are connected to the BEEP pin. Pop noise may occur if the SPK-Amp output is enabled before the BEEP-Amp input is stabilized. The BEEP Amp is powered up after VCOM voltage rise. The maximum rise-up time of VCOM is 2msec.
e.g. R=86kΩ(max), C=0.1μF: Recommended Wait Time (max.): 2msec + 5τ = 45ms or more
(4) Enter Speaker-Amp Power-save mode: SPPSN bit = "1" → "0"
(5) Power Down BEEP-Amp and Speaker: PMBP = PMSPK bits = "1" → "0"
(6) Disable the path of BEEP → SPK-Amp: BEEPS bit = "1" → "0"

■ Stereo Line Output

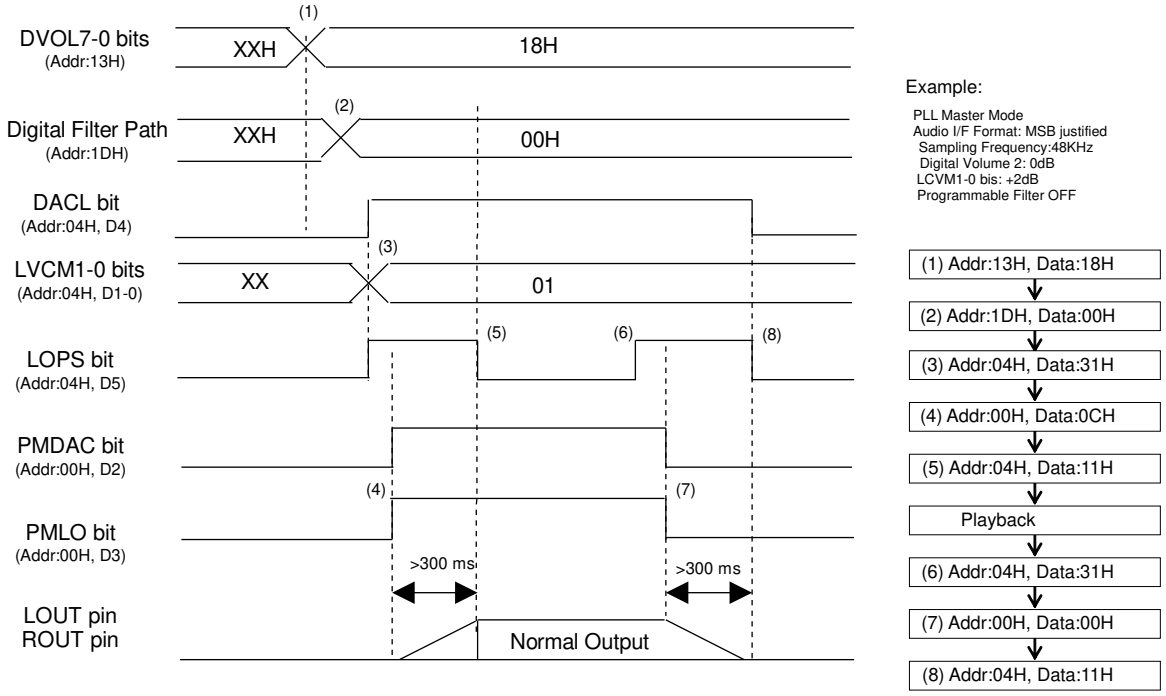


Figure 91. Stereo Lineout Sequence

<Sequence>

At first, clocks should be supplied according to "Clock Set Up" sequence.

(1) Set up output digital volume 2. (Addr = 13H)
(2) Set up Programmable Filter Path (PFDAC, ADCPF, PFSDO bits). (Addr = 1DH)
(3) Set up the path of "DAC → Stereo Line-Amp": DACL bit = "0" → "1" (Addr = 04H)
Stereo Line Output Amplifier Setting: LVCM1-0 bits = "xx" → "01"
Set the stereo line amplifier to power save mode: LOPS bit = "0" → "1"
(4) Power up Stereo Line-Amp: PMDAC= PMLO bits = "0" → "1" (Addr = 00H)
LOUT and ROUT pins rise up to VCOM voltage after PMLO bit is changed to "1". Rise time to 99% VCOM voltage is 300ms (max.) when C = 1μF and R_L=10kΩ.
(5) Exit power-save mode of Stereo Line-Amp: LOPS bit = "1" → "0" (Addr = 04H)
LOPS bit should be set to "0" after LOUT and ROUT pins rise up. Stereo Line-Amp goes to normal operation by setting LOPS bit to "0".
(6) Enter power save mode of Stereo Line-Amp: LOPS bit = "0" → "1" (Addr = 04H)
(7) Power down DAC and Stereo Line-Amp: PMDAC = PMLO bits = "1" → "0" (Addr = 00H)
LOUT and ROUT pins fall down to 1% of the VCOM voltage. Fall time is 300ms (max.) at C = 1μF and R_L=10kΩ.
(8) Disable the path of "DAC → Stereo Line-Amp": DACL bit = "1" → "0" (Addr = 04H)
Exit power-save mode of the Stereo Line-Amp: LOPS bit = "1" → "0"
LOPS bit should be set to "0" after LOUT and ROUT pins fall down.

■ Video Input/Output

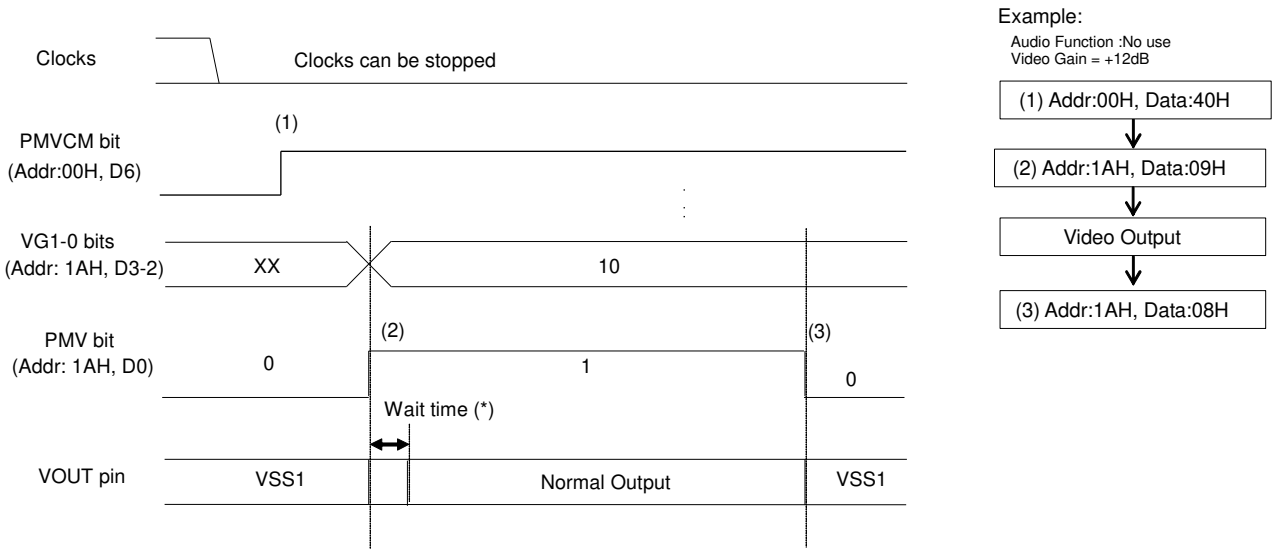


Figure 92. Video Output Sequence

<Sequence>

When only the video block is in operation, the clocks are not needed.

(1) Power up VCOM: PMVCM bit = "0" → "1"

(2) Set up Video Gain (VG1-0 bits)

Video Amp Power Up: PMV bit = "0" → "1"

(*) Wait time is the time until the video clamp circuit output is stabled. It depends on the value of a DC-cut capacitor for the VIN pin. The wait time is 50ms (max.) when the DC-cut capacitor of the VIN pin input is 0.047μF. (It is a rising time without a DC offset)

(3) Video Amp Power Down: PMV bit = "1" → "0"

The VOUT pin output is stopped and becomes 0V.

■ Stop of Clock

1. PLL Master Mode

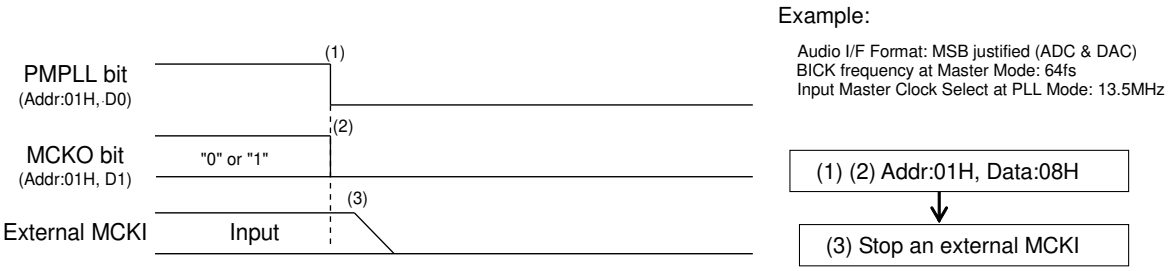


Figure 93. Clock Stopping Sequence (1)

<Sequence>
(1) Power down PLL: PMPLL bit = "1" → "0"
(2) Stop MCKO clock: MCKO bit = "1" → "0"
(3) Stop an external master clock.

2. PLL Slave Mode (BICK pin)

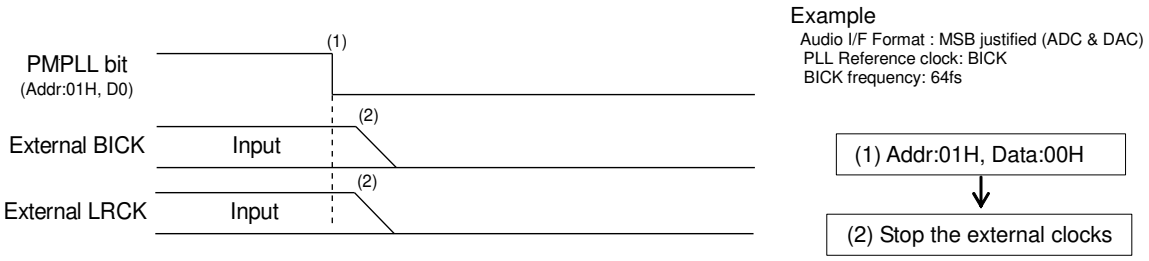


Figure 94. Clock Stopping Sequence (2)

<Sequence>
(1) Power down PLL: PMPLL bit = "1" → "0"
(2) Stop an external master clock.

3. PLL Slave Mode (MCKI pin)

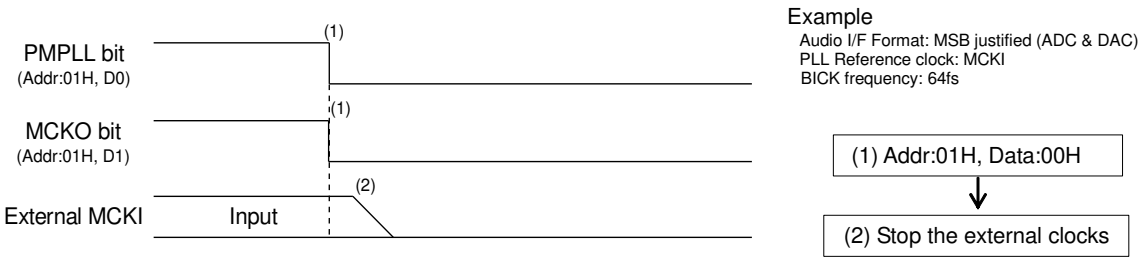


Figure 95. Clock Stopping Sequence (3)

<Sequence>
(1) Power down PLL: PMPLL bit = "1" → "0"
Stop MCKO output: MCKO bit = "1" → "0"
(2) Stop the external master clock

4. EXT Slave Mode

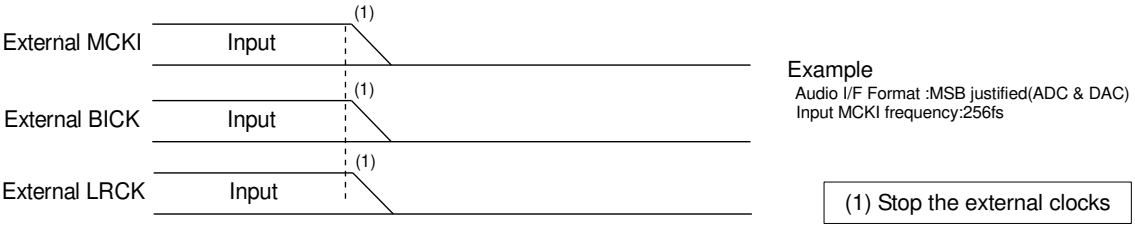


Figure 96. Clock Stopping Sequence (4)

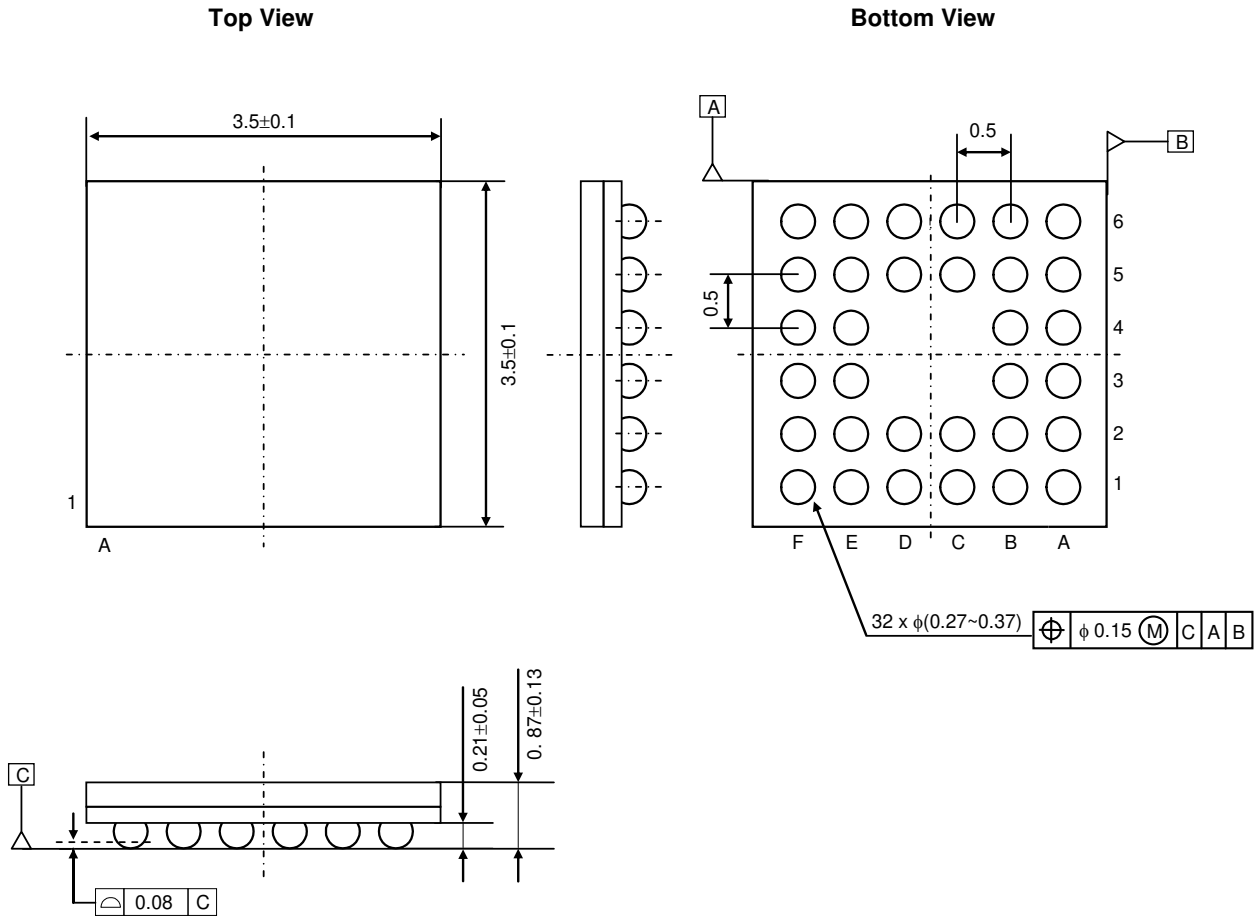
<Sequence>
(1) Stop the external MCKI, BICK and LRCK clocks.

■ Power Down

Power supply current cannot be shut down by stopping clocks and setting PMVCM bit = "0". Power supply current can be shut down (typ. 1μA) by stopping clocks and setting the PDN pin = "L". When the PDN pin = "L", all registers are initialized.

PACKAGE (AK4958EG)

32pin BGA (Unit: mm)

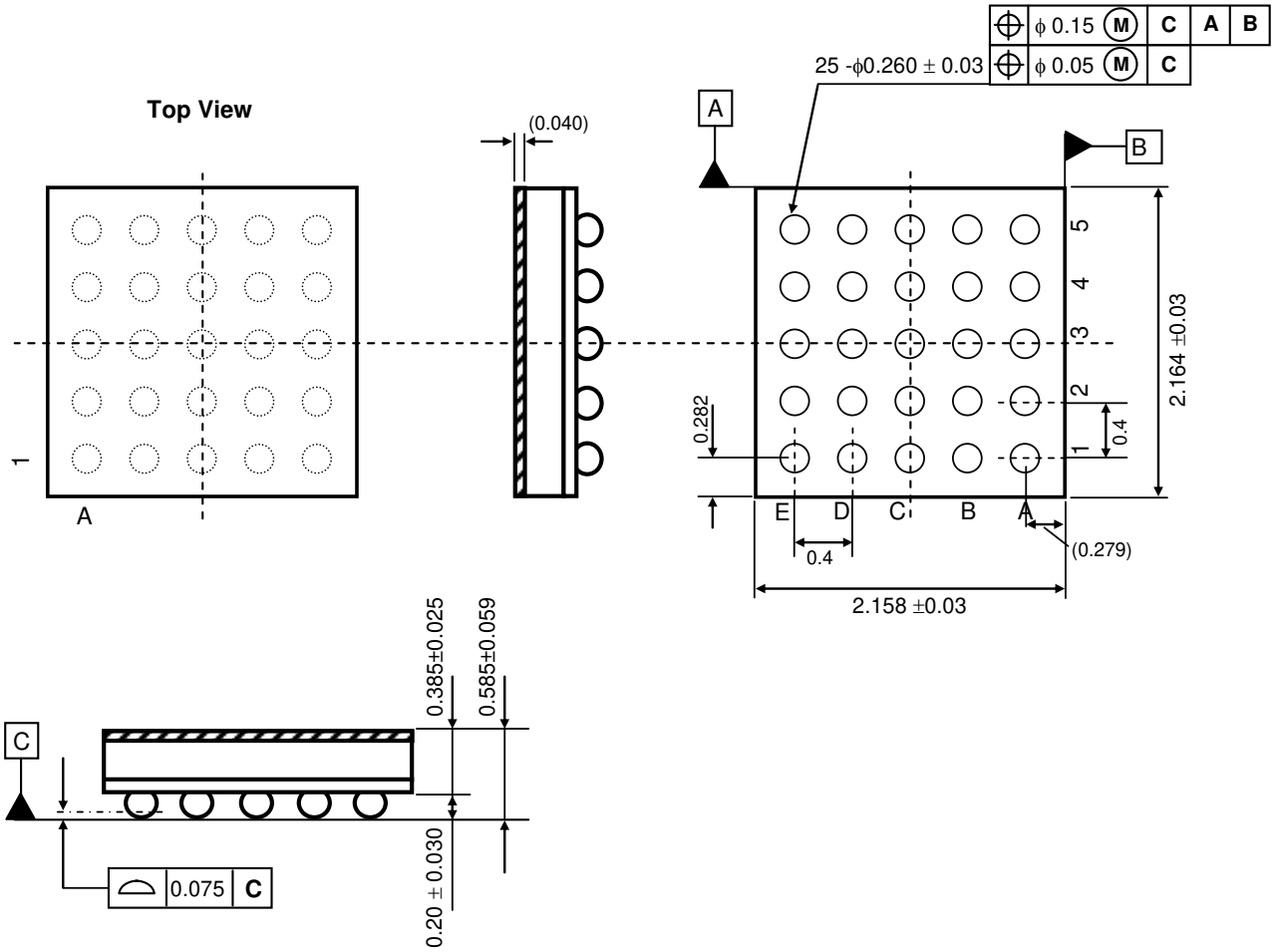


■ Material & Lead finish

Package material: Epoxy Resin, Halogen (Br and Cl) free
Solder ball material: SnAgCuNi (LF35)

PACKAGE (AK4958ECB)

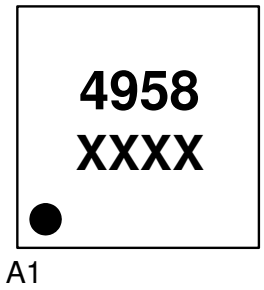
25pin CSP (Unit: mm)



■ Material & Lead finish

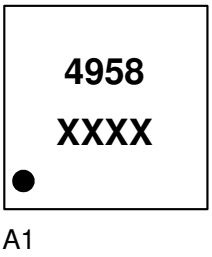
Package material: Polyimide Resin, Halogen (Br and Cl) free
Solder ball material: SnAgCu

MARKING (AK4958EG)



XXXX: Date code (4 digit)
Pin #A1 indication

MARKING (AK4958ECB)



XXXX: Date code (4 digit)
Pin #A1 indication

REVISION HISTORY

Date (Y/M/D)	Revision	Reason	Page/Line	Contents
13/09/13	00	First Edition		
13/10/25	01	Error Correction	139	Package dimension was corrected. (AK4958EG) Stand off: 0.16±0.5 → 0.21±0.05 Total thickness: Max 1 → 0.87±0.13
14/08/06	02	Spec. Change	2, 3, 17, 90	The setting of the video amplifier gain was added. (AK4958EG) VG1-0 bits = "00": +6dB