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NTE74HC273
Integrated Circuit
TTL – High Speed CMOS,
Octal D–Type Flip–Flop with Reset

Description:

The NTE74HC273 is a high speed octal D–type flip–flop with a direct clear input in a 20–Lead DIP type package manufactured with silicon–gate CMOS technology that posses the low power consumption of standard CMOS integrated circuits.

Information at the D inputs is transferred to the Q outputs on the positive–going edge of the clock pulse. All eight flip–flops are controlled by common clock (CP) and a common reset ($\overline{MR}$). Resetting is accomplished by a low voltage level independent of the clock. All eight Q outputs are reset to a logic 0.

Features:

- Wide Power Supply Range: 2V to 6V
- High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V
- Common Clock and Asynchronous Master Reset
- Positive Edge Triggering
- Buffered Inputs
- Fanout (Over Temperature Range):
  - Standard Outputs . . . 10 LS–TTL Loads
  - Bus Driver Outputs . . 15 LS–TTL Loads
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LS–TTL Logic ICs

Absolute Maximum Ratings: (Note 1, Note 2)

Supply Voltage, V_{CC} . . . . . –0.5 to +7.0V
Clamp Diode Current, I_{IK}, I_{OK} . . . . . ±20mA
DC Drain Current (Per Output), I_{OUT} . . . . . ±25mA
DC Output Source or Sink Current (Per Output), I_{OUT} . . . . . ±25mA
DC V_{CC} or GND Current (Per Pin), I_{CC} . . . . . ±50mA
Maximum Junction, T_J . . . . . +150°C
Storage Temperature Range, T_{stg} . . . . . –65°C to +150°C
Typical Thermal Resistance, Junction–to–Ambient, R_{thJA} . . . . . 69°C/W
Lead Temperature (During Soldering, 10sec), T_L . . . . . +300°C

Note 1. Absolute Maximum Ratings are those values beyond which damage to the device may occur.
Note 2. Unless otherwise specified, all voltages are referenced to GND.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	2.0	–	6.0	V
DC Input or Output Voltage	V_{IN}, V_{OUT}	0	–	V_{CC}	V
Operating Temperature Range	T_A	−40	–	+85	°C
Input Rise or Fall Times	t_r, t_f				
V_{CC} = 2.0V		–	–	1000	ns
V_{CC} = 4.5V		–	–	500	ns
V_{CC} = 6.0V		–	–	400	ns

DC Electrical Characteristics:

Parameter	Symbol	Test Conditions		V_{CC}	T_A = +25°C Typ	T_A = −40° to +85°C Guaranteed Limits		Unit
Minimum HIGH Level Input Voltage	V_{IH}			2.0	–	1.5	1.5	V
				4.5	–	3.15	3.15	V
				6.0	–	4.2	4.2	V
Maximum LOW Level Input Voltage	V_{IL}			2.0	–	0.5	0.5	V
				4.5	–	1.35	1.35	V
				6.0	–	1.8	1.8	V
Minimum HIGH Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OUT} = −20μA	–	V_{CC}	V_{CC} −0.1	V_{CC} −0.1	V
			I_{OUT} = −6mA	4.5	–	3.98	3.84	V
			I_{OUT} = −7.8mA	6.0	–	5.48	5.34	V
Minimum LOW Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OUT} = 20μA	–	–	0.1	0.1	V
			I_{OUT} = 6mA	4.5	0.2	0.26	0.33	V
			I_{OUT} = 7.8mA	6.0	0.2	0.26	0.33	V
Maximum Input Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	–	±0.1	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND, I_{OUT} = 0μA		6.0	–	8.0	80	μA

Prerequisite for Switching Specifications:

Parameter	Symbol	Test Conditions	V_{CC}	T_A = +25°C Typ	T_A = −40° to +85°C Guaranteed Limits		Unit
Maximum Clock Frequency	f_{MAX}		2.0	–	6	5	MHz
			4.5	–	30	25	MHz
			6.0	–	35	29	MHz
$\overline{MR}$ Pulse Width	t_W		2.0	–	60	75	ns
			4.5	–	12	15	ns
			6.0	–	10	13	ns
Clock Pulse Width	t_W		2.0	–	80	100	ns
			4.5	–	16	20	ns
			6.0	–	14	17	ns
Setup Time (Date to Clock)	t_{SU}		2.0	–	60	75	ns
			4.5	–	12	15	ns
			6.0	–	10	13	ns
Hold Time (Date to Clock)	t_H		All	–	3	3	ns
Removal Time ($\overline{MR}$ to Clock)	t_{REM}		2.0	–	50	65	ns
			4.5	–	10	13	ns
			6.0	–	9	11	ns

Switching Specifications: ($t_r = t_f$ = 6ns unless otherwise specified)

Parameter	Symbol	Test Conditions	V_{CC}	T_A = +25°C	T_A = −40° to +85°C		Unit
				Typ	Guaranteed Limits		
Propagation Delay Time (Clock to Output)	t_{PLH}, t_{PHL}	C_L = 50pF	2.0	–	150	190	ns
			4.5	–	30	38	ns
		C_L = 15pF	5.0	12	–	–	ns
		C_L = 50pF	6.0	–	26	30	ns
Propagation Delay Time ($\overline{MR}$ to Output)	t_{PHL}	C_L = 50pF	2.0	–	150	190	ns
			4.5	–	30	38	ns
			6.0	–	26	30	ns
Output Transition Time	t_{TLH}, t_{THL}	C_L = 50pF	2.0	–	75	95	ns
			4.5	–	15	19	ns
			6.0	–	13	16	ns
Maximum Input Capacitance	C_{IN}		–	–	10	10	pF
Maximum Clock Frequency	f_{MAX}	C_L = 15pF	5.0	60	–	–	MHz
Power Dissipation Capacitance	C_{PD}	Note 3	5.0	25	–	–	pF

Note 3. C_{PD} is used to determine the dynamic power consumption, per channel.
$P_D = C_{PD} V_{CC}^2 f_i \Sigma (C_L V_{CC}^2 + f_O)$ where f_i = Input Frequency, f_O = Output Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

Truth Table:

Inputs			Output
Reset (MR)	**Clock CP**	**Data D_n**	**Q**
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

H = HIGH Level
L = LOW Level
X = Don't Care
↑ = Transition from LOW to HIGH Level
Q_{io} = The level before the indicated steady state input conditions were established.

Pin Connection Diagram