ISL28915

Nano Power, Push/Pull Output Comparator

FN8343
Rev.0.00
Jul 16, 2012

The ISL28915 is a nano power comparator optimized for low-power applications. This device is designed for single-supply operation from 1.8V to 5.5V and typically consumes 500nA of supply current. These devices also feature a push/pull output stage with rail-to-rail input and output swing (RRIO), allowing for maximum battery usage.

The combination of small footprint, low power, single supply, and rail-to-rail operation makes them ideally suited for all battery operated devices.

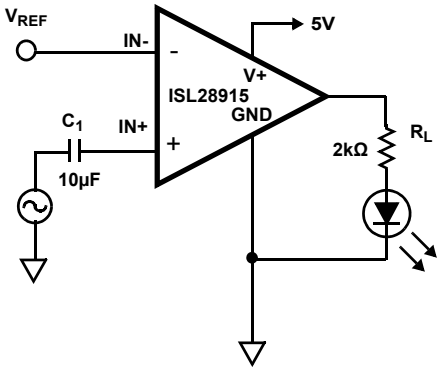
The ISL28915 features an enable pin and is offered in the 6 Ld SOT-23 package. The device operates over the -40°C to +125°C temperature range.

Features

- Low Active Current . . . . . 600nA Max
- Low Disable Current. . . . . 20nA Max
- Propagation Delay 150µs
- Rail-to-Rail Input/Output Voltage Range (RRIO)
- Wide Supply Range . . . . . 1.8V to 5.5V
- Operating Temperature Range. . . . . -40°C to +125°C

Applications

- Battery-Powered/Portable Systems
- Telemetry and Remote Systems
- Alarm and Monitoring Systems
- Oscillator Circuits
- Window Comparators
- Threshold Detectors/Discriminators



AUDIO SIGNAL PEAK DETECTOR

FIGURE 1. TYPICAL APPLICATION CIRCUIT

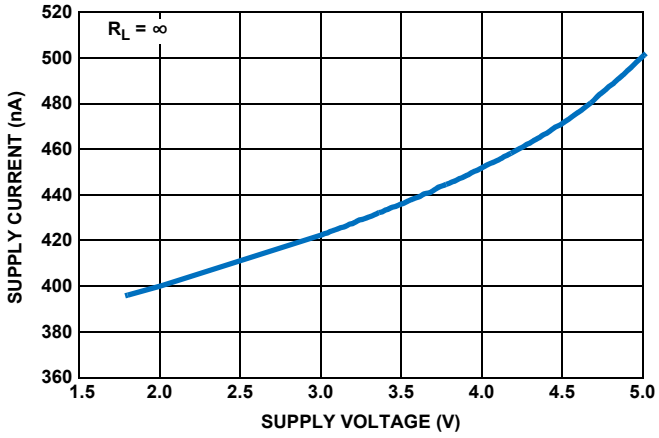


FIGURE 2. SUPPLY CURRENT vs SUPPLY VOLTAGE

Ordering Information

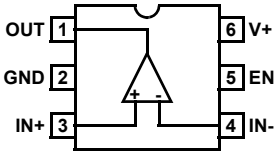
PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP RANGE (°C)	PACKAGE TAPE & REEL (Pb-Free)	PKG. DWG. #
ISL28915FH6Z-T7	BENA	-40°C to +125°C	SOT23-6	P6.064A

NOTES:

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL28915. For more information on MSL please see techbrief TB363.

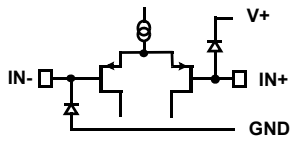
Pin Configuration

ISL28915FH6Z
(6 LD SOT-23)
TOP VIEW

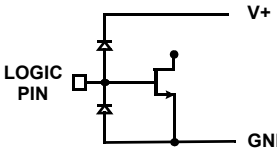


Pin Descriptions

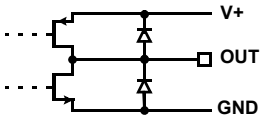
ISL28915FH6Z (6 LD SOT-23)	PIN NAME	EQUIVALENT CIRCUIT	DESCRIPTION
1	OUT	Circuit 3	Comparator output
2	GND	Circuit 4	GROUND terminal
3	IN+	Circuit 1	Comparator non-inverting input
4	IN-	Circuit 1	Comparator inverting input
5	EN	Circuit 2	Comparator enable pin; Logic “1” selects the enabled state: Logic “0” selects the disabled state
6	V+	Circuit 4	Positive power supply



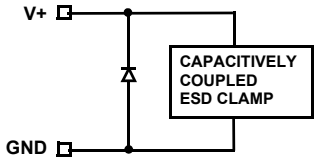
CIRCUIT 1



CIRCUIT 2



CIRCUIT 3



CIRCUIT 4

Absolute Maximum Ratings

Maximum Supply Voltage 5.75V
Supply Turn-On Voltage Slew Rate 1V/µs
Maximum Differential Input Current 5mA
Maximum Differential Input Voltage . . . . . GND - 0.5V to V+ + 0.5V
Min/Max Input Voltage . . . . . GND - 0.5V to V+ + 0.5V
Output Short-Circuit Duration . . . . . Indefinite
ESD Tolerance
Human Body Model (Tested per JESD22-A114F) 3kV
Machine Model (Tested per JESD22-A115-C) 150V
Charged Device Model (Tested per JESD22-C110D) 1kV
Latch-up (Tested per JESD-78B; Class 2, Level A) . . . . . at +125°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
6 Ld SOT-23 Package (Notes 4, 5)	239	108

Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

Ambient Temperature Range (T_A) . . . . . -40°C to +125°C
Operating Junction Temperature . . . . . +125°C
Supply Voltage . . . . . 1.8V to 5.5V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
5. For θ_{JC}, the "case temp" location is taken at the package top center.

Electrical Specifications

V+ = 5V, GND = 0V, V_{CM} = 2.5V, T_A = +25°C, unless otherwise specified. **Boldface limits apply over -40°C to +125°C.**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
V_{OS}	Input Offset Voltage		-2	-0.2	2	mV
			-2.5		**2.5**	mV
I_{OS}	Input Offset Current		-25	-3	25	pA
			-67		**67**	pA
I_B	Input Bias Current		-31	1.2	31	pA
			-100		**100**	pA
CMIR	Common Mode Input Range	Established by CMRR test	**0**		**5**	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = 0.5V to 3.5V	72	98		dB
			70			dB
		V_{CM} = 0V to 5V	60			dB
PSRR	Power Supply Rejection Ratio	V+ = 1.8V to 5.5V	77	100		dB
			70			dB
V_{OUT}	Maximum Output Voltage Swing R_L terminated to V+/2	Output low, R_L = 10kΩ		35	70	mV
		Output high, R_L = 10kΩ	4.930	4.990		V
$I_{S,ON}$	Supply Current, Enabled	V_{EN} = V+ - 0.3V		500	600	nA
					900	nA
$I_{S,OFF}$	Supply Current, Disabled	V_{EN} = GND + 0.3V		0.25	20	nA
					50	nA
V_{SUPPLY}	Supply Voltage Range		**1.8**		**5.5**	V
C_{IN}	Input Capacitance			6		pF
ENABLE INPUT						
V_{ENH}	Enable Pin High Level		V+ - 0.3			V
V_{ENL}	Enable Pin Low Level				GND + 0.3	V
$I_{EN-H,L}$	Enable Pin Input Current	V_{EN} = 0V, 5V	-80	2.2	80	nA
			-200		**200**	nA

Electrical Specifications V+ = 5V, GND = 0V, V_{CM} = 2.5V, T_A = +25°C, unless otherwise specified. **Boldface limits apply over -40°C to +125°C. (Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
TIMING						
t_{PD}±	Propagation Delay Low to High and High to Low	C_L = 10pF, 20mV Overdrive		150	260	µs
t_R/t_F	Output Rise/Fall Time	C_L = 10pF		11	20	µs

NOTE:

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Typical Performance Curves

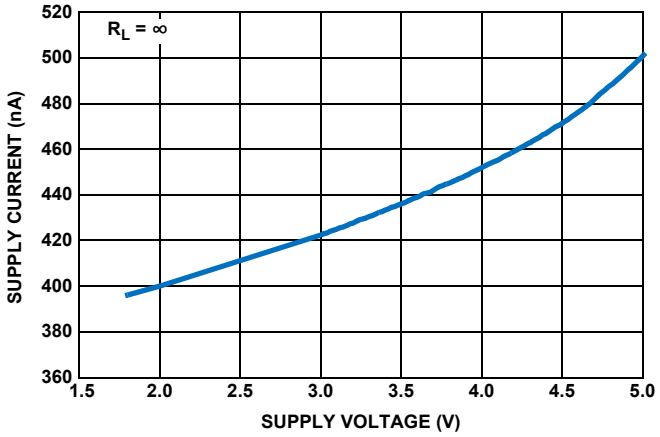


FIGURE 3. SUPPLY CURRENT vs SUPPLY VOLTAGE

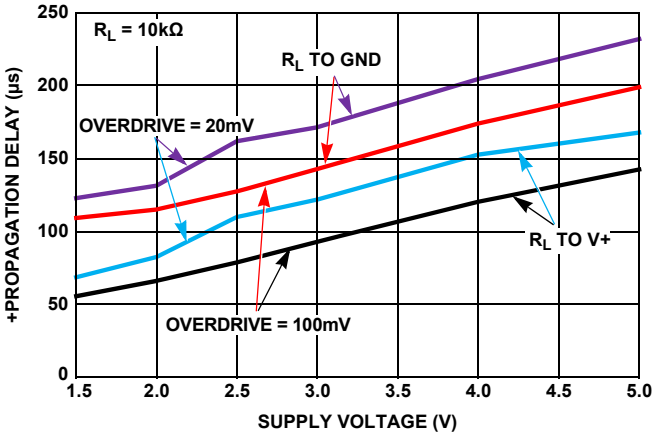


FIGURE 4. PROPAGATION DELAY vs SUPPLY VOLTAGE (RISING EDGE)

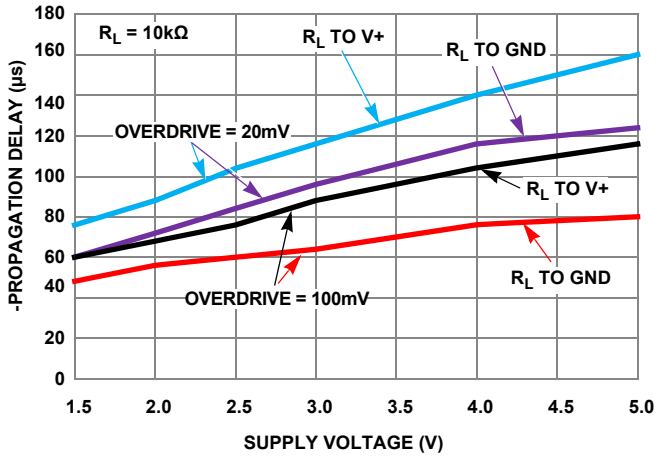


FIGURE 5. PROPAGATION DELAY vs SUPPLY VOLTAGE (FALLING EDGE)

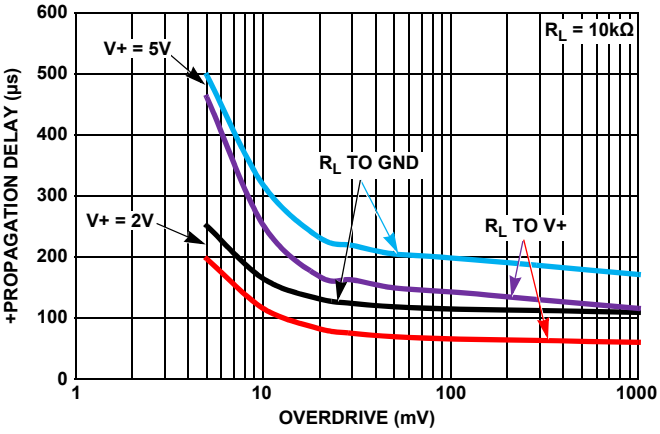


FIGURE 6. PROPAGATION DELAY vs OVERDRIVE (RISING EDGE)

Typical Performance Curves (Continued)

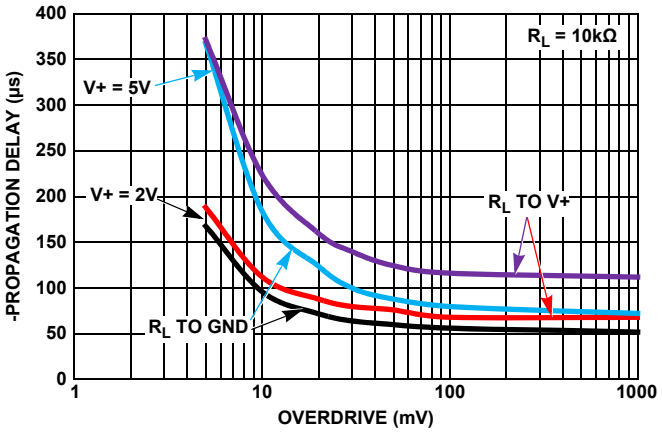


FIGURE 7. PROPAGATION DELAY vs OVERDRIVE (FALLING EDGE)

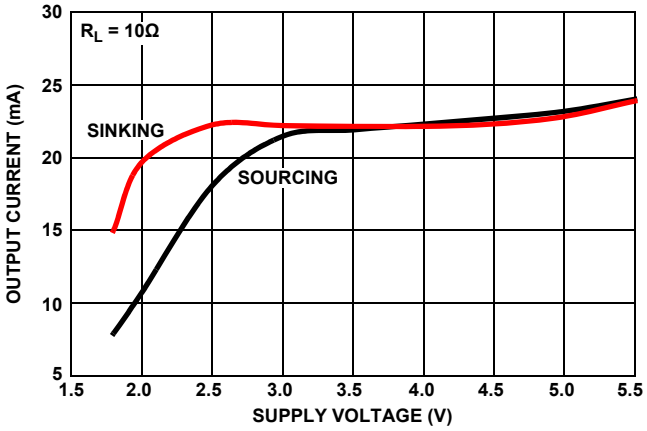


FIGURE 8. SHORT CIRCUIT CURRENT vs SUPPLY VOLTAGE

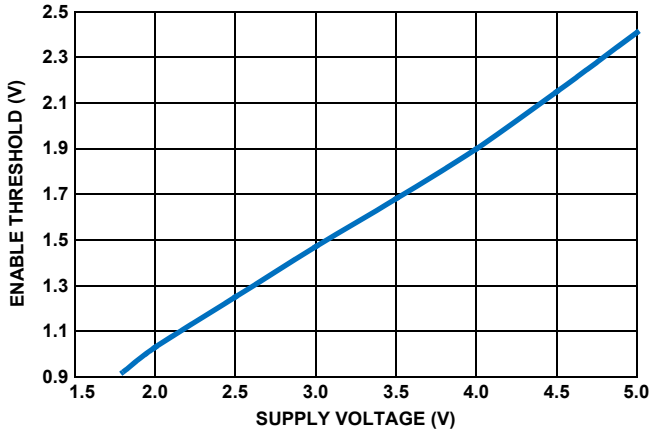


FIGURE 9. ENABLE THRESHOLD VOLTAGE vs SUPPLY VOLTAGE

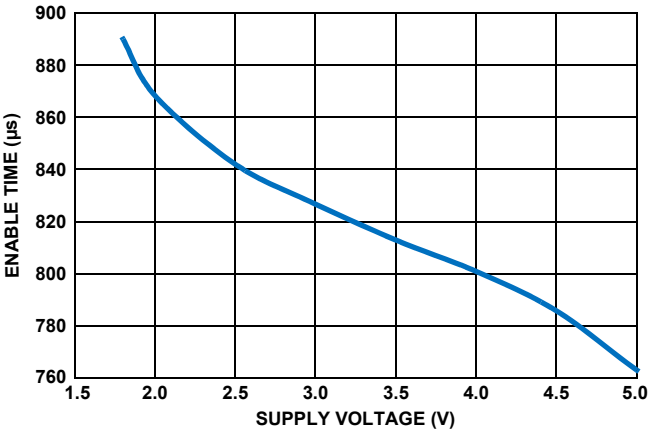


FIGURE 10. ENABLE TO OUTPUT DELAY TIME vs SUPPLY VOLTAGE

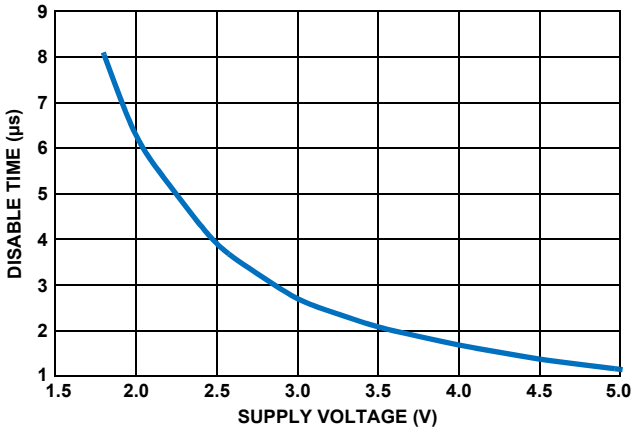


FIGURE 11. ENABLE LOW TO OUTPUT TURN-OFF TIME vs SUPPLY VOLTAGE

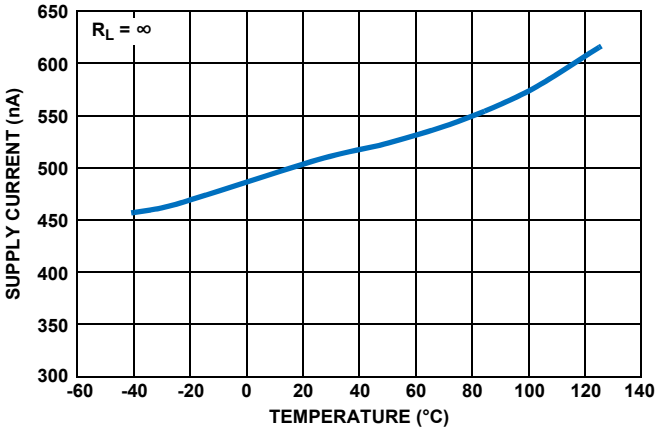


FIGURE 12. SUPPLY CURRENT vs TEMPERATURE, V+, GND = ±2.5V

Typical Performance Curves (Continued)

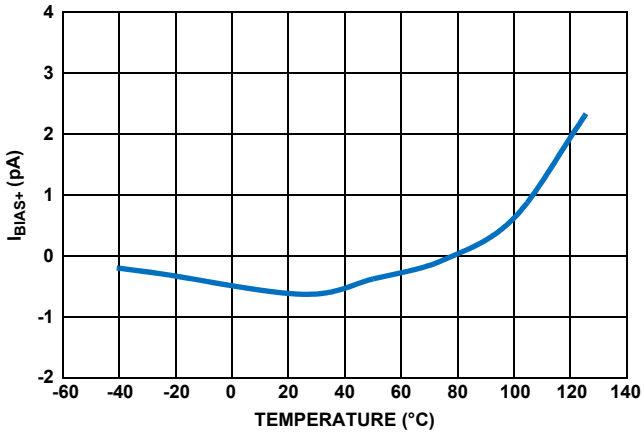


FIGURE 13. I_{BIAS+} vs TEMPERATURE, V+, GND = ±2.5V

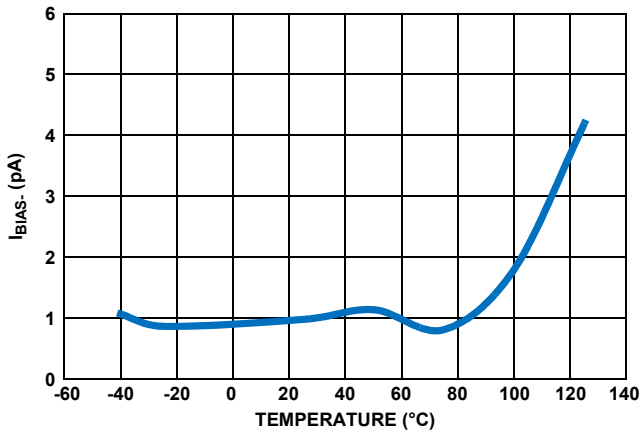


FIGURE 14. I_{BIAS-} vs TEMPERATURE, V+, GND = ±2.5V

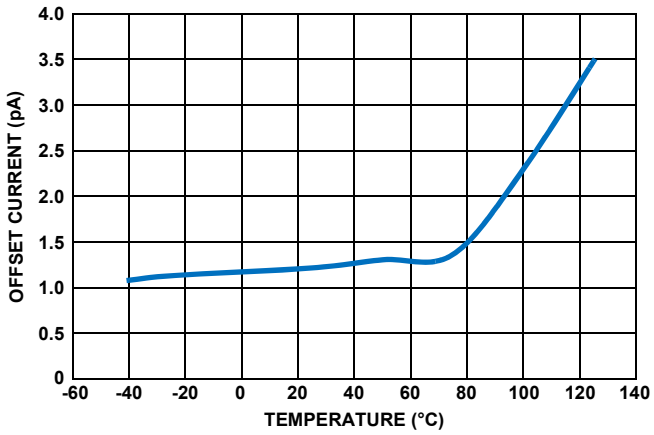


FIGURE 15. I_{OS} vs TEMPERATURE, V+, GND = ±2.5V

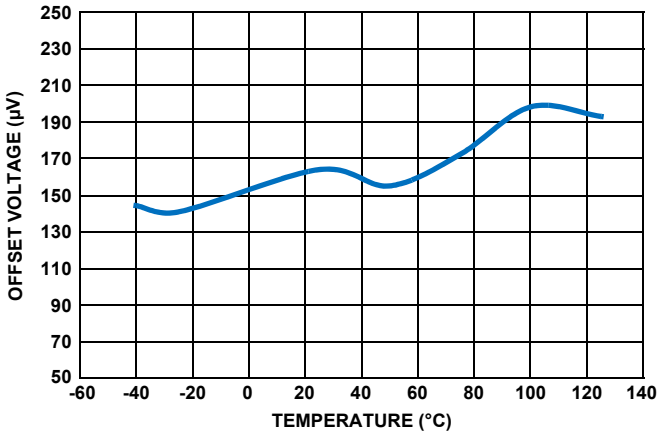


FIGURE 16. V_{OS} vs TEMPERATURE, V+, GND = ±2.5V, V_{CM} = 0V

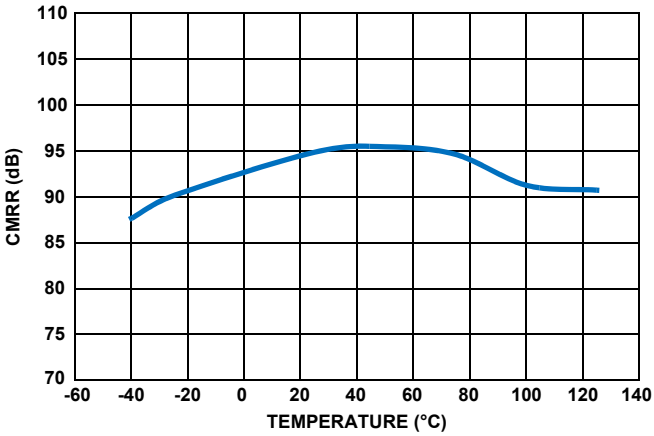


FIGURE 17. CMRR vs TEMPERATURE,
V_{CM} = 0.5V TO 3.5, V+, GND = ±2.5V

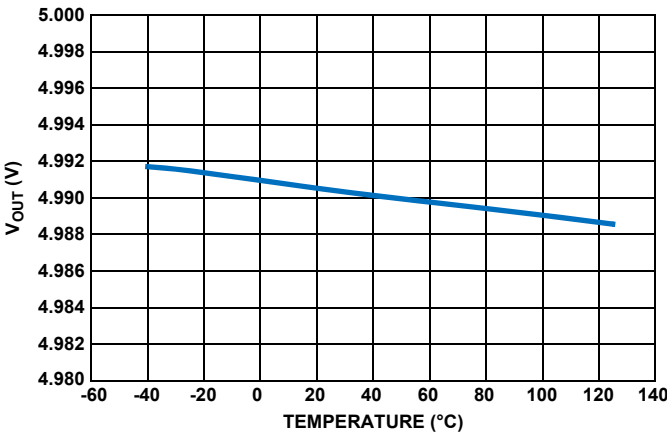


FIGURE 18. V_{OUT} HIGH vs TEMPERATURE,
V+, GND = ±2.5V, R_L = 10k

Typical Performance Curves (Continued)

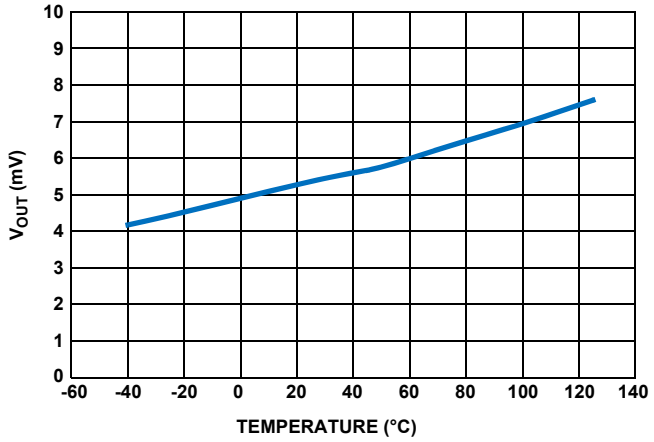


FIGURE 19. V_{OUT} LOW vs TEMPERATURE, V+, GND = ±2.5V, R_L = 10k

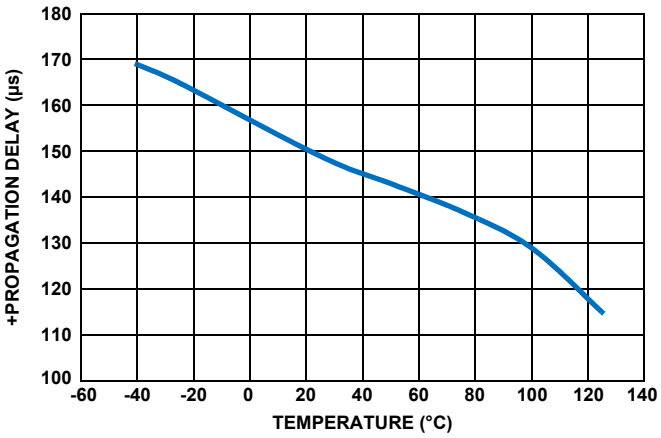


FIGURE 20. POSITIVE PROPAGATION DELAY vs TEMPERATURE 50% TO 50%, V+ = 5V

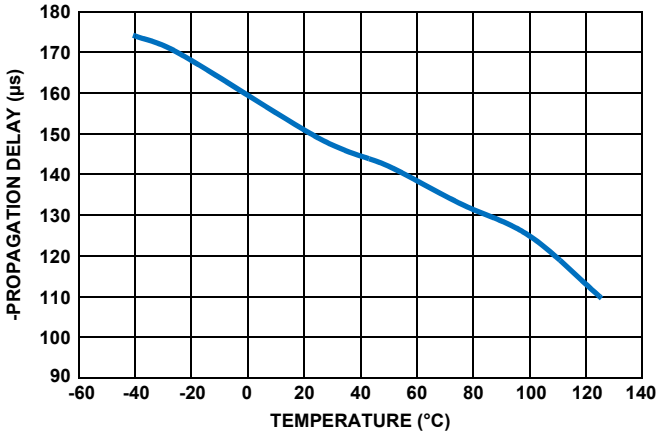


FIGURE 21. NEGATIVE PROPAGATION DELAY vs TEMPERATURE 50% TO 50%, V+ = 5V

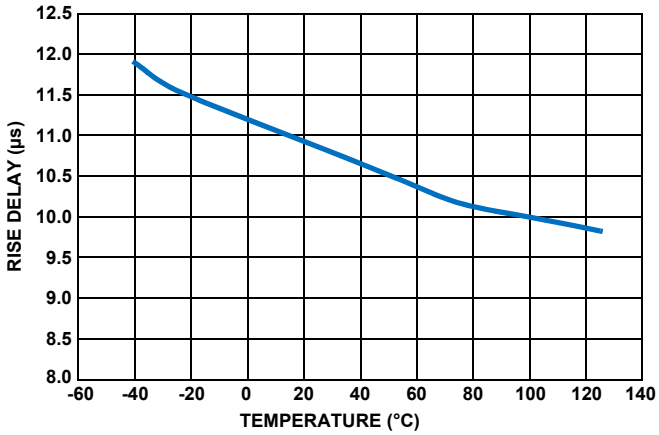


FIGURE 22. RISE TIME vs TEMPERATURE 20% TO 80%, V+ = 5V

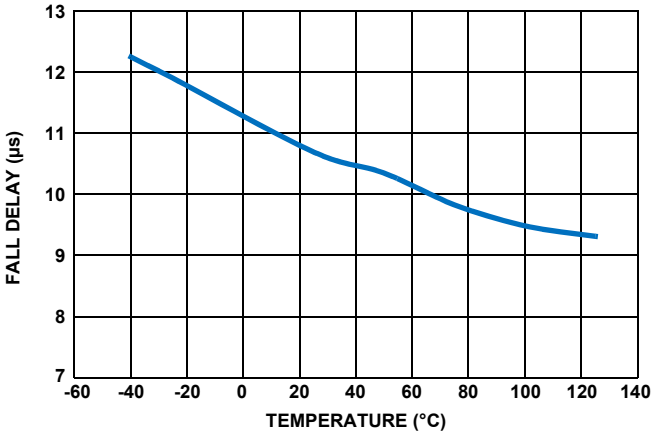


FIGURE 23. FALL TIME vs TEMPERATURE 20% TO 80%, V+ = 5V

Applications Information

Introduction

The ISL28915 is a CMOS rail-to-rail input and output (RRIO) nanopower comparator. This device is designed to operate from single supply (1.8V to 5.5V) and have an input common mode range that extends to the positive rail and to the negative supply rail for true rail-to-rail performance. The CMOS output can swing within tens of millivolts to the rails. Featuring worst case maximum supply current of only 900nA, this comparator is ideally suited for solar and battery powered applications.

Input Protection

All input terminals have internal ESD protection diodes to both positive and negative supply rails, limiting the input voltage to within one diode beyond the supply rails. The ISL28915 has a maximum input differential voltage that extends beyond the rails (V+ + 0.5V to GND - 0.5V).

Rail-to-Rail Output

A pair of complementary MOSFET devices are used to achieve the rail-to-rail output swing. The NMOS sinks current to swing the output in the negative direction. The PMOS sources current to swing the output in the positive direction. The ISL28915 with a 10kΩ load will typically swing to within 10mV of the positive supply rail and within 35mV of ground.

Break-Before-Make Operation of the Output

The output circuit has a break-before-make response. This means that the P-Channel turns off before the N-Channel turns on during a high to low transition of the output (reference Figure 24). Likewise, the N-Channel turns off before the P-Channel turns on during a low to high transition. This results in different propagation delay times depending upon where the output load resistor is tied to. If the load resistor is tied to ground (Figure 25A), then the propagation delay is controlled by the P-Channel. For a high to low transition, the propagation delay does not include the additional break-before-make time because the load resistor will pull the output low once the P-Channel has turned off.

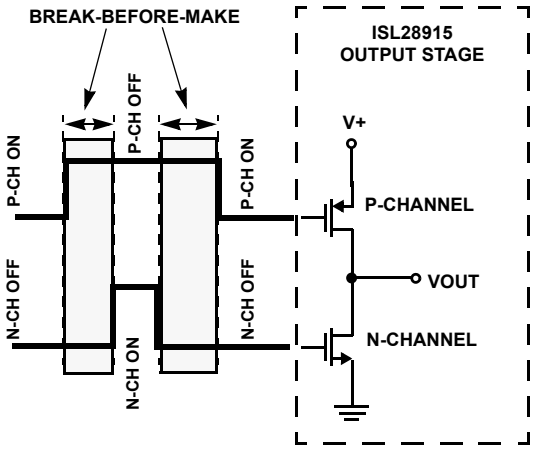


FIGURE 24. MAKE-BEFORE-BREAK ACTION OF THE OUTPUT STAGE

During the low to high transition, however, if the load resistor is tied to ground, then the additional break-before-make time is added to the propagation delay time because the output won't pull high until the P-Channel turns on.

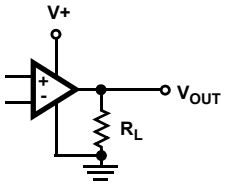


FIGURE 25A. R_L TO GND

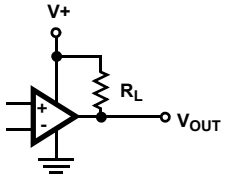


FIGURE 25B. R_L TO V+

FIGURE 25. CONNECTION OF R_L TO GND AND V+

If the load resistor is tied to V+ (Figure 25B), then the propagation delay is controlled by the N-Channel. For this condition, the additional delay time is added to the high to low transition because the output won't pull low until the N-Channel turns on. Figures 4 through 7 show the differences in propagation delay depending upon where the load is tied.

Propagation Delay

The input to output propagation delay has a dependency on power supply voltage, overdrive and whether the output is sourcing or sinking current. Figures 4 and 5 show a decreasing time propagation delay vs supply voltage for the ISL28915. The output break-before-make mechanism results in a difference in propagation delay, depending on whether the output stage NMOS and PMOS are sourcing or sinking current. This delay difference is shown in the figures as a function of where the load is terminated (V+ or GND) and also as a function of supply voltage. The dependence of propagation delay as a function of power supply voltage and input overdrive (from 5mV to 1V) is shown in Figures 6 and 7. Propagation delay is measured from the time the input signal reached 50% of its final value to the time the output reaches 50% of its final value. Rise and fall times are measured from the time the signal is at 20% of its final value to the time it reaches 80% of the final value.

Enable Feature

The ISL28915 in the 6 Ld SOT-23 package offers an EN pin that enables the device when pulled high. The enable threshold is referenced to the GND terminal and has a level proportional to the total supply voltage (reference Figure 9 for EN Threshold vs Supply Voltage). The enable circuit has a delay time that changes as a function of supply voltage. Figures 10 and 11 show the effect of supply voltage on the enable and disable times. The enable and disable delay is measured from the time the signal crosses the enable threshold to the time the output reaches 20% of its final value. For supply voltages less than 3V, it is recommended that the user account for the increased enable/disable delay time.

In the disabled state (output in a high impedance state), the supply current is reduced to a typical of only 0.25nA. By disabling the devices, multiple parts can be connected together as a MUX. In this configuration, the outputs are tied together in parallel and a channel can be selected by the EN pin. The EN pin should never be left floating. The EN pin should be connected directly to the V+ supply when not in use.

Proper Layout Maximizes Performance

To achieve the maximum performance of the high input impedance, care should be taken in the circuit board layout. The PC board surface must remain clean and free of moisture to avoid leakage currents between adjacent traces. Surface coating of the circuit board will reduce surface moisture and provide a humidity barrier, reducing parasitic resistance on the board. When input leakage current is a concern, the use of guard rings around the comparator inputs will further reduce leakage currents.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

DATE	REVISION	CHANGE
July 16, 2012	FN8343.0	Initial Release

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing, and high-end consumer markets.

For the most updated datasheet, application notes, related documentation, and related parts, see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support.

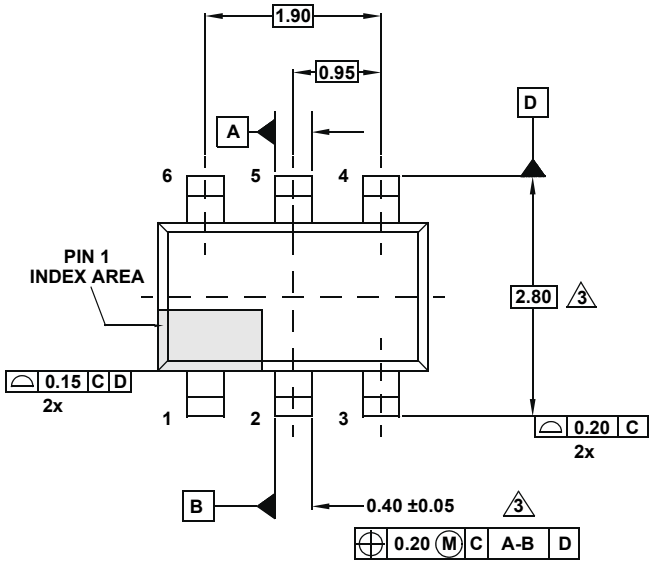
Package Outline Drawing

For the most recent package outline drawing, see P6.064A.

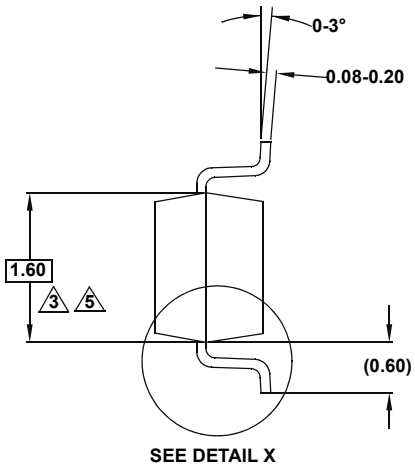
P6.064A

6 LEAD SMALL OUTLINE TRANSISTOR PLASTIC PACKAGE

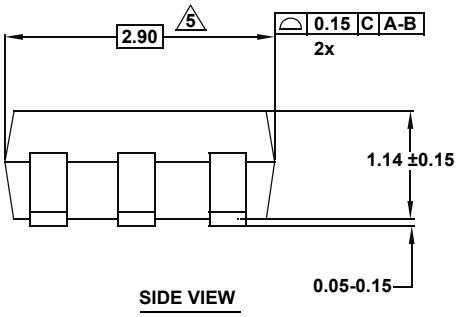
Rev 0, 2/10



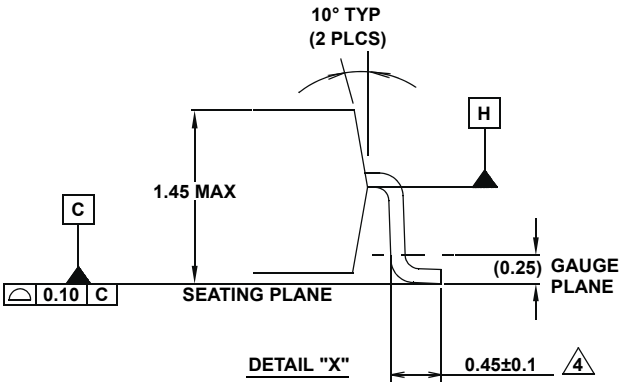
TOP VIEW

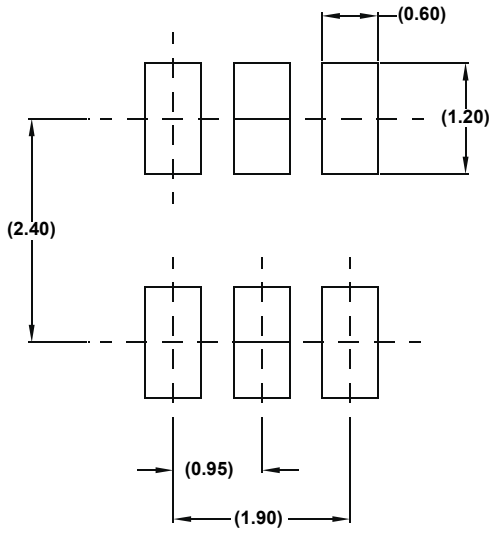


END VIEW



SIDE VIEW





TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
3. Dimension is exclusive of mold flash, protrusions or gate burrs.
4. Foot length is measured at reference to guage plane.
5. This dimension is measured at Datum “H”.
6. Package conforms to JEDEC MO-178AA.