

To our customers,

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## Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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MOS FIELD EFFECT TRANSISTOR  
**2SK2461**

**SWITCHING  
 N-CHANNEL POWER MOS FET  
 INDUSTRIAL USE**

**DESCRIPTION**

The 2SK2461 is N-Channel MOS Field Effect Transistor designed for high speed switching applications.

**FEATURES**

- Low On-Resistance  
 $R_{DS(on)1} = 80 \text{ m}\Omega \text{ MAX. (@ } V_{GS} = 10 \text{ V, } I_D = 10 \text{ A)}$   
 $R_{DS(on)2} = 0.1 \text{ }\Omega \text{ MAX. (@ } V_{GS} = 4 \text{ V, } I_D = 10 \text{ A)}$
- Low  $C_{iss}$   $C_{iss} = 1400 \text{ pF TYP.}$
- Built-in G-S Gate Protection Diodes
- High Avalanche Capability Ratings

**ABSOLUTE MAXIMUM RATINGS ( $T_A = 25 \text{ }^\circ\text{C}$ )**

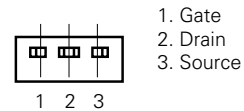
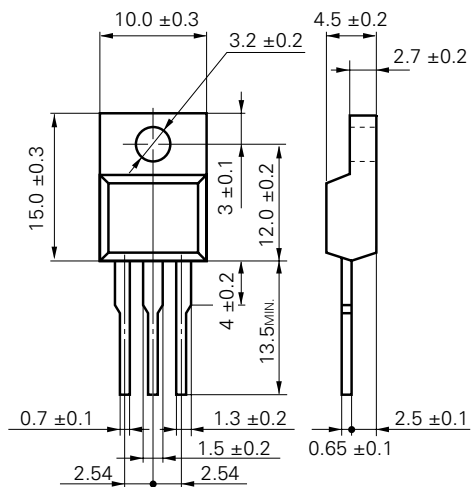
Drain to Source Voltage	$V_{DSS}$	100	V
Gate to Source Voltage	$V_{GSS}$	$\pm 20$	V
Drain Current (DC)	$I_{D(DC)}$	$\pm 20$	A
Drain Current (pulse)*	$I_{D(pulse)}$	$\pm 80$	A
Total Power Dissipation ( $T_c = 25 \text{ }^\circ\text{C}$ )	$P_{T1}$	35	W
Total Power Dissipation ( $T_A = 25 \text{ }^\circ\text{C}$ )	$P_{T2}$	2.0	W
Channel Temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$
Single Avalanche Current**	$I_{AS}$	20	A
Single Avalanche Energy**	$E_{AS}$	40	mJ

\*  $PW \leq 10 \text{ }\mu\text{s}$ , Duty Cycle  $\leq 1 \%$

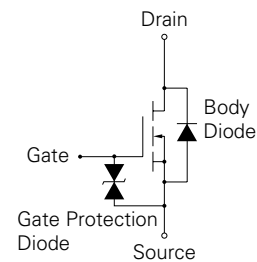
\*\* Starting  $T_{ch} = 25 \text{ }^\circ\text{C}$ ,  $R_G = 25 \text{ }\Omega$ ,  $V_{GS} = 20 \text{ V} \rightarrow 0$

**PACKAGE DIMENSIONS**

(in millimeters)



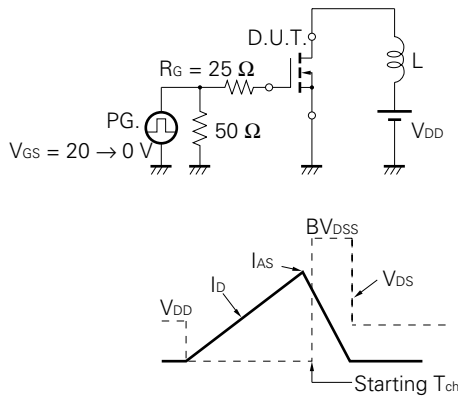
**MP-45F (ISOLATED TO-220)**



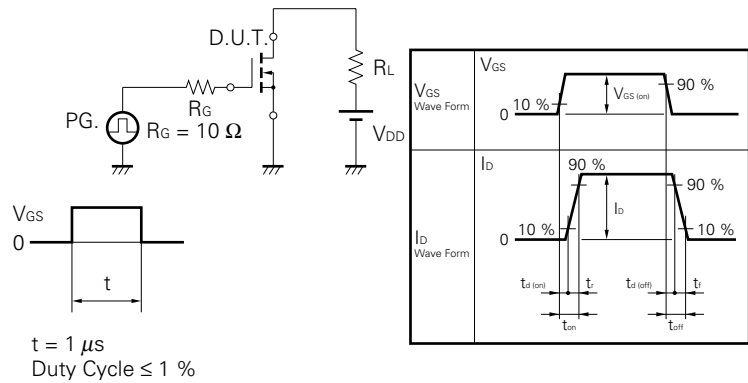
**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C)**

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-Resistance	R <sub>DS(on)1</sub>		58	80	mΩ	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A
Drain to Source On-Resistance	R <sub>DS(on)2</sub>		70	100	mΩ	V <sub>GS</sub> = 4 V, I <sub>D</sub> = 10 A
Gate to Source Cutoff Voltage	V <sub>GS(off)</sub>	1.0	1.7	2.0	V	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA
Forward Transfer Admittance	y <sub>fs</sub>	12	19		S	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 10 A
Drain Leakage Current	I <sub>bss</sub>			10	μA	V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0
Gate to Source Leakage Current	I <sub>gss</sub>			±10	μA	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0
Input Capacitance	C <sub>iss</sub>		1400		pF	V <sub>DS</sub> = 10 V
Output Capacitance	C <sub>oss</sub>		470		pF	V <sub>GS</sub> = 0
Reverse Transfer Capacitance	C <sub>rss</sub>		150		pF	f = 1 MHz
Turn-On Delay Time	t <sub>d(on)</sub>		21		ns	I <sub>D</sub> = 10 A
Rise Time	t <sub>r</sub>		110		ns	V <sub>GS(on)</sub> = 10 V
Turn-Off Delay Time	t <sub>d(off)</sub>		140		ns	V <sub>DD</sub> = 50 V
Fall Time	t <sub>f</sub>		110		ns	R <sub>G</sub> = 10 Ω
Total Gate Charge	Q <sub>G</sub>		51		nC	I <sub>D</sub> = 20 A
Gate to Source Charge	Q <sub>GS</sub>		4.9		nC	V <sub>DD</sub> = 80 V
Gate to Drain Charge	Q <sub>GD</sub>		15		nC	V <sub>GS</sub> = 10 V
Body Diode Forward Voltage	V <sub>F(S-D)</sub>		1.1		V	I <sub>F</sub> = 20 A, V <sub>GS</sub> = 0
Reverse Recovery Time	t <sub>rr</sub>		170		ns	I <sub>F</sub> = 20 A, V <sub>GS</sub> = 0
Reverse Recovery Charge	Q <sub>rr</sub>		770		nC	di/dt = 100 A/μs

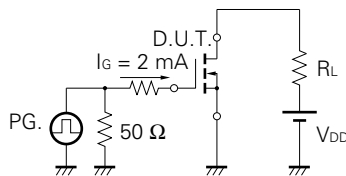
**Test Circuit 1 Avalanche Capability**



**Test Circuit 2 Switching Time**

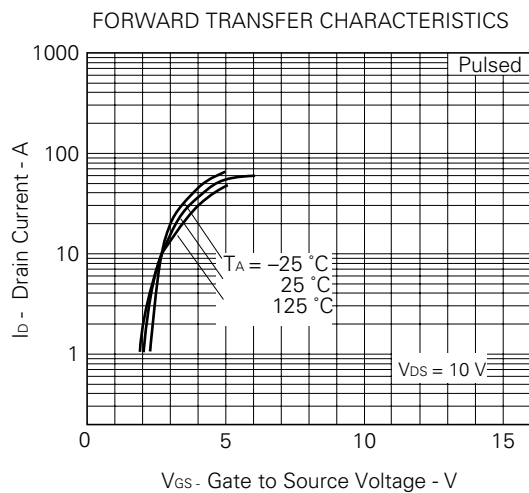
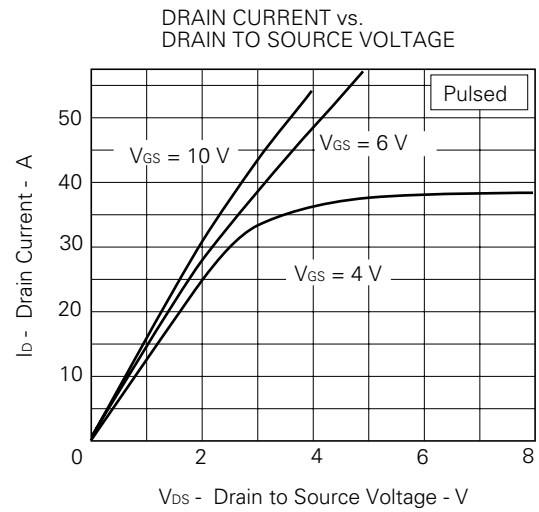
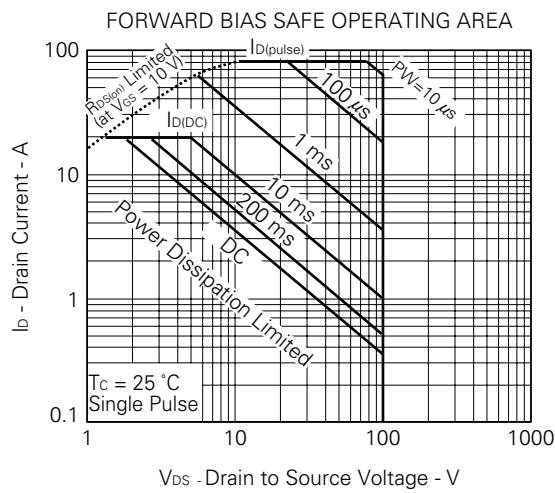
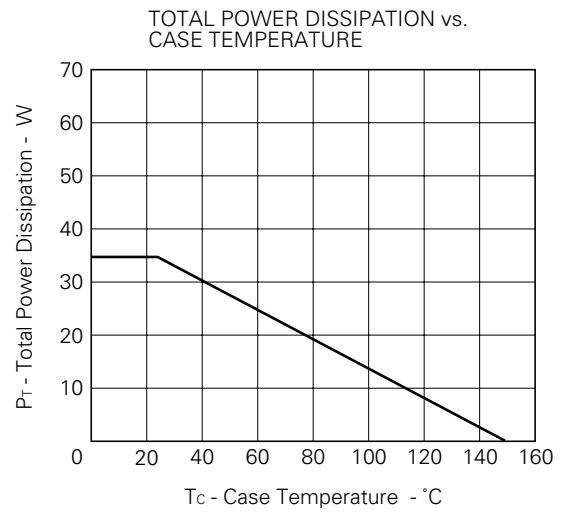
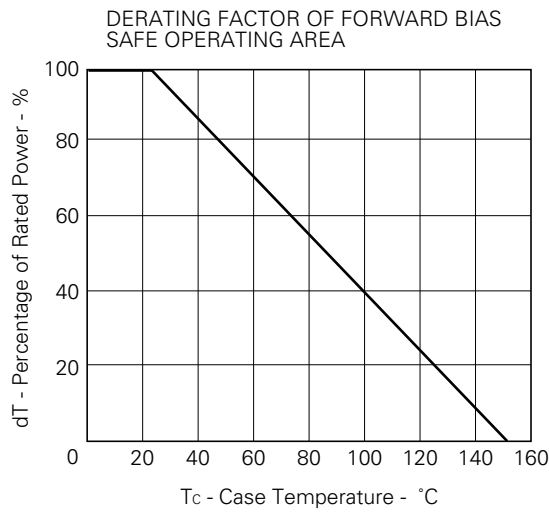


**Test Circuit 3 Gate Charge**

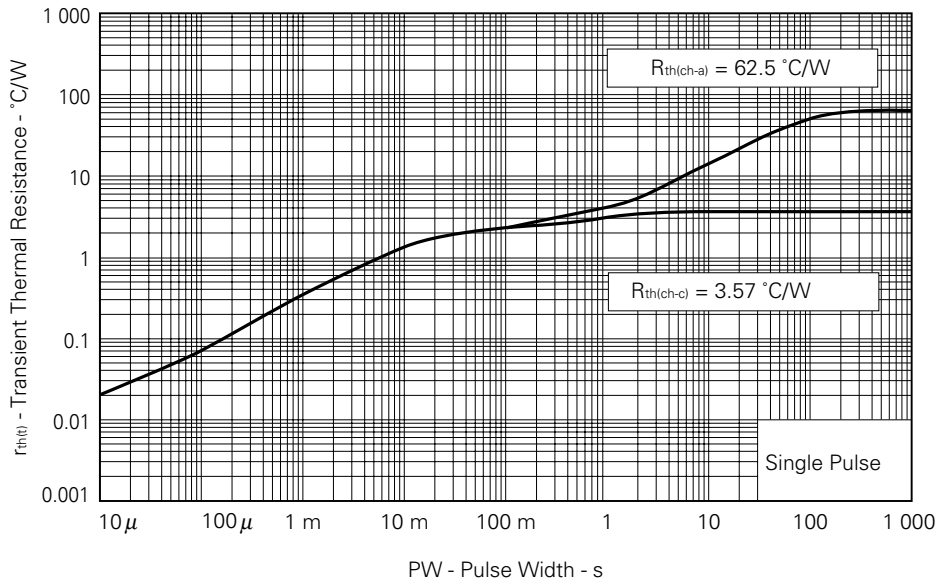


The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

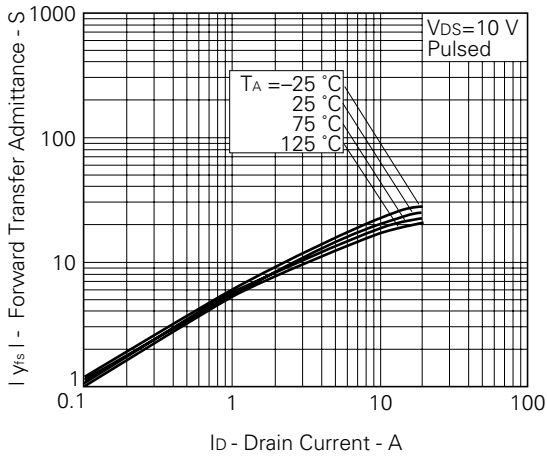
TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C)



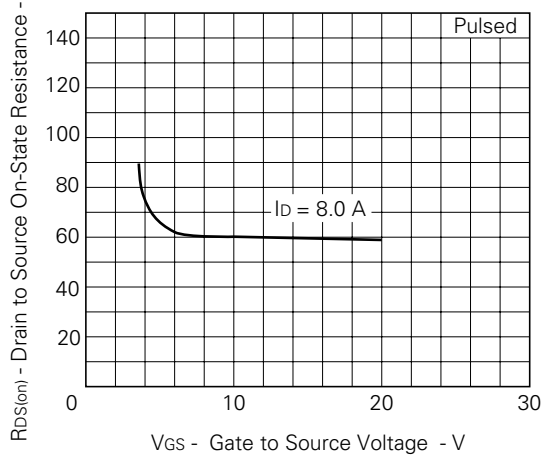
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



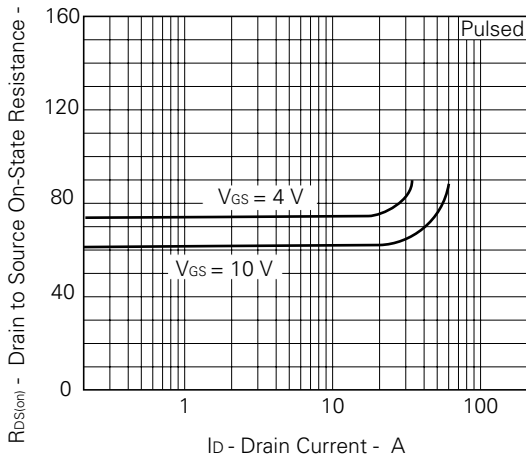
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



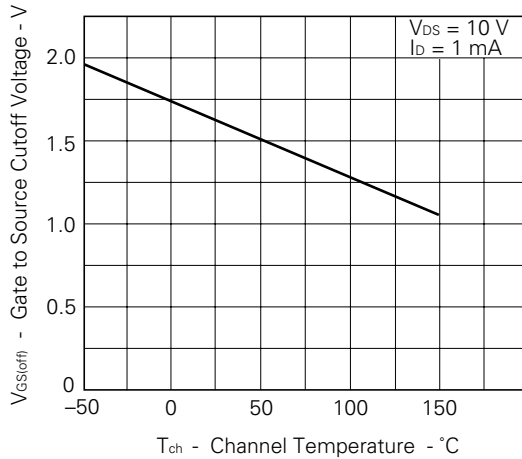
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



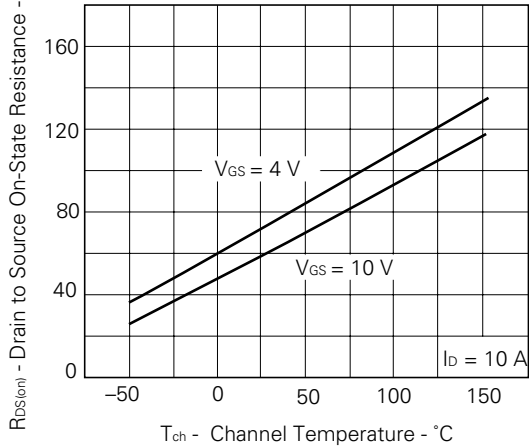
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



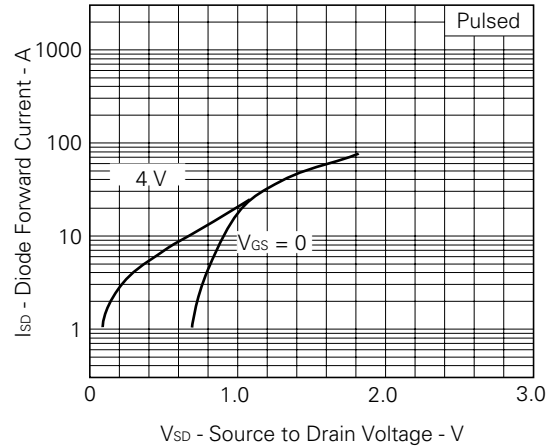
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE



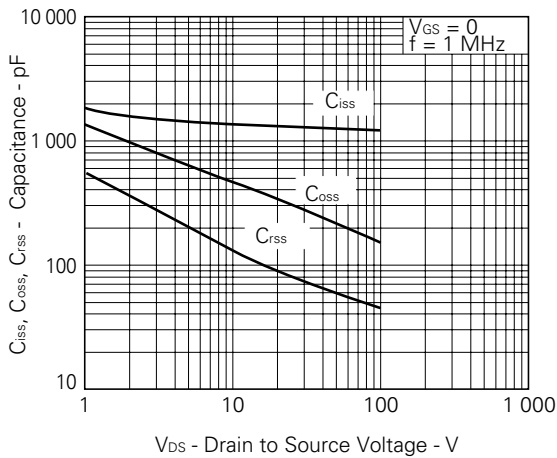
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



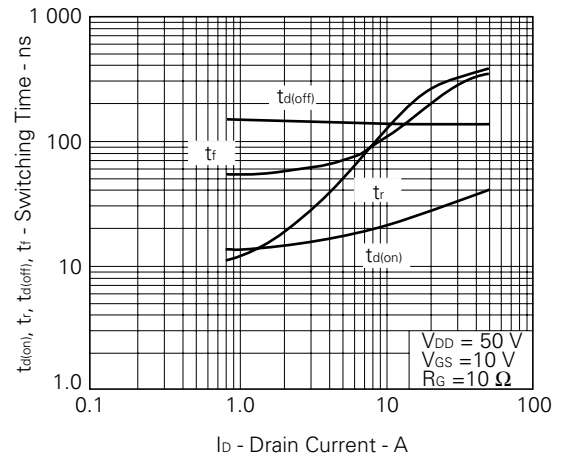
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



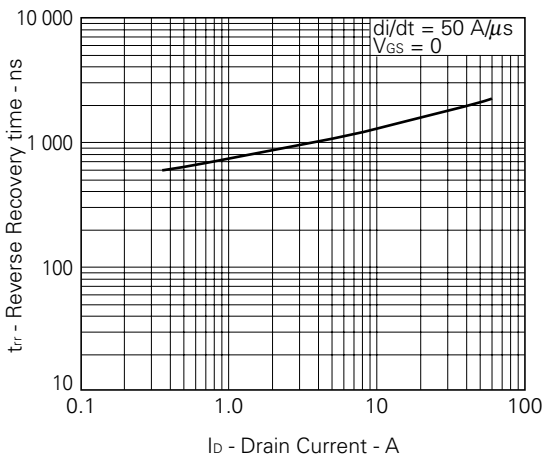
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



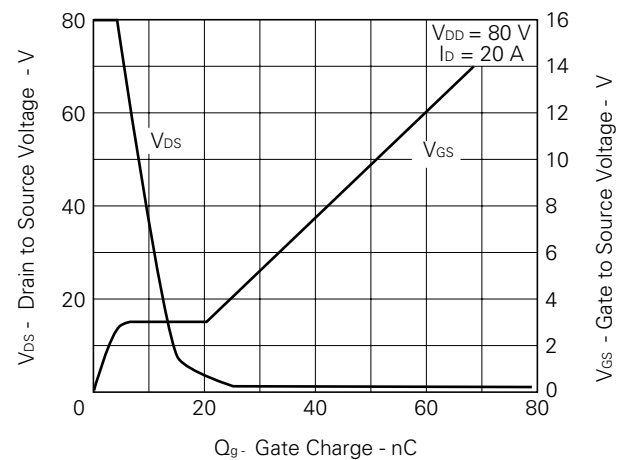
SWITCHING CHARACTERISTICS

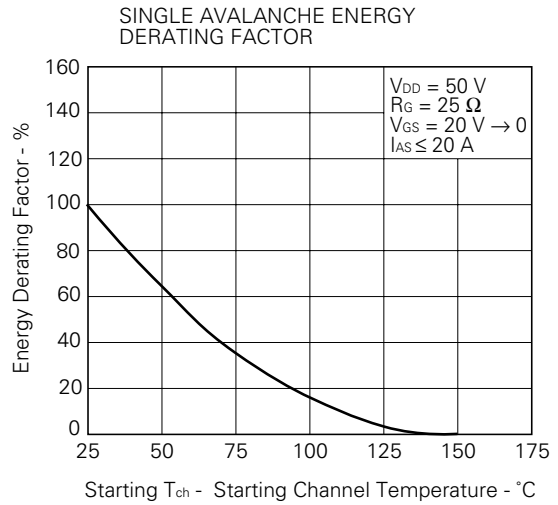
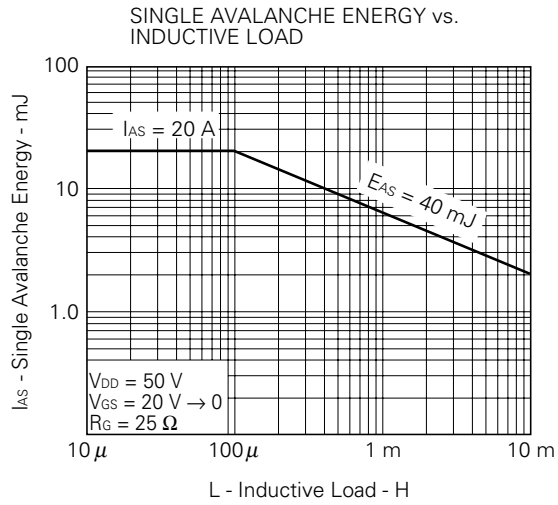


REVERSE RECOVERY TIME vs. DRAIN CURRENT



DYNAMIC INPUT/OUTPUT CHARACTERISTICS







**REFERENCE**

Document Name	Document No.
NEC semiconductor device reliability/quality control system.	TEI-1202
Quality grade on NEC semiconductor devices.	IEI-1209
Semiconductor device mounting technology manual.	IEI-1207
Semiconductor device package manual.	IEI-1213
Guide to quality assurance for semiconductor devices.	MEI-1202
Semiconductor selection guide.	MF-1134
Power MOS FET features and application switching power supply.	TEA-1034
Application circuits using Power MOS FET.	TEA-1035
Safe operating area of Power MOS FET.	TEA-1037

The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device is actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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