ART700FH; ART700FHS; ART700FHG Power LDMOS transistor

AMPLEON Product data sheet

Product profile 1.

1.1 General description

Based on Advanced Rugged Technology (ART), this 700 W LDMOS RF power transistor has been designed to cover a wide range of applications for ISM, broadcast and non cellular communications. The unmatched transistor has a frequency range of 1 MHz to 450 MHz.

Table 1. **Application information**

Test signal	f	V _{DS}	PL	Gp	ησ
	(MHz)	(V)	(W)	(dB)	(%)
CW pulsed [1][2]	108	50	700	27	81.5
CW pulsed [1][2]	108	55	800	28.5	80
CW [1]	108	55	800	27.5	79.5

[1] Production circuit.

[2] $t_p = 100 \ \mu s; \delta = 10 \%$.

1.2 Features and benefits

- High breakdown voltage enables class E operation at V_{DS} = 48 V
- Suitable for V_{DS} = 50 and 55 V
- Qualified up to a maximum of V_{DS} = 55 V
- Characterized from 30 V to 55 V to support a wide range of applications
- Integrated dual sided ESD protection enables class C operation and complete switch off of the transistor
- Excellent ruggedness with no device degradation
- High efficiency
- Excellent thermal stability
- Designed for broadband operation
- For RoHS compliance see the product details on the Ampleon website

1.3 Applications

- Industrial, scientific and medical applications
 - Plasma generators
 - MRI systems
 - ◆ CO₂ lasers
 - Particle accelerators
- Broadcast
 - FM radio
 - VHF TV
- Communications
 - Non cellular communications
 - UHF radar

2. Pinning information

Pin	Description	Simplified outline	Graphic symbol
ART700F	H (SOT1214A)		
1	drain1		
2	drain2		
3	gate1		
4	gate2	3 4	3 5
5	source	[1]	
			z sym117
ART700F	HS (SOT1214B)		
1	drain1		
2	drain2		1
3	gate1		
4	gate2	3 4 5	3 - 5
5	source	[1]	
			۲
			2 sym117
ART700F	HG (SOT1214C)		
1	drain1		
2	drain2		1
3	gate1		
4	gate2		3 5
5	source	<u>[1]</u>	
			٣
			2 sym117

[1] Connected to flange.

ART2K0FE_2K0FES_2K0FEG

3. Ordering information

Table 3. Ordering information						
Package name	Orderable part number	12NC	Packing description	Min. orderable quantity (pieces)		
SOT1214A	ART700FHU	9349 604 89112	Tray; 20-fold; non-dry pack	60		
SOT1214B	ART700FHSU	9349 605 47112	Tray; 20-fold; non-dry pack	60		
SOT1214C	ART700FHGJ	9349 605 48118	TR13; 100-fold; 44 mm; non-dry pack	100		

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage		-	177	V
V _{GS}	gate-source voltage		-9	+13	V
T _{stg}	storage temperature		-65	+150	°C
Tj	junction temperature	[1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Тур	Unit
R _{th(j-c)}	thermal resistance from junction to case	$T_j = 120 \ ^{\circ}C$ [1][2]	0.175	K/W
Z _{th(j-c)}	transient thermal impedance from junction to case	$ T_{j} = 120 \ ^{\circ}C; \ t_{p} = 100 \ \mu s; \qquad $	0.052	K/W

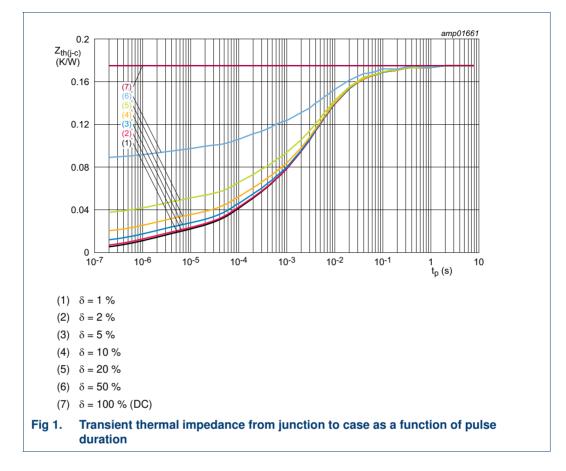
[1] T_j is the junction temperature.

[2] R_{th(j-c)} is measured under RF conditions.

[3] See Figure 1.

ART700FH(S)(G)

Power LDMOS transistor



6. Characteristics

Table 6. DC characteristics

 $T_i = 25 \ ^{\circ}C$; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{(BR)DSS}	drain-source breakdown voltage	$V_{GS} = 0 V; I_D = 2.8 mA$	177	191	-	V
V _{GS(th)}	gate-source threshold voltage	$V_{DS} = 20 \text{ V}; \text{ I}_{D} = 275 \text{ mA}$	1.5	2.1	2.5	V
I _{DSS}	drain leakage current	$V_{GS} = 0 V; V_{DS} = 50 V$	-	-	1.4	μA
I _{DSX}	drain cut-off current	$\label{eq:VGS} \begin{array}{l} V_{GS} = V_{GS(th)} + 3.75 \ V; \\ V_{DS} = 20 \ V \end{array}$	-	40	-	A
I _{GSS}	gate leakage current	V _{GS} = 13 V; V _{DS} = 0 V	-	-	140	nA
R _{DS(on)}	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75 V;$ I _D = 9.625 A	-	0.171	-	Ω

Power LDMOS transistor

Table 7.	AC	characteristics
Table 7.	AC	characteristics

 $T_i = 25 \ ^{\circ}C$; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
C _{rs}	feedback capacitance	V _{GS} = 0 V; f = 1 MHz				
		V _{DS} = 50 V	-	1.04	-	pF
		V _{DS} = 55 V	-	1.00	-	pF
C _{iss}	input capacitance	V _{GS} = 0 V; f = 1 MHz				
		V _{DS} = 50 V	-	312	-	pF
		V _{DS} = 55 V	-	312	-	pF
C _{oss}	output capacitance	V _{GS} = 0 V; f = 1 MHz				
		V _{DS} = 50 V	-	97	-	pF
		V _{DS} = 55 V	-	93	-	pF

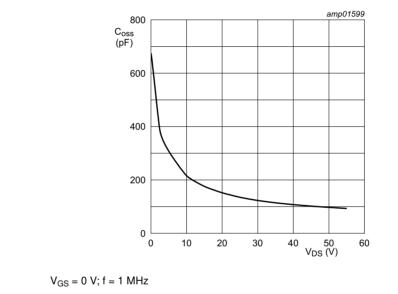


Fig 2. Output capacitance as a function of drain-source voltage; typical values per section

Table 8. RF characteristics

Test signal: pulsed RF; $t_p = 100 \ \mu s$; $\delta = 10 \ \%$; $f = 108 \ MHz$; RF performance at $V_{DS} = 55 \ V$; $I_{Dq} = 25 \ mA$ per section; $T_{case} = 25 \ ^{\circ}C$; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
G _p	power gain	P _L = 800 W	26.8	28.6	-	dB
RL _{in}	input return loss	P _L = 800 W	-	-32.7	-	dB
η _D	drain efficiency	P _L = 800 W	73.0	77.6	-	%

7. Test information

7.1 Ruggedness in class-AB operation

The ART700FH, ART700FHS and ART700FHG are capable of withstanding a load mismatch corresponding to VSWR ≥ 65 : 1 through all phases under the following conditions: P_L = 700 W pulsed at V_{DS} = 50 V and P_L = 800 W pulsed at V_{DS} = 55 V; I_{Dg} = 50 mA per section; t_p = 100 µs; δ = 10 %; f = 108 MHz.

7.2 Impedance information

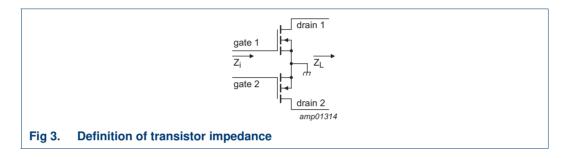


Table 9.Typical push-pull impedanceSimulated Z_i and Z_L device impedance.

f	Zi	ZL	PL
(MHz)	(Ω)	(Ω)	(W)
V _{DS} = 50 V			
108	4.75 – j17.00	6.60 + j1.10	700
V _{DS} = 55 V			
108	4.75 – j17.00	6.95 + j1.30	800

7.3 Test circuit

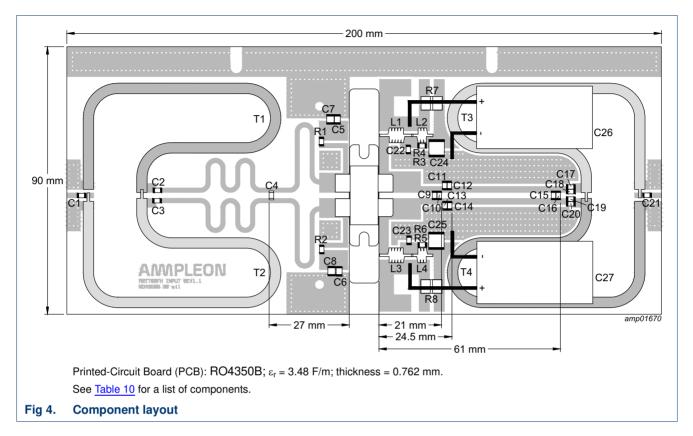


Table 10. List of components

For test circuit see Figure 4.

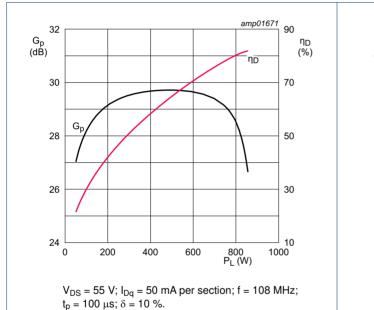
Component	Description	Value	Remarks
C1	multilayer ceramic chip capacitor	510 pF 🚺	
C2, C3	multilayer ceramic chip capacitor	62 pF [1]	
C4	multilayer ceramic chip capacitor	160 pF [1]	
C5, C6, C22, C23	multilayer ceramic chip capacitor	820 pF [1]	
C7, C8	multilayer ceramic chip capacitor	4.7 μF, 50 V	Murata: GRM32ER71H475KA88L
C9, C10	multilayer ceramic chip capacitor	36 pF [1]	
C11, C12, C13, C14	multilayer ceramic chip capacitor	56 pF [1]	
C15	multilayer ceramic chip capacitor	43 pF [1]	
C16	multilayer ceramic chip capacitor	47 pF [1]	
C17, C18, C19, C20	multilayer ceramic chip capacitor	62 pF [1]	
C21	multilayer ceramic chip capacitor	220 pF [1]	
C24, C25	multilayer ceramic chip capacitor	4.7 μF, 100 V	TDK: C5750X7R2A475KT/A
C26, C27	electrolytic capacitor	1500 μF, 80 V	radial leaded
L1, L3	1 mm copper wire	5 turn, D = 4 mm	
L2, L4	1 mm copper wire	3 turn, D = 4 mm	
R1, R2	chip resistor	4.7 kΩ	SMD 1206

Table 10. List of components ...continued

Component	Description	Value	Remarks
R3, R4, R5, R6	chip resistor	20 kΩ	SMD 1206
R7, R8	chip resistor	0.01 Ω	Vishay: WSHP2818
T1, T2, T3, T4	hand formable coax	50 Ω, 160 mm	SUCOFORM 141

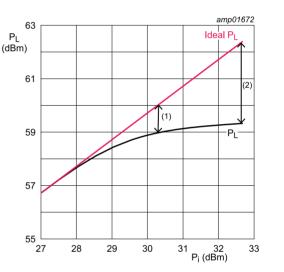
[1] AVX type 800B or capacitor of same quality.

7.4 Graphical data



7.4.1 1-Tone CW pulsed



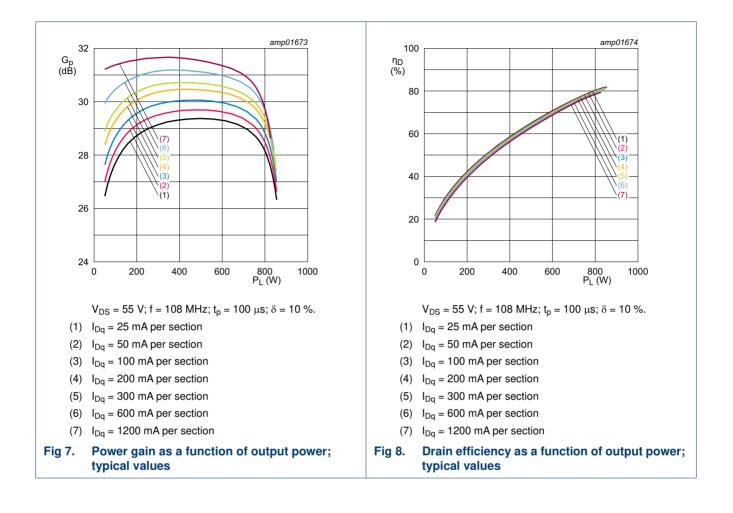


 V_{DS} = 55 V; I_{Dq} = 50 mA per section; f = 108 MHz; t_p = 100 $\mu s;$ δ = 10 %.

- (1) P_{L(1dB)} = 58.95 dBm (785 W)
- (2) $P_{L(3dB)} = 59.32 \text{ dBm} (855 \text{ W})$
- Fig 6. Output power as a function of input power; typical values

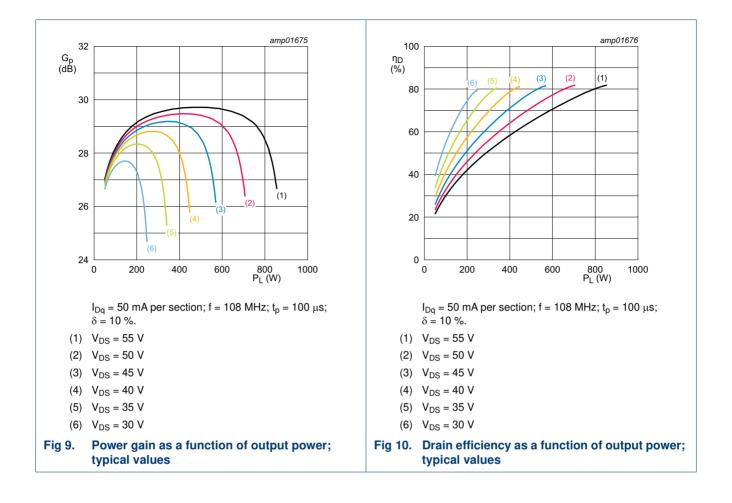
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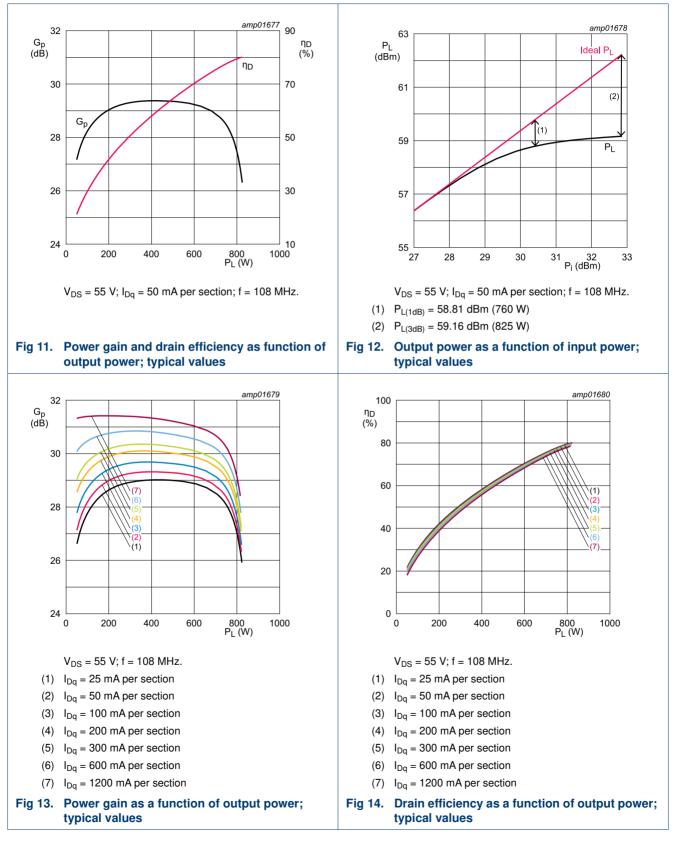


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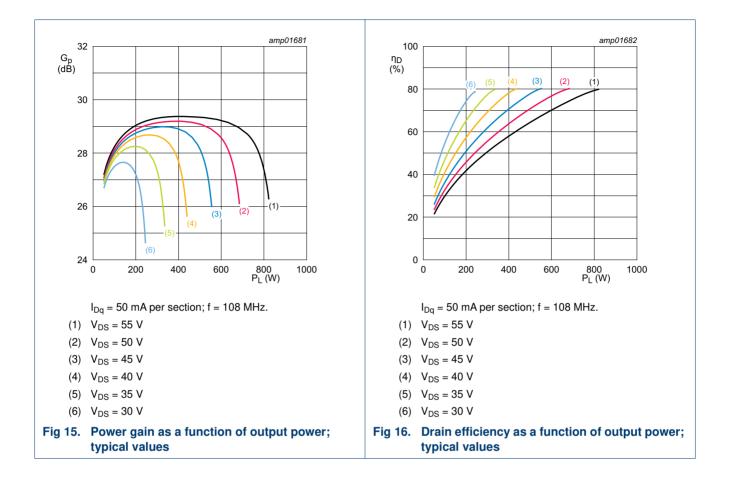


7.4.2 1-Tone CW



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ART700FH(S)(G) Power LDMOS transistor



ART700FH(S)(G) Power LDMOS transistor

8. Package outline

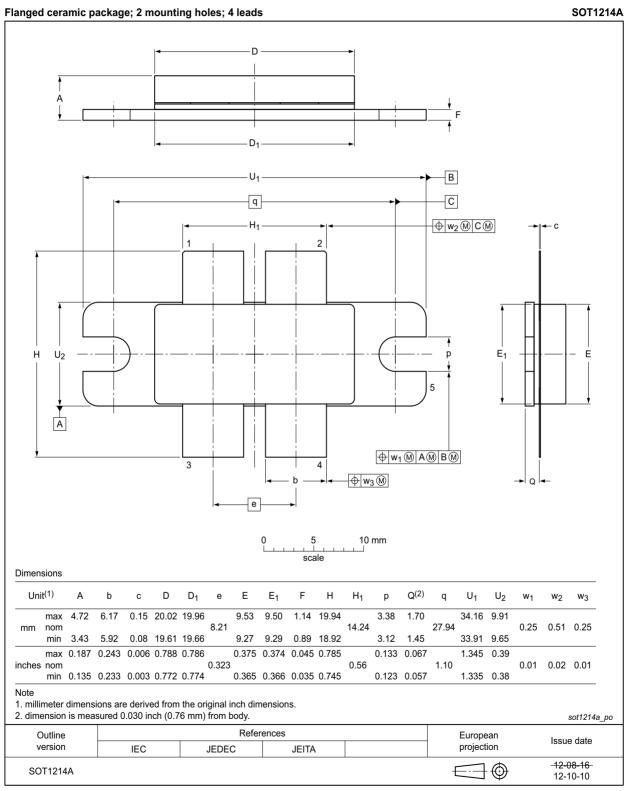


Fig 17. Package outline SOT1214A

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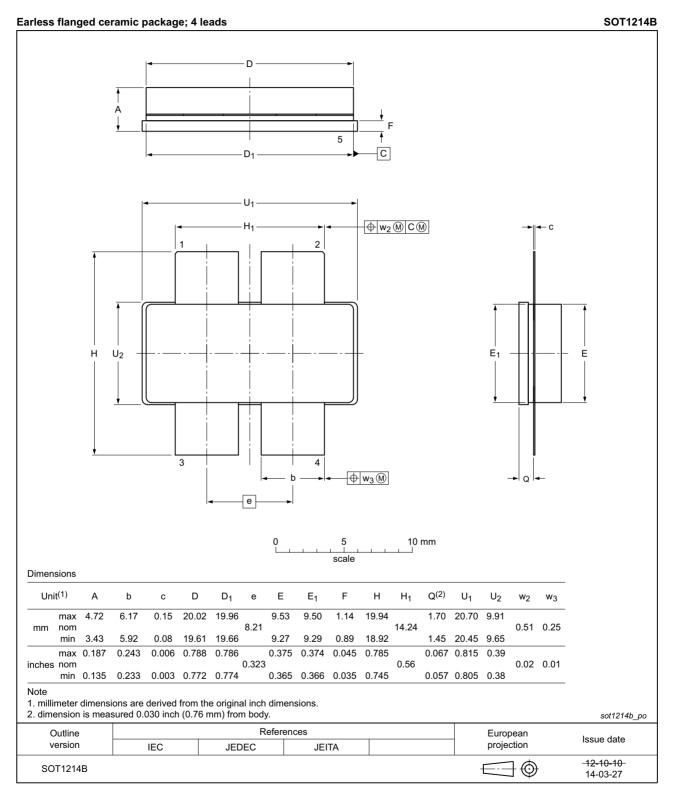


Fig 18. Package outline SOT1214B

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Product data sheet

ART700FH(S)(G) Power LDMOS transistor

SOT1214C

Earless flanged LDMOST ceramic package; 4 leads

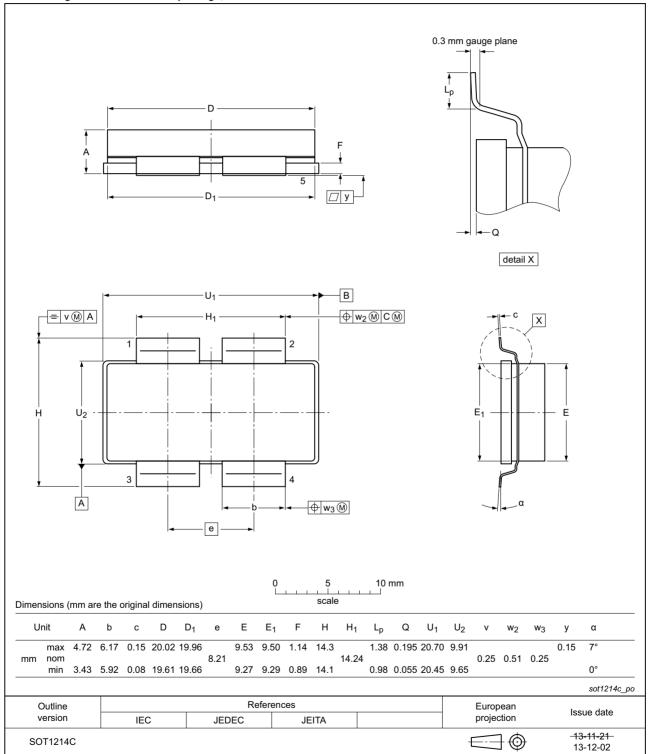


Fig 19. Package outline SOT1214C

ART2K0FE_2K0FES_2K0FEG

Product data sheet

9. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A or equivalent standards.

Table 11.ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A 🛄
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

[1] CDM classificationC2A is granted to any part that passes after exposure to an ESD pulse of 500 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V.

10. Abbreviations

Table 12. Abbreviations		
Acronym	Description	
CW	Continuous Wave	
ESD	ElectroStatic Discharge	
FM	Frequency Modulation	
ISM	Industrial, Scientific and Medical	
LDMOS	Laterally Diffused Metal-Oxide Semiconductor	
MRI	Magnetic Resonance Imaging	
MTF	Median Time to Failure	
RoHS	Restriction of Hazardous Substances	
SMD	Surface Mounted Device	
UHF	Ultra High Frequency	
VHF	Very High Frequency	
VSWR	Voltage Standing Wave Ratio	

11. Revision history

Table 13.Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
ART700FH_700FHS_700FHG v.3	20221118	Product data sheet	-	ART700FH_700FHS_700FHG v.2
Modifications:	Table 3 or	page 3: orderable p	art number of SO	T1214C changed to ART700FHGJ
ART700FH_700FHS_700FHG v.2	20220708	Product data sheet	-	ART700FH v.1
ART700FH v.1	20210924	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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