74AHC30; 74AHCT30

8-input NAND gate

Rev. 4 — 22 July 2015 Product data sheet

1. General description

The 74AHC30; 74AHCT30 is a high-speed Si-gate CMOS device and is pin compatible with Low-power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard No. 7-A.

The 74AHC30; 74AHCT30 provides an 8-input NAND function.

2. Features and benefits

- Balanced propagation delays
- All inputs have Schmitt-trigger actions
- Inputs accept voltages higher than V_{CC}
- Input levels:
  - For 74AHC30: CMOS level
  - For 74AHCT30: TTL level
- ESD protection:
  - HBM JESD22-A114E exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
  - CDM JESD22-C101C exceeds 1000 V
- Multiple package options
- Specified from −40 °C to +85 °C and from −40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AHC30D	−40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74AHCT30D				
74AHC30PW	−40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74AHCT30PW				
74AHC30BQ	−40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1
74AHCT30BQ				
74AHC30GU12	−40 °C to +125 °C	XQFN12	plastic, extremely thin quad flat package; no leads; 12 terminals; body 1.70 × 2.00 × 0.50 mm	SOT1174-1

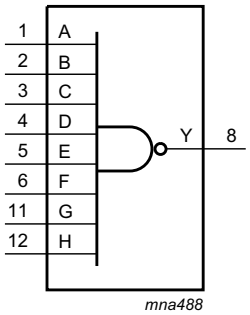
4. Marking

Table 2. Marking codes

Type number	Marking
74AHC30D	74AHC30D
74AHCT30D	74AHCT30D
74AHC30PW	AHC30
74AHCT30PW	AHCT30
74AHC30BQ	AHC30
74AHCT30BQ	AHT30
74AHC30GU12	A3[1]

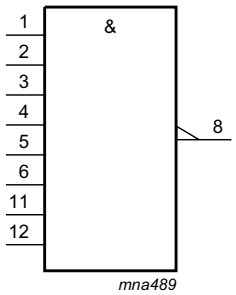
[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram



Pin numbers are shown for SO14, TSSOP14 and DHVQFN14 packages only

Fig 1. Logic symbol



Pin numbers are shown for SO14, TSSOP14 and DHVQFN14 packages only

Fig 2. IEC logic symbol

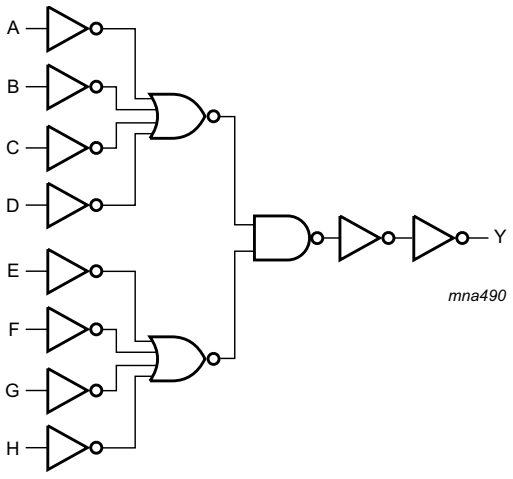


Fig 3. Logic diagram

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6. Pinning information

6.1 Pinning

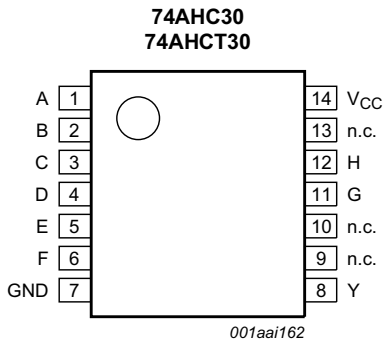
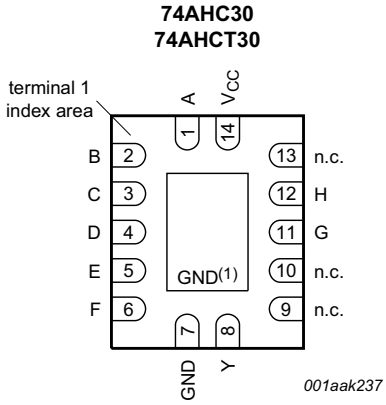


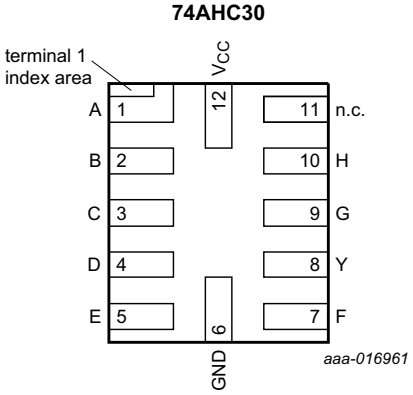
Fig 4. Pin configuration SO14 and TSSOP14



Transparent top view

(1) This is not a supply pin, the substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad, however if it is soldered the solder land should remain floating or be connected to GND

Fig 5. Pin configuration DHVQFN14



Transparent top view

Fig 6. Pin configuration XQFN12 (SOT1174-1)

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6.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	SO14, TSSOP14 and DHVQFN14	XQFN12	
A	1	1	data input
B	2	2	data input
C	3	3	data input
D	4	4	data input
E	5	5	data input
F	6	7	data input
GND	7	6	ground (0 V)
Y	8	8	data output
n.c.	9	-	not connected
n.c.	10	-	not connected
G	11	9	data input
H	12	10	data input
n.c.	13	11	not connected
V_{CC}	14	12	supply voltage

7. Functional description

Table 4. Function table[1]

Input								Output
A	B	C	D	E	F	G	H	Y
L	X	X	X	X	X	X	X	H
X	L	X	X	X	X	X	X	H
X	X	L	X	X	X	X	X	H
X	X	X	L	X	X	X	X	H
X	X	X	X	L	X	X	X	H
X	X	X	X	X	L	X	X	H
X	X	X	X	X	X	L	X	H
X	X	X	X	X	X	X	L	H
H	H	H	H	H	H	H	H	L

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care.

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8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			−0.5	+7.0	V
V_I	input voltage			−0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V	[1]	−20	-	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	[1]	−20	+20	mA
I_O	output current	$V_O = -0.5$ V to $(V_{CC} + 0.5$ V)		−25	+25	mA
I_{CC}	supply current			-	+75	mA
I_{GND}	ground current			−75	-	mA
T_{stg}	storage temperature			−65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C				
		SO14, TSSOP14 and DHVQFN14	[2]	-	500	mW
		XQFN12		-	250	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SO14 packages: above 70 °C, the value of P_{tot} derates linearly at 8 mW/K.
For TSSOP14 packages: above 60 °C, the value of P_{tot} derates linearly at 5.5 mW/K.
For DHVQFN14 packages: above 60 °C, the value of P_{tot} derates linearly at 4.5 mW/K.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74AHC30			74AHCT30			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
V_I	input voltage		0	-	5.5	0	-	5.5	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		−40	+25	+125	−40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 3.3$ V ± 0.3 V	-	-	100	-	-	-	ns/V
		$V_{CC} = 5.0$ V ± 0.5 V	-	-	20	-	-	20	ns/V

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10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74AHC30										
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
		V_{CC} = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V_{CC} = 5.5 V	3.85	-	-	3.85	-	3.85	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.5	-	0.5	-	0.5	V
		V_{CC} = 3.0 V	-	-	0.9	-	0.9	-	0.9	V
		V_{CC} = 5.5 V	-	-	1.65	-	1.65	-	1.65	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}								
		I_O = –50 μA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I_O = –50 μA; V_{CC} = 3.0 V	2.9	3.0	-	2.9	-	2.9	-	V
		I_O = –50 μA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = –4.0 mA; V_{CC} = 3.0 V	2.58	-	-	2.48	-	2.40	-	V
		I_O = –8.0 mA; V_{CC} = 4.5 V	3.94	-	-	3.80	-	3.70	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}								
		I_O = 50 μA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 50 μA; V_{CC} = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 50 μA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 3.0 V	-	-	0.36	-	0.44	-	0.55	V
		I_O = 8.0 mA; V_{CC} = 4.5 V	-	-	0.36	-	0.44	-	0.55	V
I_I	input leakage current	V_I = 5.5 V or GND; V_{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	2.0	-	20	-	40	μA
C_I	input capacitance	$V_I = V_{CC}$ or GND	-	3	10	-	10	-	10	pF
C_O	output capacitance		-	4	-	-	-	-	-	pF

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Table 7. Static characteristics *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74AHCT30										
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V								
		I_O = –50 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = –8.0 mA	3.94	-	-	3.80	-	3.70	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V								
		I_O = 50 μA	-	0	0.1	-	0.1	-	0.1	V
		I_O = 8.0 mA	-	-	0.36	-	0.44	-	0.55	V
I_I	input leakage current	V_I = 5.5 V or GND; V_{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	2.0	-	20	-	40	μA
ΔI_{CC}	additional supply current	per input pin; V_I = V_{CC} – 2.1 V; other pins at V_{CC} or GND; I_O = 0 A; V_{CC} = 4.5 V to 5.5 V	-	-	1.35	-	1.5	-	1.5	mA
C_I	input capacitance	V_I = V_{CC} or GND	-	3	10	-	10	-	10	pF
C_O	output capacitance		-	4	-	-	-	-	-	pF

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 8.

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
74AHC30										
t_{pd}	propagation delay	A, B, C, D, E, F, G, H to Y; see Figure 7 and 8 [2]								
		V_{CC} = 3.0 V to 3.6 V								
		C_L = 15 pF	-	5.0	9.5	1.0	11.0	1.0	12.0	ns
		C_L = 50 pF	-	6.7	12.0	1.0	14.5	1.0	15.5	ns
		V_{CC} = 4.5 V to 5.5 V								
		C_L = 15 pF	-	3.6	6.5	1.0	7.5	1.0	8.0	ns
		C_L = 50 pF	-	4.9	8.0	1.0	9.5	1.0	10.5	ns
C_{PD}	power dissipation capacitance	f_i = 1 MHz; V_I = GND to V_{CC} [3]	-	10	-	-	-	-	-	pF

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Table 8. Dynamic characteristics *…continued*

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 8.

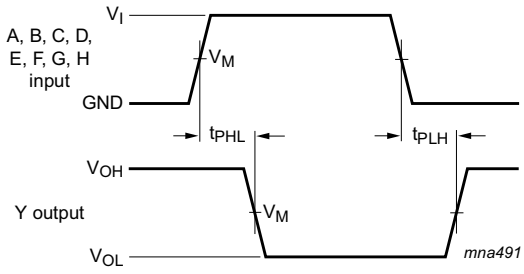
Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
74AHCT30; V_{CC} = 4.5 V to 5.5 V										
t_{pd}	propagation delay	A, B, C, D, E, F, G, H to Y; see Figure 7 and 8 [2]								
		C_L = 15 pF	-	3.3	6.5	1.0	7.5	1.0	8.0	ns
		C_L = 50 pF	-	4.7	8.5	1.0	9.5	1.0	10.5	ns
C_{PD}	power dissipation capacitance	f_i = 1 MHz; V_I = GND to V_{CC} [3]	-	12	-	-	-	-	-	pF

[1] Typical values are measured at nominal supply voltage (V_{CC} = 3.3 V and V_{CC} = 5.0 V).

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

12. Waveforms



Measurement points are given in Table 9.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 7. Input to output propagation delays

Table 9. Measurement points

Type	Input	Output
	V_M	V_M
74AHC30	0.5 × V_{CC}	0.5 × V_{CC}
74AHCT30	1.5 V	0.5 × V_{CC}

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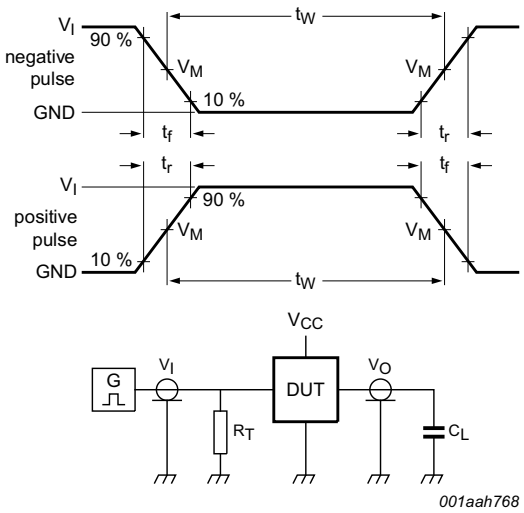

Test data is given in Table 10.

Definitions for test circuit:

R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

C_L = load capacitance including jig and probe capacitance.

Fig 8. Test circuit for measuring switching times

Table 10. Test data

Type	Input		Load	Test
	V_I	t_r, t_f	C_L	
74AHC30	V_{CC}	≤ 3.0 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}
74AHCT30	3.0 V	≤ 3.0 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}

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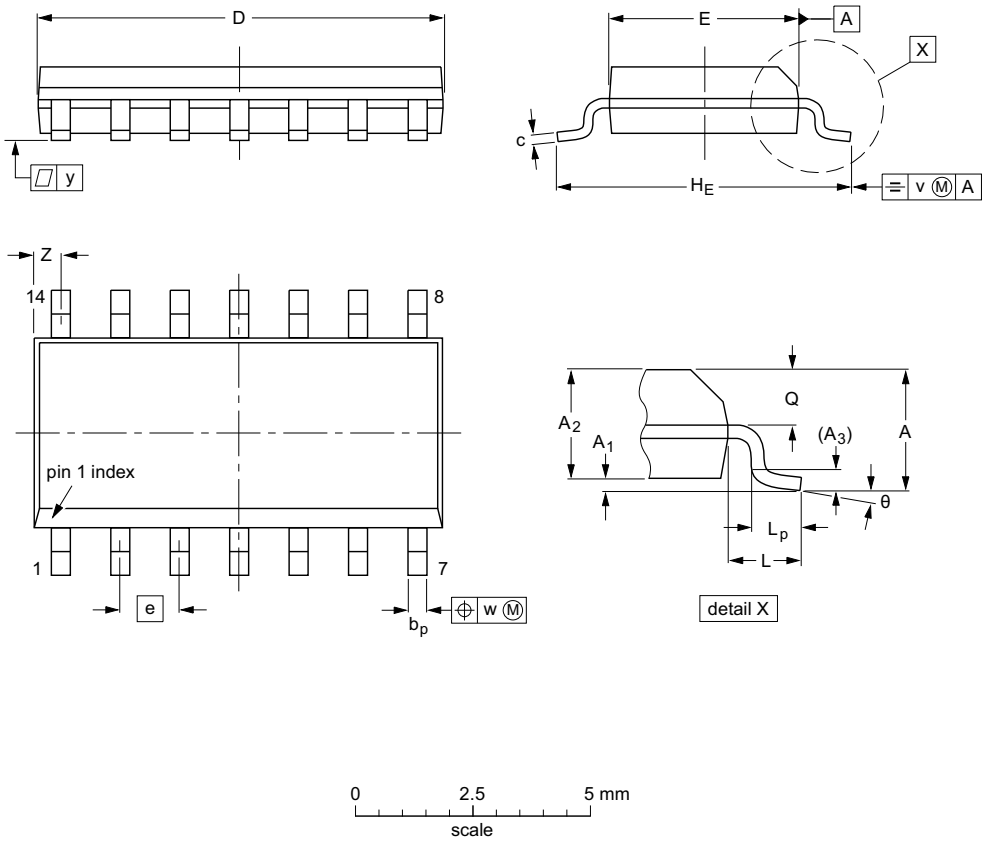
13. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Fig 9. Package outline SOT108-1 (SO14)

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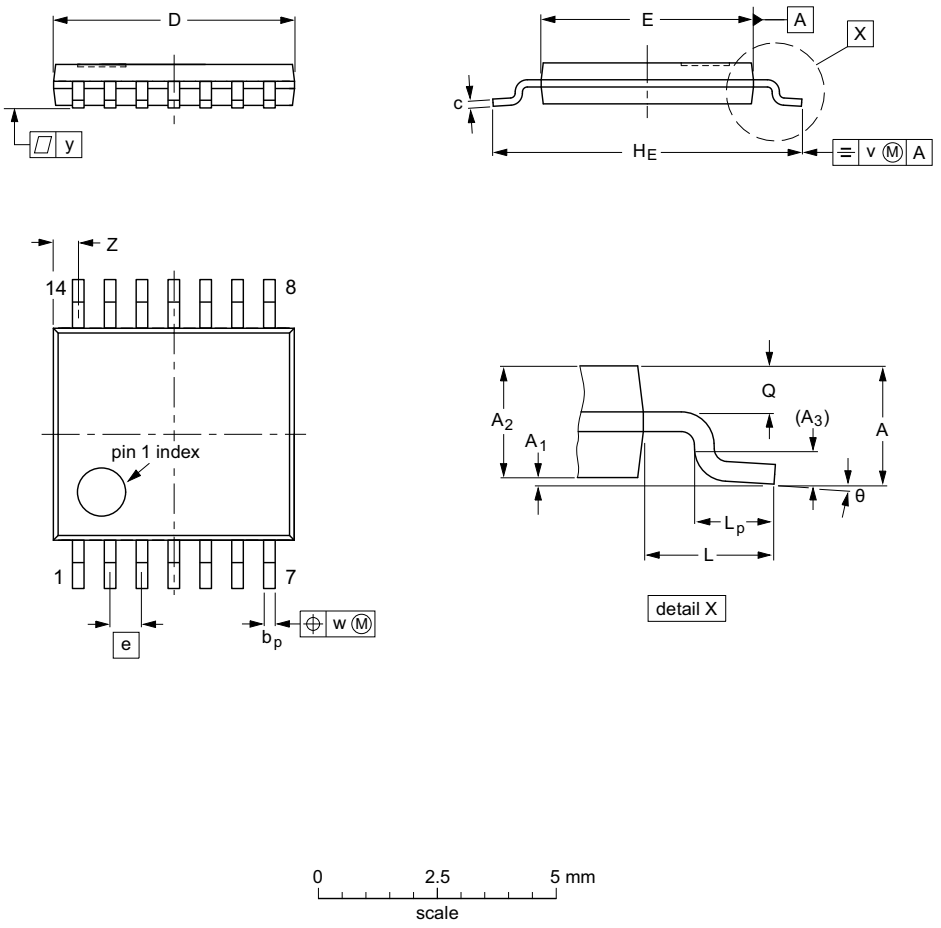
TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

Fig 10. Package outline SOT402-1 (TSSOP14)

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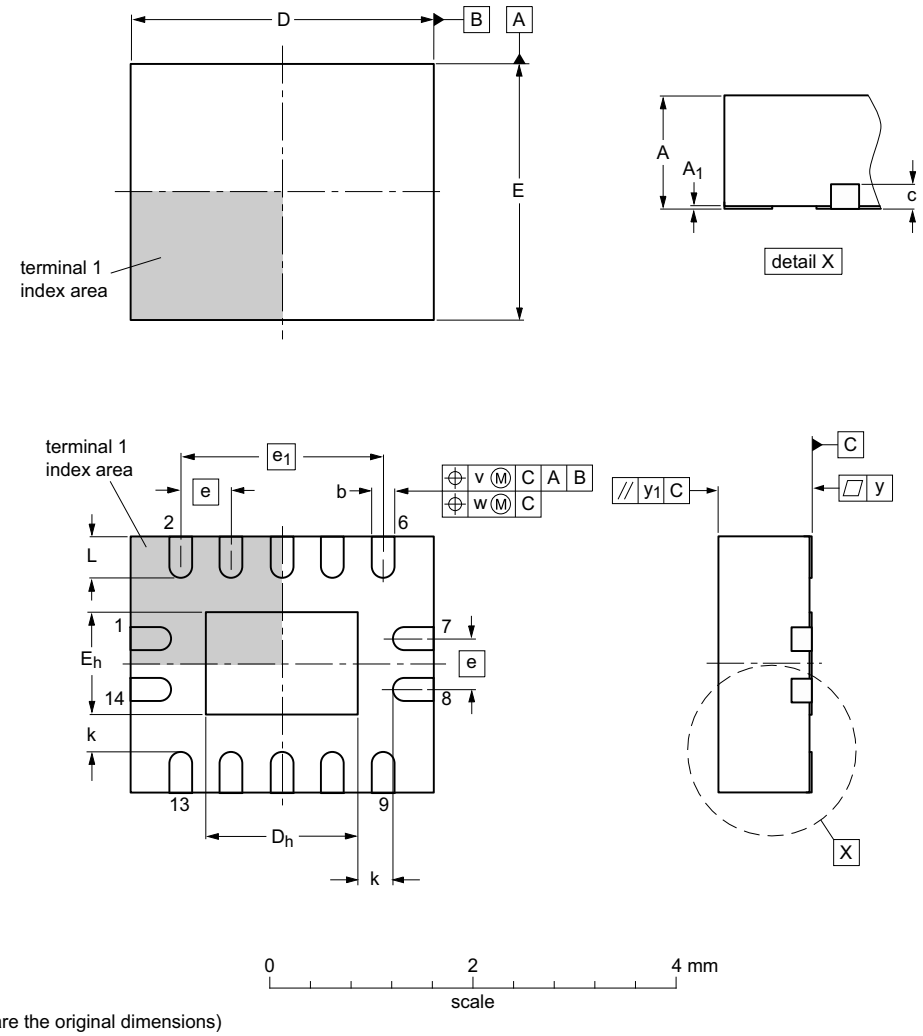
DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm **SOT762-1**



Dimensions (mm are the original dimensions)

Unit		$A^{(1)}$	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	k	L	v	w	y	y_1
	max	1	0.05	0.30		3.1	1.65	2.6	1.15				0.5				
mm	nom		0.02	0.25	0.2	3.0	1.50	2.5	1.00	0.5	2		0.4	0.1	0.05	0.05	0.1
	min		0.00	0.18		2.9	1.35	2.4	0.85			0.2	0.3				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot762-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT762-1		MO-241				~~15-04-10~~ 15-05-05

Fig 11. Package outline SOT762-1 (DHVQFN14)

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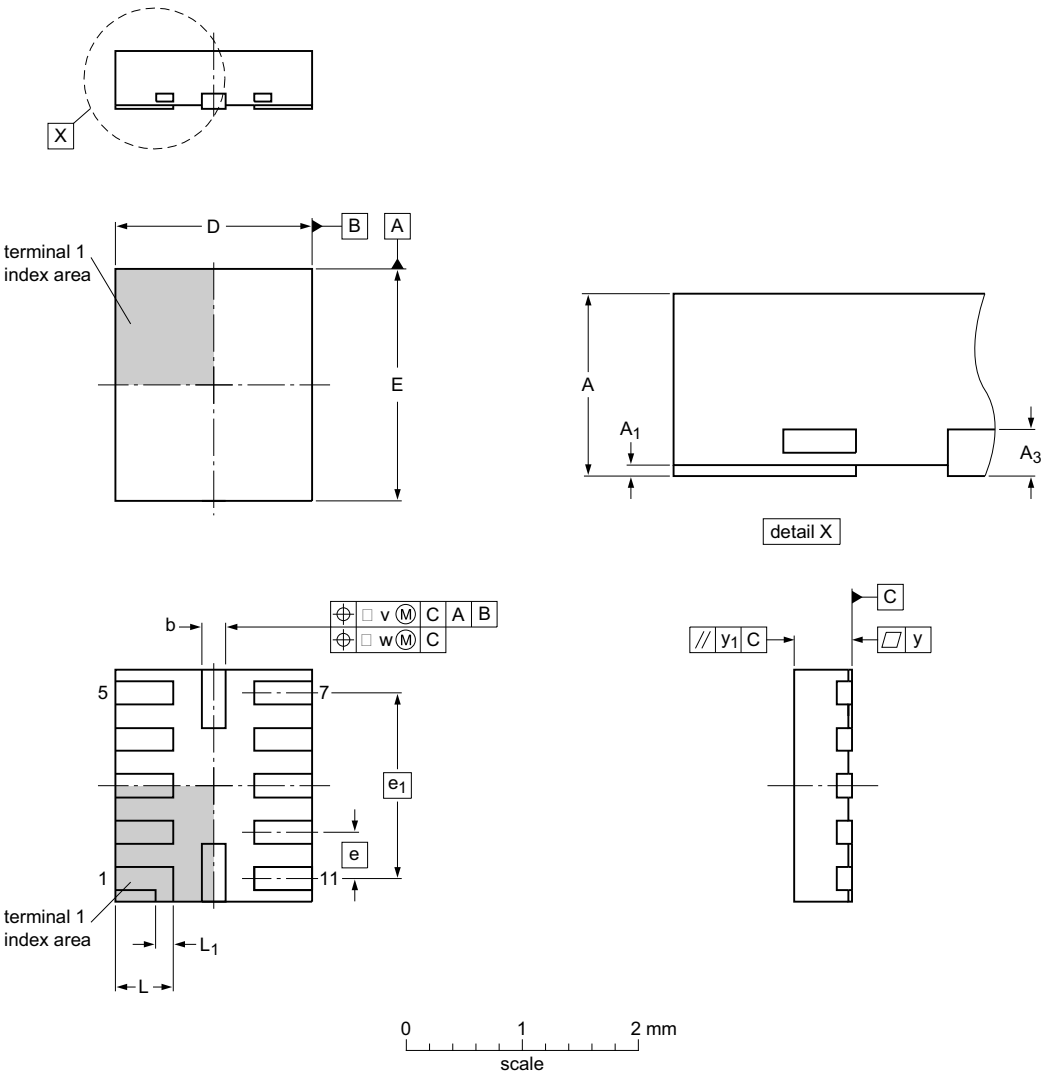
XQFN12: plastic, extremely thin quad flat package; no leads; 12 terminals; body 1.70 x 2.00 x 0.50 mm **SOT1174-1**



Dimensions

Unit(1)		A	A_1	A_3	b	D	E	e	e_1	L	L_1	v	w	y	y_1
	max	0.5	0.05		0.25	1.8	2.1			0.55					
mm	nom			0.127	0.20	1.7	2.0	0.4	1.6	0.50	0.15	0.1	0.05	0.05	0.05
	min		0.00		0.15	1.6	1.9			0.45					

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1174-1_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT1174-1	- - -	MO-288	- - -		10-04-07 10-04-21

Fig 12. Package outline SOT1174-1 (XQFN12)

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14. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
LSTTL	Low-power Schottky Transistor-Transistor Logic
MM	Machine Model

15. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT30 v.4	20150722	Product data sheet	-	74AHC_AHCT30 v.3
Modifications:	• Added type number 74AHC30GU12.			
74AHC_AHCT30 v.3	20090626	Product data sheet	-	74AHC_AHCT30 v.2
Modifications:	• Section 3: DHVQFN14 package added. • Section 8: derating values added for DHVQFN14 package. • Section 13: outline drawing added for DHVQFN14 package.			
74AHC_AHCT30 v.2	20080530	Product data sheet	-	74AHC_AHCT30 v.1
74AHC_AHCT30 v.1	19991130	Product specification	-	-

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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