

# UG 512: Si5381/82A-E Evaluation Board User's Guide

The Si5381/82A-E-EB is used for evaluating the Ultra-Low Phase Noise Quad/Dual PLL. The Si5381/82 employs fourth-generation DSPLL technology to enable clock generation for LTE/ JESD204B applications which require the highest level of jitter performance. The Si5381/82A-E-EB has four independent input clocks and a total of 12 outputs with 4/2 PLLs. The Si5381/82A-E-EB also has four independent input clocks and a total of 12 outputs with 2 PLLs. The Si5381/82A-E-EB can be easily controlled and configured using Skyworks' Clock Builder Pro<sup>®</sup> (CBPro) software tool.

The device revision is distinguished by a white 1 inch x 0.187 inch label with the text "Si5381/82A-E-EB" installed in the lower left hand corner of the board. (For ordering purposes only, the terms "EB" and "EVB" refer to the board and the kit respectively. For the purpose of this document, the terms are synonymous in context.)

#### EVB FEATURES

- Powered from USB port or external power supply
- Onboard 54 MHz XO provides holdover mode of operation on the Si5381/82
- CBPro GUI programmable VDDO supplies allow each of the ten primary outputs to have its own supply voltage selectable from 3.3, 2.5, or 1.8 V
- CBPro GUI-controlled voltage, current, and power measurements of VDD and all VDDO supplies
- Status LEDs for power supplies and control/status signals of Si5381/82
- SMA connectors for input clocks and output clocks



UG 512: Si5381/82A-E Evaluation Board User's Guide • Si5381/82 Functional Block Diagram

# 1. Si5381/82 Functional Block Diagram

Below is a functional block diagram of the Si5381/82A-E-EB. This EB can be connected to a PC via the main USB connector for programming, control, and monitoring. See 2. Quick Start and Jumper Defaults or 6.1 Installing ClockBuilder Pro Desktop Software for more information.

Note: All Si5381/82 schematics, BOMs, User's Guides, and software can be found online at the following link: https://www.skywork-sinc.com/search?q=si538%20evaluation

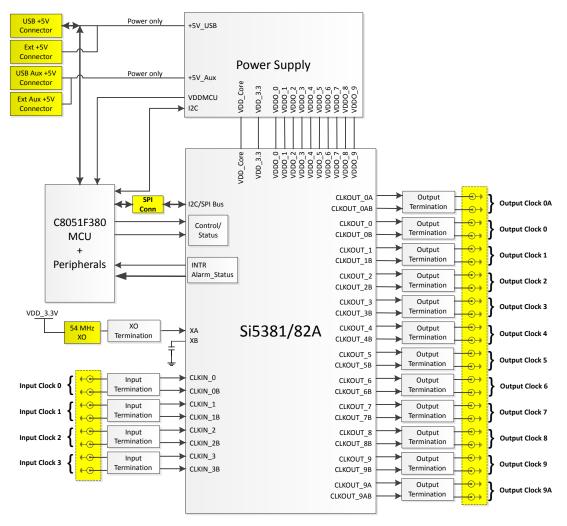


Figure 1.1. Functional Block Diagram of Si5381/82A-E-EB

UG 512: Si5381/82A-E Evaluation Board User's Guide • Quick Start and Jumper Defaults

# 2. Quick Start and Jumper Defaults

Perform the following steps to quick-start the ClockBuilder Pro software.

- 1. Download and install the ClockBuilder Pro desktop software.
- 2. Connect a USB cable from the Si5381/82A-E-EB to the PC where the software was installed.
- 3. Confirm jumpers are installed as shown in the table below.
- 4. Launch the ClockBuilder Pro Software.
- 5. You can use ClockBuilder Pro to create, download, and verify a frequency plan on the Si5381/82A-E-EB.
- 6. Download the Si5381/82 data sheet for more information.

The following table lists the Si5381/82A-E-EB jumper defaults.

Location	Туре	l = Installed O = Open	Location	Туре	l = Installed O = Open
JP1	2 pin	0	JP23	2 pin	0
JP2	2 pin	0	JP24	3 pin	all open
JP3	2 pin	0	JP25	2 pin	0
JP4	2 pin	I	JP26	3 pin	all open
JP5	2 pin	I	JP27	2 pin	0
JP6	2 pin	I	JP28	3 pin	all open
JP7	2 pin	I	JP29	2 pin	0
JP8	2 pin	0	JP30	3 pin	all open
JP9	2 pin	0	JP31	2 pin	0
JP13	2 pin	0	JP33	2 pin	0
JP14	2 pin	I	JP34	3 pin	all open
JP15	3 pin	1 to 2	JP35	2 pin	0
JP16	3 pin	1 to 2	JP36	3 pin	all open
JP17	2 pin	0	JP39	2 pin	0
JP18	3 pin	all open	JP40	2 pin	0
JP19	2 pin	0	JP41	2 pin	0
JP20	3 pin	all open	JP43	2 pin	I
JP21	2 pin	0			
JP22	3 pin	all open	J36	5x2 Hdr	All 5 installed

# 3. Status LEDs

Location	Silkscreen	Color	Status Function Indication
D11	INTRB	Blue	DUT Interrupt Active
D21	READY	Green	MCU Ready
D22	3P3V	Blue	DUT +3.3 V is present
D24	BUSY	Green	MCU Busy
D25	INTR	Red	MCU Interrupt active
D26	VDD DUT	Blue	DUT VDD voltage present
D27	5VUSBMAIN	Blue	Main USB +5 V present

#### Table 3.1. Si5381/82A-E-EVB Status LEDs

D27, D22, and D26 are illuminated when USB +5 V, Si5381/82 +3.3 V, and Si5381/82 Output +5 V supply voltages, respectively, are present. D25, D21, and D24 are status LEDs showing on-board MCU activity. D11 and D12 are status indicators from the DUT.

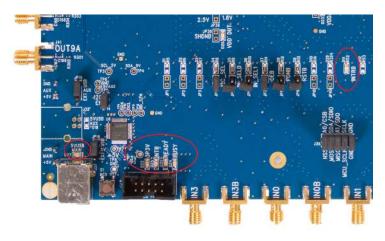


Figure 3.1. Status LEDs

UG 512: Si5381/82A-E Evaluation Board User's Guide • External Reference Input (XA/XB)

# 4. External Reference Input (XA/XB)

An external XO is used to produce an ultra-low jitter reference clock for the DSPLL and to provide a stable reference for the free-run and holdover modes. The XO footprint on the Si5381/82A-E-EVB can accommodate both 3.2mm x 5 mm and 2.5 mm x 3.2 mm package sizes. The XO frequency must be 54 MHz (recommended) or 48.0231 MHz for Si5381/82A devices.

When JP43 is shorted the XO shares the VDD\_3.3V DUT power supply sourced from an on-board ultra low noise LDO. When JP43 is left open an external supply must be used to power the XO. See section 9 for Si5381/82A-E-EVB schematic details.

**Note:** The remaining components marked "NI" are not installed.

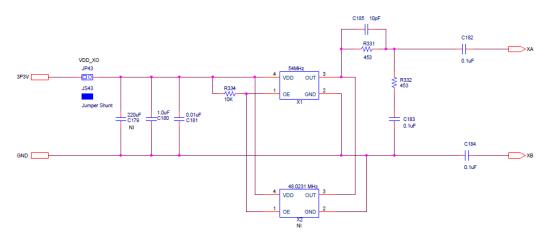


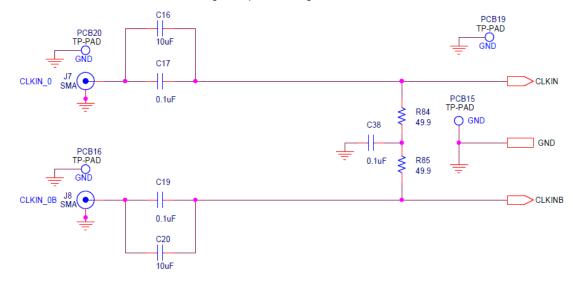
Figure 4.1. External Reference Input Circuit

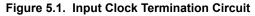
UG 512: Si5381/82A-E Evaluation Board User's Guide • Clock Input and Output Circuits

# 5. Clock Input and Output Circuits

#### 5.1 Clock Input Circuits (INx/INxB and FB\_IN/FB\_INB)

The Si5381/82A-E-EB has eight SMA connectors (IN0/IN0B–IN2/IN2B and IN3(FB\_IN)/IN3B(FB\_INB)) for receiving external clock signals. All input clocks are terminated as shown in the figure below. Note input clocks are ac coupled and 50  $\Omega$  terminated. This represents four differential input clock pairs. Single-ended clocks can be used by appropriately driving one side of the differential pair with a single-ended clock. For details on how to configure inputs as single-ended, refer to the Si5381/82 Data Sheet.





#### 5.2 Clock Output Circuits (OUTx/OUTxB)

Each of the twenty-four output drivers (12 differential pairs) is ac coupled to its respective SMA connector. The output clock termination circuit is shown in the figure below. The output signal will have no dc bias. If dc coupling is required, the ac coupling capacitors can be replaced with a resistor of appropriate value. The Si5381/82A-E-EB provides pads for optional output termination resistors and/or low frequency capacitors. Note that components with schematic "NI" designation are not normally populated on the Si5381/82A-E-EB, and provide locations on the PCB for optional dc/ac terminations by the end user.

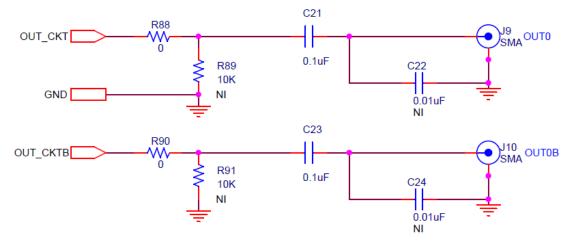


Figure 5.2. Output Clock Termination Circuit

# 6. Using the Si5381/82A-E-EVB and Installing ClockBuilder Pro Desktop Software

#### 6.1 Installing ClockBuilder Pro Desktop Software

To install the CBPro software on any Windows 7 (or above) PC:

Go to https://www.skyworksinc.com/en/application-pages/clockbuilder-pro-software and download the ClockBuilder Pro software.

Installation instructions, release notes, and a user's guide for ClockBuilder Pro can be found at the download link shown above. Follow the instructions as indicated.

#### 6.2 Connecting the EVB to Your Host PC

Once ClockBuilder Pro software in installed, connect to the EVB with a USB cable as shown below.

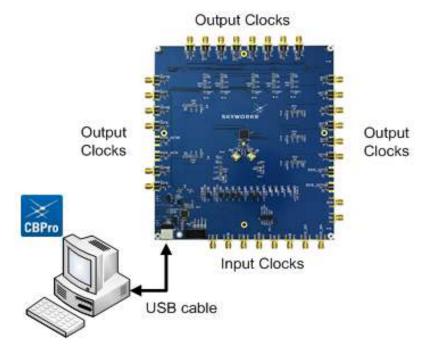


Figure 6.1. EVB Connection Diagram

#### 6.3 Additional Power Supplies

The Si5381/82A-E-EB comes preconfigured with jumpers installed on JP15 and JP16 (pins 1-2 in both cases) in order to select "USB". These jumpers, together with the components installed, configure the evaluation board to obtain +5 V power to all EVB power solely through the J37 USB connector. This setup is the default EVB configuration and is sufficient to configure the device and run multiple clock outputs simultaneously.

In some cases when enabling all outputs or at high output frequencies, the EVB requires more power than a single USB connection can provide. This may result in intermittent device behavior or undesired increases in jitter/phase-noise. This condition may be checked using the EVB GUI, which is described further below. Selecting the "**All Voltages**" tab of the GUI and clicking on the "**Read All**" button produces a display similar to this one:

nfo DUT SPI DUT Settin	ngs Editor	DUT Register Editor	Regulators	All Voltages	GPIO	Status Registers	- Control Registers
Voltage @ Regulator Pins	-		Voltage @				Soft Reset and Calibration
VDD_PIN	1.951 V	Read		VDD_REG	1.793 \	/ Read	SOFT_RST_ALL
VDDA_PIN	3.423 V	Read		VDDA_REG	3.300 \	/ Read	SOFT_RST
VDDO0_PIN	1.000 m	Read		VDDO0_REG	1.000 r	nV Read	
VDDO1_PIN	1.000 m <sup>1</sup>	Read		VDDO1_REG	1.000 r	nV Read	Hard Reset, Sync, & Power Dov
VDDO2_PIN	1.000 m	Read		VDDO2_REG	1.000 r	nV Read	HARD_RST
VDDO3_PIN	1.000 m <sup>v</sup>	V Read		VDDO3_REG	1.000 r	nV Read	SYNC
VDDO4_PIN	1.000 m	V Read		VDDO4_REG	1.000 r	nV Read	PDN: 0
VDDO5_PIN	1.000 m	V Read		VDDO5_REG	1.000 r	nV Read	PDN: U
VDDO6_PIN	1.000 m <sup>v</sup>	V Read		VDDO6_REG	1.000 r	nV Read	
VDD07_PIN	1.000 m <sup>v</sup>	V Read		VDD07_REG	1.000 r	nV Read	
VDDO8_PIN	1.000 m <sup>v</sup>	V Read		VDDO8_REG	1.000 r	nV Read	
VDDO9_PIN	1.000 m <sup>v</sup>	V Read		VDDO9_REG	1.000 r	nV Read	
Misc Rails RAIL_5V	4.924 V						
RAIL_3P3V	3.347 V	Read					
		Read					
g							
Itered 🔄 Auto Scroll	: On 🔽 🏾	Insert Marker	Clear	Copy to Clipbo	bard	Pause	
	Message						
:47:37.669 EVB	Finished Re	ad_ADC(num_samp	les=10) => 7	07.4			

Figure 6.2. EVB GUI - Power Supply Check

Verify that the "**RAIL\_5V**" measurement shows the EVB voltage > 4.5 V. An EVB voltage lower than this level may cause the issues described above.

In this case, J33 can be used to provide power to the output drivers separately from the main Si5381/82 device supplies. To make this change, move jumper JP15 to connect pins 2-3 "EXT". Connect J33 to an external 5 V, 0.5 A or higher power source. Make sure that the polarity of the +5 V and GND connections are correct. Verify that the RAIL\_5V voltage is 4.7 V or higher. The EVB should be powered by the USB connector when turning this auxiliary 5 V supply on or off.

See the figure below for the correct installation of the jumper shunts at JP15 and JP16 for default or standard operation.

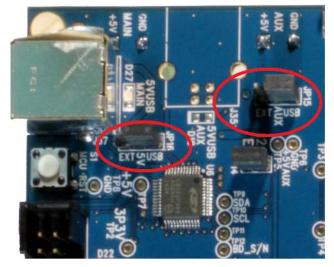


Figure 6.3. JP15-JP16 Standard Jumper Shunt Installation

#### 6.4 Overview of ClockBuilder Pro Applications

Note: The following instructions and screen captures may vary slightly depending on your version of ClockBuilder Pro.

The ClockBuilder Pro installer will install two main applications.

#### **Application 1:**

CB ClockBuilder Pro Wizard - Skyworks	– 🗆 X				
<ul> <li>ClockBuilder Pro Wizard</li> <li>We Make Timing Simple</li> </ul>	SKYWORKS				
Work With a Design	Quick Links				
Create New Project	Skyworks Timing Solutions Knowledge Base				
E Open Project	Custom Part Number Lookup				
Convert Existing Project/NVM File	Applications Documentation <u>10/40/100G Line Card Whitepaper</u>				
ex Open Sample Project	Clock Generators for Cloud Data Centers Optimizing SiS34x Jitter Performance				
Evaluation Board Detected Si5380A Rev D EVB Open Default Plan EVB GUI	Selecting the Right Clocks for Timing Synchronization Applications PCIe Gen 4.0 Jitter Requirements Selecting a PCIe Reference Clock Source Making Accurate Clock Jitter Measurements				
LELL TOPS UNK	ClockBuilder Pro Documentation				
	CBPro Overview CBPro Tools & Support for In-System Programming CLI User's Guide Release Notes				
0.	Version 4.1.5.100 Built on 11/15/2021				

Figure 6.4. ClockBuilder Pro Wizard

Use the CBPro Wizard to do the following:

- · Create a new design.
- · Review or edit an existing design.
- · Export: Create in-system programming files.

#### **Application 2:**

Help							
DUT SPI E	OUT Settings Editor	DUT Register Editor	Regulators	All Voltages	GPIO	Status Registers	Control Registers
VDD	1.80V	n 1.795 V	157 m	A 282	mW	Read	Soft Reset and Calibration
VDDA	3.30V	n 3.300 V	126 m	A 416	mW [	Read	SOFT_RST_ALL
VDDO0	1.80V	Off 0.001 V	0 m	A O	mW [	Read	SOFT_RST
VDDO1	1.80V	n 1.795 V	0 m	A O	mW [	Read	Hard Reset, Sync, & Power Do
VDDO2	1.80V	n 1.788 V	0 m	A 0	mW [	Read	HARD_RST
VDDO3	1.80V 🔽 🚺	n 1.795 V	0 m	A 0	mW [	Read	SYNC
VDDO4	1.80V 🔽 🚺	n 1.794 V	0 m	A O	mW [	Read	PDN: 0
VDDO5	1.80V 🔽 🚺	n 1.799 V	0 m	A O	mW	Read	
VDDO6	1.80V	n 1.786 V	0 m	A 0	mW [	Read	
VDD07	1.80V	n 1.787 V	0 m	A 0	mW [	Read	
VDDO8	1.80V	Off 0.001 V	0 m	A 0	mW [	Read	
VDDO9	1.80V	Off 0.001 V	0 m	A O	mW [	Read	
All Output	Select Voltage	Total	283 m	nA 0.698	w	Read All	
Supplies	Power On Po	wer Off Co	mpare Desigr	Estimates to	Measu	rements	
	uto Scroll: On 📘	Insert Marker	Clear	opy to Cli <mark>p</mark> b	oard	Pause	
nestamp Sou	rce Message						
50:18.319 EVB		leasure_Regulator(reg rrent: 0.000A, Power:	CONTRACTOR OF A CONTRACTOR	D_9) => Volt	ge_Reg	: 0.001V, Voltage_Pin:	A V

Figure 6.5. EVB GUI

Use the EVB GUI to do the following:

- Download configuration to EVB's DUT (Si5381/82).
- Control the EVB's regulators.
- · Monitor voltage, current, power on the EVB.

#### 6.5 Common ClockBuilder Pro Work Flow Scenarios

There are three common workflow scenarios when using CBPro and the Si5381/82A-E-EB. These workflow scenarios are:

- Workflow Scenario #1: Testing a Skyworks-created Default Configuration
- · Workflow Scenario #2: Modifying the Default Skyworks-created Device Configuration
- · Workflow Scenario #3: Testing a User-created Device Configuration

Each is described in more detail in the following sections.

#### 6.6 Workflow Scenario #1: Testing a Skyworks-Created Default Configuration

Verify that the PC and EVB are connected, then launch ClockBuilder Pro by clicking on this icon on your PC's desktop:



Figure 6.6. ClockBuilder Pro Icon

CBPro automatically detects the EVB and device type. When the EVB has been detected, click on the "Open Default Plan" button.

CB ClockB	Builder Pro Wizard - Skyworks
9 Q	<b>ClockBuilder Pro Wizard</b> We Make Timing Simple
Work	With a Design
[ò 🤇	Create New Project
	<u>Open Project</u>
	Convert Existing Project/NVM File
ex 🤇	Open Sample Project
ामा	Evaluation Board Detected Si5380A Rev D EVB Open Default Plan EVB GUI

Figure 6.7. CBPro—Open Default Plan Button

Once you open the default plan, a popup will appear.

CB Clo	ckBuilder Pro v4.1.5.100	_		×
A	Write Design to EVB?			
	The EVB may be out-of-sync with your design. Would your design to the EVB?	d you lil	ke to wr	ite
	Yes No			

Figure 6.8. CBPro—Write Design Dialog

Select "Yes" to write the default plan to the Si5381/82 device mounted on your EVB. This ensures the device on the EVB is configured with the latest parameters from Skyworks.

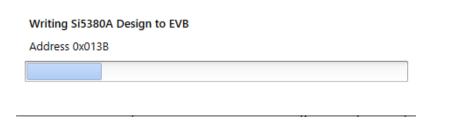


Figure 6.9. CBPro—Write Progress Window

After CBPro writes the default plan to the EVB, click on "Open EVB GUI" as shown in the figure below.

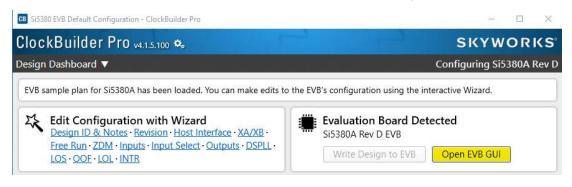


Figure 6.10. CBPro—Open EVB GUI Button

The EVB GUI window will appear on the desktop. Note all power supplies on the "**Regulators**" tab will be set to the values defined in the device's default CBPro project, as shown in the figure below.

CB Si5380A Rev D EVB - ClockBuilder Pro									
File Help									
Info DUT SPI E	OUT Settings Editor	DUT Regist	er Editor	Regulators	All Voltages	GPIO	Status Registers		
VDD	1.80V	n	1.795 V	157 r	mA 282 i	mW	Read		
VDDA	3.30V	n	3.300 V	126 r	mA 416 i	mW 🗌	Read		
VDDO0	1.80V	Off	0.001 V	0 r	mA 0ı	mW 🗌	Read		
VDD01	2.50V 🔽 🖸	n	1.795 V	0 r	mA 0ı	mW 🗌	Read		
VDDO2	2.50V 🔽 🖸	n	1.788 V	0 r	mA 0ı	mW 🗌	Read		
VDDO3	2.50V 🔽 🖸	n	1.795 V	0 r	mA 0ı	mW 🗌	Read		
VDDO4	2.50V 🔽 🖸	n	1.794 V	0 r	mA 0ı	mW 🗌	Read		
VDDO5	2.50V 🔽 🖸	n	1.799 V	0 r	mA 0ı	mW 🗌	Read		
VDDO6	2.50V	n	1.786 V	0 r	mA 0ı	mW 🗌	Read		
VDD07	2.50V	n	1.787 V	0 r	mA 0ı	mW 🗌	Read		
VDDO8	2.50V 🔽 🖸	n	0.001 V	0 r	mA 0ı	mW 🗌	Read		
VDDO9	1.80V	Off	0.001 V	0 r	mA 0ı	mW 🗌	Read		
All Output	Select Voltage		Total	283 r	mA 0.698	w	Read All		
Supplies	Power On Po	wer Off	Co	mpare Desig	n Estimates to	Measu	rements		

Figure 6.11. EVB GUI—Regulators

#### 6.6.1 Verify Free-Run Mode Operation

Assuming no external clocks have yet been connected to the INPUT CLOCK differential SMA connectors, labeled "INx/INxB" and located around the perimeter of the EVB, the DUT should now be operating in free-run mode and locked to the onboard XO.

You can run a quick check to determine if the device is powered up, generating output clocks, and consuming power by clicking on the "**Read All**" button highlighted above and then reviewing the voltage, current and power readings for each VDDx supply.

**Note:** Turning  $V_{DD}$  or  $V_{DDA}$  "Off" will power-down and reset the DUT. Once both of these supplies are turned "On" again, you must reload the desired frequency plan back into the device memory by selecting the "**Write Design to EVB**" button on the CBPro home screen:

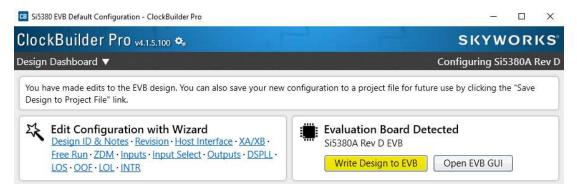


Figure 6.12. CBPro—Write Design Button

Failure to do the step above will cause the device to read in the preprogrammed plan from its non-volatile memory (NVM). However, the plan loaded from the NVM may not be the latest plan recommended by Skyworks for evaluation.

At this point, you should verify the presence and frequencies of the output clocks, running in free-run mode from the XO, using external instrumentation connected to the output clock SMA connectors, labeled OUTx/OUTs. To verify plan inputs, go to the appropriate configuration page or click on "Frequency Plan Valid" to see the design report.

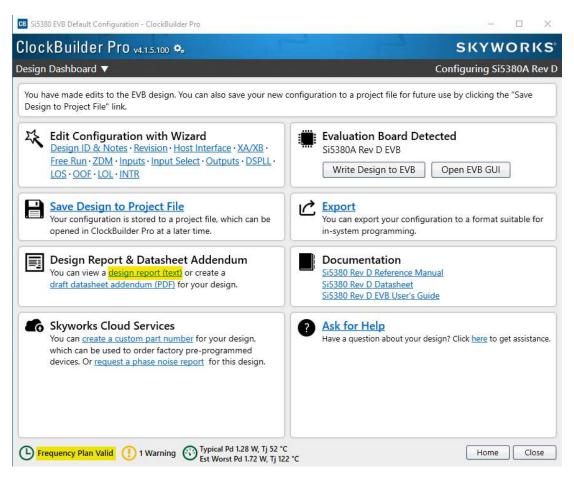


Figure 6.13. CBPro—Design Report Button and Link

Your configuration's design report will appear in a new window, as shown below. Compare the observed output clocks to the frequencies and formats noted in your default project's Design Report.

CB Si5380A D	Design Report	_		×
Design Rep	ort			
54 MH	z (XO - External Oscillator)			
Inputs:				_
· · · ·	30.72 MHz			
	Standard			
IN1:	61.44 MHz			
	Standard			
IN2:	122.88 MHz			
	Standard			
IN3:	245.76 MHz			
	Standard			
Outputs:				
	Unused			
OUTØ:	Unused			
OUT1:	122.88 MHz			
	Enabled, LVDS 2.5 V			
OUT2:	245.76 MHz			
	Enabled, LVDS 2.5 V			
OUT3:	491.52 MHz			
	Enabled, LVDS 2.5 V			
OUT4:	983.04 MHz			
	Enabled, LVDS 2.5 V			
OUT5:	7.68 MHz			
	Enabled, LVDS 2.5 V			
OUT6:	7.68 MHz			
	Enabled, LVDS 2.5 V			
OUT7:	1.2288 GHz			
	Enabled, LVDS 2.5 V			
OUT8:	1.47456 GHz			
	Enabled, LVDS 2.5 V			
	Unused			
OUT9A:	Unused			
Frequenc				
Fvco = 1	4.7456 GHz			w
Copy to C	lipboard Save Report Ask for Help		Clos	se

Figure 6.14. CBPro—Design Report

#### 6.6.2 Verify Locked Mode Operation

Now, assuming that you connect the input clocks to the EVB as shown in the Design Report above, the DUT on your EVB will be running in "locked" mode.

#### 6.7 Workflow Scenario #2: Modifying the Default Skyworks-Created Device Configuration

To modify the configuration using the CBPro Wizard, click on the appropriate category. The category may also be selected from a dropdown list by clicking on the "**Design Dashboard**" button above this section.

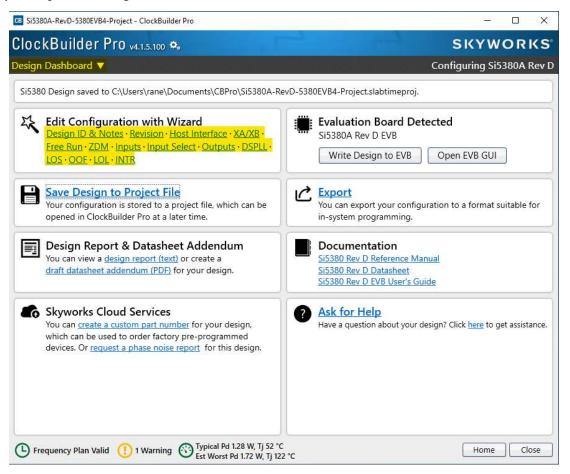


Figure 6.15. CBPro—Edit Settings Links and Pulldown

You will now be taken to the Wizard's step-by-step menu pages to allow you to change any of the default plan's operating configurations.

313500A-RevD-350	0EVB4-Project - ClockBuilder Pro	-		×
lockBuild	er Pro v4.1.5.100 🎭	SKYW	/OR	ĸs
ep 1 of 14 - De	sign ID & Notes ▼	Configuring Si	5380A	Rev
D <b>esign ID</b> The device has 8 re Design ID:	egisters, DESIGN_ID0 through DESIGN_ID7, that can be used to store a design/configuration/rev 5380EVB4 (optional; max 8 characters) The string you enter here is stored as ASCII bytes in registers DESIGN_ID0 through DESIGN_II			
Padding Mode:	<ul> <li>NULL Padded         If you do not enter the full 8 characters, the remaining bytes of DESIGN_IDx will be padd character).         </li> <li>Space Padded         If you do not enter the full 8 characters, the remaining bytes of DESIGN_IDx will be padd character).     </li> </ul>			
While the text is w This sample pl	i want here. The text is stored in your project file and included in design reports and custom pai ord wrapped in reports, you can use newlines to start a new paragraph. an for the S15380 demonstrates performance over a wide range of output frequ utput frequencies from 122.88 MHz to 1.47456 GHz are included, though there	encies. A number	of com	
	uts are set up as low frequency 7.68 MHz SYSREF outputs with independently a our independent skew adjusts are available for controlling Device Clock to S lications.			204B

Figure 6.16. CBPro—Design ID and Notes Edit Page

As you edit the settings, you may notice the "Frequency Plan Valid" link in the lower left corner updating. You can click on this link to bring up the design report to confirm that the information is correct. When you are finished editing each page, you may click on the "> Next" or "< Back" buttons to move from page to page. When you are done making all your desired changes, you can click on "Write to EVB" to reconfigure your device. The Design Write status window will appear each time you write to the EVB.



Figure 6.17. CBPro—Design Write Progress Window

When you have verified your design settings, you may save the design project. Click on the "**Finish**" button to return to the home page and then click on the "**Save Design to Project File**" link. You can use the windows file browser to reach the correct location and enter a filename for this new project.

#### 6.8 Workflow Scenario #3: Testing a User-Created Device Configuration

CB ClockBuilder Pro Wizard - Skyworks	- 🗆 X
<ul> <li>ClockBuilder Pro Wizard</li> <li>We Make Timing Simple</li> </ul>	SKYWORKS
Work With a Design	Quick Links
Create New Project	Skyworks Timing Solutions Knowledge Base
🖶 <mark>Open Project</mark>	Custom Part Number Lookup
Convert Existing Project/NVM File	Applications Documentation
ex Open Sample Project	Clock Generators for Cloud Data Centers Optimizing Si534x Jitter Performance Selecting the Right Clocks for Timing Synchronization
Evaluation Board Detected Si5380A Rev D EVB Open Default Plan EVB GUI	Applications PCle Gen 4.0 Jitter Requirements Selecting a PCle Reference Clock Source Making Accurate Clock Jitter Measurements
Antonio 12 - 21 million	ClockBuilder Pro Documentation
	CBPro Overview CBPro Tools & Support for In-System Programming CLI User's Guide Release Notes
۵.	Version 4.1.5.100 Built on 11/15/2021

Figure 6.18. CBPro—Open Design Project Link

Using the windows file browser popup, locate your CBPro design file (\*.slabtimeproj or \*.sitproj file).

→ · · · · · · · · · · · · · · · · · · ·	ٽ ~	Search CBPro	م التحقيق Size . 12 KB
Organize 🔻 New folder			• 🔳 (
OneDrive - Person Name	Date modified	Туре	Size
This PC	1/6/2022 3:57 PM	Skyworks Timing	12 KB
3D Objects			
🦲 Desktop			
🛱 Documents 💙			
		<ul> <li>Skyworks Timing P</li> </ul>	roiect

Figure 6.19. CBPro—Windows File Browser

Select "Yes" when the WRITE DESIGN to EVB popup appears:

CB Clo	ckBuilder Pro v4.1.5.100	—		×
A	Write Design to EVB?			
	The EVB may be out-of-sync with your design. Would your design to the EVB?	l you lik	e to writ	te
	Yes No			

Figure 6.20. CBPro—Write Design Dialog

The progress bar will be launched. Once the new design project file has been written to the device, verify the presence and frequencies of your output clocks and other operating configurations using external instrumentation.

#### 6.9 Exporting the Register Map File for Device Programming by a Host Processor

You can also export your configuration to a file format suitable for in-system programming by selecting "Export" as shown below:

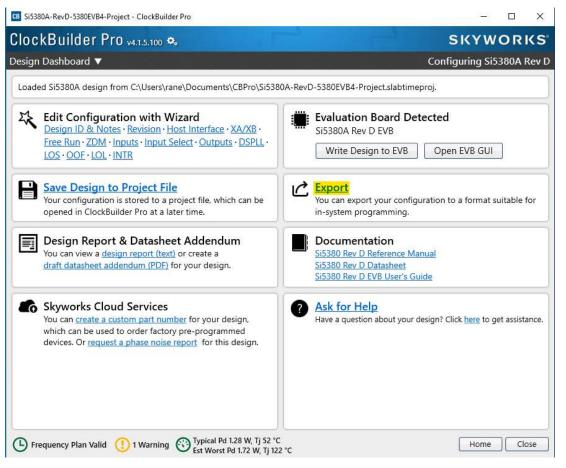


Figure 6.21. CBPro—Export Design Programming File

You can now write your device's complete configuration to file formats suitable for in-system programming.

Register File	Settings File	Multi-Project Register/Settings	Regmap		
ster Export					
	e registers that	t need to be written to the Si538	80A to achieve	your desig	n/
l line version o		vailable. Type CBProProjectRegi	stersExportI	nelp from a	1
2:					
line in the file i lata fields.			A comma sepa	arates the a	address
egister write se directly in firm	ware code.	ressed in C code via an array of	address,data p	oairs. This c	an be
ed, an informa	tional header				
control registe sures the device nload is comp	rs must be wri e is stable duri	tten before and after writing the ng configuration download and	l resumes norn	nal operation	on after
	ster Export will contain the on. d line version o prompt to learn ma Separated V line in the file i lata fields. de Header File egister write se directly in firm summary head ed, an informa I by the # char. camp. pre- and post- control registe sures the device mload is comp	ster Export will contain the registers that on. d line version of this tool is ave prompt to learn more. as ma Separated Values (CSV) Fi- line in the file is an address, d lata fields. de Header File egister write sequence is exp directly in firmware code. summary header ed, an informational header of by the # character. The head samp. pre- and post-write control r control registers must be wri- sures the device is stable duri vnload is complete. You can t	ster Export will contain the registers that need to be written to the Si534 on. d line version of this tool is available. Type CBProProjectRegi prompt to learn more. e: ma Separated Values (CSV) File line in the file is an address,data pair in hexadecimal format. lata fields. de Header File egister write sequence is expressed in C code via an array of directly in firmware code. summary header ed, an informational header will be included at the top of the l by the # character. The header will contain some basic infor tamp. pre- and post-write control register writes control registers must be written before and after writing the sures the device is stable during configuration download and whoad is complete. You can turn inclusion of this sequence of the sequence of the	ster Export will contain the registers that need to be written to the Si5380A to achieve on. d line version of this tool is available. Type CBProProjectRegistersExportI brompt to learn more. e: ma Separated Values (CSV) File line in the file is an address,data pair in hexadecimal format. A comma sepa lata fields. de Header File egister write sequence is expressed in C code via an array of address,data p directly in firmware code. summary header ed, an informational header will be included at the top of the file. Each line I by the # character. The header will contain some basic information about tamp. pre- and post-write control register writes control registers must be written before and after writing the volatile confi- sures the device is stable during configuration download and resumes norm whoad is complete. You can turn inclusion of this sequence off if your host if	ster Export will contain the registers that need to be written to the Si5380A to achieve your desig on. d line version of this tool is available. Type CBProProjectRegistersExporthelp from a borompt to learn more. e: ma Separated Values (CSV) File line in the file is an address,data pair in hexadecimal format. A comma separates the a lata fields. de Header File egister write sequence is expressed in C code via an array of address,data pairs. This c directly in firmware code. summary header ed, an informational header will be included at the top of the file. Each line in the heal I by the # character. The header will contain some basic information about the design tamp.

Figure 6.22. CBPro—Export Configuration Window

UG 512: Si5381/82A-E Evaluation Board User's Guide • Writing A New Frequency Plan or Device Configuration to Non-volatile Memory (OTP)

# 7. Writing A New Frequency Plan or Device Configuration to Non-volatile Memory (OTP)

The Si5381/82 device loads the Non-Volatile Memory (OTP) on either a powerup or a hard reset, overwriting any previous volatile register changes. This allows the device to begin functioning as desired on powerup/hard-reset without manual intervention. To restart the device while preserving volatile changes and without loading the OTP, use soft-reset through the registers or EVB-GUI.

**Note:** Writing to the device non-volatile memory (OTP) is NOT the same as writing a configuration into the Si5381/82 using ClockBuilder Pro on the Si5381/82A-E-EB. Writing a configuration into the EVB from ClockBuilder Pro is done using Si5381/82 RAM space and can be done virtually an unlimited number of times. Writing to OTP is limited as described below.

Refer to the Si5381/82 Family Reference Manual and device datasheet for information on how to write a configuration to the EVB DUT's non-volatile memory (OTP). The OTP can be programmed a maximum of **two** times only. Care must be taken to ensure the configuration desired is valid when choosing to write to OTP.

UG 512: Si5381/82A-E Evaluation Board User's Guide • Serial Device Communications (Si5381/82 <-> MCU)

# 8. Serial Device Communications (Si5381/82 <-> MCU)

#### 8.1 Onboard SPI Support

The MCU on-board the Si5381/82A-E-EB communicates with the Si5381/82 device through a 4-wire SPI (Serial Peripheral Interface) link. The MCU is the SPI master and the Si5381/82 device is the SPI slave. The Si5381/82 device can also support a 2-wire I<sup>2</sup>C serial interface, although the Si5381/82A-E-EB does NOT support the I<sup>2</sup>C mode of operation. SPI mode was chosen for the EVB because of the relatively higher speed transfers supported by SPI vs. I<sup>2</sup>C.

#### 8.2 External I<sup>2</sup>C Support

I<sup>2</sup>C can be supported if driven from an external I<sup>2</sup>C controller. The serial interface signals between the MCU and Si5381/82 pass through shunts loaded on header J36. These jumper shunts must be installed in J36 for normal EVB operation using SPI with CBPro. If testing of I<sup>2</sup>C operation via external controller is desired, the shunts in J36 can be removed thereby isolating the on-board MCU from the Si5381/82 device. The shunt at J4 (I2C\_SEL) must also be removed to select I<sup>2</sup>C as Si5381/82 interface type. An external I<sup>2</sup>C controller connected to the Si5381/82 side of J36 can then communicate to the Si5381/82 device. (For more information on I<sup>2</sup>C signal protocol, refer to the Si5381/82 Data Sheet.)

The figure below illustrates the J36 header schematic. J36 even numbered pins (2, 4, 6, etc.) connect to the Si5381/82 device and the odd numbered pins (1, 3, 5, etc.) connect to the MCU. Once the jumper shunts have been removed from J36 and J4,  $I^{2}C$  operation should use J36 pin 4 (DUT\_SDA\_SDIO) as the  $I^{2}C$  SDA and J36 pin 8 (DUT\_SCLK) as the  $I^{2}C$  SCLK. Please note the external  $I^{2}C$  controller will need to supply its own  $I^{2}C$  signal pull-up resistors.

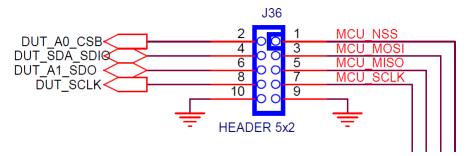


Figure 8.1. Serial Communications Header J36

UG 512: Si5381/82A-E Evaluation Board User's Guide • Si5381/82-E-EB Schematic and Bill of Materials (BOM)

# 9. Si5381/82-E-EB Schematic and Bill of Materials (BOM)

The Si5381/82-E-EB Schematic and Bill of Materials (BOM) can be found online at: https://www.skyworksinc.com/search? g=si538%20evaluation

Note: Please be aware the Si5381/82-E-EB schematic is in OrCad Capture hierarchical format and not in a typical "flat" schematic format.

# SKYWORKS

# **ClockBuilder Pro**

Customize Skyworks clock generators, jitter attenuators and network synchronizers with a single tool. With CBPro you can control evaluation boards, access documentation, request a custom part number, export for in-system programming and more!

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