CY7C1345G

4-Mbit (128K x 36) Flow Through Sync SRAM

Features

- 128K x 36 common IO
- 3.3V core power supply (V_{DD})
- 2.5V or 3.3V IO supply (V_{DDQ})
- Fast clock-to-output times
  - 6.5 ns (133 MHz version)
- Provide high performance 2-1-1-1 access rate
- User selectable burst counter supporting Intel Pentium interleaved or linear burst sequences
- Separate processor and controller address strobes
- Synchronous self-timed write
- Asynchronous output enable
- Available in Pb-free 100-Pin TQFP package, Pb-free and non-Pb-free 119-Ball BGA package
- ZZ Sleep Mode option

Functional Description

The CY7C1345G is a 128K x 36 synchronous cache RAM designed to interface with high speed microprocessors with minimum glue logic. The maximum access delay from clock rise is 6.5 ns (133 MHz version). A two-bit on-chip counter captures the first address in a burst and increments the address automatically for the rest of the burst access. All synchronous inputs are gated by registers controlled by a positive edge triggered Clock Input (CLK). The synchronous inputs include all addresses, all data inputs, address pipelining Chip Enable ($\overline{CE_1}$), depth expansion Chip Enables (CE_2 and $\overline{CE_3}$), Burst Control inputs ($\overline{ADSC}$, $\overline{ADSP}$, and $\overline{ADV}$), Write Enables ($\overline{BW_x}$, and $\overline{BWE}$), and Global Write ($\overline{GW}$). Asynchronous inputs include the Output Enable ($\overline{OE}$) and the ZZ pin.

The CY7C1345G enables either interleaved or linear burst sequences, selected by the MODE input pin. A HIGH selects an interleaved burst sequence, while a LOW selects a linear burst sequence. Burst accesses are initiated with the Processor Address Strobe ($\overline{ADSP}$) or the cache Controller Address Strobe ($\overline{ADSC}$) inputs.

Addresses and chip enables are registered at rising edge of clock when either Address Strobe Processor ($\overline{ADSP}$) or Address Strobe Controller ($\overline{ADSC}$) is active. Subsequent burst addresses are internally generated as controlled by the Advance pin ($\overline{ADV}$).

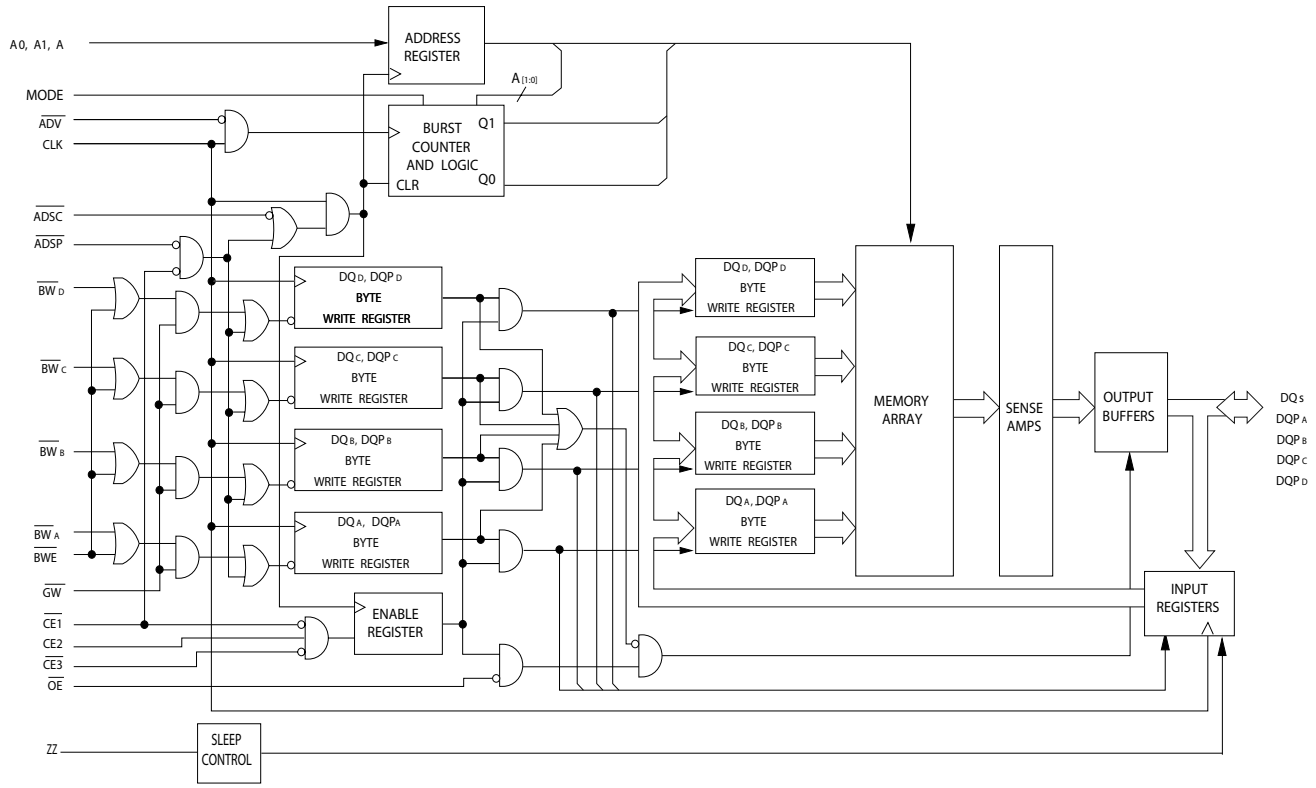
The CY7C1345G operates from a +3.3V core power supply while all outputs operate with either a +2.5 or +3.3V supply. All inputs and outputs are JEDEC standard JESD8-5 compatible.

For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines.

Selection Guide

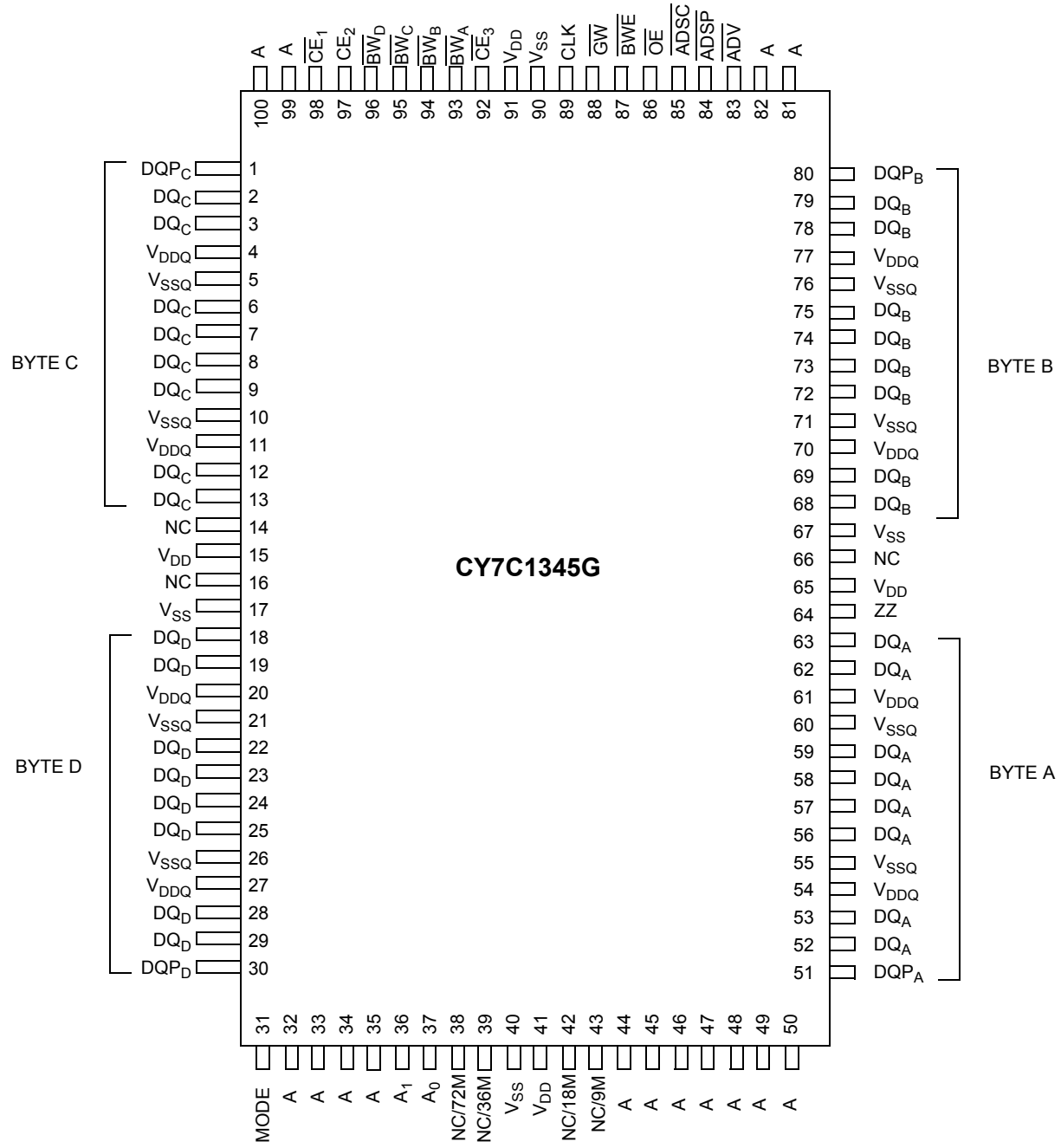
Parameter	133 MHz	100 MHz	Unit
Maximum Access Time	6.5	8.0	ns
Maximum Operating Current	225	205	mA
Maximum Standby Current	40	40	mA

Logic Block Diagram



Pin Configurations

100-Pin TQFP Pinout



Pin Configurations (continued)

119-Ball BGA Pinout

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	$\overline{ADSP}$	A	A	V_{DDQ}
B	NC/288M	CE_2	A	$\overline{ADSC}$	A	$\overline{CE}_3$	NC/576M
C	NC/144M	A	A	V_{DD}	A	A	NC/1G
D	DQ_C	DQP_C	V_{SS}	NC	V_{SS}	DQP_B	DQ_B
E	DQ_C	DQ_C	V_{SS}	$\overline{CE}_1$	V_{SS}	DQ_B	DQ_B
F	V_{DDQ}	DQ_C	V_{SS}	$\overline{OE}$	V_{SS}	DQ_B	V_{DDQ}
G	DQ_C	DQ_C	$\overline{BW}_C$	$\overline{ADV}$	$\overline{BW}_B$	DQ_B	DQ_B
H	DQ_C	DQ_C	V_{SS}	$\overline{GW}$	V_{SS}	DQ_B	DQ_B
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	DQ_D	DQ_D	V_{SS}	CLK	V_{SS}	DQ_A	DQ_A
L	DQ_D	DQ_D	$\overline{BW}_D$	NC	$\overline{BW}_A$	DQ_A	DQ_A
M	V_{DDQ}	DQ_D	V_{SS}	$\overline{BWE}$	V_{SS}	DQ_A	V_{DDQ}
N	DQ_D	DQ_D	V_{SS}	A1	V_{SS}	DQ_A	DQ_A
P	DQ_D	DQP_D	V_{SS}	A0	V_{SS}	DQP_A	DQ_A
R	NC	A	MODE	V_{DD}	NC	A	NC
T	NC	NC/72M	A	A	A	NC/36M	ZZ
U	V_{DDQ}	NC	NC	NC	NC	NC	V_{DDQ}

Pin Definitions

Name	IO	Description
A0, A1, A	Input Synchronous	**Address Inputs Used to Select One of the 128K Address Locations**. Sampled at the rising edge of the CLK if $\overline{ADSP}$ or $\overline{ADSC}$ is active LOW, and $\overline{CE}_1$, CE_2, and $\overline{CE}_3$ are sampled active. $A_{[1:0]}$ feed the two-bit counter.
$\overline{BW}_A$, $\overline{BW}_B$ $\overline{BW}_C$, $\overline{BW}_D$	Input Synchronous	**Byte Write Select Inputs, Active LOW**. Qualified with $\overline{BWE}$ to conduct byte writes to the SRAM. Sampled on the rising edge of CLK.
$\overline{GW}$	Input Synchronous	**Global Write Enable Input, Active LOW**. When asserted LOW on the rising edge of CLK, a global write is conducted (ALL bytes are written, regardless of the values on $\overline{BW}_{[A:D]}$ and $\overline{BWE}$).
$\overline{BWE}$	Input Synchronous	**Byte Write Enable Input, Active LOW**. Sampled on the rising edge of CLK. This signal is asserted LOW to conduct a byte write.
CLK	Input Clock	**Clock Input**. Used to capture all synchronous inputs to the device. Also used to increment the burst counter when ADV is asserted LOW, during a burst operation.
$\overline{CE}_1$	Input Synchronous	**Chip Enable 1 Input, Active LOW**. Sampled on the rising edge of CLK. Used in conjunction with CE_2 and $\overline{CE}_3$ to select or deselect the device. ADSP is ignored if $\overline{CE}_1$ is HIGH. $\overline{CE}_1$ is sampled only when a new external address is loaded.
CE_2	Input Synchronous	**Chip Enable 2 Input, Active HIGH**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $\overline{CE}_3$ to select or deselect the device. CE_2 is sampled only when a new external address is loaded.
$\overline{CE}_3$	Input Synchronous	**Chip Enable 3 Input, Active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and CE_2 to select or deselect the device. $\overline{CE}_3$ is sampled only when a new external address is loaded.
$\overline{OE}$	Input Asynchronous	**Output Enable, asynchronous Input, Active LOW**. Controls the direction of the IO pins. When LOW, the IO pins act as outputs. When deasserted HIGH, IO pins are tri-stated and act as input data pins. $\overline{OE}$ is masked during the first clock of a read cycle when emerging from a deselected state.
$\overline{ADV}$	Input Synchronous	**Advance Input Signal,** Sampled on the Rising Edge of CLK. When asserted, it automatically increments the address in a burst cycle.
$\overline{ADSP}$	Input Synchronous	**Address Strobe from Processor, sampled on the rising edge of CLK, Active LOW**. When asserted LOW, addresses presented to the device are captured in the address registers. $A_{[1:0]}$ are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized. ASDP is ignored when $\overline{CE}_1$ is deasserted HIGH.
$\overline{ADSC}$	Input Synchronous	**Address Strobe from Controller, sampled on the rising edge of CLK, Active LOW**. When asserted LOW, addresses presented to the device are captured in the address registers. $A_{[1:0]}$ are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized.
ZZ	Input Asynchronous	**ZZ sleep Input, Active HIGH**. When asserted HIGH places the device in a non-time critical sleep condition with data integrity preserved. During normal operation, this pin is low or left floating. ZZ pin has an internal pull down.
DQs DQP_A, DQP_B DQP_C, DQP_D	IO Synchronous	**Bidirectional Data IO lines**. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by the addresses presented during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$. When $\overline{OE}$ is asserted LOW, the pins act as outputs. When HIGH, DQs and $DQP_{[A:D]}$ are placed in a tri-state condition.
V_{DD}	Power Supply	**Power supply inputs to the core of the device**.
V_{SS}	Ground	**Ground for the core of the device**.
V_{DDQ}	IO Power Supply	**Power supply for the IO circuitry**.
V_{SSQ}	IO Ground	**Ground for the IO circuitry**.

Pin Definitions (continued)

Name	IO	Description
MODE	Input Static	**Selects Burst Order**. When tied to GND selects linear burst sequence. When tied to V_{DD} or left floating selects interleaved burst sequence. This is a strap pin and must remain static during device operation. Mode Pin has an internal pull up.
NC		**No Connects**. Not Internally connected to the die.
NC/9M, NC/18M, NC/36M NC/72M, NC/144M, NC/288M, NC/576M, NC/1G	–	**No Connects**. Not internally connected to the die. NC/9M, NC/18M, NC/36M, NC/72M, NC/144M, NC/288M, NC/576M, and NC/1G are address expansion pins and are not internally connected to the die.

Functional Overview

All synchronous inputs pass through input registers controlled by the rising edge of the clock. Maximum access delay from the clock rise (t_{CO}) is 6.5 ns (133 MHz device).

The CY7C1345G supports secondary cache in systems using either a linear or interleaved burst sequence. The interleaved burst order supports Pentium and i486™ processors. The linear burst sequence is suited for processors that use a linear burst sequence. The burst order is user selectable and is determined by sampling the MODE input. Accesses are initiated with either the Processor Address Strobe ($\overline{ADSP}$) or the Controller Address Strobe ($\overline{ADSC}$). Address advancement through the burst sequence is controlled by the $\overline{ADV}$ input. A two-bit on-chip wrap around burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

Byte write operations are qualified with the Byte Write Enable ($\overline{BWE}$) and Byte Write Select ($\overline{BW}_{[A:D]}$) inputs. A Global Write Enable ($\overline{GW}$) overrides all byte write inputs and writes data to all four bytes. All writes are simplified with on-chip synchronous self-timed write circuitry.

Three synchronous Chip Selects ($\overline{CE}_1$, CE_2, and $\overline{CE}_3$) and an asynchronous Output Enable ($\overline{OE}$) provide for easy bank selection and output tri-state control. $\overline{ADSP}$ is ignored if $\overline{CE}_1$ is HIGH.

Single Read Accesses

A single read access is initiated when the following conditions are satisfied at clock rise:

1. $\overline{CE}_1$, CE_2, and $\overline{CE}_3$ are all asserted active.
2. $\overline{ADSP}$ or $\overline{ADSC}$ is asserted LOW (if the access is initiated by $\overline{ADSC}$, the write inputs are deasserted during this first cycle).

The address presented to the address inputs is latched into the address register and the burst counter or control logic and presented to the memory core. If the $\overline{OE}$ input is asserted LOW, the requested data is available at the data outputs a maximum to t_{CDV} after clock rise. $\overline{ADSP}$ is ignored if $\overline{CE}_1$ is HIGH.

Single Write Accesses Initiated by $\overline{ADSP}$

Single write access is initiated when the following conditions are satisfied at clock rise:

1. $\overline{CE}_1$, CE_2, and $\overline{CE}_3$ are all asserted active
2. $\overline{ADSP}$ is asserted LOW.

The addresses presented are loaded into the address register and the burst inputs ($\overline{GW}$, $\overline{BWE}$, and $\overline{BW}_x$) are ignored during this first clock cycle. If the write inputs are asserted active (see **Write Cycle Descriptions table** for appropriate states that indicate a write) on the next clock rise, the appropriate data is latched and written into the device. Byte writes are allowed. During byte writes, $\overline{BW}_A$ controls DQ_A and $\overline{BW}_B$ controls DQ_B, BW_C controls DQ_C, and $\overline{BW}_D$ controls DQ_D. All IOs are tri-stated during a byte write. Since this is a common IO device, the asynchronous $\overline{OE}$ input signal is deasserted and the IOs are tri-stated prior to the presentation of data to DQ_s. As a safety precaution, the data lines are tri-stated once a write cycle is detected, regardless of the state of $\overline{OE}$.

Single Write Accesses Initiated by ADSC

This write access is initiated when the following conditions are satisfied at clock rise:

1. $\overline{CE}_1$, CE_2, and $\overline{CE}_3$ are all asserted active.
2. $\overline{ADSC}$ is asserted LOW.
3. $\overline{ADSP}$ is deasserted HIGH
4. The write input signals ($\overline{GW}$, $\overline{BWE}$, and $\overline{BW}_x$) indicate a write access. $\overline{ADSC}$ is ignored if $\overline{ADSP}$ is active LOW.

The addresses presented are loaded into the address register and the burst counter or control logic and delivered to the memory core. The information presented to $DQ_{[D:A]}$ is written into the specified address location. Byte writes are allowed. During byte writes, $\overline{BW}_A$ controls DQ_A, $\overline{BW}_B$ controls DQ_B, $\overline{BW}_C$ controls DQ_C, and $\overline{BW}_D$ controls DQ_D. All IOs and even a byte write are tri-stated when a write is detected. Since this is a common IO device, the asynchronous $\overline{OE}$ input signal is deasserted and the IOs are tri-stated prior to the presentation of data to DQs. As a safety precaution, the data lines are tri-stated once a write cycle is detected, regardless of the state of $\overline{OE}$.

Burst Sequences

The CY7C1345G provides an on-chip two-bit wrap around burst counter inside the SRAM. The burst counter is fed by $A_{[1:0]}$ and follows either a linear or interleaved burst order. The burst order is determined by the state of the MODE input. A LOW on MODE selects a linear burst sequence. A HIGH on MODE selects an interleaved burst order. Leaving MODE unconnected causes the device to default to a interleaved burst sequence.

Table 1. Interleaved Burst Address Table (MODE = Floating or V_{DD})

First Address A1, A0	Second Address A1, A0	Third Address A1, A0	Fourth Address A1, A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Table 2. Linear Burst Address Table (MODE = GND)

First Address A_1, A_0	Second Address A_1, A_0	Third Address A_1, A_0	Fourth Address A_1, A_0
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation sleep mode. Two clock cycles are required to enter into or exit from this sleep mode. In this mode, data integrity is guaranteed. Accesses pending when entering the sleep mode are not considered valid nor is the completion of the operation guaranteed. The device is deselected prior to entering the sleep mode. CEs, ADSP, and ADSC must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min	Max	Unit
I_{DDZZ}	Sleep mode standby current	ZZ $\geq V_{DD} - 0.2V$		40	mA
t_{ZZS}	Device operation to ZZ	ZZ $\geq V_{DD} - 0.2V$		$2t_{CYC}$	ns
t_{ZZREC}	ZZ recovery time	ZZ $\leq 0.2V$	$2t_{CYC}$		ns
t_{ZZI}	ZZ Active to sleep current	This parameter is sampled		$2t_{CYC}$	ns
t_{RZZI}	ZZ Inactive to exit sleep current	This parameter is sampled	0		ns

Truth Table

The truth table for CY7C1345G follows. [1, 2, 3, 4, 5]

Cycle Description	Address Used	$\overline{CE_1}$	CE_2	$\overline{CE_3}$	ZZ	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselected Cycle, Power down	None	H	X	X	L	X	L	X	X	X	L-H	Tri-State
Deselected Cycle, Power down	None	L	L	X	L	L	X	X	X	X	L-H	Tri-State
Deselected Cycle, Power down	None	L	X	H	L	L	X	X	X	X	L-H	Tri-State
Deselected Cycle, Power down	None	L	L	X	L	H	L	X	X	X	L-H	Tri-State
Deselected Cycle, Power down	None	X	X	X	L	H	L	X	X	X	L-H	Tri-State
Sleep Mode, Power down	None	X	X	X	H	X	X	X	X	X	X	Tri-State
Read Cycle, Begin Burst	External	L	H	L	L	L	X	X	X	L	L-H	Q
Read Cycle, Begin Burst	External	L	H	L	L	L	X	X	X	H	L-H	Tri-State
Write Cycle, Begin Burst	External	L	H	L	L	H	L	X	L	X	L-H	D
Read Cycle, Begin Burst	External	L	H	L	L	H	L	X	H	L	L-H	Q
Read Cycle, Begin Burst	External	L	H	L	L	H	L	X	H	H	L-H	Tri-State
Read Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	L	L-H	Q
Read Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	H	L-H	Tri-State
Read Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	L	L-H	Q
Read Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	H	L-H	Tri-State
Write Cycle, Continue Burst	Next	X	X	X	L	H	H	L	L	X	L-H	D
Write Cycle, Continue Burst	Next	H	X	X	L	X	H	L	L	X	L-H	D
Read Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	L	L-H	Q
Read Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	H	L-H	Tri-State
Read Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	L	L-H	Q
Read Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	H	L-H	Tri-State
Write Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	L	X	L-H	D
Write Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	L	X	L-H	D

Notes

1. X = "Do Not Care," H = Logic HIGH, and L = Logic LOW.
2. WRITE = L when any one or more Byte Write enable signals ($\overline{BW_A}$, $\overline{BW_B}$, $\overline{BW_C}$, $\overline{BW_D}$) and $\overline{BWE}$ = L or $\overline{GW}$ = L. $\overline{WRITE}$ = H when all Byte write enable signals ($\overline{BW_A}$, $\overline{BW_B}$, $\overline{BW_C}$, $\overline{BW_D}$), $\overline{BWE}$, $\overline{GW}$ = H.
3. The DQ pins are controlled by the current cycle and the $\overline{OE}$ signal. $\overline{OE}$ is asynchronous and is not sampled with the clock.
4. The SRAM always initiates a read cycle when $\overline{ADSP}$ is asserted, regardless of the state of $\overline{GW}$, $\overline{BWE}$, or $\overline{BW_{[A:D]}}$. Writes may occur only on subsequent clocks after the $\overline{ADSP}$ or with the assertion of $\overline{ADSC}$. As a result, $\overline{OE}$ is driven HIGH prior to the start of the write cycle to enable the outputs to tri-state. $\overline{OE}$ is a "Do Not Care" for the remainder of the write cycle.
5. $\overline{OE}$ is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle all data bits are tri-state when $\overline{OE}$ is inactive or when the device is deselected, and all data bits behave as output when $\overline{OE}$ is active (LOW).

Truth Table for Read or Write

The partial truth table for read or write follows. [1, 6]

Function	$\overline{GW}$	$\overline{BWE}$	$\overline{BW_D}$	$\overline{BW_C}$	$\overline{BW_B}$	$\overline{BW_A}$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write Byte (A, DQP_A)	H	L	H	H	H	L
Write Byte (B, DQP_B)	H	L	H	H	L	H
Write Bytes (B, A, DQP_A, DQP_B)	H	L	H	H	L	L
Write Byte (C, DQP_C)	H	L	H	L	H	H
Write Bytes (C, A, DQP_C, DQP_A)	H	L	H	L	H	L
Write Bytes (C, B, DQP_C, DQP_B)	H	L	H	L	L	H
Write Bytes (C, B, A, DQP_C, DQP_B, DQP_A)	H	L	H	L	L	L
Write Byte (D, DQP_D)	H	L	L	H	H	H
Write Bytes (D, A, DQP_D, DQP_A)	H	L	L	H	H	L
Write Bytes (D, B, DQP_D, DQP_A)	H	L	L	H	L	H
Write Bytes (D, B, A, DQP_D, DQP_B, DQP_A)	H	L	L	H	L	L
Write Bytes (D, B, DQP_D, DQP_B)	H	L	L	L	H	H
Write Bytes (D, B, A, DQP_D, DQP_C, DQP_A)	H	L	L	L	H	L
Write Bytes (D, C, A, DQP_D, DQP_B, DQP_A)	H	L	L	L	L	H
Write All Bytes	H	L	L	L	L	L
Write All Bytes	L	X	X	X	X	X

Note
6. This table is only a partial listing of the byte write combinations. Any combination of $\overline{BW_x}$ is valid. Appropriate write is done based on the active byte write.

Maximum Ratings

Exceeding the maximum ratings may shorten the battery life of the device. These user guidelines are not tested.

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage on V_{DD} Relative to GND .....–0.5V to +4.6V

Supply Voltage on V_{DDQ} Relative to GND.....–0.5V to +V_{DD}

DC Voltage Applied to Outputs in tri-state.....–0.5V to V_{DDQ} + 0.5V

DC Input Voltage ..... –0.5V to V_{DD} + 0.5V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage (MIL-STD-883, Method 3015) ..... >2001V

Latch up Current..... >200 mA

Operating Range

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Commercial	0°C to +70°C	3.3V –5%/+10%	2.5V –5% to V_{DD}
Industrial	–40°C to +85°C		

Electrical Characteristics

Over the Operating Range [7, 8]

Parameter	Description	Test Conditions		Min	Max	Unit
V_{DD}	Power Supply Voltage			3.135	3.6	V
V_{DDQ}	IO Supply Voltage			2.375	V_{DD}	V
V_{OH}	Output HIGH Voltage	for 3.3V IO, I_{OH} = –4.0 mA		2.4		V
		for 2.5V IO, I_{OH} = –1.0 mA		2.0		V
V_{OL}	Output LOW Voltage	for 3.3V, IO, I_{OL}= 8.0 mA			0.4	V
		for 2.5V IO, I_{OL} = 1.0 mA			0.4	V
V_{IH}	Input HIGH Voltage	for 3.3V IO		2.0	V_{DD} + 0.3V	V
		for 2.5V IO		1.7	V_{DD} + 0.3V	V
V_{IL}	Input LOW Voltage[7]	for 3.3V IO		–0.3	0.8	V
		for 2.5V IO		–0.3	0.7	V
I_X	Input Leakage Current except ZZ and MODE	GND ≤ V_I ≤ V_{DDQ}		–5	5	µA
	Input Current of MODE	Input = V_{SS}		–30		µA
		Input = V_{DD}			5	µA
	Input Current of ZZ	Input = V_{SS}		–5		µA
		Input = V_{DD}			30	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{DDQ}, Output Disabled		–5	5	µA
I_{DD}	V_{DD} Operating Supply Current	V_{DD} = Max, I_{OUT} = 0 mA, f = f_{MAX}= $1/t_{CYC}$	7.5 ns cycle, 133 MHz		225	mA
			10 ns cycle, 100 MHz		205	mA
I_{SB1}	Automatic CE Power down Current—TTL Inputs	Max V_{DD}, Device Deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}, inputs switching	7.5 ns cycle, 133 MHz		90	mA
			10 ns cycle, 100 MHz		80	mA
I_{SB2}	Automatic CE Power down Current—CMOS Inputs	Max V_{DD}, Device Deselected, V_{IN} ≥ V_{DD} – 0.3V or V_{IN} ≤ 0.3V, f = 0, inputs static	All speeds		40	mA
I_{SB3}	Automatic CE Power down Current—CMOS Inputs	Max V_{DD}, Device Deselected, V_{IN} ≥ V_{DDQ} – 0.3V or V_{IN} ≤ 0.3V, f = f_{MAX}, inputs switching	7.5 ns cycle, 133 MHz		75	mA
			10 ns cycle, 100 MHz		65	mA
I_{SB4}	Automatic CE Power down Current—TTL Inputs	Max V_{DD}, Device Deselected, V_{IN} ≥ V_{DD} – 0.3V or V_{IN} ≤ 0.3V, f = 0, inputs static	All speeds		45	mA

Notes

7. Overshoot: V_{IH}(AC) < V_{DD} +1.5V (Pulse width less than t_{CYC}/2), undershoot: V_{IL}(AC) > –2V (Pulse width less than t_{CYC}/2).
8. $T_{Power\ up}$: Assumes a linear ramp from 0V to V_{DD}(min) within 200 ms. During this time V_{IH} < V_{DD} and V_{DDQ} ≤ V_{DD}.

Capacitance

Tested initially and after any design or process change that may affect these parameters.

Parameter	Description	Test Conditions	100 TQFP Max	119 BGA Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{DD} = 3.3V. V_{DDQ} = 3.3V	5	5	pF
C_{CLK}	Clock Input Capacitance		5	5	pF
C_{IO}	Input or Output Capacitance		5	7	pF

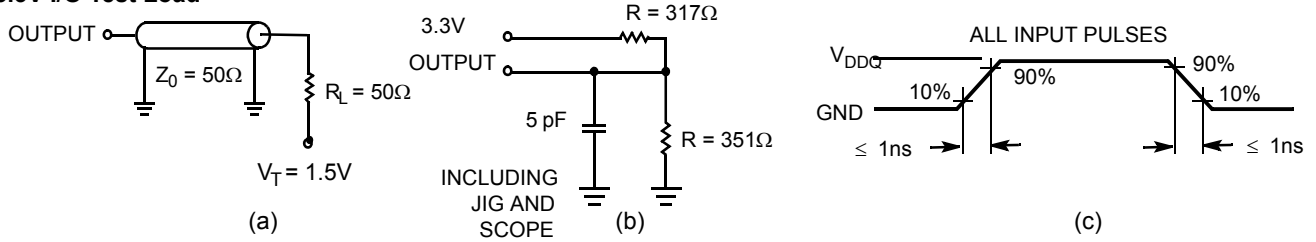
Thermal Resistance

Tested initially and after any design or process change that may affect these parameters.

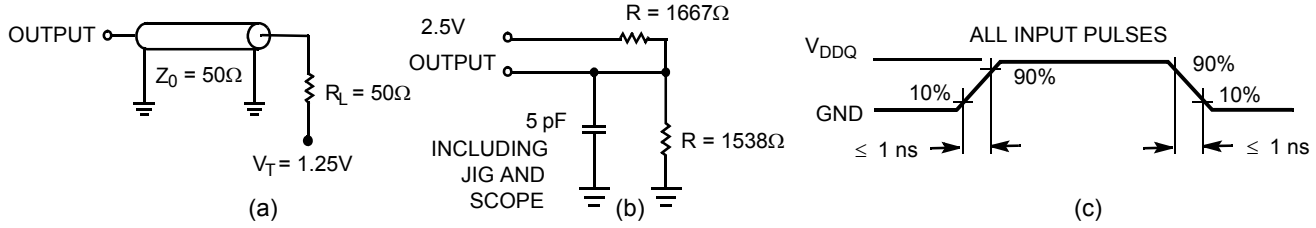
Parameter	Description	Test Conditions	100 TQFP Package	119 BGA Package	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	30.32	34.1	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		6.85	14.0	°C/W

AC Test Loads and Waveforms

3.3V I/O Test Load



2.5V I/O Test Load



Switching Characteristics

Over the Operating Range [9, 10]

Parameter	Description	–133		–100		Unit
		Min	Max	Min	Max	
t_{POWER}	V_{DD}(Typical) to the first Access[11]	1		1		ms
Clock						
t_{CYC}	Clock Cycle Time	7.5		10		ns
t_{CH}	Clock HIGH	2.5		4.0		ns
t_{CL}	Clock LOW	2.5		4.0		ns
Output Times						
t_{CDV}	Data Output Valid After CLK Rise		6.5		8.0	ns
t_{DOH}	Data Output Hold After CLK Rise	2.0		2.0		ns
t_{CLZ}	Clock to Low Z[12, 13, 14]	0		0		ns
t_{CHZ}	Clock to High Z[12, 13, 14]		3.5		3.5	ns
t_{OEV}	$\overline{OE}$ LOW to Output Valid		3.5		3.5	ns
t_{OELZ}	$\overline{OE}$ LOW to Output Low Z[12, 13, 14]	0		0		ns
t_{OEHZ}	$\overline{OE}$ HIGH to Output High Z[12, 13, 14]		3.5		3.5	ns
Setup Times						
t_{AS}	Address Setup Before CLK Rise	1.5		2.0		ns
t_{ADS}	$\overline{ADSP}$, $\overline{ADSC}$ Setup Before CLK Rise	1.5		2.0		ns
t_{ADVS}	$\overline{ADV}$ Setup Before CLK Rise	1.5		2.0		ns
t_{WES}	$\overline{GW}$, $\overline{BWE}$, $\overline{BW_X}$ Setup Before CLK Rise	1.5		2.0		ns
t_{DS}	Data Input Setup Before CLK Rise	1.5		2.0		ns
t_{CES}	Chip Enable Setup	1.5		2.0		ns
Hold Times						
t_{AH}	Address Hold After CLK Rise	0.5		0.5		ns
t_{ADH}	$\overline{ADSP}$, $\overline{ADSC}$ Hold After CLK Rise	0.5		0.5		ns
t_{WEH}	$\overline{GW}$, $\overline{BWE}$, $\overline{BW_X}$ Hold After CLK Rise	0.5		0.5		ns
t_{ADVH}	$\overline{ADV}$ Hold After CLK Rise	0.5		0.5		ns
t_{DH}	Data Input Hold After CLK Rise	0.5		0.5		ns
t_{CEH}	Chip Enable Hold After CLK Rise	0.5		0.5		ns

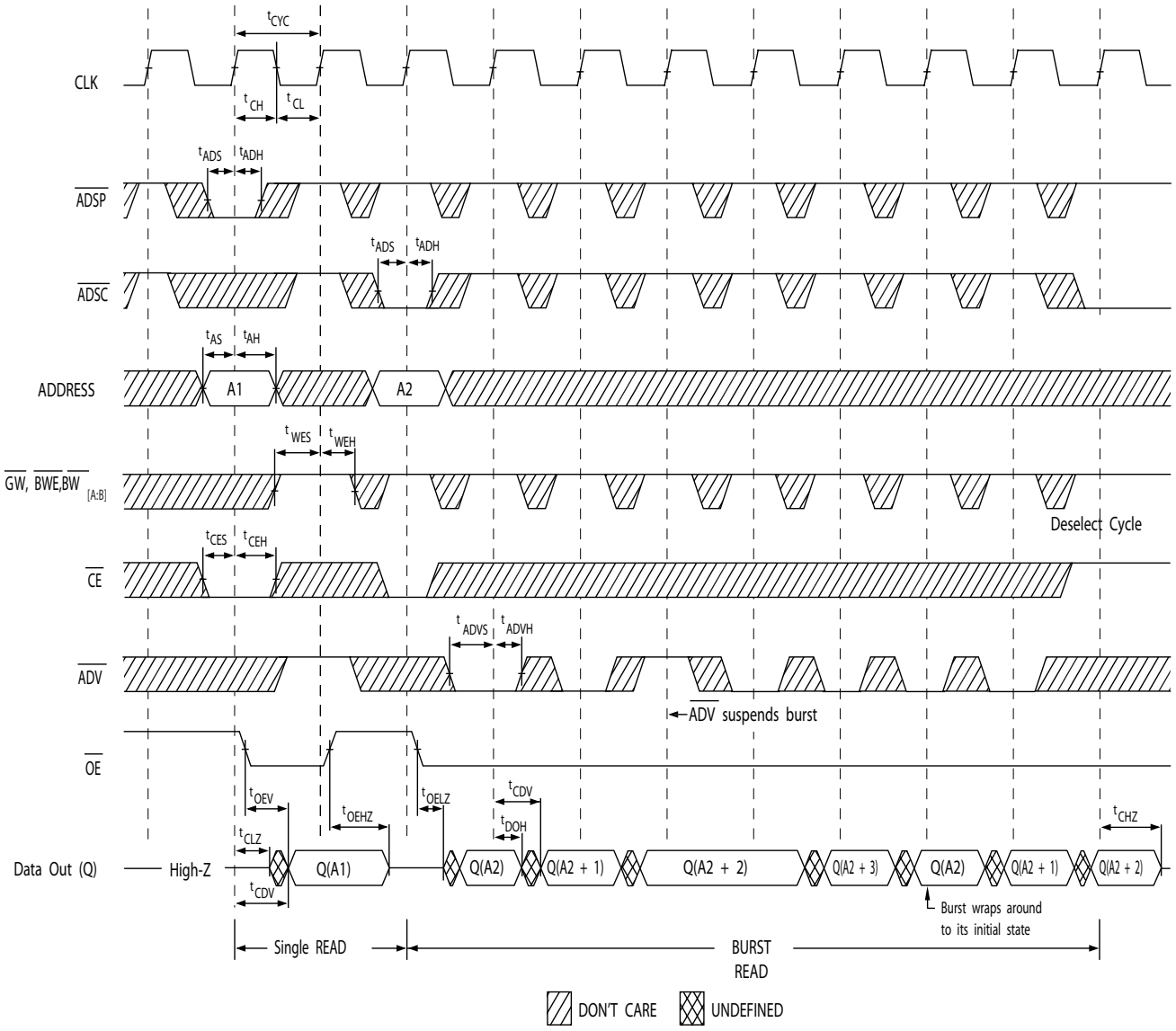
Notes

9. Timing reference level is 1.5V when V_{DDQ} = 3.3V and is 1.25V when V_{DDQ} = 2.5V.
10. Test conditions shown in (a) of Latch up Current >200 mA unless otherwise noted.
11. This part has a voltage regulator internally; t_{POWER} is the time that the power needs to be supplied above V_{DD}(minimum) initially before a read or write operation is initiated.
12. t_{CHLZ}, t_{CLZ},t_{OELZ}, and t_{OEHZ} are specified with AC test conditions shown in (b) of AC Test Loads. Transition is measured ± 200 mV from steady state voltage.
13. At any voltage and temperature, t_{OEHZ} is less than t_{OELZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve High Z prior to Low Z under the same system conditions.
14. This parameter is sampled and not 100% tested.

Timing Diagrams

Figure 1 shows the read cycle timing. [15]

Figure 1. Read Cycle Timing

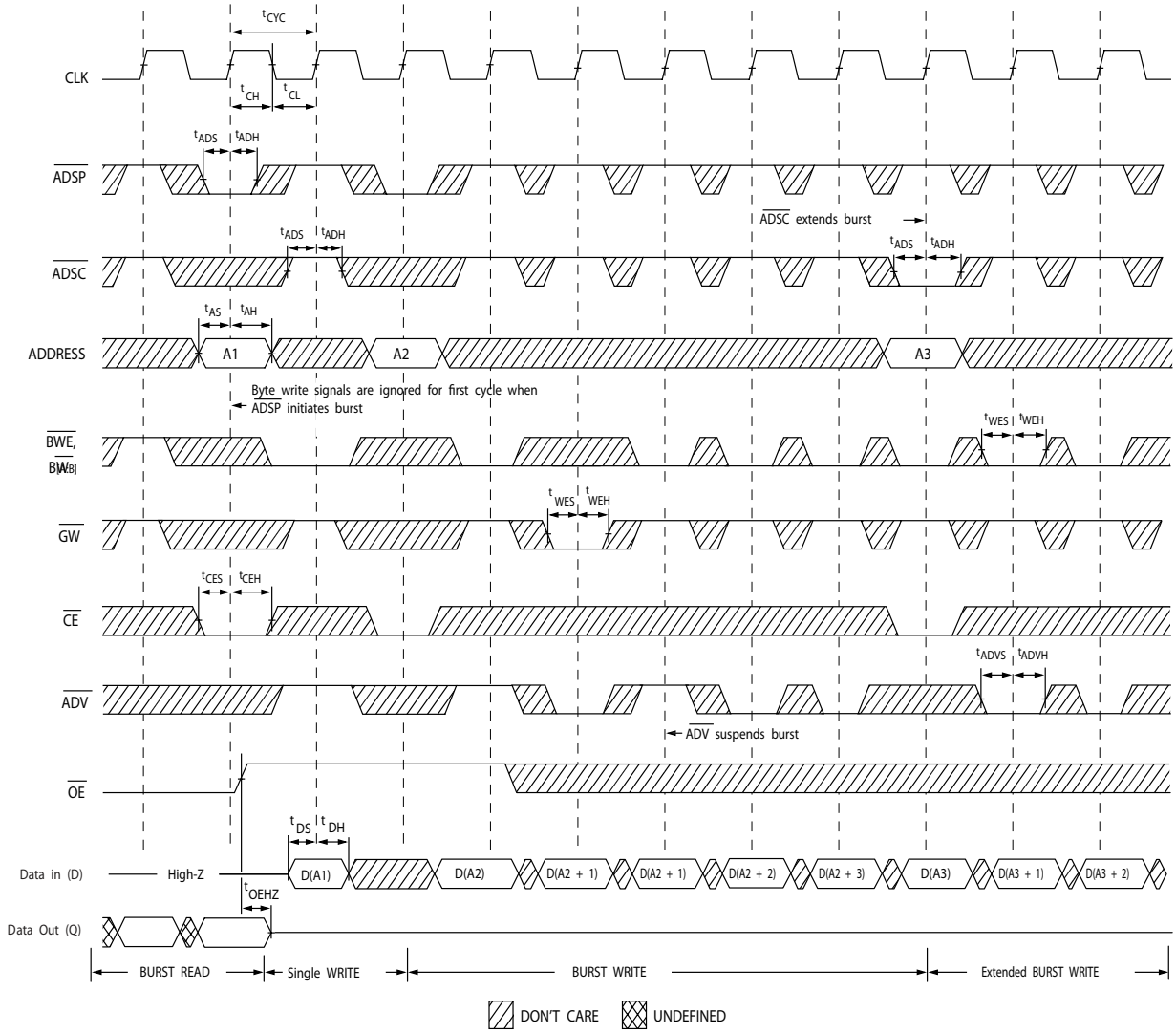


Note:
15. On this diagram, when $\overline{CE}$ is LOW: $\overline{CE}_1$ is LOW, CE_2 is HIGH and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH: $\overline{CE}_1$ is HIGH or CE_2 is LOW or $\overline{CE}_3$ is HIGH.

Timing Diagrams (continued)

Figure 2 shows the write cycle timing. [15, 16]

Figure 2. Write Cycle Timing

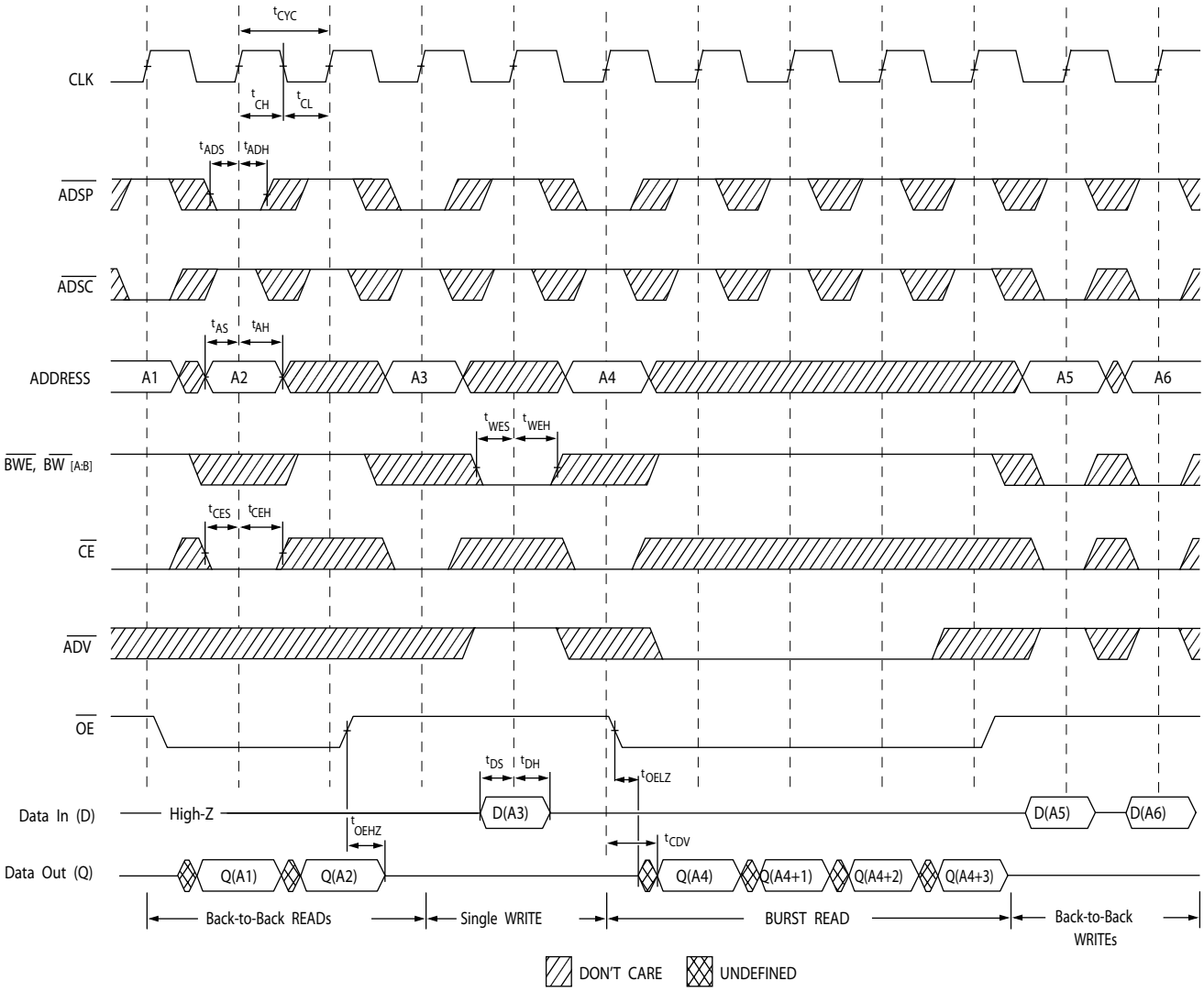


Note:
16. Full width write can be initiated by either $\overline{GW}$ LOW; or by $\overline{GW}$ HIGH, $\overline{BWE}$ LOW and $\overline{BW}_x$ LOW.

Timing Diagrams (continued)

Figure 3 shows the read and write timing. [16, 17, 18]

Figure 3. Read/Write Timing

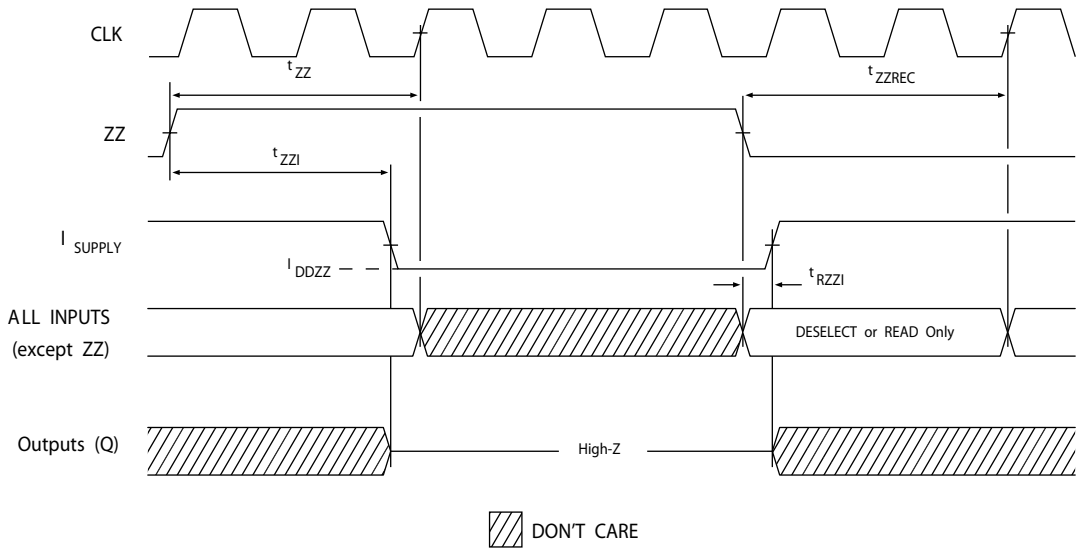


Notes:
17. The data bus (Q) remains in high-Z following a WRITE cycle, unless a new read access is initiated by $\overline{ADSP}$ or $\overline{ADSC}$.
18. $\overline{GW}$ is HIGH.

Timing Diagrams (continued)

Figure 4 shows the ZZ mode timing. [19, 20]

Figure 4. ZZ Mode Timing



Notes:
19. Device must be deselected when entering ZZ mode. See "Truth Table" on page 8 for all possible signal conditions to deselect the device.
20. DQs are in high-Z when exiting ZZ sleep mode.

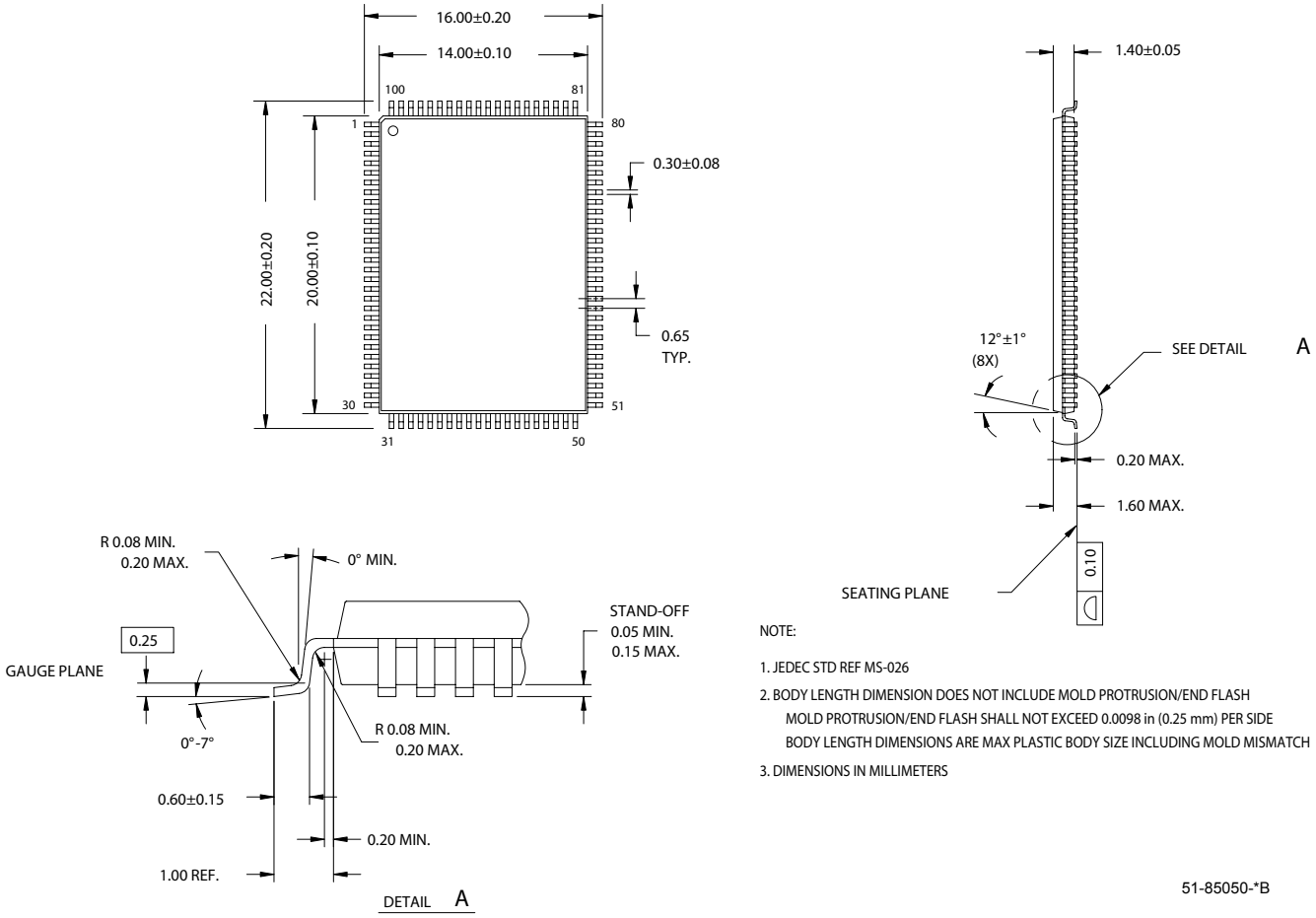
Ordering Information

Not all of the speed, package and temperature ranges are available. Please contact your local sales representative or visit www.cypress.com for actual products offered.

Speed (MHz)	Ordering Code	Package Diagram	Part and Package Type	Operating Range
133	CY7C1345G-133AXC	51-85050	100-Pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Pb-Free	Commercial
	CY7C1345G-133BGC	51-85115	119-Ball Grid Array (14 x 22 x 2.4 mm)	
	CY7C1345G-133BGXC		119-Ball Grid Array (14 x 22 x 2.4 mm) Pb-Free	
	CY7C1345G-133AXI	51-85050	100-Pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Pb-Free	Industrial
	CY7C1345G-133BGI	51-85115	119-Ball Grid Array (14 x 22 x 2.4 mm)	
	CY7C1345G-133BGXI		119-Ball Grid Array (14 x 22 x 2.4 mm) Pb-Free	
100	CY7C1345G-100AXC	51-85050	100-Pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Pb-Free	Commercial
	CY7C1345G-100BGC	51-85115	119-Ball Grid Array (14 x 22 x 2.4 mm)	
	CY7C1345G-100BGXC		119-Ball Grid Array (14 x 22 x 2.4 mm) Pb-Free	
	CY7C1345G-100AXI	51-85050	100-Pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Pb-Free	Industrial
	CY7C1345G-100BGI	51-85115	119-Ball Grid Array (14 x 22 x 2.4 mm)	
	CY7C1345G-100BGXI		119-Ball Grid Array (14 x 22 x 2.4 mm) Pb-Free	

Package Diagrams

Figure 5. 100-Pin Thin Plastic Quad Flatpack (14 x 20 x 1.4 mm), 51-85050



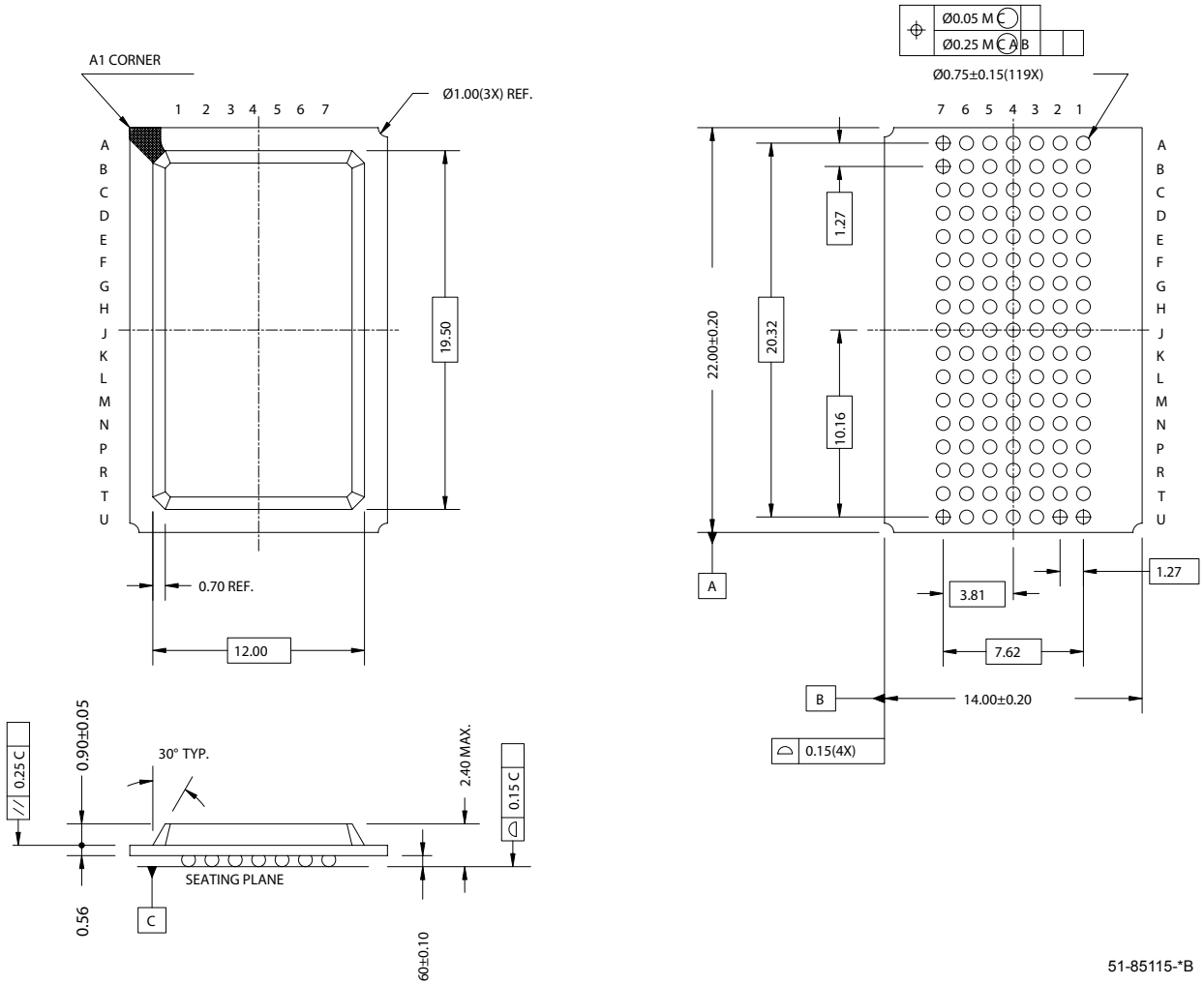
NOTE:

1. JEDEC STD REF MS-026
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH
   MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE
   BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH
3. DIMENSIONS IN MILLIMETERS

51-85050-*B

Package Diagrams (continued)

Figure 6.119-Ball BGA (14 x 22 x 2.4 mm), 51-85115



Document History Page

Document Title: CY7C1345G, 4-Mbit (128K x 36) Flow Through Sync SRAM Document Number: 38-05517				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	224365	See ECN	RKF	New datasheet
*A	278513	See ECN	VBL	Deleted 66 MHz Changed TQFP package to Pb-free TQFP in Ordering Information section Added BG Pb-free package
*B	333626	See ECN	SYT	Modified Address Expansion balls in the pinouts for 100 TQFP and 119 BGA Packages as per JEDEC standards and updated the Pin Definitions accordingly Modified V_{OL}, V_{OH} test conditions Replaced 'Snooze' with 'Sleep' Removed 117 MHz speed bin Replaced TBDs for Θ_{JA} and Θ_{JC} to their respective values on the Thermal Resistance table Removed comment on the availability of BG Pb-free package Updated the Ordering Information by shading and unshading MPNs as per availability
*C	418633	See ECN	RXU	Converted from Preliminary to Final Changed address of Cypress Semiconductor Corporation on Page# 1 from "3901 North First Street" to "198 Champion Court" Modified test condition from $V_{IH} \leq V_{DD}$ to $V_{IH} < V_{DD}$. Modified test condition from $V_{DDQ} < V_{DD}$ to $V_{DDQ} \leq V_{DD}$ Modified Input Load to Input Leakage Current except ZZ and MODE in the Electrical Characteristics Table Replaced Package Name column with Package Diagram in the Ordering Information table Replaced Package Diagram of 51-85050 from *A to *B Updated the Ordering Information
*D	480124	See ECN	VKN	Added the Maximum Rating for Supply Voltage on V_{DDQ} Relative to GND Updated the Ordering Information table.
*E	1274724	See ECN	VKN	Corrected Write Cycle timing waveform