5A Synchronous Boost Converter with Output Isolation MOS

General Description

The RT4841 is Synchronous Boost Converter with output isolation MOS for active matrix thin film transistor (TFT) liquid crystal displays (LCDs).

The Device incorporates current mode, fixed-frequency, pulse width modulation (PWM) circuitry and fully integrated synchronous boost converter with a 80mΩ power switch and a 80mΩ rectifier switch to achieve high efficiency, small size and fast transient response in TFT-LCD applications. Moreover, Device contains one ISO MOSFET controller for power on sequence of step-up converter. The RT4841 has a wide input voltage range from 8.6V to 15.9V and device has 5A (min.) switching current capability. The RT4841 is available in a WQFN-20L 4x4 package.

Ordering Information

RT4841 □□

Package Type
QW : WQFN-20L 4x4 (W-Type)
(Exposed Pad-Option 1)

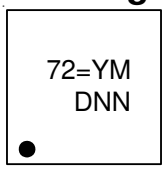
Lead Plating System
G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information



72= : Product Code

YMDNN : Date Code

Features

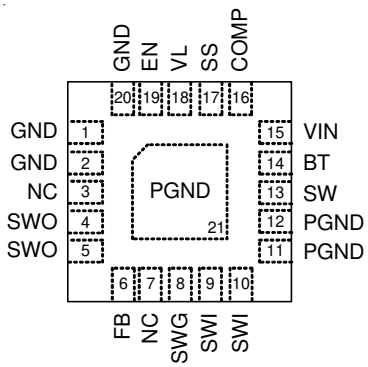
- **8.6V to 15.9V Input Supply Voltage**
- **A Synchronous Boost Converter**
- **Isolation Switch Controller**
- **VIN Under Voltage Lockout**
- **Fixed 500kHz Switching Frequency**
- **Over-Temperature Protection**
- **Cycle by Cycle OCP Protection**
- **Thin 20-Lead WQFN Package**

Applications

- TFT LCD Monitor Panel
- TFT LCD TV Panel

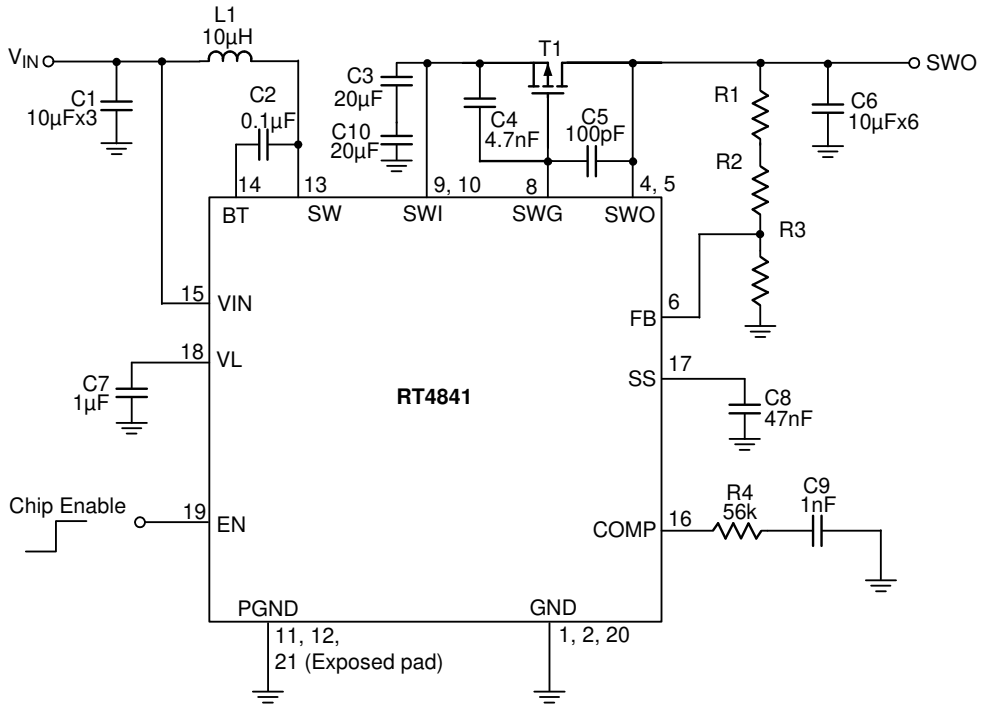
Pin Configuration

(TOP VIEW)

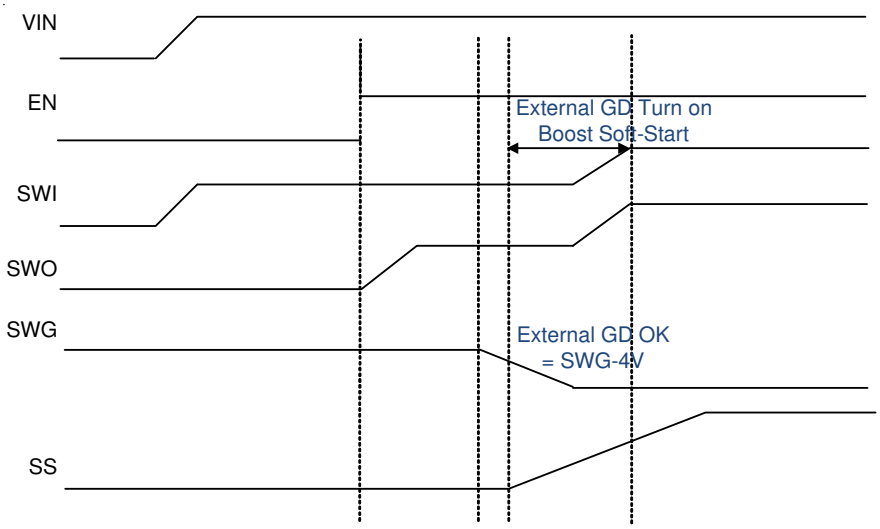


WQFN-20L 4x4

Typical Application Circuit



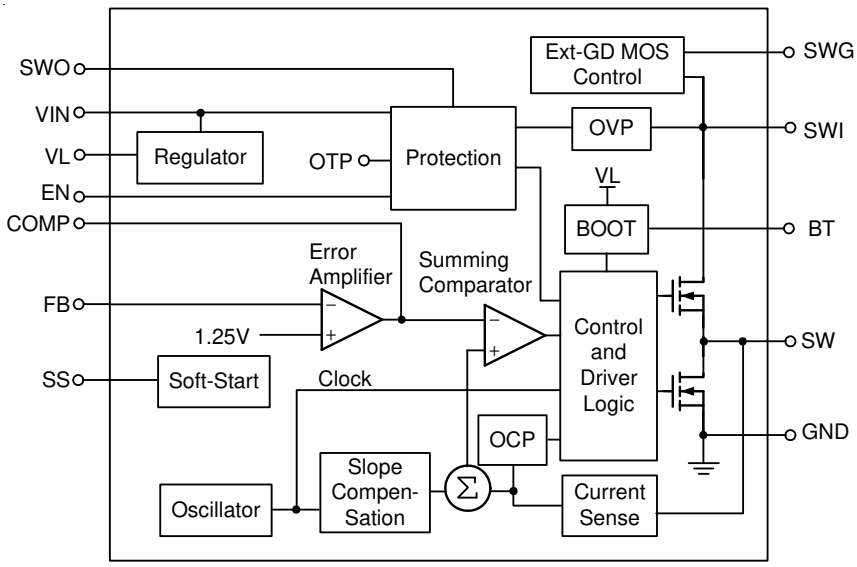
Timing Diagram



Functional Pin Description

Pin No.	Pin Name	Pin Function
1, 2, 20	GND	Ground pin.
3, 7	NC	Not connected. Should be floating or connected to GND.
4, 5	SWO	Boost regulator external p-channel pass switch out.
6	FB	Feedback of SWO. Connect to the center of resistor voltage divider to program the output voltage.
8	SWG	Boost regulator external p-channel pass switch gate input.
9, 10	SWI	Output voltage of step-up converter.
11, 12	PGND	Power ground.
13	SW	Switch node of Boost.
14	BT	Power supply for high-side MOSFET gate driver. A ceramic capacitor of 0.1μF must be connected between this pin and the SW pin.
15	VIN	Power supply input.
16	COMP	Compensation pin for error amplifier. Connect a series RC from COMP to ground.
17	SS	Soft-start control. Connect a soft-start capacitor (C_{SS}) to this pin. The soft-start capacitor is charged with a constant current of 5μA. The soft-start capacitor is discharged to ground when EN is low.
18	VL	Internal 5V linear regulator output.
19	EN	Chip enable control pin. Pull EN pin high and to turn on these channels. A 1MΩ pull down resistor is connected from this pin to ground.
21 (Exposed Pad)	PGND	Power ground. The Exposed Pad should be soldered to a large PCB and connected to PGND for maximum thermal dissipation.

Functional Block Diagram



Operation

The RT4841 is a 5A Synchronous Boost Converter with Output Isolation MOS. It is a synchronous current mode boost converter integrated with a 22V/5A isolation power switch, covering a wide VIN range from 8.6V to 15.9V. It performs high efficiency and fast transient responses to generate source driver supplies for TFT LCD display. The synchronous step-up converter uses a current mode, pulse width modulation (PWM) topology with a built in N-MOSFET to achieve high efficiency and fast transient response in TFT-LCD applications. The output voltage can be adjusted by setting the resistive voltage-divider sensing at the FB pin. The error amplifier varies the COMP voltage by sensing the FB pin to regulate the output voltage. For better stability, the slope compensation signal summed with the current sense signal will be compared with the COMP voltage to determine the current trip point and duty cycle.

Absolute Maximum Ratings (Note 1)

- SW, SWO, SWG, SWI to GND ---------- –0.3 to 22V
- BT to GND ---------- –0.3 to 26V
- VIN to GND ---------- –0.3 to 16.5V
- SWI to SWO ---------- –0.3 to 22V
- VL, COMP, SS, FB, EN to GND ---------- –0.3 to 6.5V
- Power Dissipation, P_D @ T_A = 25°C
  WQFN-20L 4x4 ---------- 3.57W
- Package Thermal Resistance (Note 2)
  WQFN-20L 4x4, θ_{JA} ---------- 28°C/W
  WQFN-20L 4x4, θ_{JC} ---------- 7°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 12V, EN = high, SWO = 14.5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
General						
Supply Voltage	V_{IN}		8.6	12	15.9	V
VIN Under Voltage	V_{UVLO}	VIN rising	6.4	6.7	7	V
Lockout Hys		VIN falling	0.6	0.8	1	V
IIN Quiescent Current	I_{QVIN}	V_{IN} = 12V	--	5	--	mA
VL Output Voltage	VL		--	5	--	V
Fault Detection						
Thermal Shutdown	T_{SD}	Temperature rising	--	150	--	°C
Thermal Shutdown Hysteresis	T_{SD_Hsy}		--	15	--	°C
Enable						
High-Level Input Voltage	V_{IH}		1.3	--	--	V
Low-Level Input Voltage	V_{IL}		--	--	0.8	V
Sync. Step-up Converter						
FB Regulation Voltage	V_{REF}	1.25V	–1%	--	1	%
Switching Frequency	f_{OSC}		450	500	550	kHz

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Maximum Duty Cycle	D_{MAX}		--	90	--	%
High Side N-MOS On-Resistance	HS_{RDSON}	I_{SW} = 500mA	--	80	--	mΩ
Low Side N-MOS On-Resistance	LS_{RDSON}	I_{SW} = 500mA	--	80	--	mΩ
Current Limit	OCP		5	5.5	--	A
SW Leakage	I_{LEAK}	V_{SW} = 14.4V/0V	--	1	10	μA
Line Regulation		9V = V_{IN} = 15.5V, I_{OUT} = 1mA	--	0.04	--	%/V
Load Regulation		1mA = I_{OUT} = 1.5A	--	0.1	--	%/A
Soft Start Charge Current	I_{SS}		--	5	--	μA
Over-Voltage Protection	OVP		20	21	22	V
Error Amplifier Transconductance	Gm		--	100	--	μs
Current Sense Transresistance	R_{CS}		--	0.25	--	V/A
Gate Output High-Level	V_{gOH}		SWO – 0.2	SWO	SWO + 0.2	V
Gate Output Low-Level	V_{gOL}		--	SWO – 5.8	--	V
Gate Pull-High Resistor	R_{swg}		8	12	16	kΩ
Gate Sink Current	I_{G_SINK}		6	10	14	μA
External Isolation MOSFET Soft Start Time	t_{SS_extgd}	When external isolation MOSFET Cgs = 4.7nF	--	2	--	ms

Note 1. Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

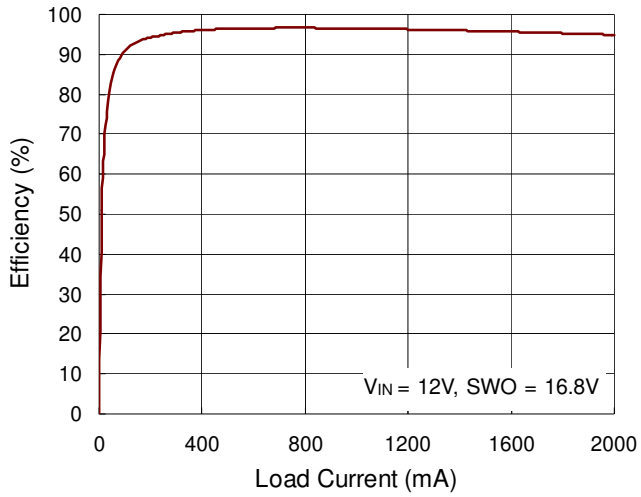
Note 4. The device is not guaranteed to function outside its operating conditions.

Protection Table

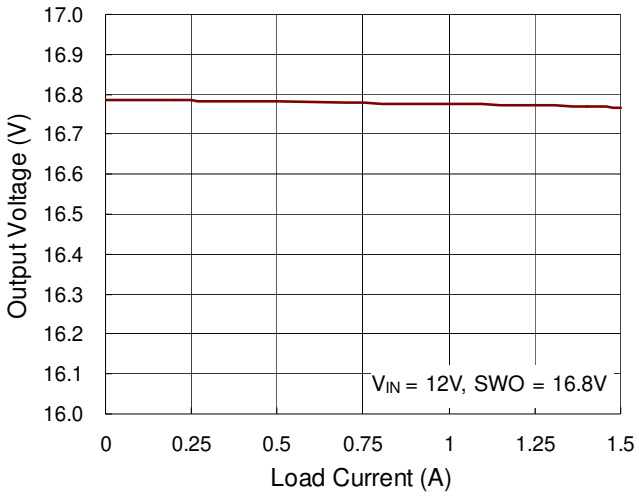
Channel	Protection	Criteria	Behavior	Recovery
Boost	OCP	I_L > 5A (min)	Cycle by cycle Current limit	
	UVP	FB < 1.25V*80%	After 50ms, IC Shut Down. Latch	Release<VIN_UVLO
	SCP	SWO < 4V	Detect only during power-on. IC Shut Down. Latch	Release<VIN_UVLO or EN = 0V
	OVP	18V < SWI < 20V	SW Stop Switching	<OVP_HYS

Typical Operating Characteristics

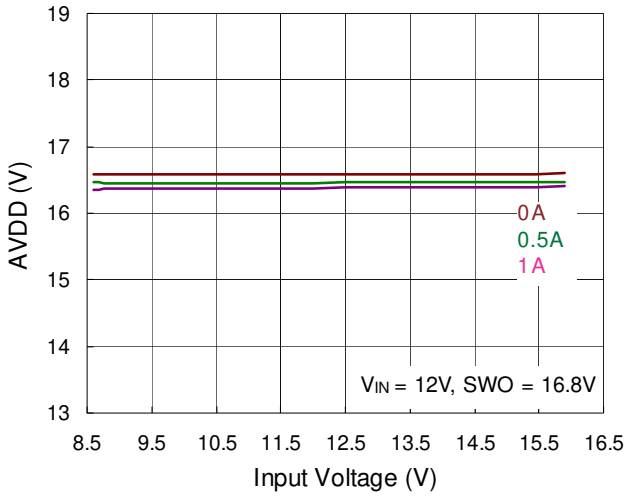
SWO Efficeiency vs. Load Current



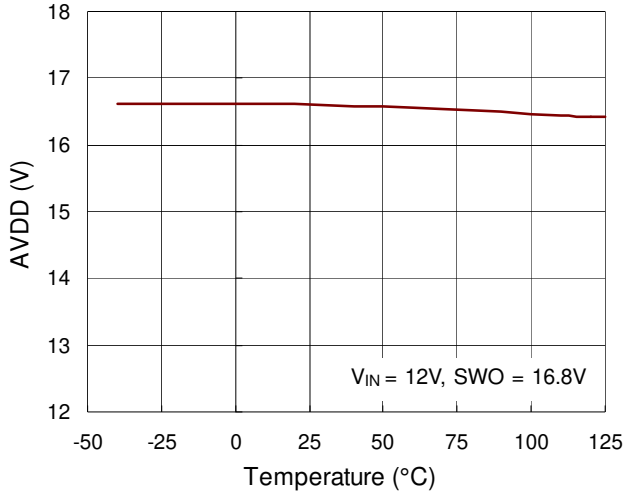
SWO Output Voltage vs. Load Current



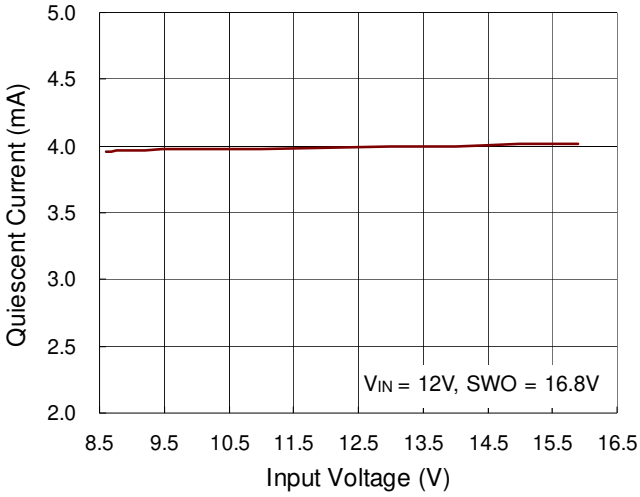
AVDD Output Voltage vs. Input Voltage



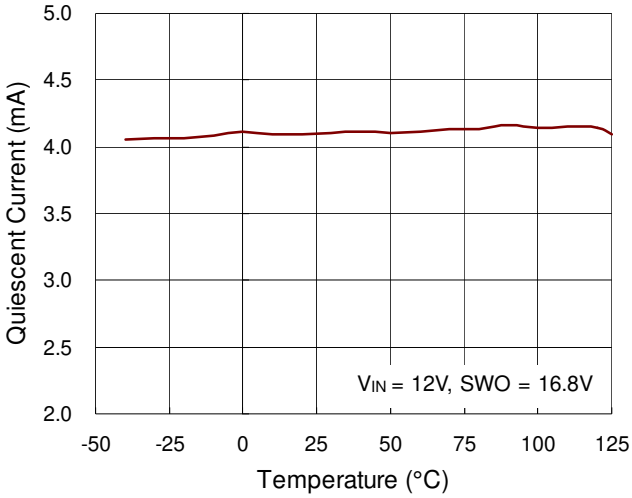
Output Voltage vs. Temperature



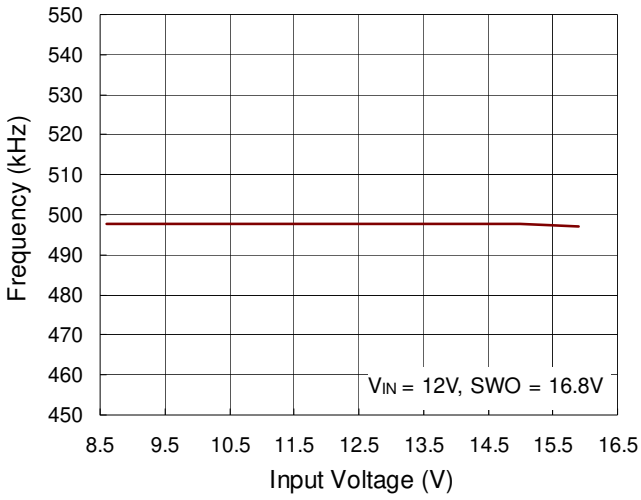
VIN Quiescent Current vs. Input Voltage



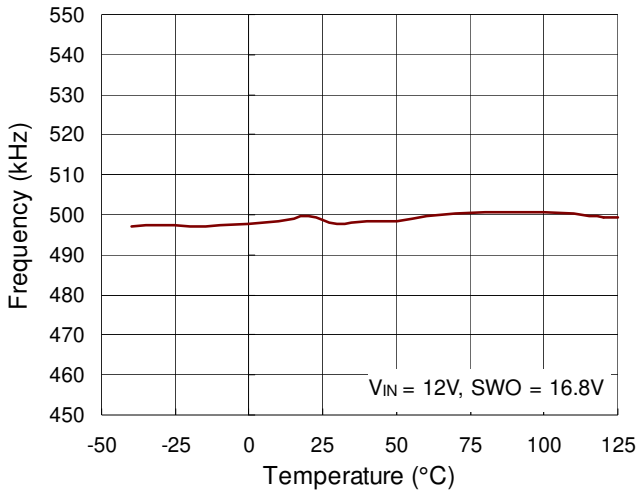
VIN Quiescent Current vs. Temperature



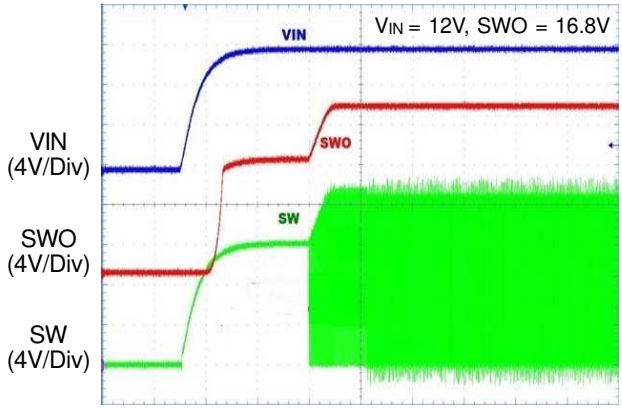
SW Frequency vs. Input Voltage



SW Frequency vs. Temperature

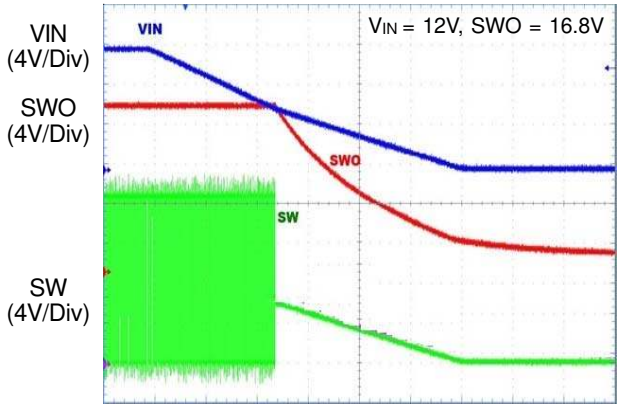


Power On



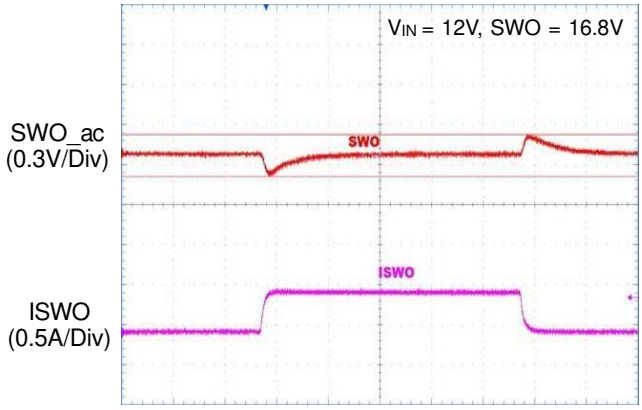
Time (10ms/Div)

Power Off



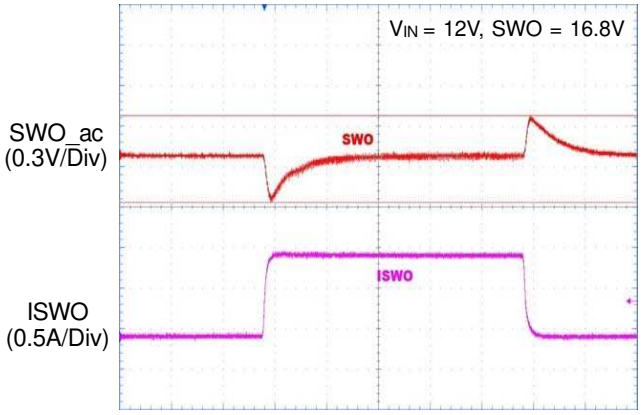
Time (20ms/Div)

Load Transient Response at 0.5A



Time (100µs/Div)

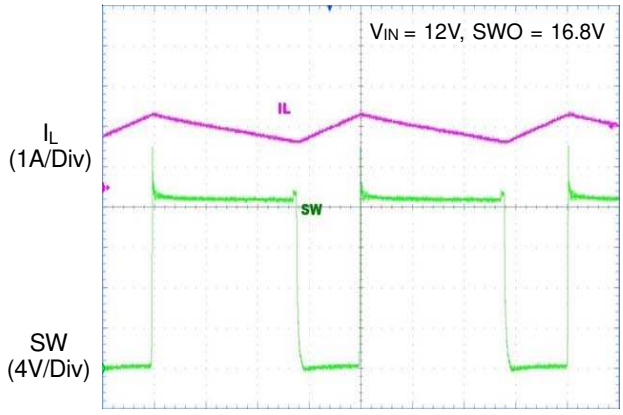
Load Transient Response at 1A



Time (100µs/Div)

Stability at 0.5A

Stability at 1A



Application Information

The RT4841 is a 5A Synchronous Boost Converter with Output Isolation MOS. It is a synchronous current mode boost converter integrated with a 22V/5A isolation power switch, covering a wide VIN range from 8.6V to 15.9V. It performs high efficiency and fast transient responses to generate source driver supplies for TFT LCD display. The synchronous step-up converter uses a current mode, pulse width modulation (PWM) topology with a built in N-MOSFET to achieve high efficiency and fast transient response in TFT-LCD applications. The following content contains detailed description and information for component selection.

Boost Regulator

The RT4841 is a synchronous current mode boost converter integrated with a 22V/5A power switch, covering a wide VIN range from 8.6V to 15.9V. It performs high efficiency and fast transient responses to generate source driver supplies for TFT LCD display . The high operation frequency allows use of smaller components to minimize the thickness of the LCD panel. The output voltage can be adjusted by setting the resistive voltage-divider sensing at the FB pin. The error amplifier varies the COMP voltage by sensing the FB pin to regulate the output voltage. For better stability, the slope compensation signal summed with the current sense signal will be compared with the COMP voltage to determine the current trip point and duty cycle.

Soft-Start

The RT4841 provides soft-start function to minimize the inrush current. When powered on, an internal constant current charges an external capacitor. The rising voltage rate on the COMP pin is limited from V_{SS} = 0V to 1.24V and the inductor peak current will also be limited at the same time. When powered off, the external capacitor will be discharged until the next soft-start time.

The soft-start function is implemented by the external capacitor with a 4μA constant current charging to the soft-start capacitor. Therefore, the capacitor should be large enough for output voltage regulation. A typical value for soft-start capacitor is 47nF.

Output Voltage Setting

The regulated output voltage is shown as the following equation :

$$V_{OUT} = V_{REF} \times \left(\frac{R1+R2+R3}{R3}\right),$$

where V_{REF} = 1.25V (typ.)

The recommended value for R3 should be at least 10kΩ without some sacrificing. Place the resistive voltage divider as close as possible to the chip to reduce noise sensitivity.

Over Current Protection

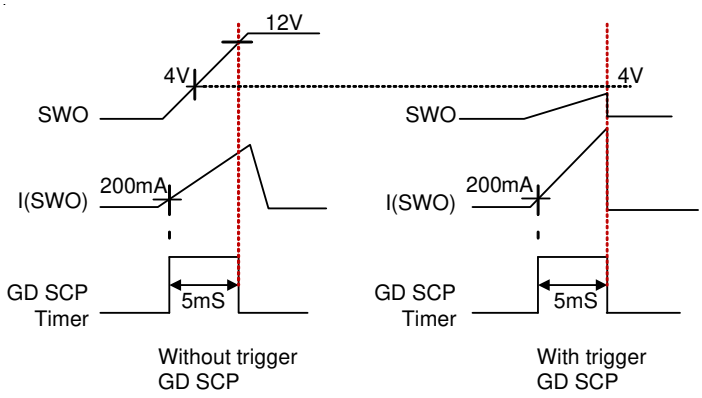
The RT4841 includes a current sensing circuitry which monitors the inductor peak current during each ON period. If the peak current crosses the current limit threshold of 5A (typical), the on cycle is terminated immediately and forcing the inductor to leave charging stage and enter discharge stage. Therefore, the inductor current can be kept below the current limit. The next cycle resumes at the next clock pulse.

Over Temperature Protection

The RT4841 step-up converter has thermal protection function to prevent the chip from overheating. When the junction temperature exceeds 150°C, the function shuts down the device. Once the device cools down by approximately 15°C, it will automatically restart to normal operation. To guarantee continuous operation, do not operate over the maximum junction temperature rating of 125°C.

Short Circuit Protection

To limit the short circuit current, the IC has a voltage detect device. If VIN power on that SWO voltage lower than 4V after 5ms, then the IC will shut down.



Inductor Short Protection

The RT4841 step-up converter has diode short protection to prevent the IC damage. It prevents huge current from input supply and output capacitor to damage internal power MOS. During power on, once happen inductor short and then internal MOSFET will turn off immediately.

Inductor Selection

The inductor value depends on the maximum input current. As a general rule the inductor ripple current is 20% to 40% of maximum input current. If 40% is selected as an example, the inductor ripple current can be calculated according to the following equation :

$$I_{IN(MAX)} = \frac{V_{OUT} \times I_{OUT(MAX)}}{\eta \times V_{IN}}$$

$$I_{RIPPLE} = 0.4 \times I_{IN(MAX)}$$

where η is the efficiency of the boost converter, $I_{IN(MAX)}$ is the maximum input current, and I_{RIPPLE} is the inductor ripple current. The input peak current can be obtained by adding the maximum input current with half of the inductor ripple current as shown in the following equation :

$$I_{PEAK} = 1.2 \times I_{IN(MAX)}$$

Note that the saturated current of inductor must be greater than I_{PEAK}. The inductance can eventually be determined according to the following equation :

$$L = \frac{\eta \times (V_{IN})^2 \times (V_{OUT} - V_{IN})}{0.4 \times (V_{OUT})^2 \times I_{OUT(MAX)} \times f_{OSC}}$$

where f_{OSC} is the switching frequency. For better system performance, a shielded inductor is preferred to avoid EMI problems.

Output Capacitor Selection

Output ripple voltage is an important index for estimating the performance. This portion consists of two parts, one is the product of I_{IN} and ESR of output capacitor, another part is formed by charging and discharging process of output capacitor. As shown in Figure 3, ΔV_{OUT1} can be evaluated based on the ideal energy equalization. According to the definition of Q, the Q value can be calculated as following equation :

$$Q = \frac{1}{2} \times \left[\left(I_{IN} + \frac{1}{2}\Delta I_L - I_{OUT} \right) + \left(I_{IN} - \frac{1}{2}\Delta I_L - I_{OUT} \right) \right] \times \frac{V_{IN}}{V_{OUT}} \times \frac{1}{f_{OSC}} = C_{OUT} \times \Delta V_{OUT1}$$

where f_{OSC} is the switching frequency and ΔI_L is the inductor ripple current. Move C_{OUT} to left side to estimate the value of ΔV_{OUT1} as following equation :

$$\Delta V_{OUT1} = \frac{D \times I_{OUT}}{\eta \times C_{OUT} \times f_{OSC}}$$

Finally, the output ripple voltage can be determined as following equation :

$$\Delta V_{OUT} = I_{IN} \times ESR + \frac{D \times I_{OUT}}{\eta \times C_{OUT} \times f_{OSC}}$$

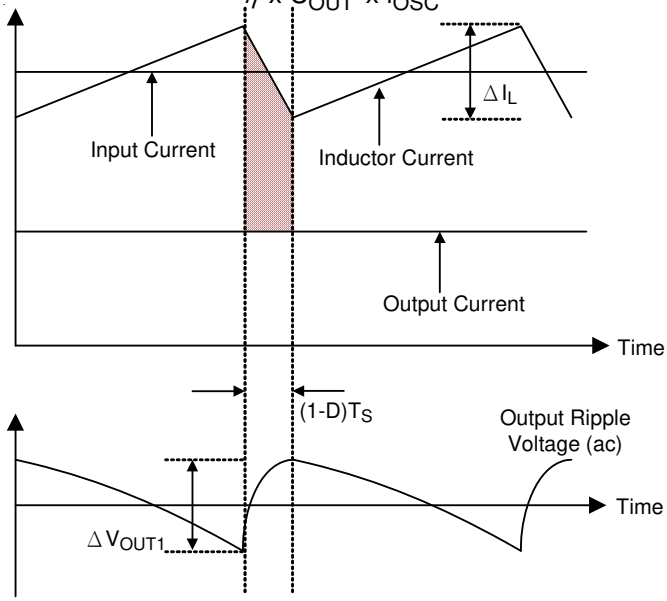


Figure 1. The Output Ripple Voltage without the Contribution of ESR

Input Capacitor Selection

For the power stage, because of the inductor current ripple, the input voltage changes if there is parasite inductance and resistance between the power supply and the inductor. It is recommended to have enough input capacitance to make smaller the input voltage ripple. Generally, three 10μF input capacitances are sufficient for most applications.

The value of the input capacitance C_{IN} of a boost converter is generally selected to limit the input voltage ripple ΔV_{IN} specified by the application. For CCM mode operation, the current flowing through C_{IN} is primarily determined by the inductor ripple current ΔI_L.

The DVIN can be calculated as the following equation :

$$C_{IN} \geq \frac{\Delta I_L \times T_{SW}}{8 \times \Delta V_{IN}}$$

Where ΔI_L is the inductor ripple current and T_{SW} is s witching period. Low ESR ceramic capacitors are recommended for input capacitor applications. Low ESR will effectively reduce the input voltage ripple. The ΔV_{ESR} can be calculated as the following equation :

ΔV_{ESR} = ESR x ΔIL

Another consideration is the voltage rating of the input capacitor which must be greater than the maximum input voltage.

Loop Compensation

The external compensation network of the RT4841 must be compensated by the designer to ensure the stability of the overall loop response. In power-supply design, a power supply is typically defined to be stable if the gain margin is greater than 10dB and the phase margin is greater than 45°. The requirement for stability is typically forcing the loop to cross over with a -1 slope, or -20dB/ Decade in the vicinity of the crossover frequency.

A relationship exists between the phase margin of a second-order closed-loop system and the quality coefficient Q of its transfer function. If the phase margin is too small, the peaking induces high output ringing, exactly as in an RLC circuit. On the contrary, if the phase margin becomes too large, it slows down the system : the overshoot goes away but to the detriment of response and recovery speed.

The stability exercise requires shaping the compensation circuit G(s) in order to provide adequate phase margin at the selected crossover point, together with a high gain in dc. Choose R4 to set high frequency integrator gain for fast transient response and C9 to set the integrator zero to maintain loop stability.

For typical application, V_{IN} = 12V, SWO = 14.5V, C6 = 10μF x 6, L1 = 10μH, while the recommended value for compensation is as follows : R4 = 33kΩ, C9 = 1nF.

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-20L 4x4, the thermal resistance, θ_{JA}, is 28°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C – 25°C) / (28°C/W) = 3.57W for a WQFN-20L 4x4 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 2 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

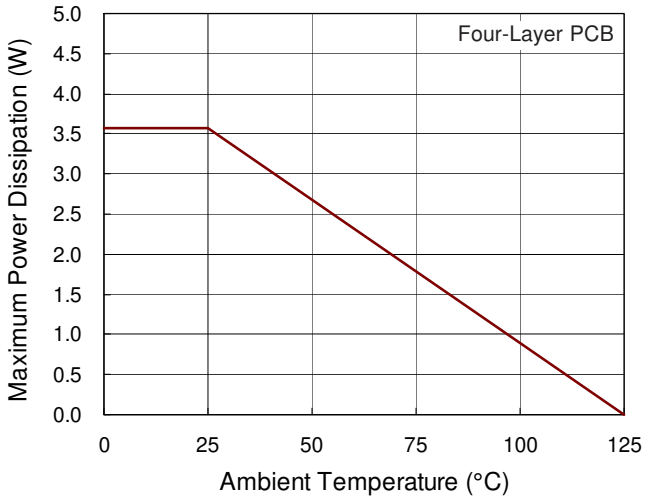


Figure 2. Derating Curve of Maximum Power Dissipation

Layout Considerations

For high frequency switching power supplies, the PCB layout is important to get good regulation, high efficiency and stability. The following descriptions are the guidelines for better PCB layout.

- For good regulation, place the power components as close as possible. The traces should be wide and short enough especially for the high current output loop.
- The feedback voltage divider resistors must be near the feedback pin. The divider center trace must be shorter and the trace must be kept away from any switching nodes.
- The compensation circuit should be kept away from the power loops and be shielded with a ground trace to prevent any noise coupling.
- Minimize the size of the SW node and keep it wide and shorter. Keep the SW node away from the FB.
- The exposed pad of the chip should be connected to a strong ground plane for maximum thermal consideration.

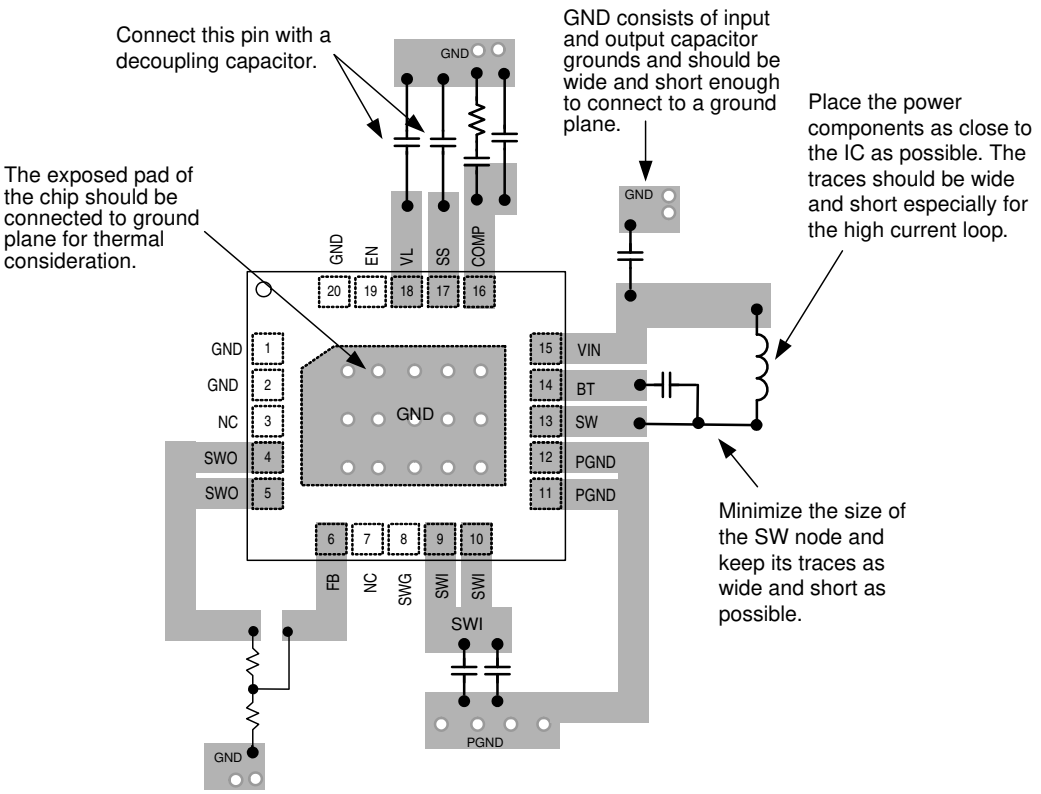
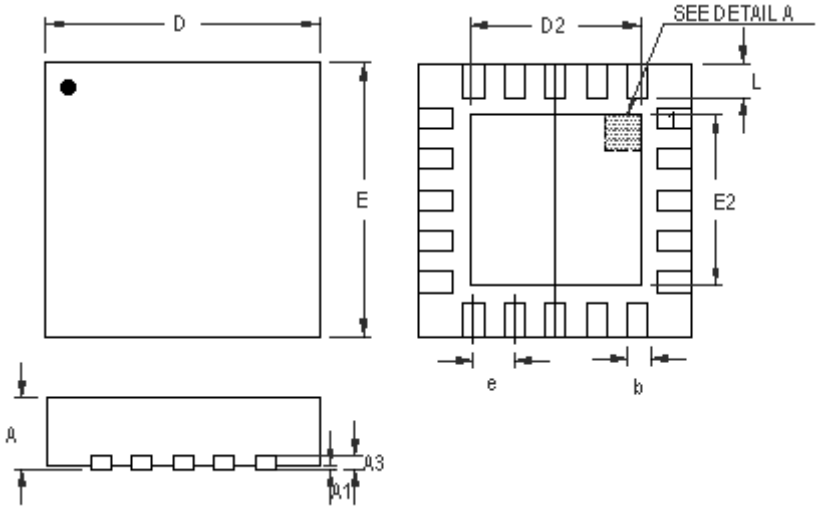
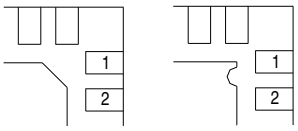


Figure 3. PCB Layout Guide

Outline Dimension





DETAIL A

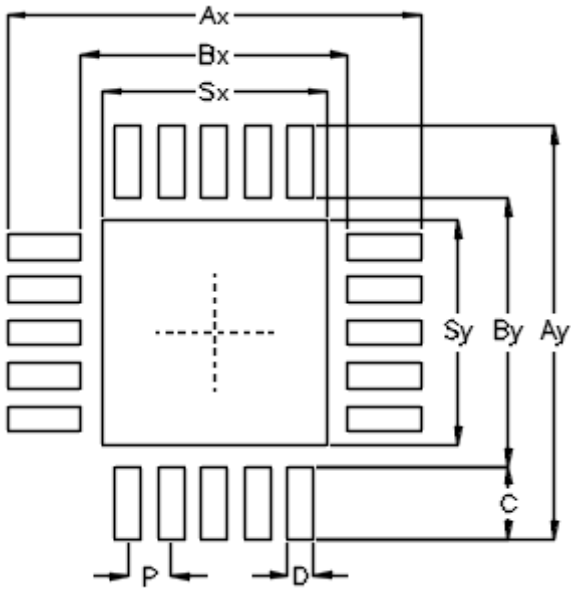
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		0.700	0.800	0.028	0.031
A1		0.000	0.050	0.000	0.002
A3		0.175	0.250	0.007	0.010
b		0.150	0.300	0.006	0.012
D		3.900	4.100	0.154	0.161
D2	Option 1	2.650	2.750	0.104	0.108
	Option 2	2.100	2.200	0.083	0.087
E		3.900	4.100	0.154	0.161
E2	Option 1	2.650	2.750	0.104	0.108
	Option 2	2.100	2.200	0.083	0.087
e		0.500		0.020	
L		0.350	0.450	0.014	0.018

W-Type 20L QFN 4x4 Package

Footprint Information



Package		Number of Pin	Footprint Dimension (mm)								Tolerance
			P	Ax	Ay	Bx	By	C	D	Sx	Sy	
V/W/U/XQFN4*4-20	Option1	20	0.50	4.80	4.80	3.10	3.10	0.85	0.30	2.60	2.60	±0.05
	Option2									2.20	2.20	

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