

NOT RECOMMENDED FOR NEW DESIGN CONTACT US



DMN61D9UDW

DUAL N-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary

BV _{DSS}	R _{DS(ON)} max	I _D max T _A = +25°C	
60V	2Ω @ V _{GS} = 5.0V	250m A	
60 V	2.5Ω @ V _{GS} = 2.5V	350mA	

Description

This MOSFET is designed to minimize the on-state resistance (R_{DS(ON)}) yet maintain superior switching performance, making it ideal for high efficiency power management applications.

Applications

- Motor controls
- · Power management functions

Features

- Dual N-Channel MOSFET
- Low On-Resistance
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- Ultra-Small Surface Mount Package
- ESD Protected Up To 2kV
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- This part is qualified to JEDEC standards (as references in AEC-Q) for High Reliability.

https://www.diodes.com/quality/product-definitions/

 An Automotive-Compliant Part is Available Under Separate Datasheet (<u>DMN61D9UDWQ</u>)

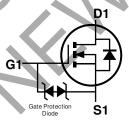
Mechanical Data

- Package: SOT363
- Package Material: Molded Plastic. "Green" Molding Compound.
 UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Matte Tin Finish Annealed over Alloy 42 Leadframe. Solderable per MIL-STD-202, Method 208 (3)
- Terminal Connections: See Diagram
- Weight: 0.006 grams (Approximate)

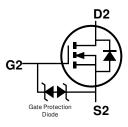




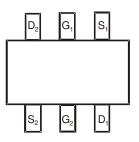
Top View



Q1 N-Channel



Q2 N-Channel



Equivalent Circuit

Top View Pin out

Ordering Information (Note 4)

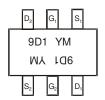
Part Number	Package	Packing			
Part Number	rackaye	Qty.	Carrier		
DMN61D9UDW-7	SOT363	3000	Tape & Reel		
DMN61D9UDW-13	SOT363	10000	Tape & Reel		

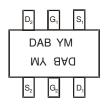
Notes:

- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
- 2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.



Marking Information





9D1 or DAB = Product Type Marking Code YM = Date Code Marking Y or Y = Year (ex: J = 2022) M = Month (ex: 9 = September)

Date Code Key

Year	2015		2022	2023	2024	2025	2026	2027	2028	2029	2030	2031
Code	С		J	K	L	М	N	0	Р	R	S	T
<u> </u>												
Month	.lan	Feh	Mar	Δnr	May	.lun	.lul	Διια	Sen	Oct	Nov	Dec
Month Code	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec

Maximum Ratings (@ $T_A = +25^{\circ}C$, unless otherwise specified.)

Characteristic				Symbol	Value	Unit
Drain-Source Voltage				VDSS	60	V
Gate-Source Voltage			7	Vgss	±20	V
Continuous Drain Current (Note 6) V _{GS} = 5V	Steady State	$T_A = +25^{\circ}C$ $T_A = +70^{\circ}C$		lp	350 290	mA
Maximum Continuous Body Diode Forward Curren	t (Note 6)			ls	0.4	Α
Pulsed Drain Current (10µs Pulse, Duty Cycle = 19	%) (Note 6			IDM	1.2	Α

Thermal Characteristics (@TA = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Total Power Dissipation (Note 5)	PD	320	mW
Thermal Resistance, Junction to Ambient (Note 5)	Steady State R _{0JA}	397	°C/W
Total Power Dissipation (Note 6)	P _D	410	mW
Thermal Resistance, Junction to Ambient (Note 6)	Steady State R _{0JA}	306	°C/W
Operating and Storage Temperature Range	TJ, TSTG	-55 to +150	°C

Notes:

5. Device mounted on FR-4 PCB, with minimum recommended pad layout.6. Device mounted on 1" x 1" FR-4 PCB with high coverage 2oz. Copper, single sided.

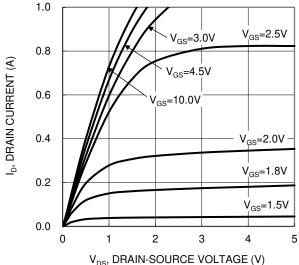


Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition	
OFF CHARACTERISTICS (Note 7)							
Drain-Source Breakdown Voltage	BVDSS	60	_		V	$V_{GS} = 0V, I_D = 250\mu A$	
Zero Gate Voltage Drain Current	IDSS	_	_	1.0	μΑ	$V_{DS} = 60V$, $V_{GS} = 0V$	
Gate-Source Leakage	I _{GSS}	_	_	±10	μΑ	$V_{GS} = \pm 20V, V_{DS} = 0V$	
ON CHARACTERISTICS (Note 7)							
Gate Threshold Voltage	V _{GS(TH)}	0.5	_	1.0	V	$V_{DS} = 10V$, $I_D = 250 \mu A$	
			1.2	2.0		$V_{GS} = 5.0V, I_{D} = 0.05A$	
Static Drain-Source On-Resistance	RDS(ON)	_	1.6	2.5	Ω	$V_{GS} = 2.5V, I_D = 0.05A$	
			2.5	3.5		$V_{GS} = 1.8V, I_D = 0.05A$	
Forward Transconductance	Y _{fs}	200	_	_	mS	$V_{DS} = 10V, I_D = 0.2A$	
Diode Forward Voltage	V _{SD}	_	0.75	1.4	V	$V_{GS} = 0V, I_{S} = 115mA$	
DYNAMIC CHARACTERISTICS (Note 8)	•		•				
Input Capacitance	Ciss	_	28.5	_	pF	201/1/	
Output Capacitance	Coss	_	3.9	.—	pF	V _{DS} = 30V, V _{GS} = 0V f = 1.0MHz	
Reverse Transfer Capacitance	Crss	_	2.5	1	pF	T = 1.0WH2	
Gate Resistance	Rg	_	65	-	Ω	$f = 1MHz$, $V_{GS} = 0V$, $V_{DS} = 0V$	
Total Gate Charge	Qg	_	0.4		nC	V (5)// 10)/	
Gate-Source Charge	Qgs		0.1		nC	Vgs = 4.5V, Vps = 10V,	
Gate-Drain Charge	Q _{gd}		0.1		nC	I _D = 250mA	
Turn-On Delay Time	tD(ON)	1-1	2.1	_	ns		
Turn-On Rise Time	tr	H	1.8		ns	VDD = 30V, VGS = 10V,	
Turn-Off Delay Time	tD(OFF)	+	14.4		ns	$R_G = 25\Omega$, $I_D = 200mA$	
Turn-Off Fall Time	tF	-	8.4		ns		

7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to product testing. Notes:





V_{DS}, DRAIN-SOURCE VOLTAGE (V) Figure 1. Typical Output Characteristic

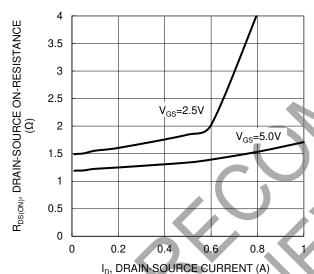


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

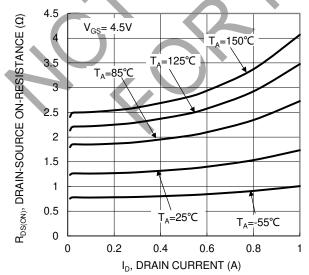


Figure 5. Typical On-Resistance vs. Drain Current and Temperature

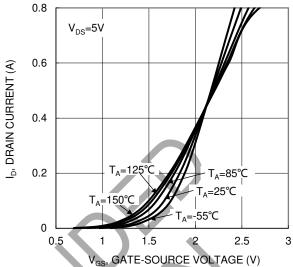
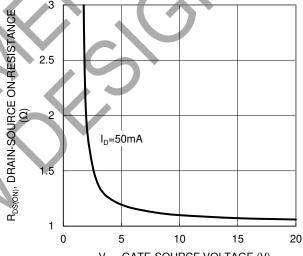


Figure 2. Typical Transfer Characteristic



V_{GS}, GATE-SOURCE VOLTAGE (V) Figure 4. Typical Transfer Characteristic

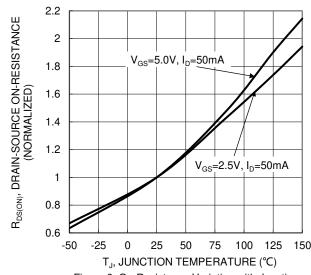


Figure 6. On-Resistance Variation with Junction Temperature





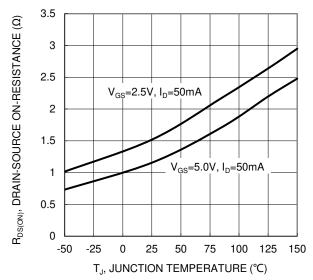
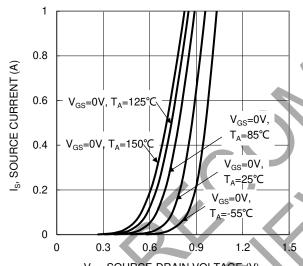
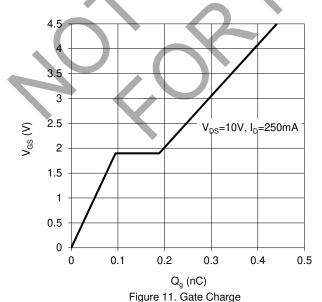


Figure 7. On-Resistance Variation with Junction Temperature



V_{SD}, SOURCE-DRAIN VOLTAGE (V) Figure 9. Diode Forward Voltage vs. Current

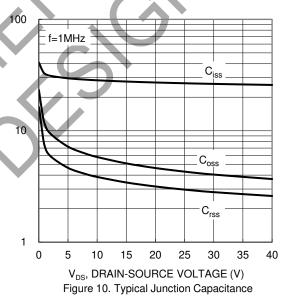


 $V_{GS(TH)},$ GATE THRESHOLD VOLTAGE (V) 1 $I_D=1mA$ 0.8 I_D=250µA 0.6 0.4 -25 50 75 100 125 150 -50 JUNCTION TEMPERATURE (°C) Figure 8. Gate Threshold Variation vs. Junction

1.2

CT, JUNCTION CAPACITANCE

Temperature



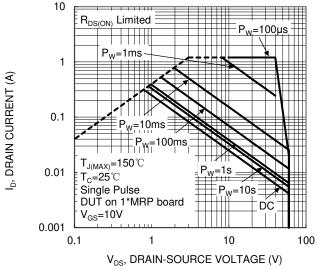


Figure 12. SOA, Safe Operation Area



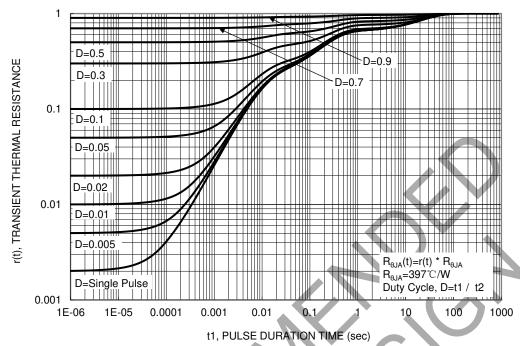
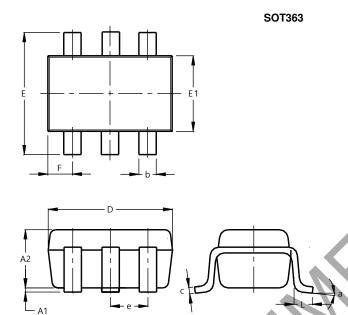


Figure 13. Transient Thermal Resistance



Package Outline Dimensions

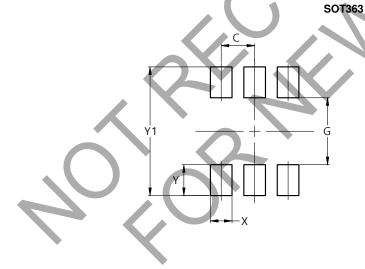
Please see http://www.diodes.com/package-outlines.html for the latest version.



SOT363								
Dim	Min	Max	Тур					
A1	0.00	0.10	0.05					
A2	0.90	1.00	0.95					
b	0.10	0.30	0.25					
С	0.10	0.22	0.11					
D	1.80	2.20	2.15					
E	2.00	2.20	2.10					
E1	1.15	1.35	1.30					
е	Q	.650 E	BSC					
F	0.40	0.45	0.425					
L	0.25	0.40	0.30					
а	0°	8						
All	Dimen	sions	in mm					

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.



Dimensions	Value
Dillielisiolis	(in mm)
С	0.650
G	1.300
Х	0.420
Υ	0.600
Y1	2.500



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