

3-Wire Hall Effect Latch

Features and Benefits

- Wide operating voltage range: from 2.7V to 24V
- Chopper-stabilized amplifier stage
- Built-in negative temperature coefficient
- Reverse Supply Voltage Protection
- High ESD rating / Excellent EMC performance

Applications

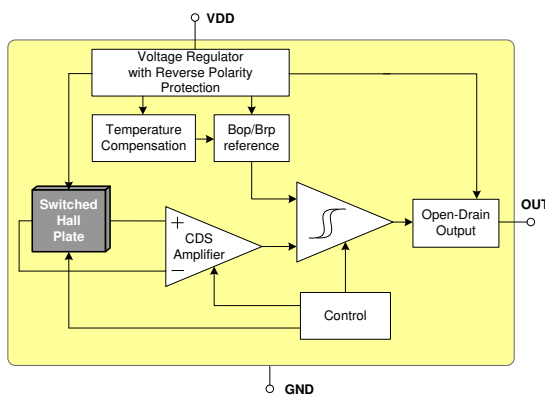
- Consumer and Industrial
- Solid-state switch
- E-Bike
- Motorcycles
- 3-phase BLDC motor commutation

Ordering information

Part No.	Temperature Code	Package Code	Comment
MLX92215LUA-AAA-000-BU	L (-40°C to 150°C)	UA (TO92-3L)	$B_{OP}/B_{RP} = \pm 3\text{mT}$, $TC = -1100\text{ ppm}/^\circ\text{C}$
MLX92215LSE-AAA-000-RE	L (-40°C to 150°C)	SE (TSOT-23)	$B_{OP}/B_{RP} = \pm 3\text{mT}$, $TC = -1100\text{ ppm}/^\circ\text{C}$
MLX92215LSE-ACA-000-RE	L (-40°C to 150°C)	SE (TSOT-23)	$B_{OP}/B_{RP} = \pm 3\text{mT}$, $TC = -2000\text{ ppm}/^\circ\text{C}$ Inverted output
MLX92215LUA-AEA-000-BU	L (-40°C to 150°C)	UA (TO92-3L)	$B_{OP}/B_{RP} = \pm 3\text{mT}$, $TC = -1100\text{ ppm}/^\circ\text{C}$
MLX92215LSE-AEA-000-RE	L (-40°C to 150°C)	SE (TSOT-23)	$B_{OP}/B_{RP} = \pm 3\text{mT}$, $TC = -1100\text{ ppm}/^\circ\text{C}$
MLX92215LSE-AFA-000-RE	L (-40°C to 150°C)	SE (TSOT-23)	North Active MLX92215LSE-AEA-000
MLX92215KLD-AAA-000-RE	K (-40°C to 125°C)	LD (UTQFN)	$B_{OP}/B_{RP} = \pm 3\text{mT}$, $TC = -1100\text{ ppm}/^\circ\text{C}$
MLX92215LST-AAA-000-RE	L (-40°C to 150°C)	ST (SOT-23)	$B_{OP}/B_{RP} = \pm 3\text{mT}$, $TC = -1100\text{ ppm}/^\circ\text{C}$

Option code	HBM
Lxx-AAA, LSE-ACA	4kV
Lxx-AEA, LSE-AFA, KLD-AAA, LST-AAA	8kV

1. Functional Diagram



2. General Description

The Melexis MLX92215 is the second generation Hall-effect latch designed in mixed signal CMOS technology. The device integrates a voltage regulator, Hall sensor with advanced offset cancellation system and an open-drain output driver, all in a single package. Based on the existing platform, the magnetic core is using an improved offset cancellation system allowing faster and more accurate processing while being temperature insensitive and stress independent. In addition is implemented a negative temperature coefficient to compensate the natural behaviour of magnets becoming weaker with rise in temperature.

The included voltage regulator operates from 2.7V to 24V, hence covering a wide range of applications. With the built-in reverse voltage protection, a serial resistor or diode on the supply line is not required so that even remote sensors can be specified for low voltage operation down to 2.7V while being reverse voltage tolerant.

With latching magnetic characteristics, the output is turned low or high respectively with a sufficiently strong South or North pole facing the package top side. When removing the magnetic field, the device keeps its previous state.

Contents

Features and Benefits.....	1
Applications.....	1
Ordering information	1
1. Functional Diagram	1
2. General Description.....	1
3. Absolute Maximum Ratings.....	4
4. General Electrical Specifications.....	5
5. Magnetic Specifications.....	6
5.1. MLX92215LSE-AAA-000 / MLX92215LUA-AAA-000.....	6
5.2. MLX92215LSE-ACA-000.....	6
5.3. MLX92215LUA-AEA-000 / MLX92215LSE-AEA-000	6
5.4. MLX92215LSE-AFA-000	6
5.5. MLX92215KLD-AAA-000	7
5.6. MLX92215LST-AAA-000.....	7
6. Output Behavior versus Magnetic Pole	8
6.1. South Pole Active	8
6.2. North Pole Active	8
7. Performance Graphs	9
7.1. Magnetic parameters vs. T_A	9
7.2. Magnetic parameters vs. V_{DD}	9
7.3. V_{DSon} vs. T_A	9
7.4. V_{DSon} vs. V_{DD}	9
7.5. I_{DD} vs. T_A	9
7.6. I_{DD} vs. V_{DD}	9
7.7. I_{OFF} vs. T_A	10
7.8. I_{OFF} vs. V_{OUT}	10
7.9. SE Power Derating vs. T_A	10
7.10. UA Voltage Derating vs. T_A	10
7.11. LD power Derating vs. T_A	10
8. Application Information.....	11
8.1. Typical Three-Wire Application Circuit.....	11
9. Standard information regarding manufacturability of Melexis products with different soldering processes.....	12

10. ESD Precautions12

11. Packages.....13

 11.1. TSOT-3L (SE Package)13

 11.2. TO92-3L (UA Package)15

 11.3. UTQFN (LD Package)17

 11.4. SOT-3L (ST Package)19

12. Contact.....21

13. Disclaimer.....21

3. Absolute Maximum Ratings

Parameter	Symbol	Value	Units
Supply Voltage ^(1, 2)	V _{DD}	+27	V
Supply Voltage (Load dump) ^(1, 3)	V _{DD}	+32	V
Supply Current ^(1, 2, 4)	I _{DD}	+20	mA
Supply Current ^(1, 3, 4)	I _{DD}	+50	mA
Reverse Supply Voltage ^(1, 2)	V _{DDREV}	-24	V
Reverse Supply Voltage (Load dump) ^(1, 3)	V _{DDREV}	-30	V
Reverse Supply Current ^(1, 2, 5)	I _{DDREV}	-20	mA
Reverse Supply Current ^(1, 3, 5)	I _{DDREV}	-50	mA
Output Voltage ^(1, 2)	V _{OUT}	+27	V
Output Current ^(1, 2, 5)	I _{OUT}	+20	mA
Output Current ^(1, 3, 6)	I _{OUT}	+75	mA
Reverse Output Voltage ⁽¹⁾	V _{OUTREV}	-0.5	V
Reverse Output Current ^(1, 2)	I _{OUTREV}	-50	mA
Operating Temperature Range	T _A	-40 to +150	°C
Storage Temperature Range	T _S	-55 to +165	°C
Maximum Junction Temperature ⁽⁷⁾	T _J	+165	°C
ESD Sensitivity – HBM ^{(8) (9)}	-	4000	V
ESD Sensitivity – HBM ^{(8) (10)}	-	8000	V
ESD Sensitivity – MM ⁽¹¹⁾	-	500	V
ESD Sensitivity – CDM ⁽¹²⁾	-	1000	V
Magnetic Flux Density	B	Unlimited	mT

Exceeding the absolute maximum ratings may cause permanent damage. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

¹ The maximum junction temperature should not be exceeded

² For maximum 1 hour

³ For maximum 0.5 s

⁴ Including current through protection device

⁵ Through protection device

⁶ For V_{OUT} ≤ 27V

⁷ For 1000 hours

⁸ Human Model according AEC-Q100-002 standard

⁹ Valid for version Lxx-AAA and LSE-ACA

¹⁰ Valid for version Lxx-AEA, LSE-AFA, KLD-AAA, LST-AAA

¹¹ Machine Model according AEC-Q100-003 standard

¹² Charged Device Model according AEC-Q100-011 standard

4. General Electrical Specifications

DC Operating Parameters $T_A = -40^{\circ}\text{C}$ to 150°C , $V_{DD} = 2.7\text{V}$ to 24V (unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ ⁽¹⁾	Max	Units
Supply Voltage	V_{DD}	Operating	2.7	-	24	V
Supply Current	I_{DD}		1.5	3.0	4.5	mA
Reverse Supply Current	I_{DDREV}	$V_{DD} = -18\text{V}$			1	mA
Output Leakage Current	I_{OFF}	$V_{OUT} = 12\text{V}$, $V_{DD} = 12\text{V}$, $B < B_{rp}$		0.1	10	μA
Output Saturation Voltage	V_{Dson}	$B > B_{OP}$, $V_{DD} = 3.8$ to 18V , $I_{OUT} = 20\text{mA}$		0.2	0.5	V
Output Rise Time ⁽²⁾ (R_{PU} dependent)	t_R	$V_{DD} = 12\text{V}$, $V_{PU}^{(3)} = 5\text{V}$, $R_{PU} = 1\text{k}\Omega$ $C_{LOAD} = 50\text{pF}$ to GND	0.1	0.3	1	μs
Output Fall Time ⁽²⁾ (On-chip controlled)	t_F	$V_{DD} = 12\text{V}$, $V_{PU} = 5\text{V}$, $R_{PU} = 1\text{k}\Omega$ $C_{LOAD} = 50\text{pF}$ to GND	0.1	0.3	1	μs
Chopping Frequency	f_{CHOP}			340		kHz
Output Refresh Period ⁽²⁾	t_{PER}			6		μs
Delay time ^(2,4)	t_D	Average over 1000 successive switching events @10kHz, square wave with $B \geq 30\text{mT}$, $t_{RISE} = t_{FALL} \leq 20\mu\text{s}$		6		μs
Output Jitter (p-p) ^(2,5)	t_{JITTER}	Over 1000 successive switching events @1kHz, square wave with $B \geq 30\text{mT}$, $t_{RISE} = t_{FALL} \leq 100\mu\text{s}$		± 3		μs
Maximum Switching Frequency ^(2,6)	f_{SW}	$B \geq 30\text{mT}$ and square wave magnetic field	30	50		kHz
Power-On Time ^(7,8)	t_{ON}	$V_{DD} = 5\text{V}$, $dV_{DD}/dt > 2\text{V}/\mu\text{s}$		16	35	μs
SE Package Thermal Resistance	R_{TH}	Single layer (1S) Jedec board		300		$^{\circ}\text{C}/\text{W}$
UA Package Thermal Resistance	R_{TH}	Single layer (1S) Jedec board		200		$^{\circ}\text{C}/\text{W}$
LD Package Thermal Resistance	R_{TH}	Single layer (1S) Jedec board		250		$^{\circ}\text{C}/\text{W}$

¹ Typical values are defined at $T_A = +25^{\circ}\text{C}$ and $V_{DD} = 12\text{V}$

² Guaranteed by design and verified by characterization, not production tested

³ R_{PU} and V_{PU} are respectively the external pull-up resistor and pull-up power supply

⁴ The Delay Time is the time from magnetic threshold reached to the start of the output switching

⁵ Output jitter is the unpredictable deviation of the Delay time

⁶ Maximum switching frequency corresponds to the maximum frequency of the applied magnetic field which is detected without loss of pulses

⁷ The Power-On Time represents the time from reaching $V_{DD} = V_{POR}$ to the first refresh of the output (first valid output state)

⁸ Power-On Slew Rate (is not critical for the proper device start-up)

5. Magnetic Specifications

5.1. MLX92215LSE-AAA-000 / MLX92215LUA-AAA-000

DC Operating Parameters $V_{DD} = 3.8$ to $24V$, $T_A = -40^{\circ}C$ to $150^{\circ}C$

Test Condition	Operating Point B_{OP} (mT)			Release Point B_{RP} (mT)			TC (ppm/ $^{\circ}C$)	Active Pole
	Min	Typ ⁽¹⁾	Max	Min	Typ ⁽¹⁾	Max		
$T_J = -40^{\circ}C$	1	3.2	5	-5	-3.2	-1	-1100	South Pole
$T_J = 25^{\circ}C$	1	3	5	-5	-3.0	-1		
$T_J = 150^{\circ}C$	0.5	2.6	5	-5	-2.6	-0.5		

5.2. MLX92215LSE-ACA-000

DC Operating Parameters $V_{DD} = 3.8$ to $24V$, $T_A = -40^{\circ}C$ to $150^{\circ}C$

Test Condition	Operating Point B_{OP} (mT)			Release Point B_{RP} (mT)			TC (ppm/ $^{\circ}C$)	Active Pole
	Min	Typ ⁽¹⁾	Max	Min	Typ ⁽¹⁾	Max		
$T_J = -40^{\circ}C$	1.2	3.2	5.5	-5.5	-3.2	-1.2	-2000	North Pole
$T_J = 25^{\circ}C$	1.0	2.8	4.7	-4.7	-2.8	-1.0		
$T_J = 150^{\circ}C$	0.5	2.1	4.2	-4.2	-2.1	-0.5		

5.3. MLX92215LUA-AEA-000 / MLX92215LSE-AEA-000

DC Operating Parameters $V_{DD} = 3.8$ to $24V$, $T_A = -40^{\circ}C$ to $150^{\circ}C$

Test Condition	Operating Point B_{OP} (mT)			Release Point B_{RP} (mT)			TC (ppm/ $^{\circ}C$)	Active Pole
	Min	Typ ⁽¹⁾	Max	Min	Typ ⁽¹⁾	Max		
$T_J = -40^{\circ}C$	1	3.2	5	-5	-3.2	-1	-1100	South Pole
$T_J = 25^{\circ}C$	1	3	5	-5	-3.0	-1		
$T_J = 150^{\circ}C$	0.5	2.6	5	-5	-2.6	-0.5		

5.4. MLX92215LSE-AFA-000

DC Operating Parameters $V_{DD} = 3.8$ to $24V$, $T_A = -40^{\circ}C$ to $150^{\circ}C$

Test Condition	Operating Point B_{OP} (mT)			Release Point B_{RP} (mT)			TC (ppm/ $^{\circ}C$)	Active Pole
	Min	Typ ⁽¹⁾	Max	Min	Typ ⁽¹⁾	Max		
$T_J = -40^{\circ}C$	1	3.2	5	-5	-3.2	-1	-1100	North Pole
$T_J = 25^{\circ}C$	1	3	5	-5	-3.0	-1		
$T_J = 150^{\circ}C$	0.5	2.6	5	-5	-2.6	-0.5		

¹ Typical values are defined at $T_A = +25^{\circ}C$ and $V_{DD} = 12V$

5.5. MLX92215KLD-AAA-000

DC Operating Parameters $V_{DD} = 3.8$ to $24V$, $T_A = -40^\circ C$ to $125^\circ C$

Test Condition	Operating Point B_{OP} (mT)			Release Point B_{RP} (mT)			TC (ppm/°C)	Active Pole
	Min	Typ ⁽¹⁾	Max	Min	Typ ⁽¹⁾	Max		
$T_J = -40^\circ C$	1	3.2	5	-5	-3.2	-1	-1100	South Pole
$T_J = 25^\circ C$	1	3	5	-5	-3.0	-1		
$T_J = 125^\circ C$	0.5	2.6	5	-5	-2.6	-0.5		

5.6. MLX92215LST-AAA-000

DC Operating Parameters $V_{DD} = 3.8$ to $24V$, $T_A = -40^\circ C$ to $150^\circ C$

Test Condition	Operating Point B_{OP} (mT)			Release Point B_{RP} (mT)			TC (ppm/°C)	Active Pole
	Min	Typ ⁽¹⁾	Max	Min	Typ ⁽¹⁾	Max		
$T_J = -40^\circ C$	1	3.2	5	-5	-3.2	-1	-1100	South Pole
$T_J = 25^\circ C$	1	3	5	-5	-3.0	-1		
$T_J = 150^\circ C$	0.5	2.6	5	-5	-2.6	-0.5		

Note: $TC = \frac{B_{T_2} - B_{T_1}}{B_{25^\circ C} \times (T_2 - T_1)} \times 10^6, \left[\frac{ppm}{^\circ C} \right]; T_1 = -40^\circ C; T_2 = 150^\circ C$

¹ Typical values are defined at $T_A = +25^\circ C$ and $V_{DD} = 12V$

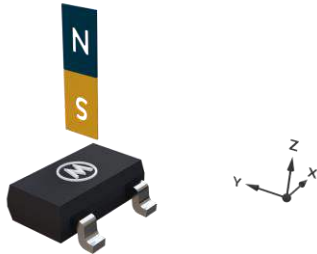
6. Output Behavior versus Magnetic Pole

Output behaviour versus magnetic pole ⁽¹⁾

6.1. South Pole Active

DC Operating Parameters $T_A = -40^{\circ}\text{C}$ to 150°C , $V_{DD} = 2.7\text{V}$ to 24V

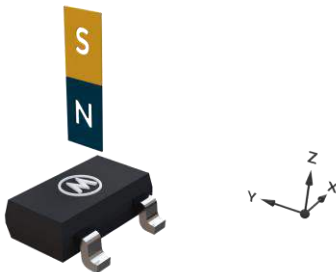
Parameter	Test Conditions	OUT
South pole	$B > B_{OP}$	Low (V_{DSon})
North pole	$B < B_{RP}$	High (V_{PU}) ⁽²⁾



6.2. North Pole Active

DC Operating Parameters $T_A = -40^{\circ}\text{C}$ to 150°C , $V_{DD} = 2.7\text{V}$ to 24V

Parameter	Test Conditions	OUT
South pole	$B > B_{OP}$	High (V_{PU}) ⁽²⁾
North pole	$B < B_{RP}$	Low (V_{DSon})

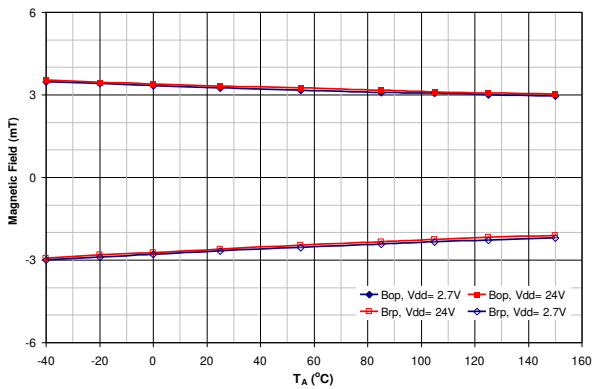


¹ Magnetic pole facing the branded/top side of the package

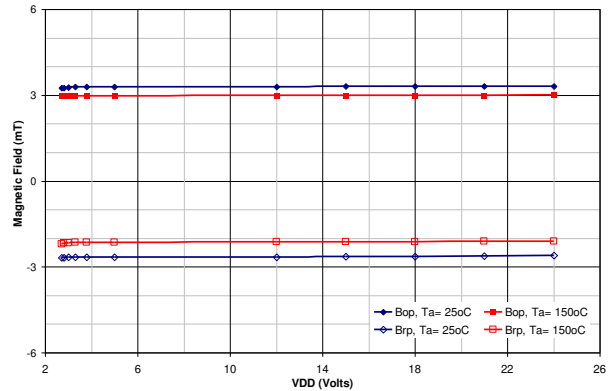
² Default Output state during power-up

7. Performance Graphs

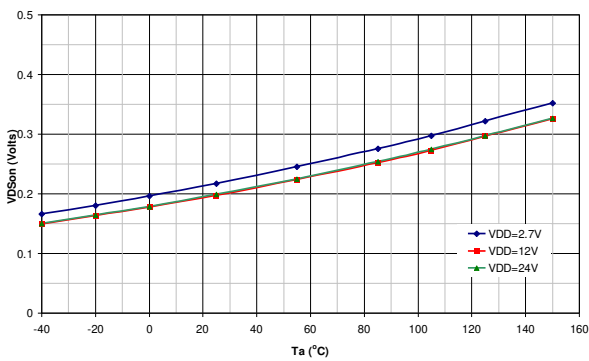
7.1. Magnetic parameters vs. T_A



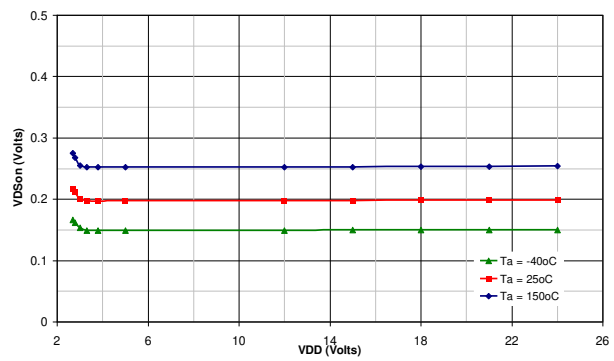
7.2. Magnetic parameters vs. V_{DD}



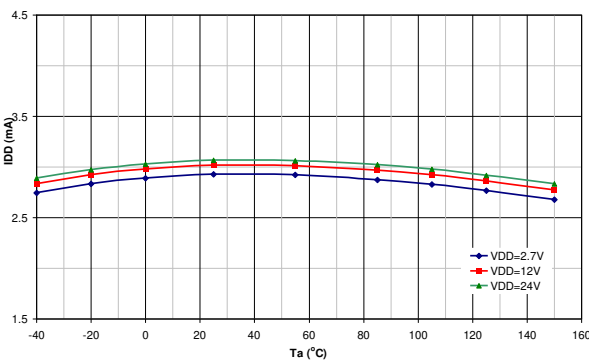
7.3. V_{Dson} vs. T_A



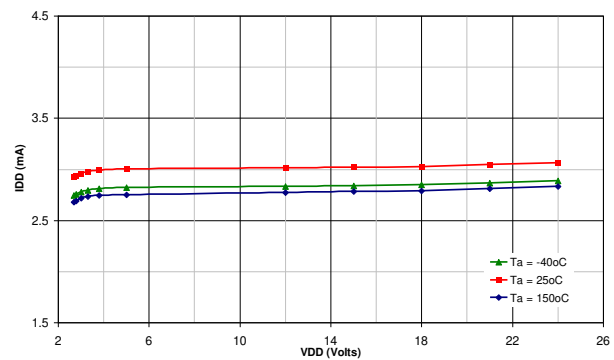
7.4. V_{Dson} vs. V_{DD}



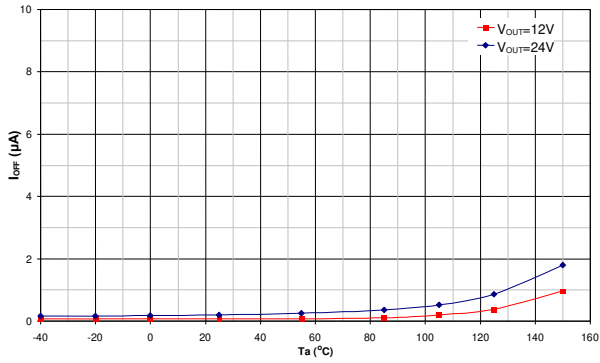
7.5. I_{DD} vs. T_A



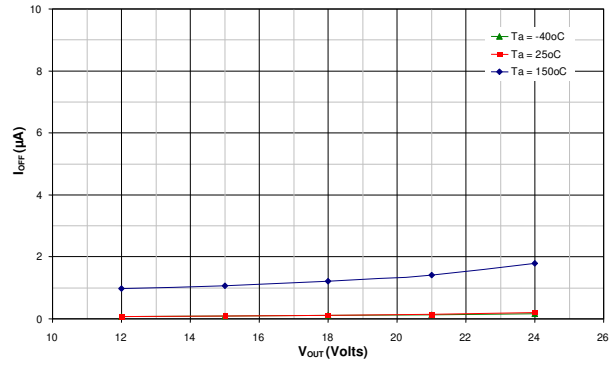
7.6. I_{DD} vs. V_{DD}



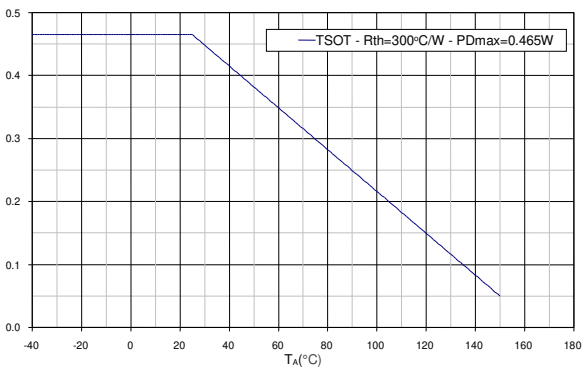
7.7. I_{OFF} vs. T_A



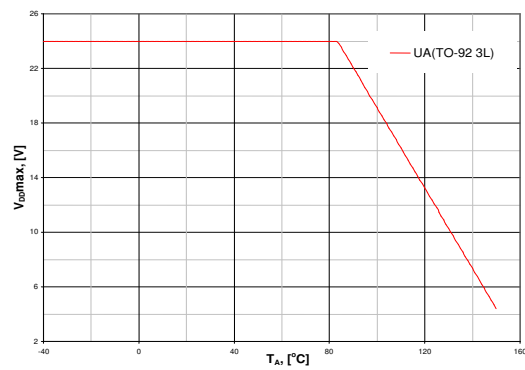
7.8. I_{OFF} vs. V_{OUT}



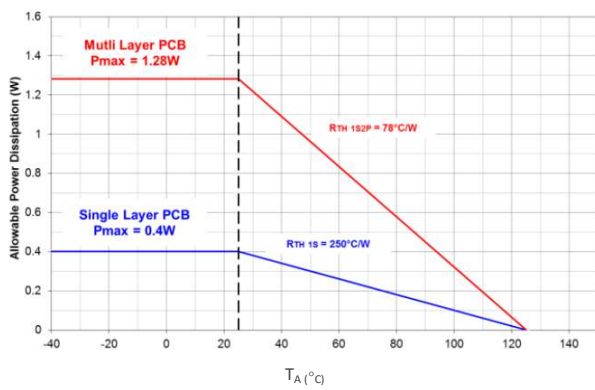
7.9. SE Power Derating vs. T_A



7.10. UA Voltage Derating vs. T_A

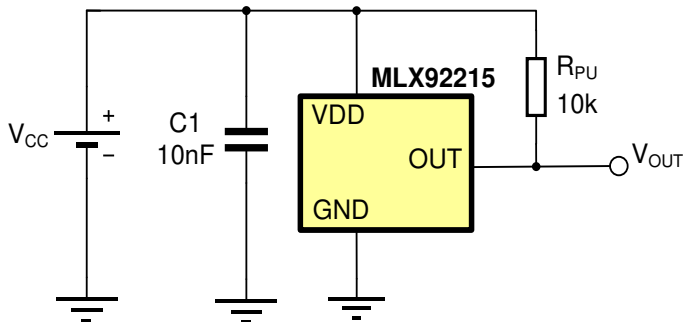


7.11. LD power Derating vs. T_A



8. Application Information

8.1. Typical Three-Wire Application Circuit



Notes:

1. For proper operation, a 10nF to 100nF bypass capacitor should be placed as close as possible to the V_{DD} and ground pin.
2. The pull-up resistor R_{PU} value should be chosen in to limit the current through the output pin below the maximum allowed continuous current for the device.
3. A capacitor connected to the output is not obligatory, because the output slope is generated internally.

9. Standard information regarding manufacturability of Melexis products with different soldering processes

Our products are classified and qualified regarding soldering technology, solderability and moisture sensitivity level according to following test methods:

Reflow Soldering SMD's (Surface Mount Devices)

- IPC/JEDEC J-STD-020
Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices (classification reflow profiles according to table 5-2)
- EIA/JEDEC JESD22-A113
Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing (reflow profiles according to table 2)

Wave Soldering SMD's (Surface Mount Devices) and THD's (Through Hole Devices)

- EN60749-20
Resistance of plastic- encapsulated SMD's to combined effect of moisture and soldering heat
- EIA/JEDEC JESD22-B106 and EN60749-15
Resistance to soldering temperature for through-hole mounted devices

Iron Soldering THD's (Through Hole Devices)

- EN60749-15
Resistance to soldering temperature for through-hole mounted devices

Solderability SMD's (Surface Mount Devices) and THD's (Through Hole Devices)

- EIA/JEDEC JESD22-B102 and EN60749-21
Solderability

For all soldering technologies deviating from above mentioned standard conditions (regarding peak temperature, temperature gradient, temperature profile etc) additional classification and qualification tests have to be agreed upon with Melexis.

The application of Wave Soldering for SMD's is allowed only after consulting Melexis regarding assurance of adhesive strength between device and board.

Melexis is contributing to global environmental conservation by promoting **lead free** solutions. For more information on qualifications of **RoHS** compliant products (RoHS = European directive on the Restriction Of the use of certain Hazardous Substances) please visit the quality page on our website: <http://www.melexis.com/quality.aspx>

10. ESD Precautions

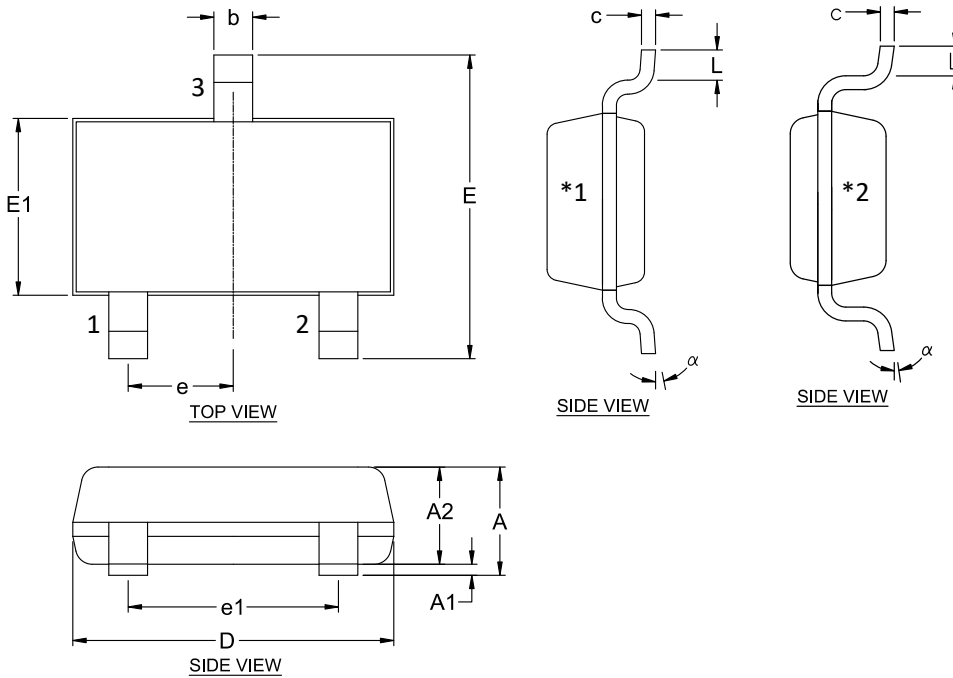
Electronic semiconductor products are sensitive to Electro Static Discharge (ESD).

Always observe Electro Static Discharge control procedures whenever handling semiconductor products.

11. Packages

11.1. TSOT-3L (SE Package)

11.1.1. TSOT-3L – Package dimension



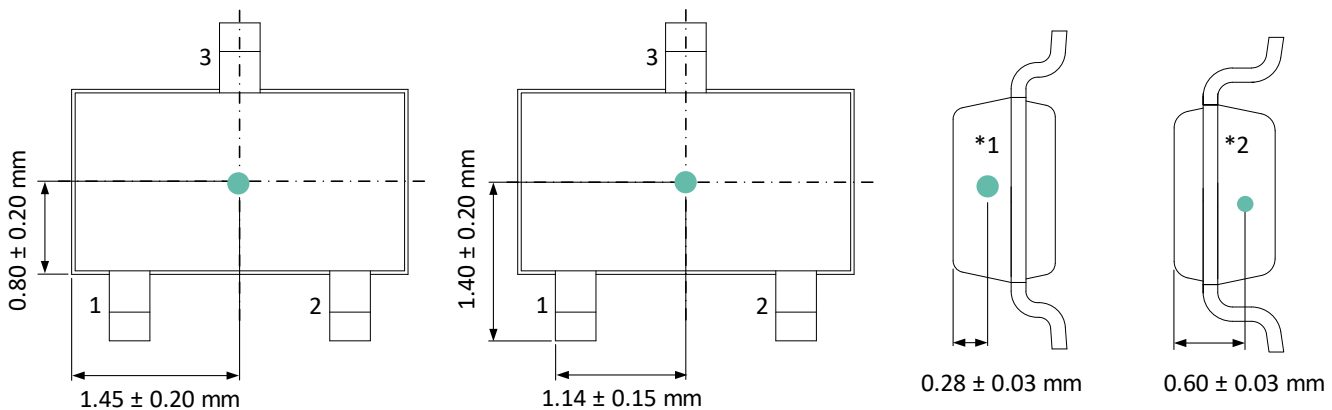
SYMBOL	MINIMUM	MAXIMUM
A	---	1.00
A1	0.025	0.10
A2	0.85	0.90
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.70
L	0.30	0.50
b	0.30	0.45
c	0.10	0.20
e	0.95 BSC	
e1	1.90 BSC	
α	0°	8°

*1 = Valid for AAA,AEA,ACA
*2 = Valid for AFA

NOTE :

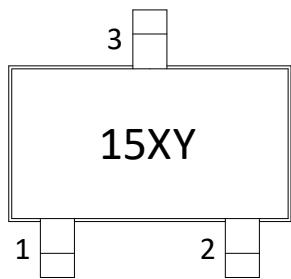
1. ALL DIMENSIONS IN MILLIMETERS (mm) UNLESS OTHERWISE STATED.
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS OF MAX 0.15 mm PER SIDE.
3. DIMENSION E DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS OF MAX 0.25 mm PER SIDE.
4. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION OF MAX 0.07 mm.
5. DIMENSION L IS THE LENGTH OF THE TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. FORMED LEAD SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITH 0.076 mm SEATING PLANE.

11.1.2. TSOT-3L – Sensitive spot

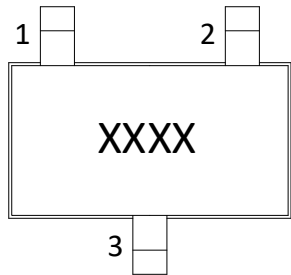
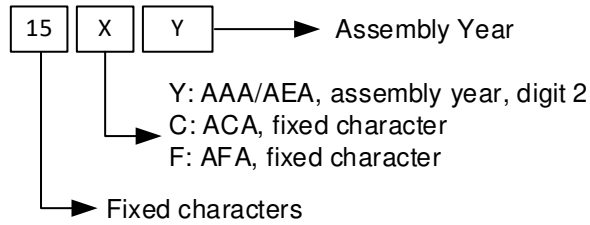


*1 = Valid for AAA,AEA,ACA
*2 = Valid for AFA

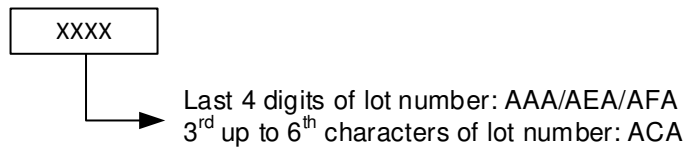
11.1.3. TSOT-3L – Package marking / Pin definition



Top



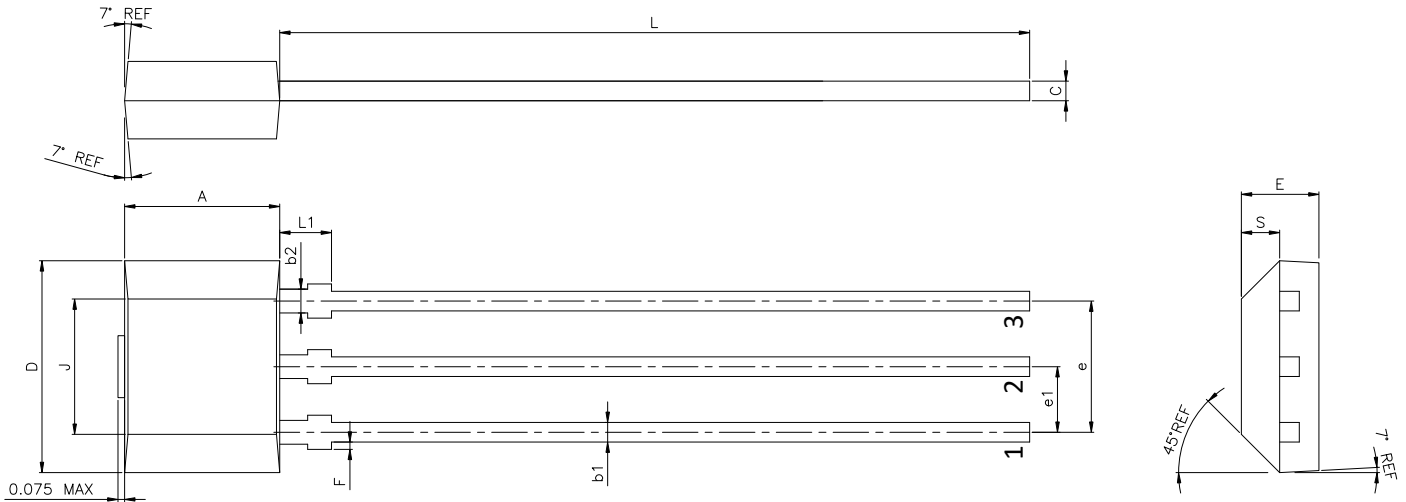
Bottom



Pin #	Name	Type	Function
1	VDD	Supply	Supply Voltage pin
2	OUT	Out	Open drain output pin
3	GND	Ground	Ground pin

11.2. T092-3L (UA Package)

11.2.1. T092-3L – Package dimension

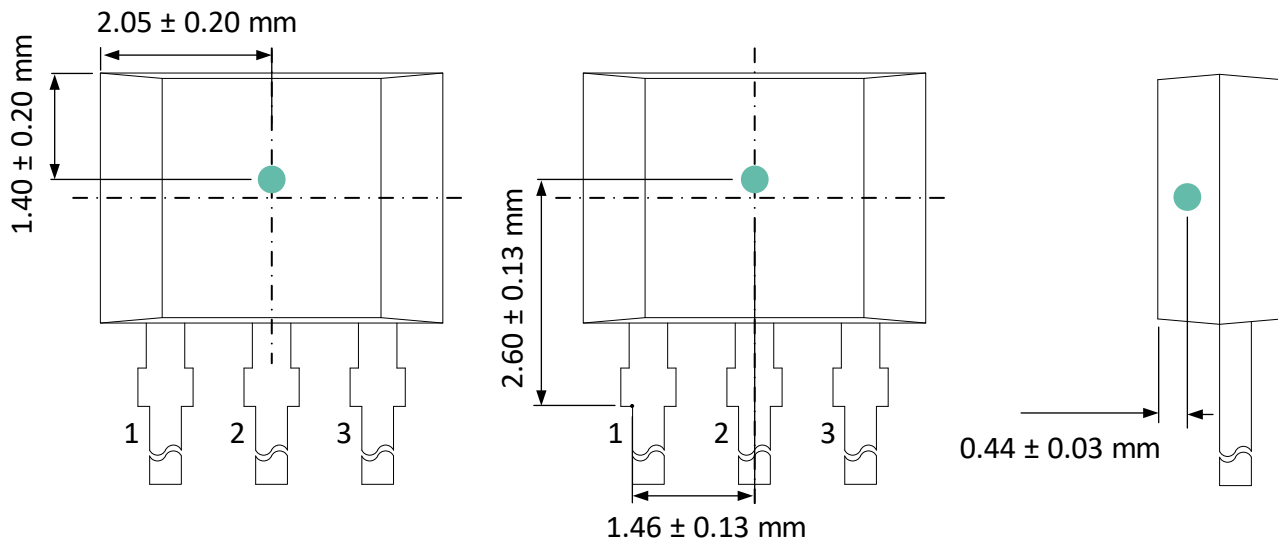


SYMBOL	MINIMUM	MAXIMUM
A	2.90	3.10
D	4.00	4.20
E	1.40	1.60
F	0.00	0.15
J	2.51	2.72
L	14.00	15.00
L1	0.90	1.10
S	0.63	0.84
b1	0.35	0.44
b2	0.43	0.52
c	0.35	0.44
e	2.51	2.57
e1	1.24	1.30

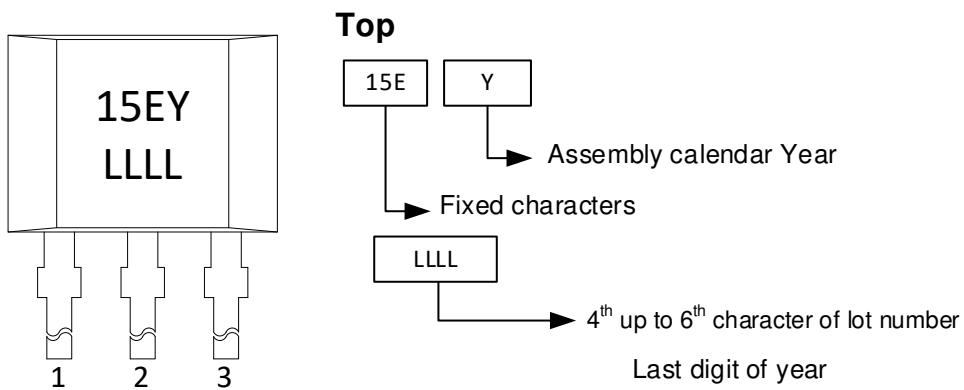
NOTES :

1. DIMENSIONS IN MILLIMETERS (mm) UNLESS NOTED OTHERWISE.
2. PACKAGE DIMENSIONS DO NOT INCLUDE MOLD FLASHES AND PROTRUSIONS.
3. DIMENSION A AND D DO NOT INCLUDE MOLD GATE AND SIDE FLASH (PROTRUSION) OF MAXIMUM 0.127 mm PER SIDE.
4. THE LEADS MAY BE SLIGHTLY DEFORMED DURING TRANSPORTATION IF PACKED IN BULK (BAG), AFFECTING e1 DIMENSION. IT IS RECOMMENDED TO ORDER RADIAL TAPE (REEL OR AMMOPACK) IF SUCH DEFORMATION IS CRITICAL FOR THE LEAD FORMING PROCESS, EVEN IF MANUAL LOADING INTO THE TOOL IS FORESEEN.

11.2.2. T092-3L – Sensitive spot



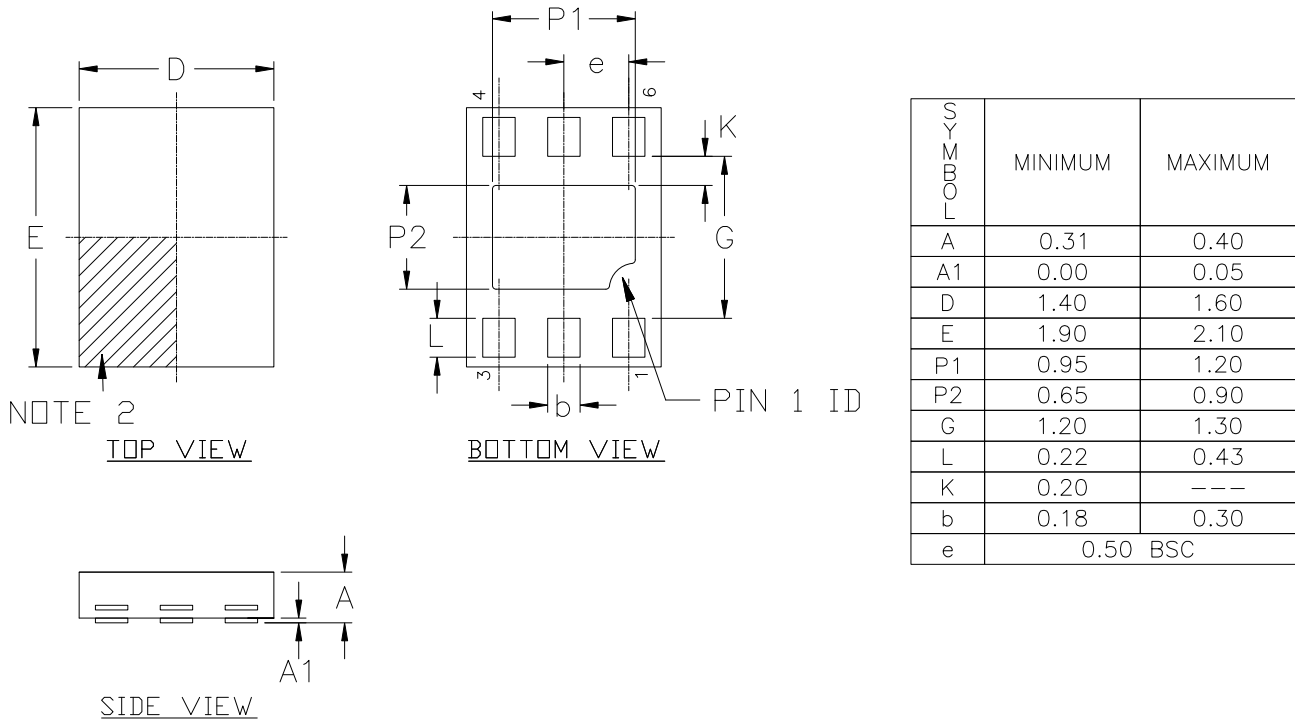
11.2.3. T092-3L – Package marking / Pin definition



Pin #	Name	Type	Function
1	VDD	Supply	Supply Voltage pin
2	GND	Ground	Ground pin
3	OUT	Out	Open drain output pin

11.3. UTQFN (LD Package)

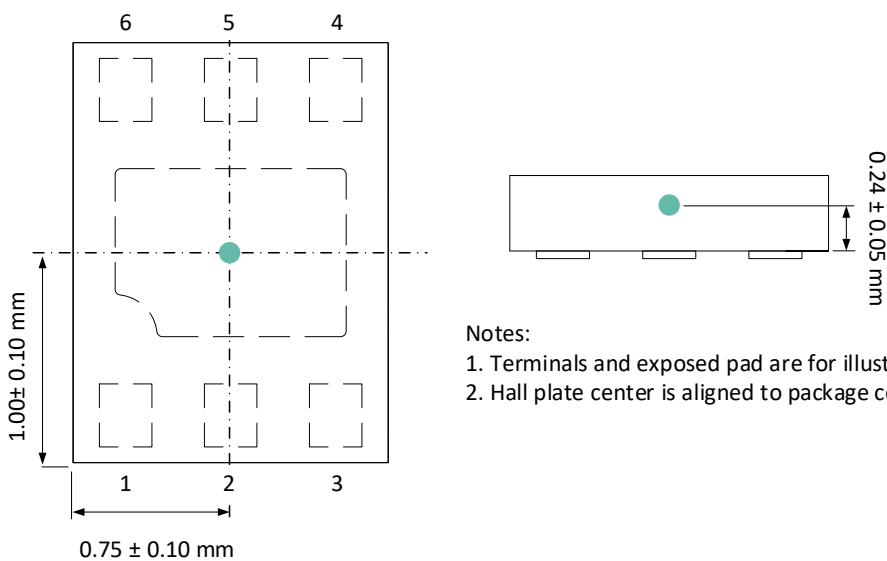
11.3.1. UTQFN – Package dimension



NOTE :

1. ALL DIMENSIONS IN MILLIMETERS (mm).
2. TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM JEDEC PUBLICATION 95 SPP-002. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE IDENTICATED. THE TERMINAL #1 IDENTIFIER MAY BE MARKED FEATURE.
3. EXPOSED TIE BAR SHOULD BE KEPT FREE FROM SOLDER.

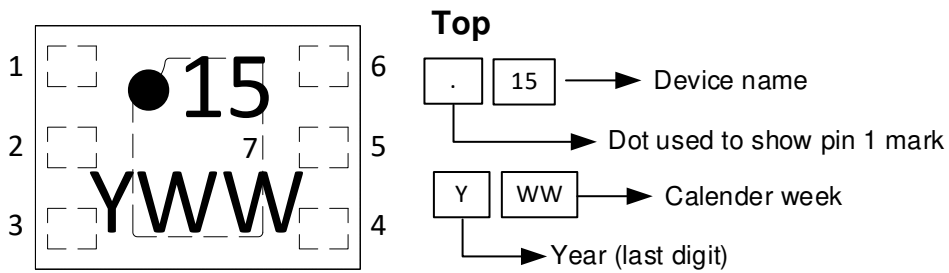
11.3.2. UTQFN – Sensitive spot



Notes:

1. Terminals and exposed pad are for illustration only.
2. Hall plate center is aligned to package center.

11.3.3. UTQFN – Package marking / Pin definition

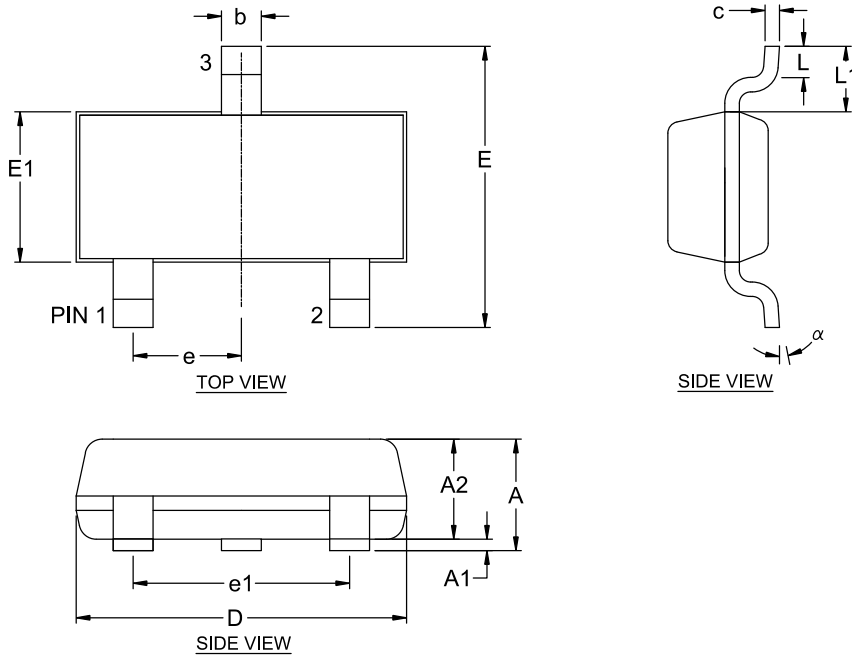


Pin #	Name	Type	Function
1	VDD	Supply	Supply Voltage pin
2,6	N.C.		Not connected
3,4	GND	Ground	Ground pin
5	OUT	Output	Open drain output pin
7	Thermal	Thermal pad	Exposed thermal pad

The exposed pad can be soldered to the PCB to improve thermal dissipation. Can be connected to the ground potential.

11.4. SOT-3L (ST Package)

11.4.1. SOT-3L – Package dimension

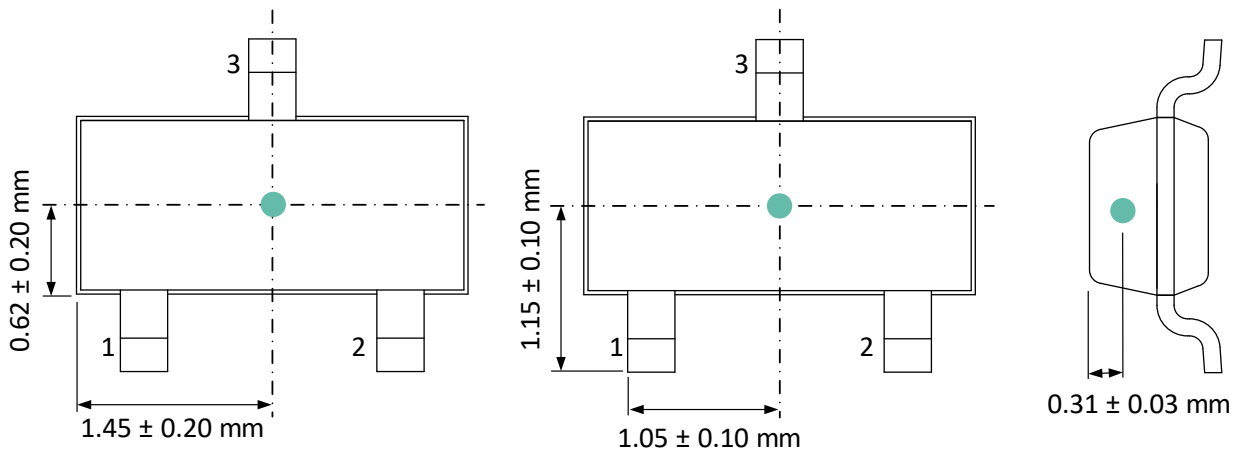


SYMBOL	MINIMUM	MAXIMUM
A	0.89	1.09
A1	0.02	0.08
A2	0.88	1.00
A3	0.41	0.67
A4	0.13	0.38
D	2.80	3.00
E	2.10	2.50
E1	1.19	1.39
L	0.40	0.55
L1	0.54 REF	
b	0.38	0.50
c	0.14	0.16
e	0.95 BSC	
e1	1.90 BSC	
α	0°	5°

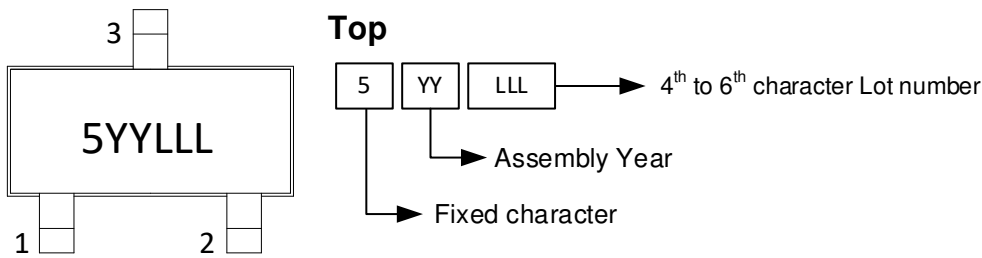
NOTE :

1. ALL DIMENSIONS IN MILLIMETERS (mm) UNLESS OTHERWISE STATED.
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS OF MAX 0.152 mm PER SIDE.
3. DIMENSION E DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS OF MAX 0.152 mm PER SIDE.
4. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION OF MAX 0.07 mm.
5. DIMENSION L IS THE LENGTH OF THE TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. FORMED LEAD SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITH 0.076 mm SEATING PLANE.

11.4.2. SOT-3L – Sensitive spot



11.4.3. SOT-3L – Package marking / Pin definition



Pin #	Name	Type	Function
1	VDD	Supply	Supply Voltage pin
2	OUT	Output	Open drain output pin
3	GND	Ground	Ground pin

12. Contact

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