MOSFET - Power, Single N-Channel, TOLL

40 V, 1.21 mΩ, 240 A

FDBL9406-F085T6

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- Lowers Switching Noise/EMI
- AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	40	V
Gate−to−Source Voltage			V_{GS}	+20/−16	V
Continuous Drain Current $R_{\theta JC}$ (Note 2)	Steady State	T_C = 25°C	I_D	240	A
		T_C = 100°C		179.4	
Power Dissipation $R_{\theta JC}$ (Note 2)		T_C = 25°C	P_D	136.4	W
		T_C = 100°C		68.2	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2)	Steady State	T_A = 25°C	I_D	45	A
		T_A = 100°C		31.8	
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)		T_A = 25°C	P_D	4.3	W
		T_A = 100°C		2.1	
Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		I_{DM}	2817	A
Operating Junction and Storage Temperature Range			T_J, T_{stg}	−55 to +175	°C
Source Current (Body Diode)			I_S	221	A
Single Pulse Drain−to−Source Avalanche Energy ($I_{L(pk)}$ = 42.5 A)			E_{AS}	271	mJ
Lead Temperature Soldering Reflow for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

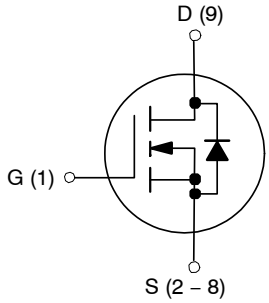
Parameter	Symbol	Value	Unit
Junction−to−Case − Steady State (Note 2)	$R_{\theta JC}$	1.1	°C/W
Junction−to−Ambient − Steady State (Note 2)	$R_{\theta JA}$	35	

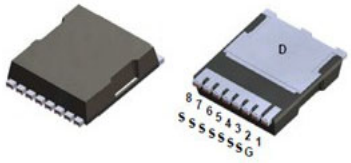
1. Surface−mounted on FR4 board using a 1 in^2 pad size, 1 oz. Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

ON Semiconductor®

www.onsemi.com

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
40 V	1.21 mΩ @ 10 V	240 A





H−PSOF8L
CASE 100CU

ORDERING INFORMATION

Device	Package	Shipping†
FDBL9406−F085T6	H−PSOF8L (Pb−Free)	2000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Table 1. ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Units
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = 250 μA, V_{GS} = 0 V		40			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	I_D = 250 μA, V_{GS} = 0 V			24.9		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V, V_{GS} = 0 V	T_J = 25°C			10	μA
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = +20/−16 V				±100	nA
ON CHARACTERISTICS (Note 3)							
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 190 μA		2	2.8	3.5	V
Negative Threshold Temperature Coefficient	$V_{GS(th)}/T_J$				−6.9		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 50 A			1.1	1.21	mΩ
Forward Transconductance	g_{FS}	V_{DS} = 15 V, I_D = 50 A			143		S
CHARGES & CAPACTIANCES							
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz			4960		pF
Output Capacitance	C_{oss}				2800		pF
Reverse Transfer Capacitance	C_{rss}				62		pF
Total Gate Charge	$Q_{G(tot)}$	V_{GS} = 10 V, V_{DS} = 20 V, I_D = 50 A			75		nC
Threshold Gate Charge	$Q_{G(th)}$				9		nC
Gate−to−Source Charge	Q_{gs}				22		nC
Gate−to−Drain Charge	Q_{gd}				16		nC
SWITCHING CHARACTERISTICS, V_{GS} = 10 V (Note 3)							
Turn−On Delay Time	$t_{d(on)}$	V_{GS} = 10 V, V_{DS} = 20 V, I_D = 50 A, R_G = 6 Ω			27		ns
Rise Time	t_r				44		ns
Turn−Off Delay Time	$t_{d(off)}$				61		ns
Fall Time	t_f				26		ns
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	I_S = 50 A, V_{GS} = 0 V	T_J = 25°C		0.8	1.2	V
		I_S = 50 A, V_{GS} = 0 V	T_J = 125°C		0.6		V
Reverse Recovery Time	t_{rr}	V_{GS} = 0 V, dI_S/d_t = 100 A/μs, I_S = 50 A			78		ns
Charge Time	t_a				39		ns
Discharge Time	t_b				39		ns
Reverse Recovery Charge	Q_{rr}				101		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Switching characteristics are independent of operating junction temperatures

TYPICAL CHARACTERISTICS

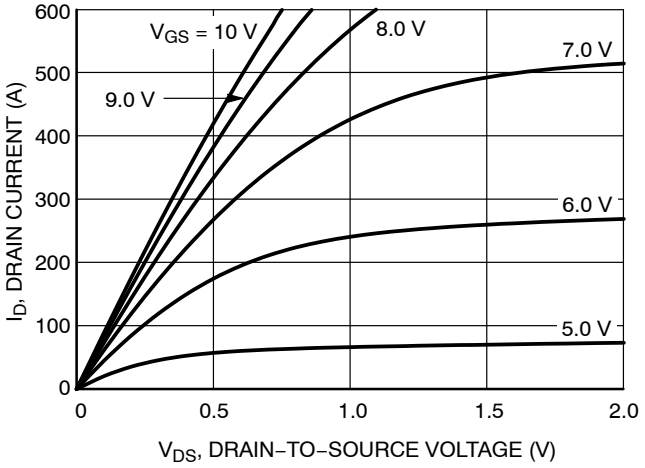


Figure 1. On−Region Characteristics

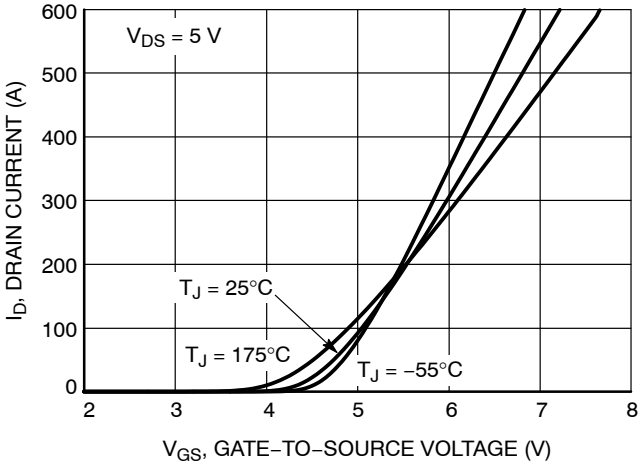


Figure 2. Transfer Characteristics

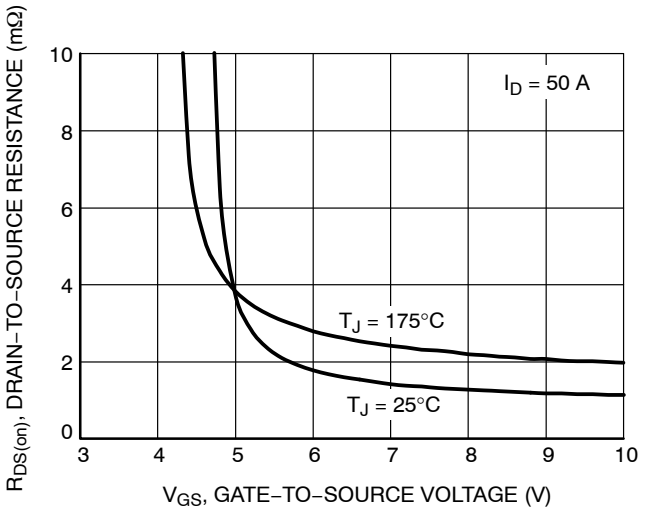


Figure 3. On−Resistance vs. Gate−to−Source Voltage

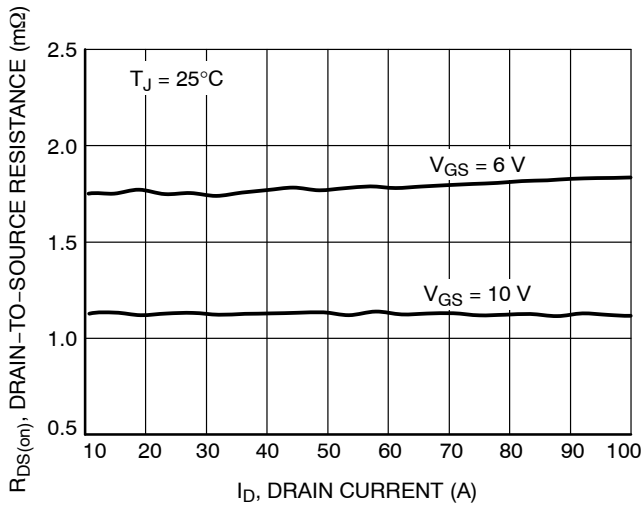


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

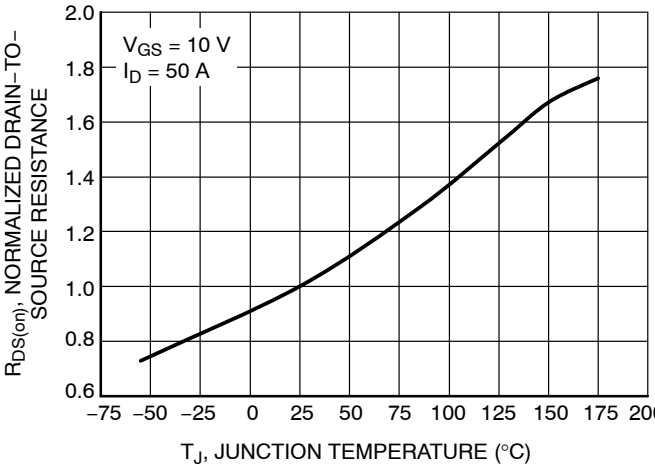


Figure 5. On−Resistance Variation with Temperature

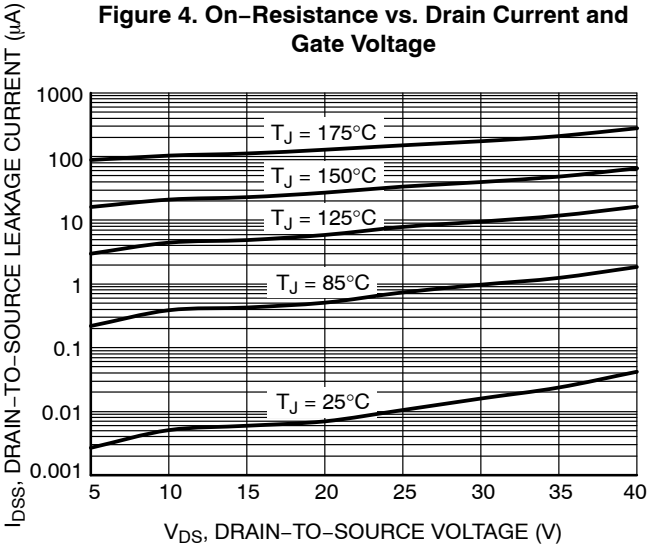


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

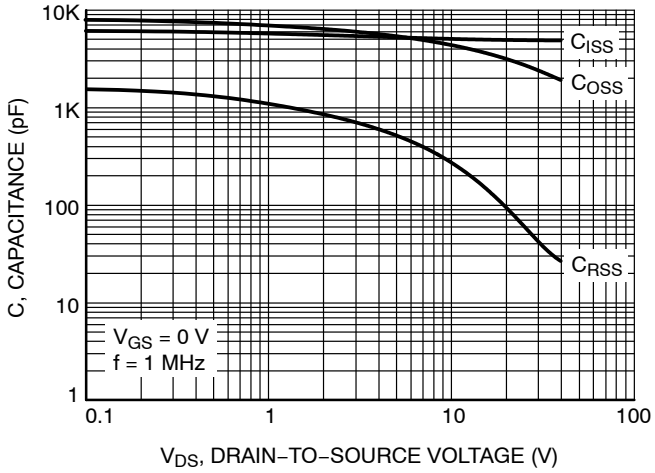


Figure 7. Capacitance Variation

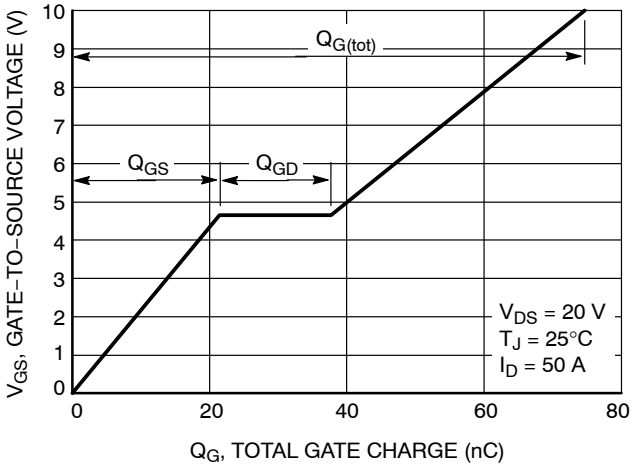


Figure 8. Gate−to−Source Voltage vs. Total Charge

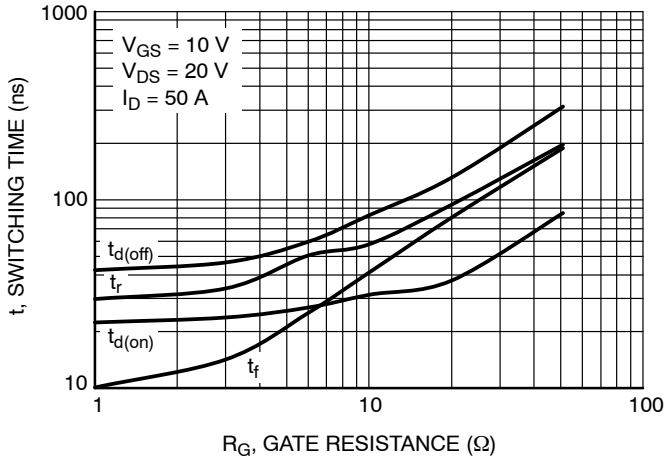


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

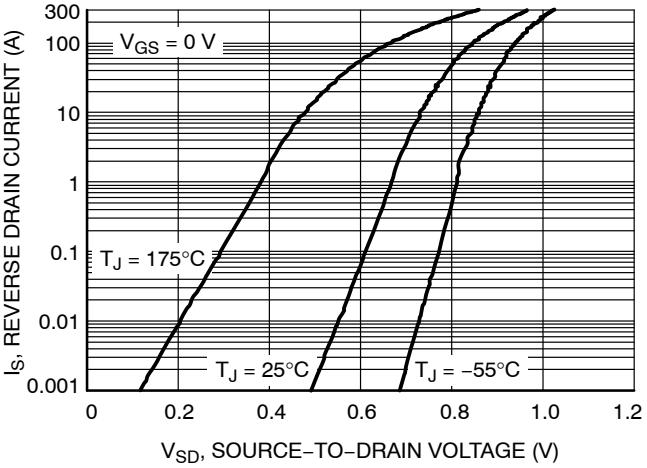


Figure 10. Diode Forward Voltage vs. Current

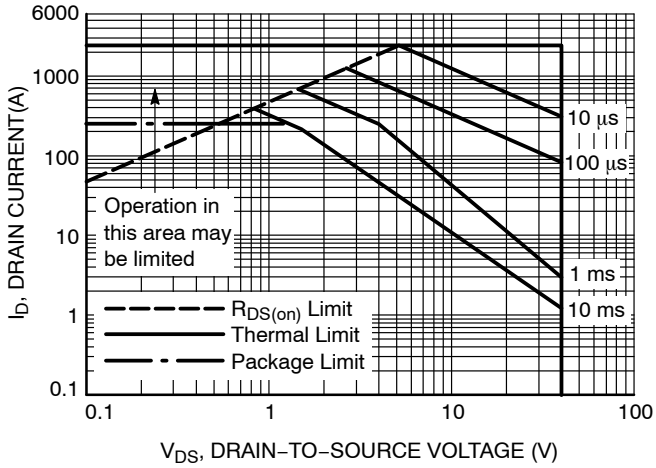


Figure 11. Maximum Rated Forward Biased Safe Operating Area

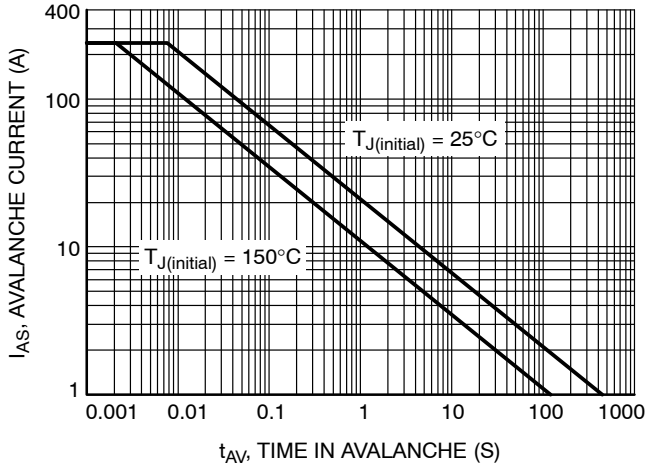


Figure 12. Maximum Drain Current vs. Time in Avalanche

TYPICAL CHARACTERISTICS

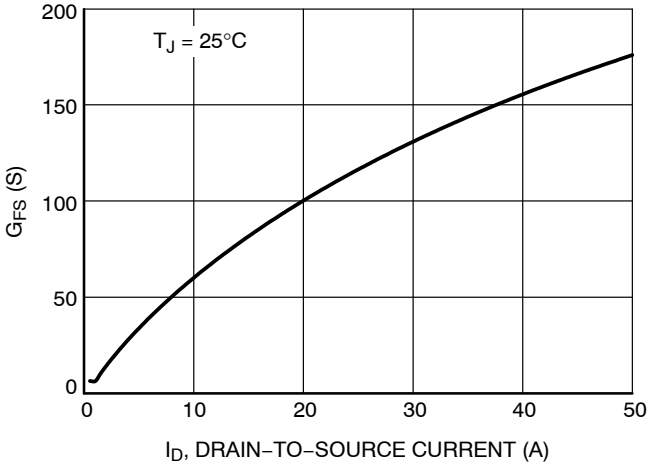


Figure 13. G_{FS} vs. I_D

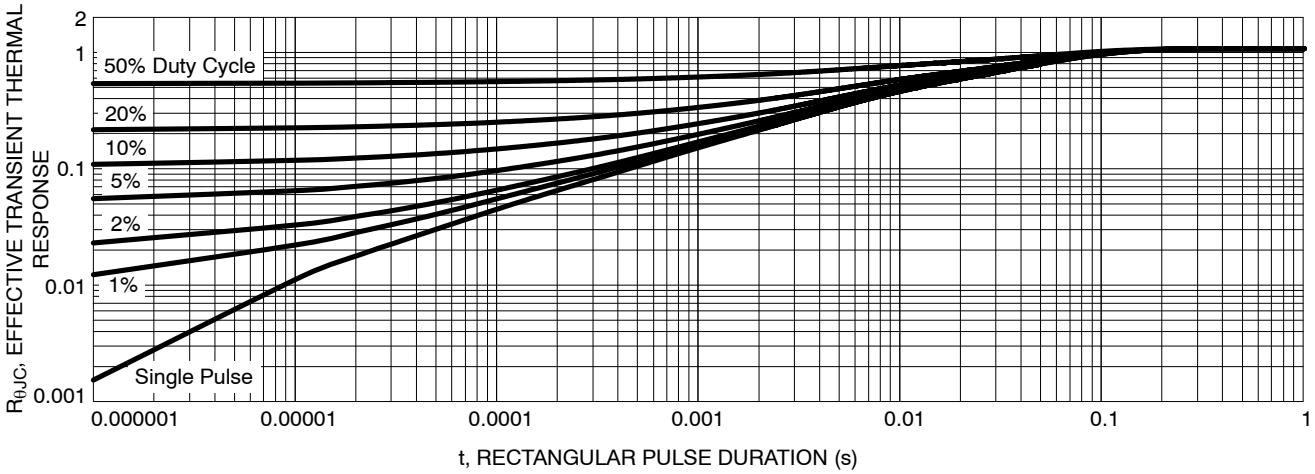
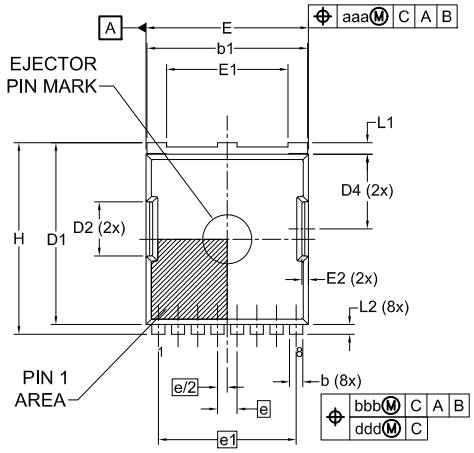


Figure 14. Thermal Response

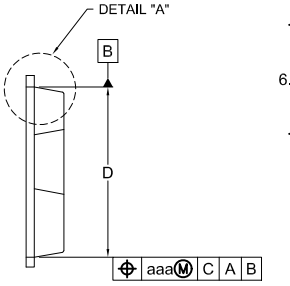
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

H−PSOF8L 11.68x9.80
CASE 100CU
ISSUE C

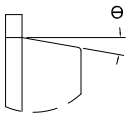
DATE 22 MAY 2023



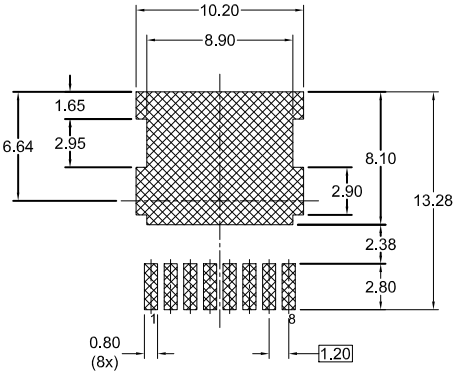
TOP VIEW



SIDE VIEW

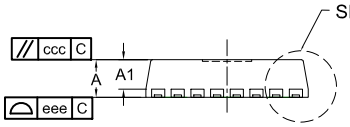


DETAIL "A"
SCALE: 2X

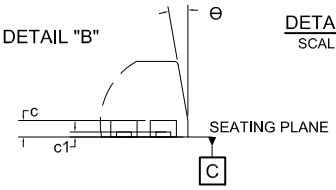


LAND PATTERN
RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.



FRONT VIEW



DETAIL "B"
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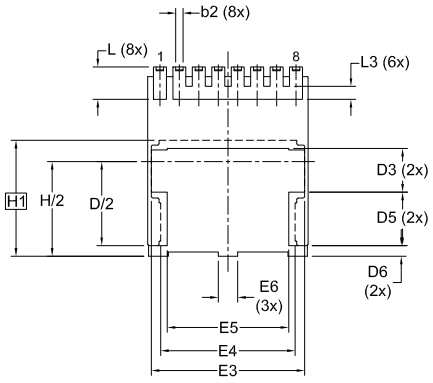


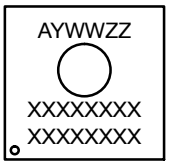
BOTTOM VIEW

NOTES:
1. PACKAGE STANDARD REFERENCE: JEDEC MO-299, ISSUE A.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
3. CONTROLLING DIMENSION: MILLIMETERS.
4. COPLANARITY APPLIES TO THE EXPOSED WELL AS THE TERMINALS.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
6. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.20	2.30	2.40
A1	1.70	1.80	1.90
b	0.70	0.80	0.90
b1	9.70	9.80	9.90
b2	0.35	0.45	0.55
c	0.40	0.50	0.60
c1	0.10	—	—
D	10.28	10.38	10.48
D/2	5.09	5.19	5.29
D1	10.98	11.08	11.18
D2	3.20	3.30	3.40
D3	2.60	2.70	2.80
D4	4.45	4.55	4.65
D5	3.20	3.30	3.40
D6	0.55	0.65	0.75
E	9.80	9.90	10.00
E1	7.30	7.40	7.50
E2	0.30	0.40	0.50
E3	9.36	9.46	9.56

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
E4	8.20	8.30	8.40
E5	7.40	7.50	7.60
E6	1.10	1.20	1.30
e	1.20 BSC		
e/2	0.60 BSC		
e1	8.40 BSC		
H	11.58	11.68	11.78
H/2	5.74	5.84	5.94
H1	7.15 BSC		
L	1.90	2.00	2.10
L1	0.60	0.70	0.80
L2	0.50	0.60	0.70
L3	0.70	0.80	0.90
Θ	0°	—	12°
aaa	0.20		
bbb	0.25		
ccc	0.20		
ddd	0.20		
eee	0.10		

GENERIC MARKING DIAGRAM*



A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code
XXXX = Specific Device Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**H−PSOF8L 11.68x9.80**	**PAGE 1 OF 1**

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