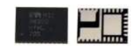
MIC38300

HELDO®
3A High-Efficiency Low Dropout Regulator



HELDO®

General Description

The MIC38300 is a 3A peak, 2.2A continuous output current step down converter. This is the first device in a new generation of HELDO® (High-Efficiency Low Dropout) regulators that provide the benefits of an LDO in respect to ease of use, fast transient performance, high PSRR, and low noise while offering the efficiency of a switching regulator.

As output voltages move lower, the output noise and transient response of a switching regulator become an increasing challenge for designers. By combining a switcher whose output is slaved to the input of a high-performance LDO, high efficiency is achieved with a clean low noise output. The MIC38300 is designed to provide less than 5mV of peak to peak noise and over 70dB of PSRR at 1kHz. Furthermore, the architecture of the MIC38300 is optimized for fast load transients that allow maintenance of less than 30mV of output voltage deviation even during ultra-fast load steps, making the MIC38300 an ideal choice for low-voltage ASICs and other digital ICs.

The MIC38300 features a fully-integrated switching regulator and LDO combo, operates with input voltages from 3.0V to 5.5V input, and offers adjustable output voltages down to 1.0V.

The MIC38300 is offered in the small 28-pin 4mm × 6mm × 0.9mm MLF® package and can operate from –40°C to +125°C.

Datasheets and support documentation are available on Micrel's web site at: www.micrel.com.

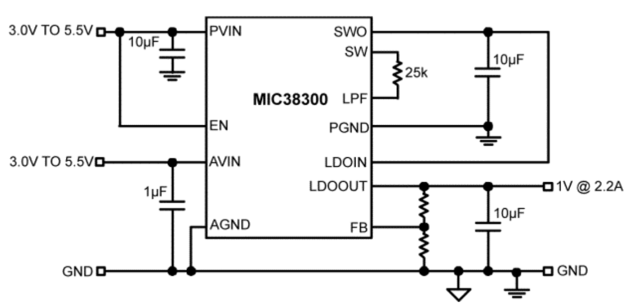
Features

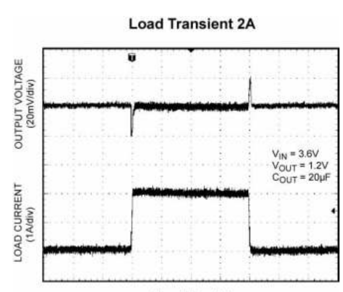
- 3A peak output current
- 2.2A continuous operating current
- Input voltage range: 3.0V to 5.5V
- Adjustable output voltage down to 1.0V
- Output noise less than 5mV
- Ultra-fast transient performance
- Unique switcher plus LDO architecture
- Fully-integrated MOSFET switches
- Micro-power shutdown
- Easy upgrade from LDO as power dissipation becomes an issue
- Thermal shutdown and current-limit protection
- 4mm × 6mm × 0.9mm MLF package

Applications

- Point-of-load applications
- Networking, server, industrial power
- Wireless base-stations
- Sensitive RF applications

Typical Application





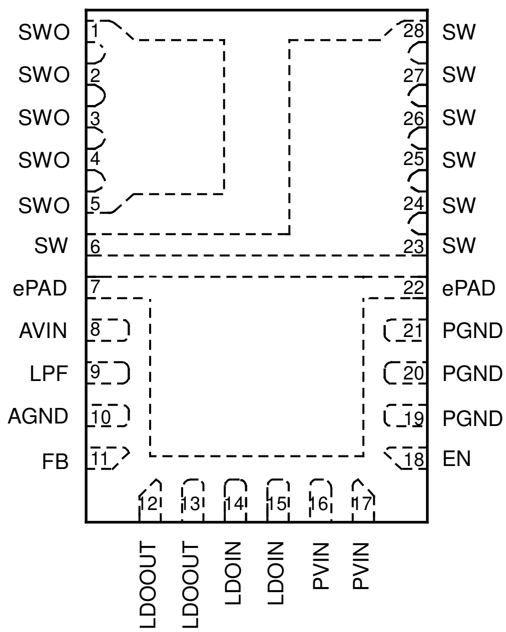
Ordering Information

Part Number	Output Current	Voltage[(1)]	Junction Temperature Range	Package
MIC38300HYHL	3.0A	Adjustable	–40°C to +125°C	Pb-Free 28-Pin 4mm × 6mm MLF

Note:

1. Other voltages are available. Contact Micrel for details.

Pin Configuration



28-Pin 4mm × 6mm MLF (ML)
(Top View)

Pin Description

Pin Number MIC38300HYHL	Pin Name	Pin Name
1, 2, 3, 4, 5	SWO	Switch (Output): This is the output of the PFM Switcher.
6, 23, 24, 25, 26, 27, 28	SW	Switch Node: Attach external resistor from LPF to increase hysteretic frequency.
7, 22	ePAD	Exposed heat-sink pad. Connect externally to PGND.
8	AVIN	Analog Supply Voltage: Supply for the analog control circuitry. Requires bypass capacitor to ground. Nominal bypass capacitor is 1µF.
9	LPF	Low Pass Filter: Attach external resistor from SW to increase hysteretic frequency.
10	AGND	Analog Ground.
11	FB	Feedback: Input to the error amplifier. Connect to the external resistor divider network to set the output voltage.

Pin Description (Continued)

Pin Number MIC38300HYHL	Pin Name	Pin Name
12, 13	LDOOUT	LDO Output: Output of voltage regulator. Place capacitor to ground to bypass the output voltage. Nominal bypass capacitor is 10µF.
14, 15	LDOIN	LDO Input: Connect to SW output. Requires a bypass capacitor to ground. Nominal bypass capacitor is 10µF.
16, 17	PVIN	Input Supply Voltage (Input): Requires bypass capacitor to GND. Nominal bypass capacitor is 10µF.
18	EN	Enable (Input): Logic low will shut down the device, reducing the quiescent current to less than 50µA. This pin can also be used as an undervoltage lockout function by connecting a resistor divider from EN/UVLO pin to VIN and GND. It should be not left open.
19, 20, 21	PGND	Power Ground.

Absolute Maximum Ratings[1]

Supply Voltage (V_{IN}) 6V
Output Switch Voltage (V_{SW}) 6V
LDO Output Voltage (V_{OUT}) 6V
Logic Input Voltage (V_{EN}) .... –0.3V to VIN
Power Dissipation .... Internally Limited[3]
Storage Temperature (T_S) .... –65°C ≤ T_J ≤ +150°C
ESD Rating[4] 1.5kV

Operating Ratings[2]

Supply voltage (V_{IN}) .... 3.0V to 5.5V
Junction Temperature Range .... –40°C ≤ T_J ≤ +125°C
Enable Input Voltage (V_{EN}) .... 0V to V_{IN}
Package Thermal Resistance
4mm × 6mm MLF-28 (θ_{JA}) .... 24°C/W

Electrical Characteristics[5]

T_A = 25°C with V_{IN} = V_{EN} = 5V; I_{OUT} = 10mA, V_{OUT} = 1.8V. **Bold** values indicate –40°C ≤ T_J ≤ +125°C, unless noted.

Parameter	Conditions	Min.	Typ.	Max.	Units
Supply Voltage Range (AVIN, PVIN)		**3.0**		**5.5**	V
Undervoltage Lockout Threshold	Turn-on		2.85		V
UVLO Hysteresis			100		mV
Quiescent Current	I_{OUT} = 0A, Not switching, open loop		1		mA
Turn-On Time	V_{OUT} to 95% of nominal		200	500	µs
Shutdown Current	V_{EN} = 0V		30	**50**	µA
Feedback Voltage	±2.5%	**0.975**	1	**1.025**	V
Feedback Current			5		nA
Dropout Voltage (V_{IN} – V_{OUT})	I_{LOAD} = 2.2A; V_{OUT} = 3V		0.85	1.2	V
Current Limit	V_{FB} = 0.9 × V_{NOM}	3	5		A
Output Voltage Load Regulation	V_{OUT} = 1.8V, 10mA to 2.2A		0.3	1	%
Output Voltage Line Regulation	V_{OUT} = 1.8V, V_{IN} from 3.0V to 5.5V		0.35	0.5	%/V
Output Ripple	I_{LOAD} = 1.5A, C_{OUTLDO} = 20µF, C_{OUTSW} = 20µF LPF = 25kΩ		2		mV
Over-Temperature Shutdown			150		°C
Over-Temperature Shutdown Hysteresis			15		°C
Enable Input[6]					
Enable Input Threshold	Regulator enable	**0.90**	1	**1.1**	V
Enable Hysteresis		**20**	100	**200**	mV
Enable Input Current			0.03	1	µA

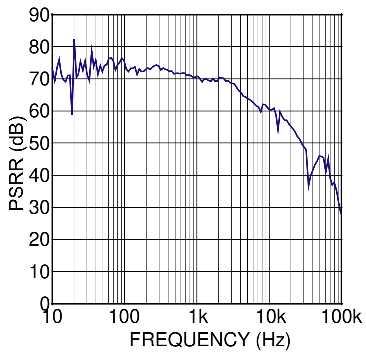
Notes:

1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.
3. The maximum allowable power dissipation of any T_A (ambient temperature) is $P_{D(max)} = (T_{J(max)} – T_A) / \theta_{JA}$. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the regulator will go into thermal shutdown.
4. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5kΩ in series with 100pF.
5. Specification for packaged product only.
6. Enable pin should not be left open.

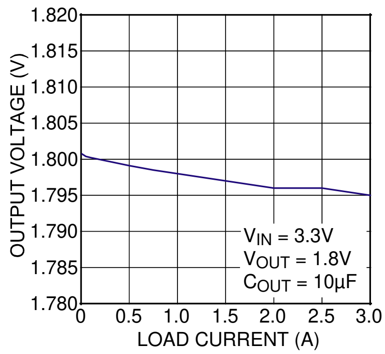
Typical Characteristics

V_{IN} = 3.3V, V_{OUT} = 1.8V, C_{OUT} = 10µF, R_{LPF} = 25kΩ, I_{OUT} = 100mA, unless noted.

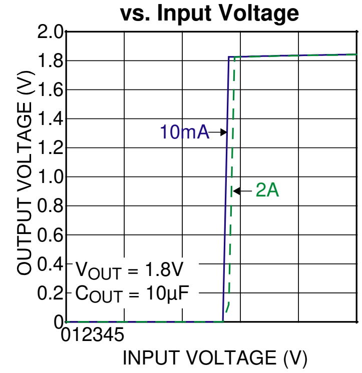
MIC38300 PSRR



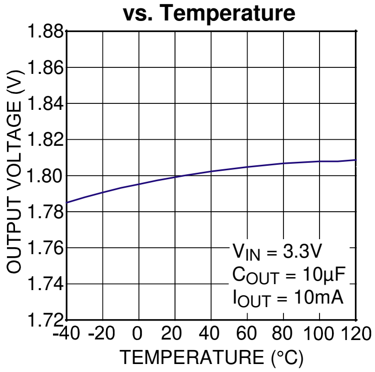
Load Regulation



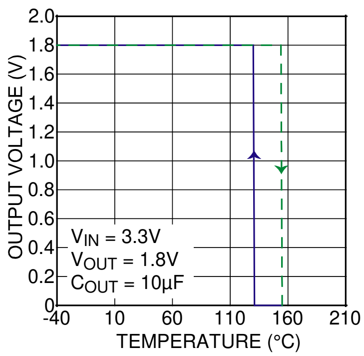
Output Voltage vs. Input Voltage



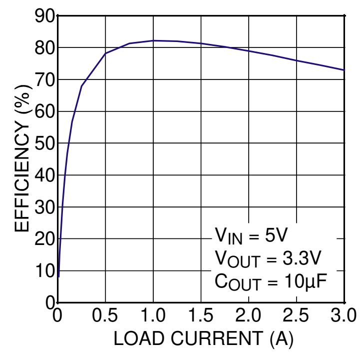
Output Voltage vs. Temperature



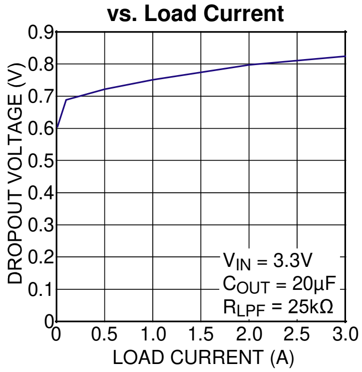
Thermal Shutdown



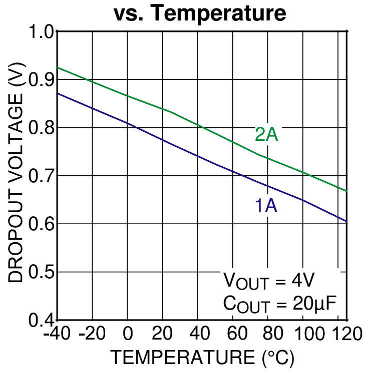
MIC38300 Efficiency



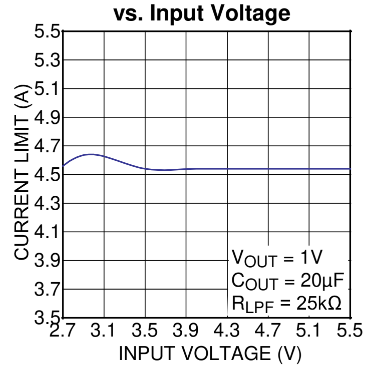
Dropout Voltage vs. Load Current



Dropout Voltage vs. Temperature



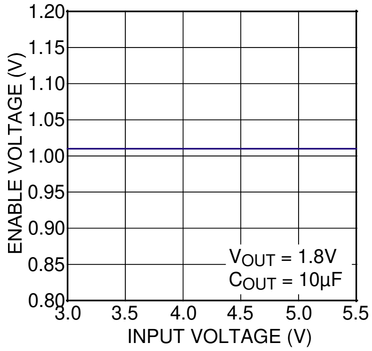
Current Limit vs. Input Voltage



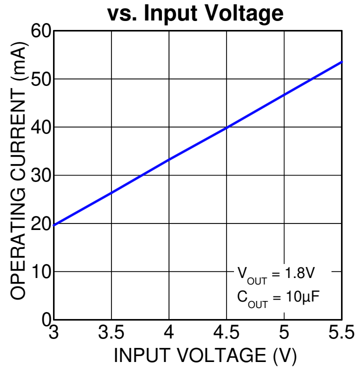
Typical Characteristics (Continued)

V_{IN} = 3.3V, V_{OUT} = 1.8V, C_{OUT} = 10µF, R_{LPF} = 25kΩ, I_{OUT} = 100mA, unless noted.

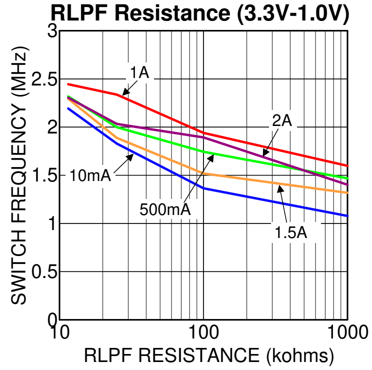
Enable Threshold



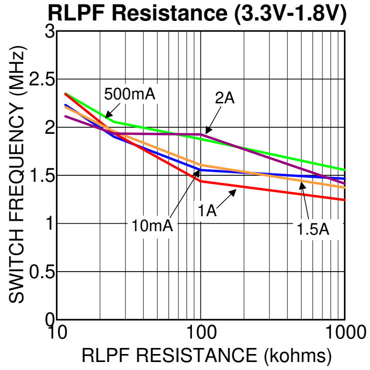
Operating Current vs. Input Voltage



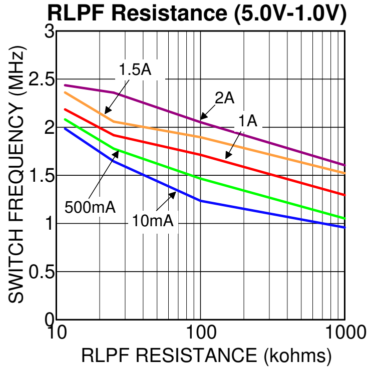
Switch Frequency vs. RLPF Resistance (3.3V-1.0V)



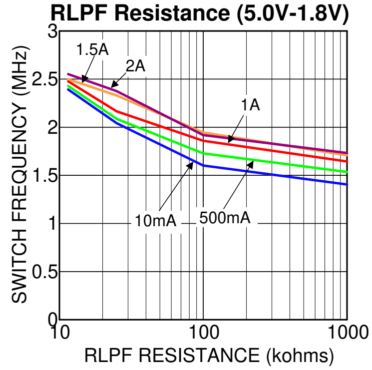
Switch Frequency vs. RLPF Resistance (3.3V-1.8V)



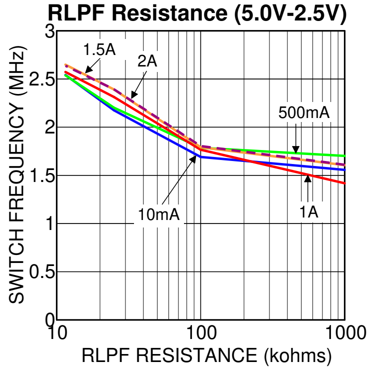
Switch Frequency vs. RLPF Resistance (5.0V-1.0V)



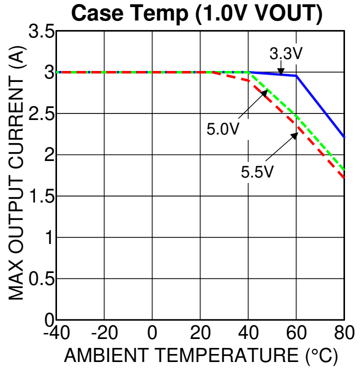
Switch Frequency vs. RLPF Resistance (5.0V-1.8V)



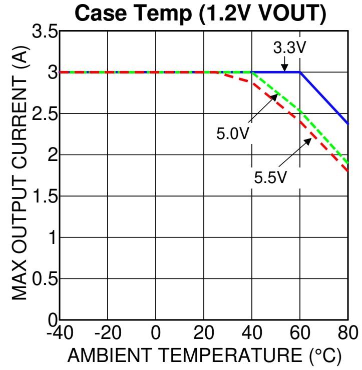
Switch Frequency vs. RLPF Resistance (5.0V-2.5V)



Max Output Current @ 110°C Case Temp (1.0V VOUT)

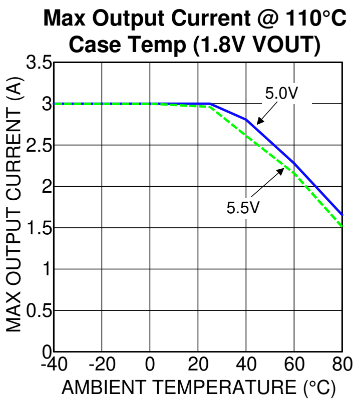


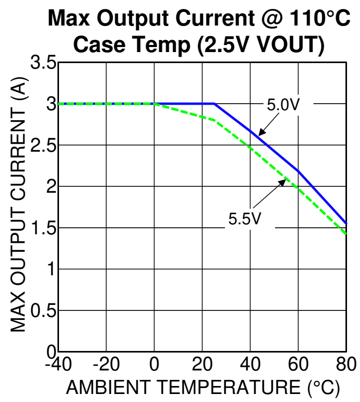
Max Output Current @ 110°C Case Temp (1.2V VOUT)



Typical Characteristics (Continued)

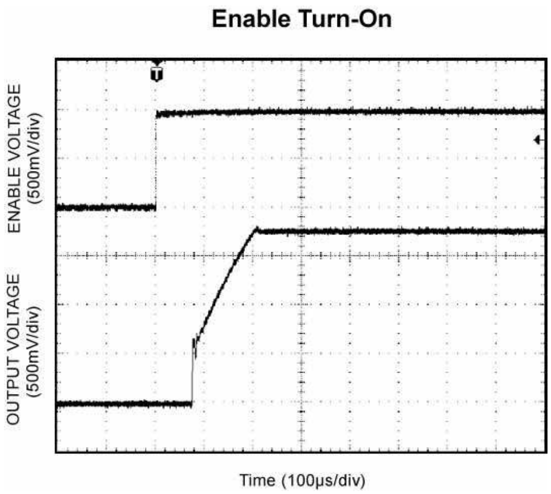
V_{IN} = 3.3V, V_{OUT} = 1.8V, C_{OUT} = 10µF, R_{LPF} = 25kΩ, I_{OUT} = 100mA, unless noted.

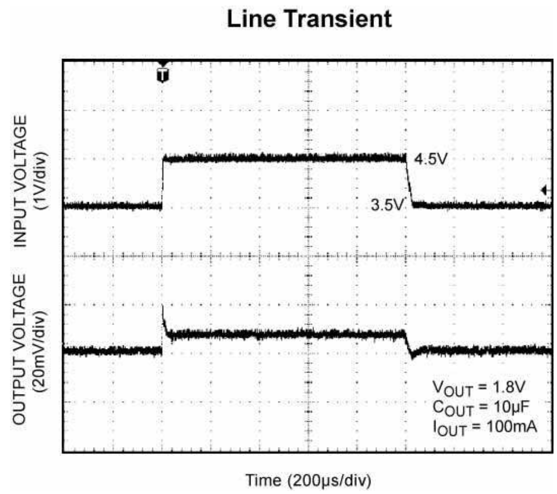


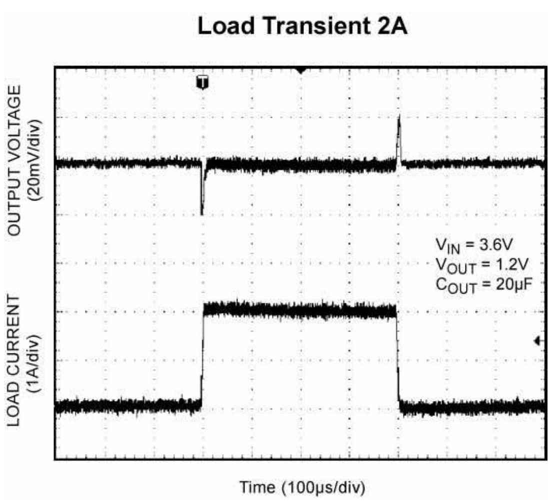


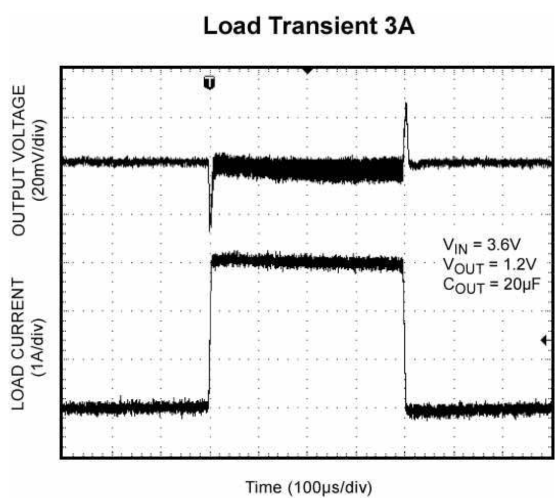
Functional Characteristics

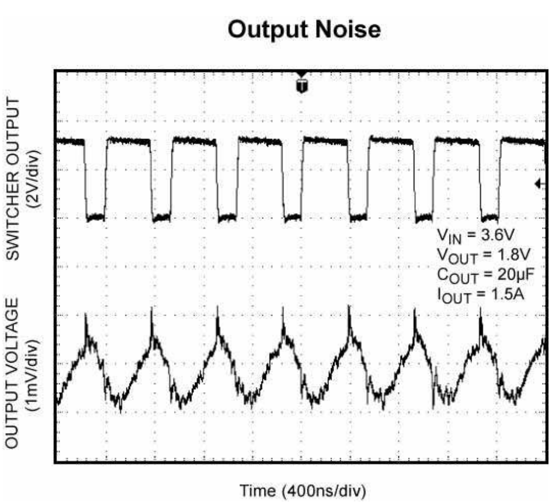
V_{IN} = 3.3V, V_{OUT} = 1.8V, C_{OUT} = 10µF, Inductor = 470nH; R_{LPF} = 25kΩ, I_{OUT} = 100mA, unless noted.



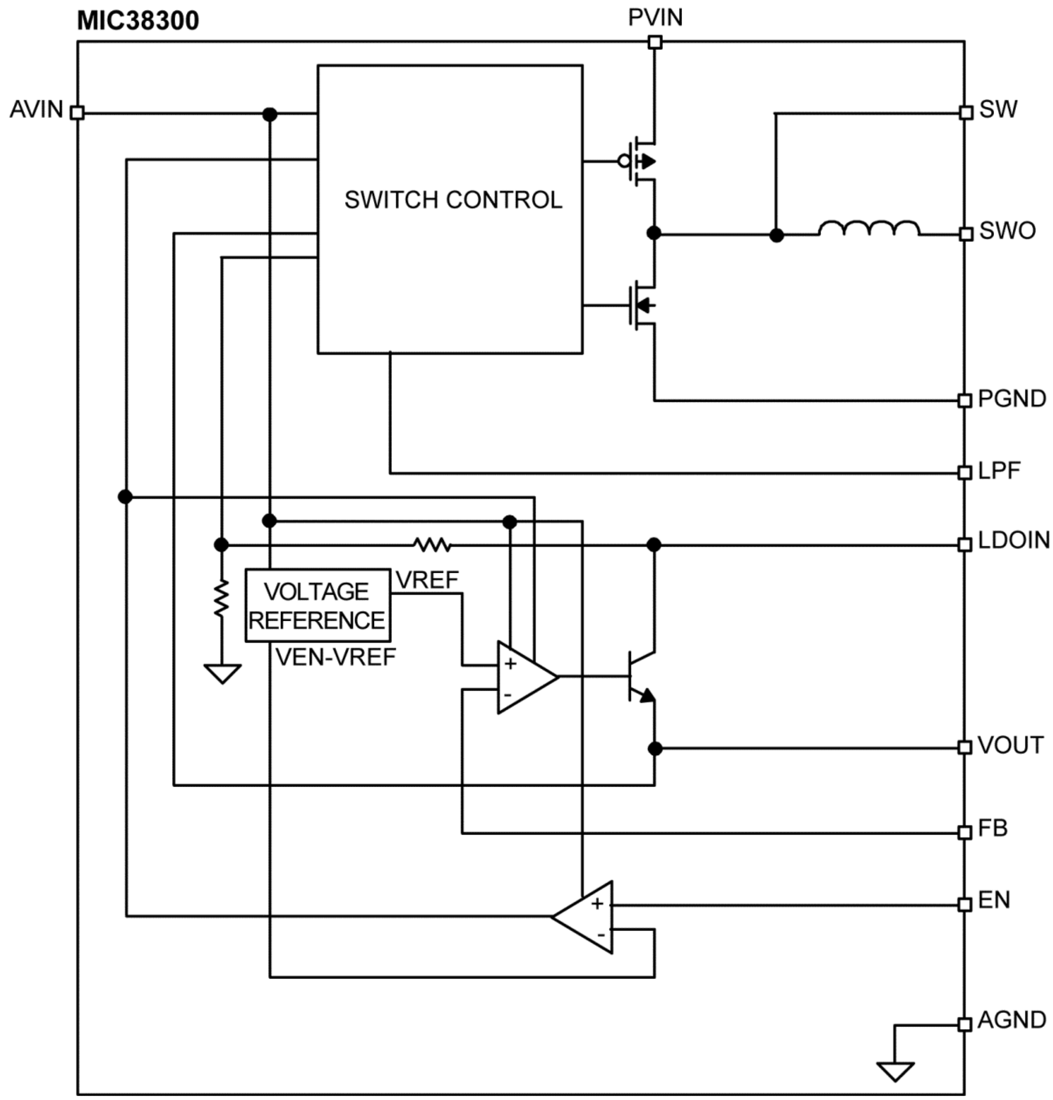






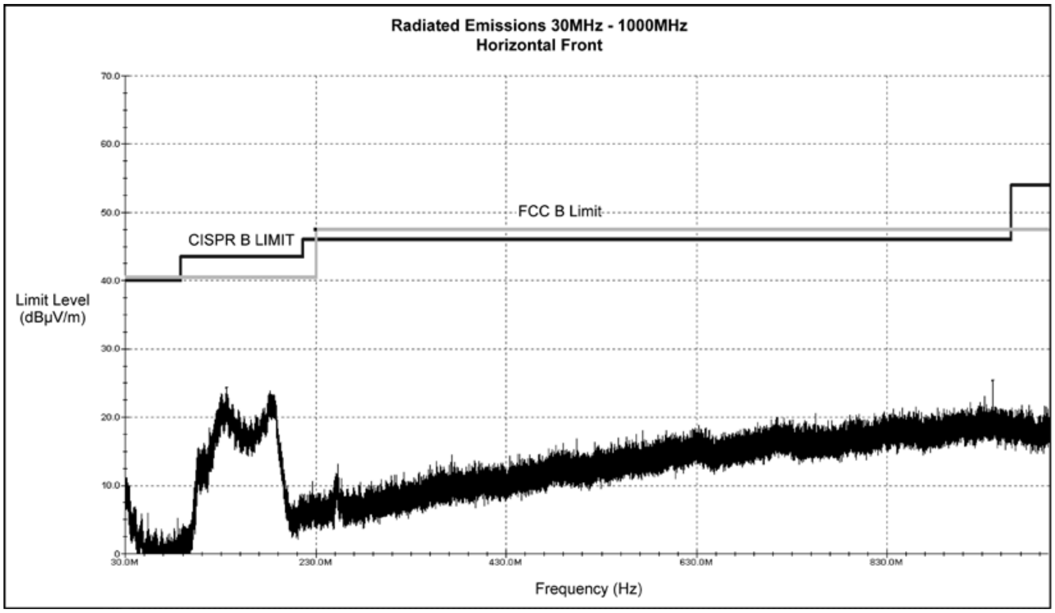


Functional Diagram

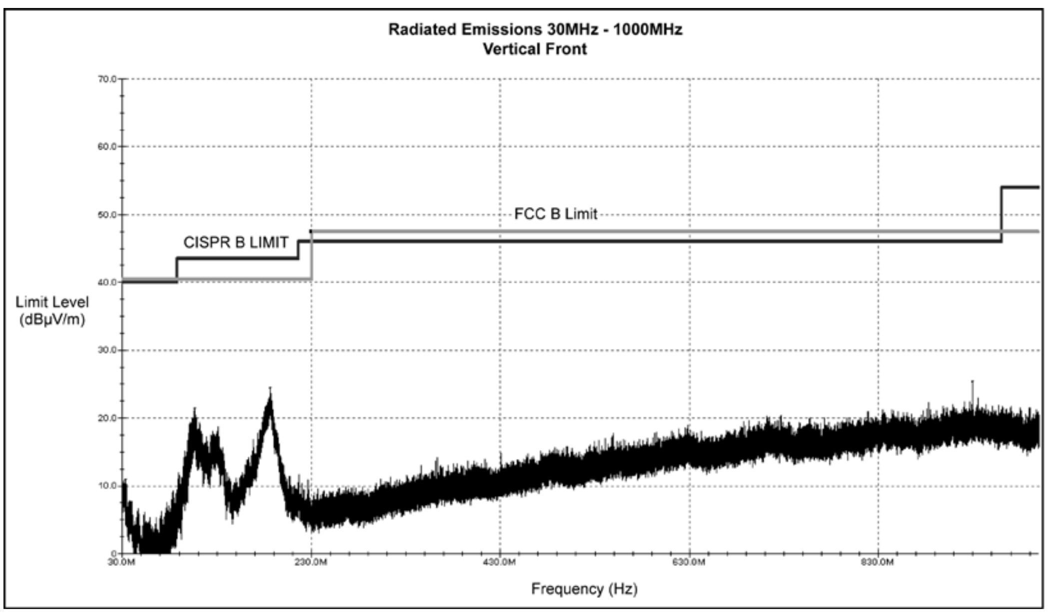


EMI Performance

V_{OUT} =1.8V, I_{OUT} = 1.2A.



EMI Test – Horizontal Front



EMI Test – Vertical Front

Additional components to MIC38150 Evaluation Board (Performance similar to MIC38300):

1. Input Ferrite Bead Inductor. Part number: BLM21AG102SN1D.
2. 0.1µF and 0.01µF ceramic bypass capacitors on PVIN, SW, SWO, and LDOOUT pins.

Application Information

Enable Input

The MIC38300 features a TTL/CMOS compatible positive logic enable input for on/off control of the device. High enables the regulator while low disables the regulator. In shutdown the regulator consumes very little current (only a few microamperes of leakage). For simple applications the enable (EN) can be connected to V_{IN} (IN).

Input Capacitor

PVIN provides power to the MOSFETs for the switch mode regulator section and the gate drivers. Due to the high switching speeds, a 10µF capacitor is recommended close to PVIN and the power ground (PGND) pin for bypassing.

Analog V_{IN} (AVIN) provides power to the analog supply circuitry. Careful layout should be considered to ensure high-frequency switching noise caused by PVIN is reduced before reaching AVIN. A 1µF capacitor as close to AVIN as possible is recommended.

Output Capacitor

The MIC38300 requires an output capacitor for stable operation. As a µCap LDO, the MIC38300 can operate with ceramic output capacitors of 10µF or greater. Values of greater than 10µF improve transient response and noise reduction at high frequency. X7R/X5R dielectric-type ceramic capacitors are recommended because of their superior temperature performance. X7R-type capacitors change capacitance by 15% over their operating temperature range and are the most stable type of ceramic capacitors. Larger output capacitances can be achieved by placing tantalum or aluminum electrolytics in parallel with the ceramic capacitor. For example, a 100µF electrolytic in parallel with a 10µF ceramic can provide the transient and high frequency noise performance of a 100µF ceramic at a significantly lower cost. Specific undershoot/overshoot performance will depend on both the values and ESR/ESL of the capacitors.

For less than 5mV noise performance at higher current loads, 20µF capacitors are recommended at LDOIN and LDOOUT.

Low Pass Filter Pin

The MIC38300 features a Low Pass Filter (LPF) pin for adjusting the switcher frequency. By tuning the frequency, the user can further improve output ripple without losing efficiency. Adjusting the frequency is accomplished by connecting a resistor between the LPF and SW pins. A small value resistor would increase the frequency while a larger value resistor decreases the frequency. Recommended R_{LPF} value is 25kΩ. Please see Typical Characteristics section for more details.

Adjustable Regulator Design

The adjustable MIC38300 output voltage can be programmed from 1V to 5.0V using a resistor divider from output to the FB pin. Resistors can be quite large, up to 100kΩ because of the very high input impedance and low bias current of the sense amplifier. For large value resistors (>50kΩ) R1 should be bypassed by a small capacitor (C_{FF} = 0.1µF bypass capacitor) to avoid instability due to phase lag at the ADJ/SNS input.

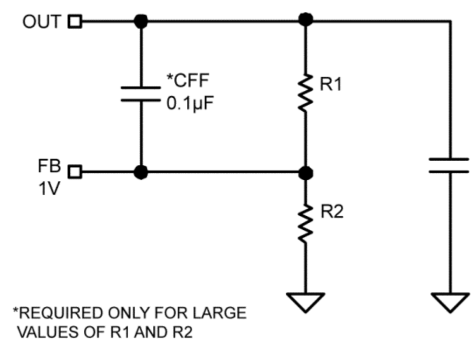


Figure 1. Adjustable Regulator with Resistors

The output resistor divider values are calculated by Equation 1:

$$V_{OUT} = 1V\left(\frac{R1}{R2} + 1\right) \qquad \text{Eq. 1}$$

Efficiency Considerations

Efficiency is defined as the amount of useful output power, divided by the amount of power supplied.

$$\text{Efficiency\_\%} = \left(\frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}}\right) \times 100 \qquad \text{Eq. 2}$$

Maintaining high efficiency serves two purposes. It reduces power dissipation in the power supply, reducing the need for heat sinks and thermal design considerations and it reduces consumption of current for battery-powered applications. Reduced current draw from a battery increases the devices operating time and is critical in handheld devices.

There are two types of losses in switching converters; DC losses and switching losses. DC losses are simply the power dissipation of I^2R. Power is dissipated in the high side switch during the on cycle. Power loss is equal to the high-side MOSFET R_{DSON} multiplied by the switch current. During the off cycle, the low side N-channel MOSFET conducts, also dissipating power. Device operating current also reduces efficiency. The product of the quiescent (operating) current and the supply voltage is another DC loss.

Over 100mA, efficiency loss is dominated by MOSFET R_{DSON} and inductor losses. Higher input supply voltages will increase the gate-to-source threshold on the internal MOSFETs, reducing the internal RD_{DSON}. This improves efficiency by reducing DC losses in the device. All but the inductor losses are inherent to the device. In which case, inductor selection becomes increasingly critical in efficiency calculations. As the inductors are reduced in size, the DC resistance (DCR) can become quite significant. The DCR losses can be calculated as in Equation 3:

$$L\_P_D = I_{OUT}^2 \times DCR \qquad \text{Eq. 3}$$

From that, the loss in efficiency due to inductor resistance can be calculated as in Equation 4:

$$Efficiency\_Loss = \left[1 - \left(\frac{V_{OUT} \times I_{OUT}}{V_{OUT} \times I_{OUT} + L\_P_D}\right)\right] \times 100$$

Eq. 4

Efficiency loss due to DCR is minimal at light loads and gains significance as the load is increased. Inductor selection becomes a trade-off between efficiency and size in this case.

Current-Sharing Circuit

Figure 2 allows two MIC38300 HELDO regulators to share the load current equally. HELDO1 senses the output voltage at the load, on the other side of a current sense resistor. As the load changes, a voltage equal to the output voltage, plus the load current times the sense resistor, is developed at the V_{OUT} terminal of HELDO1. The op-amp (MIC7300) inverting pin senses this voltage and compares it to the voltage on the V_{OUT} terminal of HELDO2.

If the current through the current sense of HELDO2 is less than the current through the current sense of HELDO1, the inverting pin will be at a higher voltage than the non-inverting pin and the op-amp will drive the FB of HELDO2 low. The low voltage sensed on HELDO2 FB pin will drive the output up until the output voltage of HELDO2 matches the output voltage of HELDO1. Since V_{OUT} will remain constant and both HELDO V_{OUT} terminals and sense resistances are matched, the output currents will be shared equally.

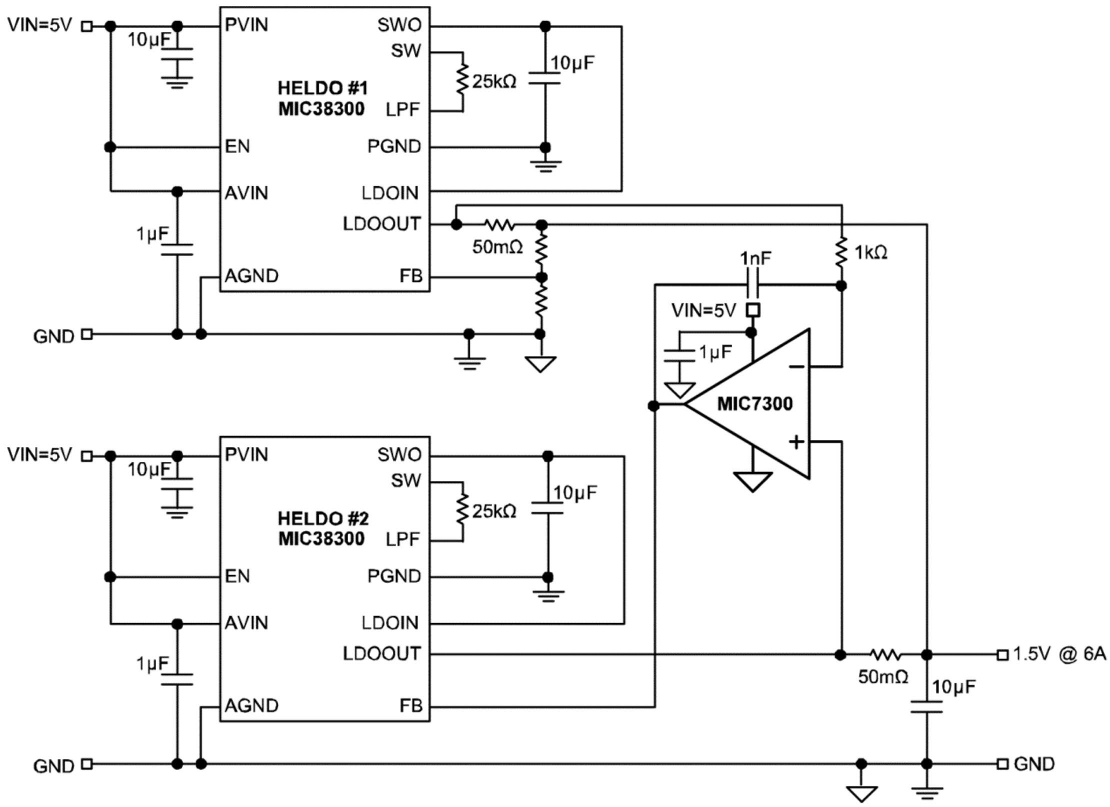
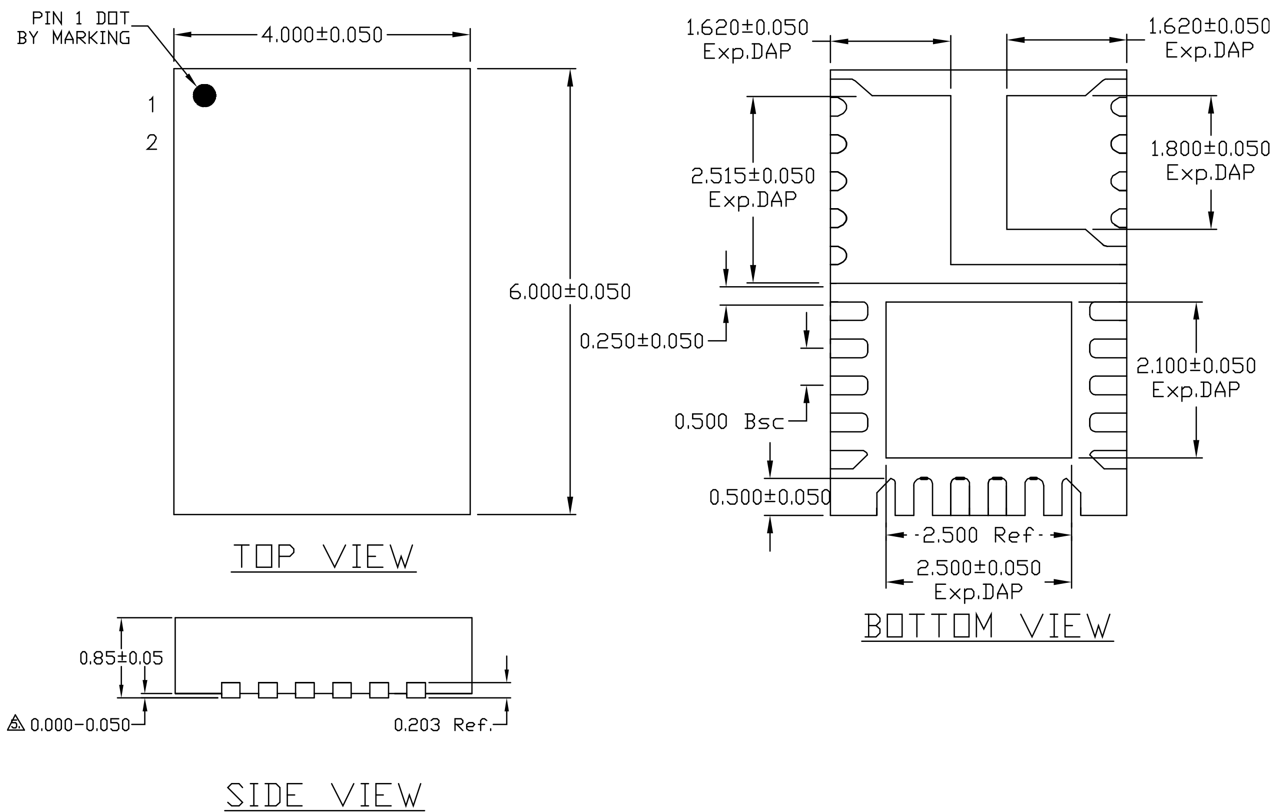


Figure 2. Current-Sharing Circuit for 6A Output

Package Information[1]



NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.
5. APPLIED ONLY FOR TERMINALS.

28-Pin 4mm × 4mm MLF (ML)

Note:

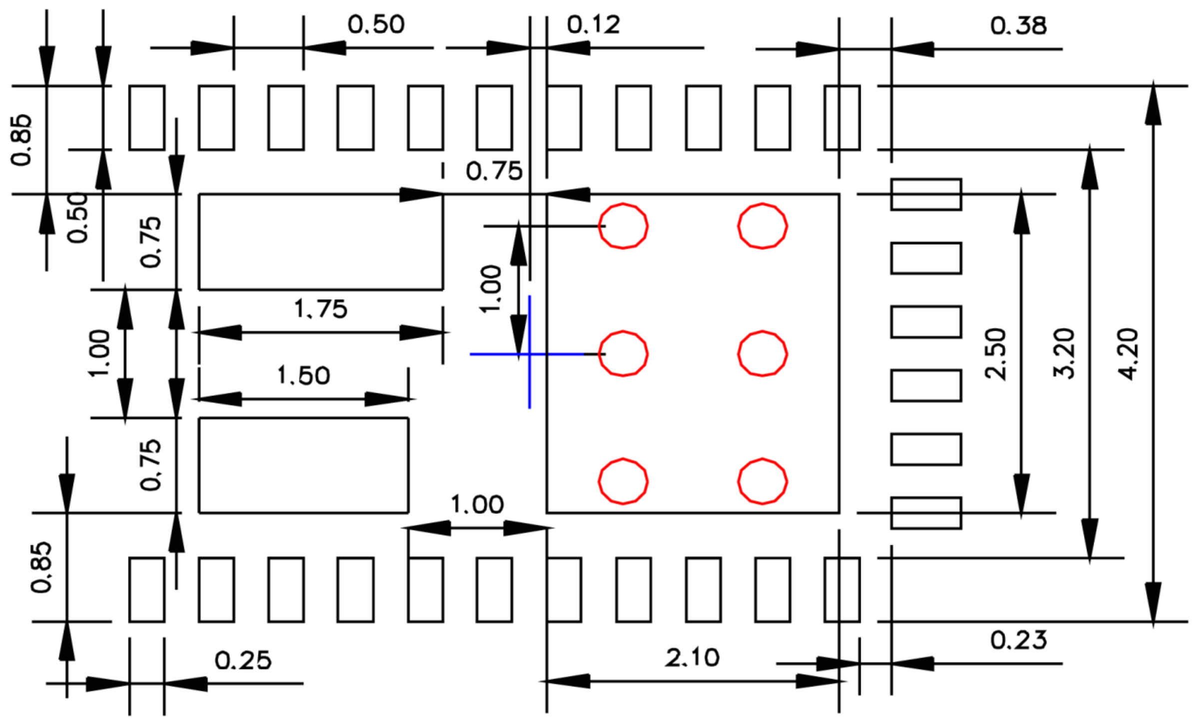
1. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

Recommended Landing Pattern

LP # HMLF46T-28LD-LP-1

All units are in mm

Tolerance ±0.05, if not noted



Red circles indicate Thermal Vias. Size should be .300mm – .350mm in diameter and it should be connected to GND plane for maximum thermal performance.

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA
TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB http://www.micrel.com