

# MOSFET - Power, Single N-Channel SuperFET<sup>®</sup> V, FRFET<sup>®</sup>, D<sup>2</sup>PAK

## 600 V, 55 mΩ, 45 A

### NVB055N60S5F

#### Description

The SUPERFET V MOSFET FRFET series has optimized body diode performance characteristics. This can allow for the removal of components in the application and improve application performance and reliability, particularly when soft switching topologies are used.

#### Features

- 650 V @ T<sub>J</sub> = 150°C / Typ. R<sub>DS(on)</sub> = 44 mΩ
- 100% Avalanche Tested
- Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

#### Applications

- Electric Vehicle On Board Chargers
- EV Main Battery DC/DC Converters

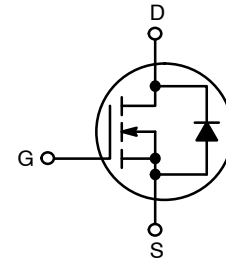
#### MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V <sub>DSS</sub>	600	V
Gate-to-Source Voltage	V <sub>GS</sub>	DC	±30
		AC (f > 1 Hz)	±30
Continuous Drain Current	I <sub>D</sub>	T <sub>C</sub> = 25°C	45
		T <sub>C</sub> = 100°C	28
Power Dissipation	P <sub>D</sub>	278	W
Pulsed Drain Current	I <sub>DM</sub>	159	A
Pulsed Source Current (Body Diode)	I <sub>SM</sub>	159	A
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C
Source Current (Body Diode)	I <sub>S</sub>	45	A
Single Pulse Avalanche Energy	E <sub>AS</sub>	417	mJ
(I <sub>L</sub> = 7 A, R <sub>G</sub> = 25 Ω)			
Avalanche Current	I <sub>AS</sub>	7	A
Repetitive Avalanche Energy (Note 1)	E <sub>AR</sub>	2.78	mJ
MOSFET dv/dt	dv/dt	120	V/ns
Peak Diode Recovery dv/dt (Note 2)		70	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T <sub>L</sub>	260	°C

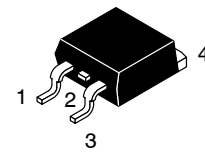
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. I<sub>SD</sub> ≤ 22.5 A, di/dt ≤ 200 A/μs, V<sub>DD</sub> ≤ 400 V, starting T<sub>J</sub> = 25°C.

V <sub>DSS</sub>	R <sub>DS(ON)</sub> MAX	I <sub>D</sub> MAX
600 V	55 mΩ @ 10 V	45 A

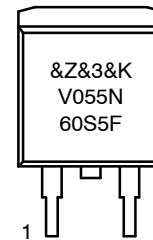


POWER MOSFET



D<sup>2</sup>PAK  
CASE 418AJ

#### MARKING DIAGRAM



&Z = Assembly Plant Code  
&3 = Date Code (Year & Week)  
&K = Assembly Lot  
V055N60S5F = Specific Device Code

#### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

# NVB055N60S5F

## THERMAL RESISTANCE

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case, Max.	$R_{\theta JC}$	0.45	°C/W
Thermal Resistance, Junction-to-Ambient, Max.	$R_{\theta JA}$	62.5	

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}, T_J = 25^\circ\text{C}$	600	-	-	V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$\Delta V_{(BR)DSS} / \Delta T_J$	$I_D = 10\text{ mA}$ , Referenced to $25^\circ\text{C}$	-	581	-	mV/°C
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}, V_{DS} = 600\text{ V}, T_J = 25^\circ\text{C}$	-	-	10	μA
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{GS} = \pm 30\text{ V}, V_{DS} = 0\text{ V}$	-	-	±100	nA

### ON CHARACTERISTICS

Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 22.5\text{ A}, T_J = 25^\circ\text{C}$	-	44	55	mΩ
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 5.2\text{ mA}, T_J = 25^\circ\text{C}$	3.2	-	4.8	V
Forward Trans-conductance	$g_{FS}$	$V_{DS} = 20\text{ V}, I_D = 22.5\text{ A}$	-	44.8	-	S

### CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	$C_{ISS}$	$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}, f = 250\text{ kHz}$	-	4603	-	pF
Output Capacitance	$C_{OSS}$		-	72.9	-	
Time Related Output Capacitance	$C_{OSS(tr)}$	$I_D = \text{Constant}, V_{DS} = 0\text{ V to } 400\text{ V}, V_{GS} = 0\text{ V}$	-	1114	-	
Energy Related Output Capacitance	$C_{OSS(er)}$		$V_{DS} = 0\text{ V to } 400\text{ V}, V_{GS} = 0\text{ V}$	-	125	
Total Gate Charge	$Q_{G(tot)}$	$V_{DD} = 400\text{ V}, I_D = 22.5\text{ A}, V_{GS} = 10\text{ V}$	-	85.2	-	nC
Gate-to-Source Charge	$Q_{GS}$		-	26.2	-	
Gate-to-Drain Charge	$Q_{GD}$		-	24.9	-	
Gate Resistance	$R_G$		$f = 1\text{ MHz}$	-	4.32	

### SWITCHING CHARACTERISTICS

Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 0/10\text{ V}, V_{DD} = 400\text{ V}, I_D = 22.5\text{ A}, R_G = 4.7\text{ }\Omega$	-	44	-	ns
Rise Time	$t_r$		-	26.2	-	
Turn-Off Delay Time	$t_{d(off)}$		-	108	-	
Fall Time	$t_f$		-	2.6	-	

### SOURCE-TO-DRAIN DIODE CHARACTERISTICS

Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0\text{ V}, I_{SD} = 22.5\text{ A}, T_J = 25^\circ\text{C}$	-	-	1.2	V
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0\text{ V}, I_{SD} = 22.5\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, V_{DD} = 400\text{ V}$	-	128	-	ns
Reverse Recovery Charge	$Q_{RR}$		-	758	-	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

### PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Marking	Package	Packing Method	Reel Size	Tape Width	Quantity
NVB055N60S5F	V055N60S5F	D <sup>2</sup> PAK	Tape & Reel†	330 mm	24 mm	800 Units

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

TYPICAL CHARACTERISTICS

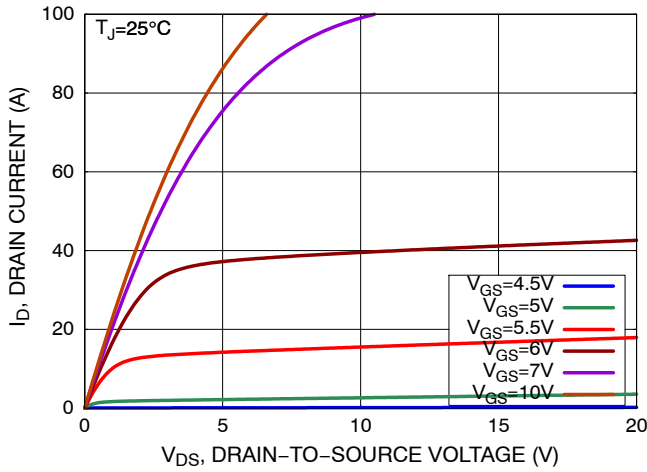


Figure 1. On-Region Characteristics

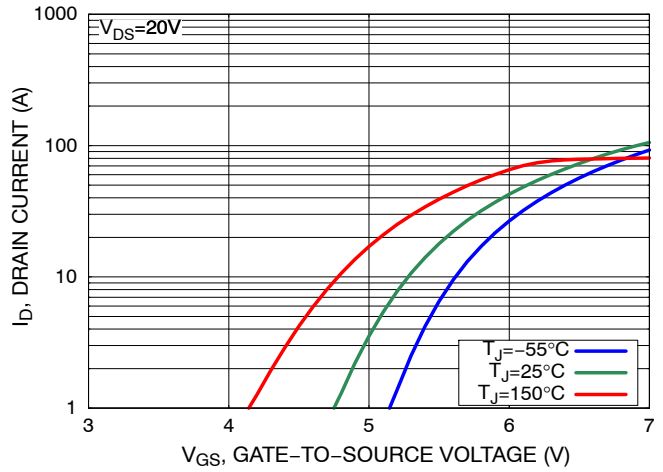


Figure 2. Transfer Characteristics

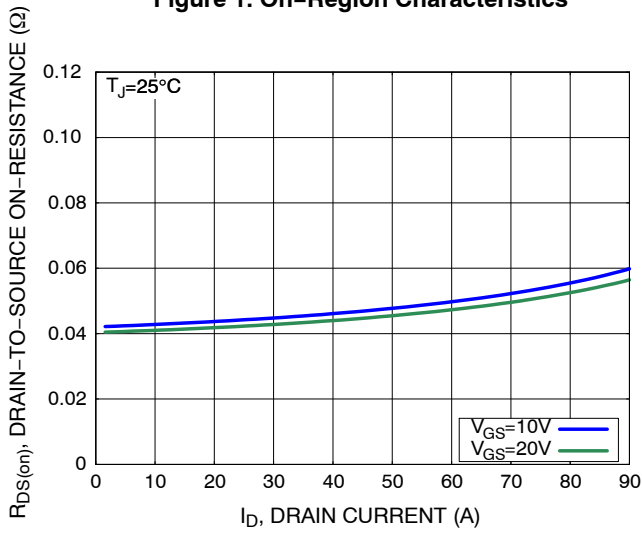


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

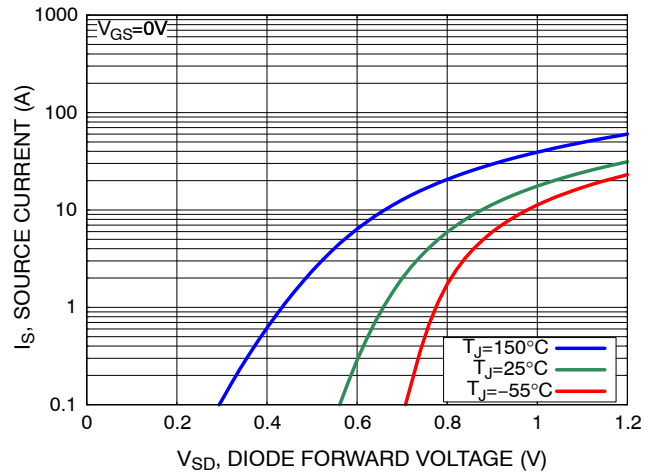


Figure 4. Diode Forward Voltage vs. Source Current

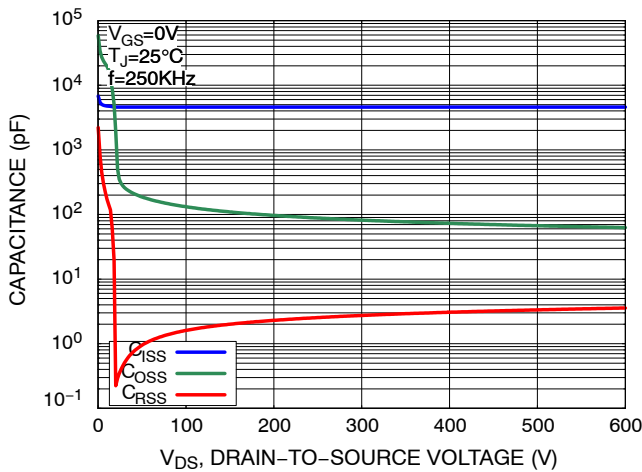


Figure 5. Capacitance Characteristics

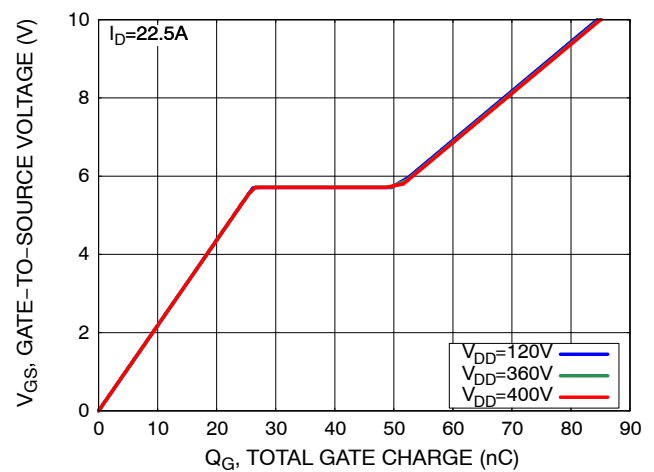
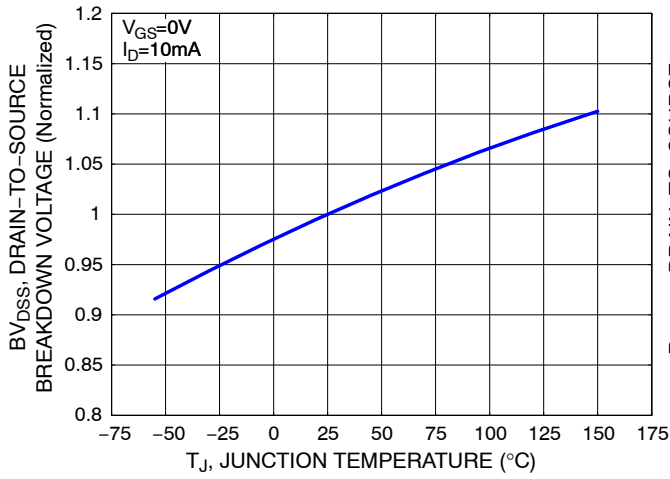


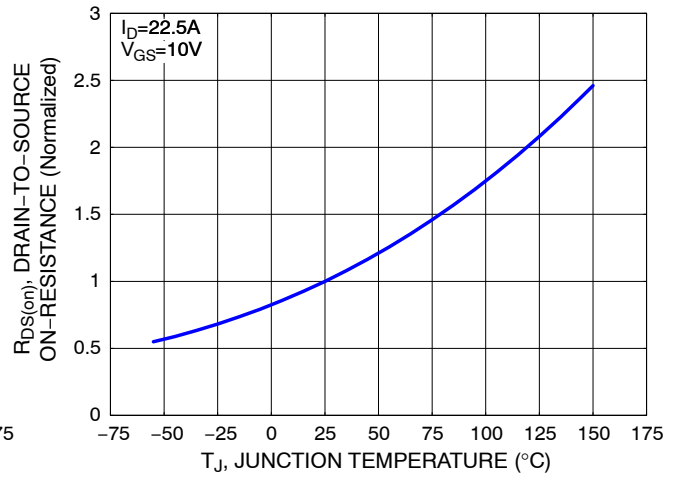
Figure 6. Gate Charge Characteristics

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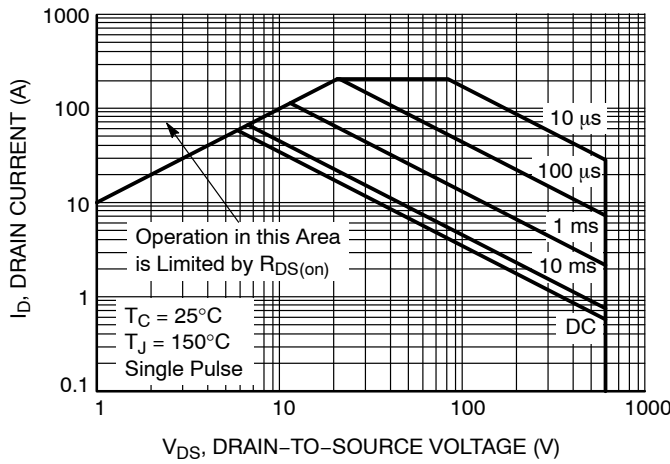
## TYPICAL CHARACTERISTICS



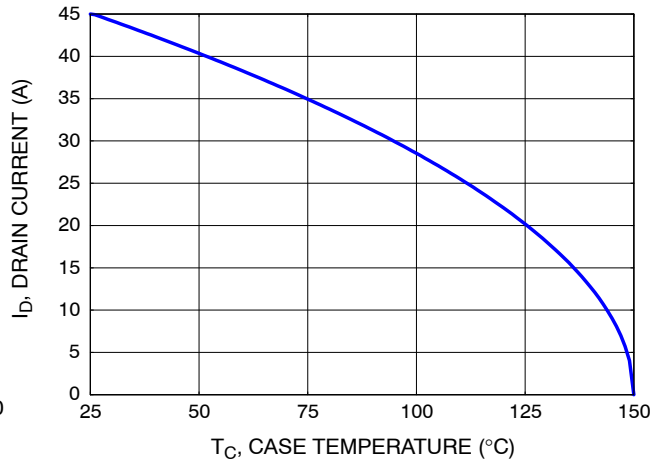
**Figure 7. Breakdown Voltage Variation vs. Temperature**



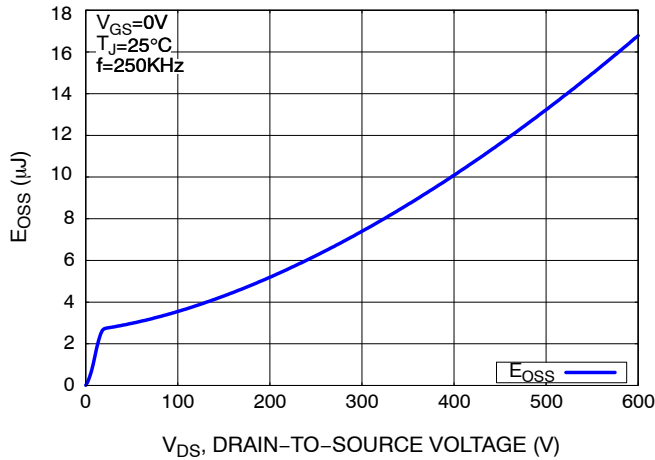
**Figure 8. On-Resistance Variation vs. Temperature**



**Figure 9. Maximum Safe Operating Area**



**Figure 10. Maximum Drain Current vs. Case Temperature**



**Figure 11. E<sub>OSS</sub> vs. Drain-to-Source Voltage**

# NVB055N60S5F

## TYPICAL CHARACTERISTICS

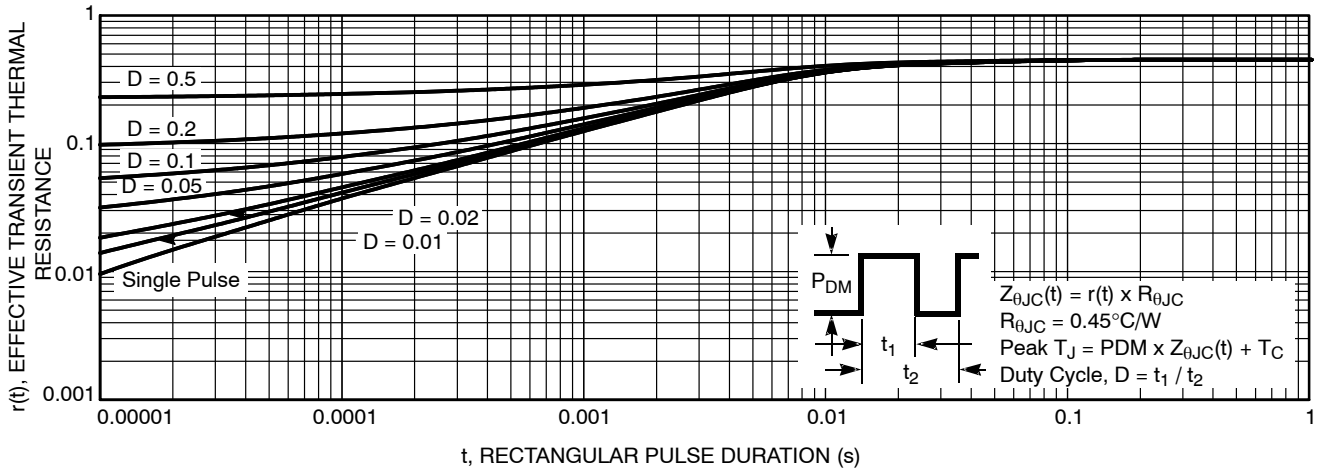


Figure 12. Transient Thermal Impedance

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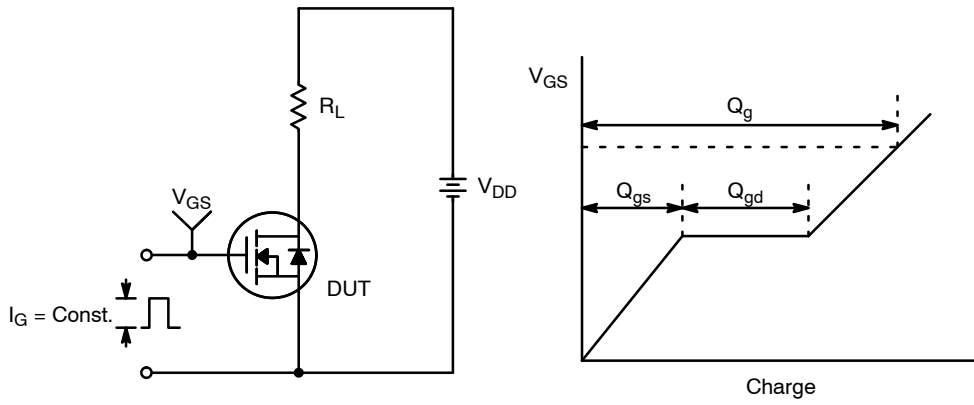


Figure 13. Gate Charge Test Circuit & Waveform

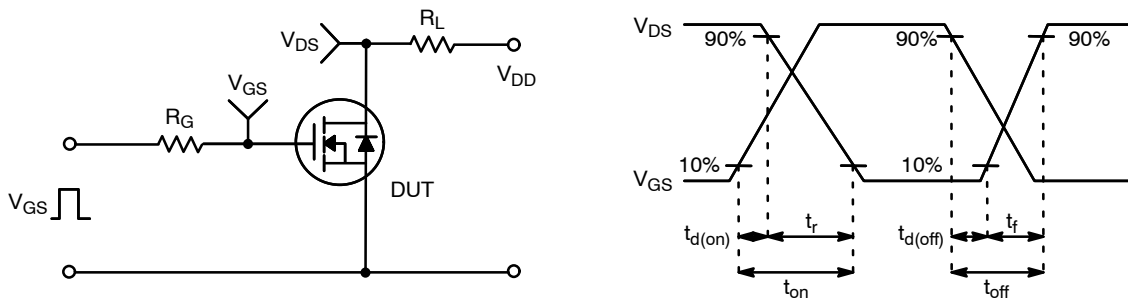


Figure 14. Resistive Switching Test Circuit & Waveforms

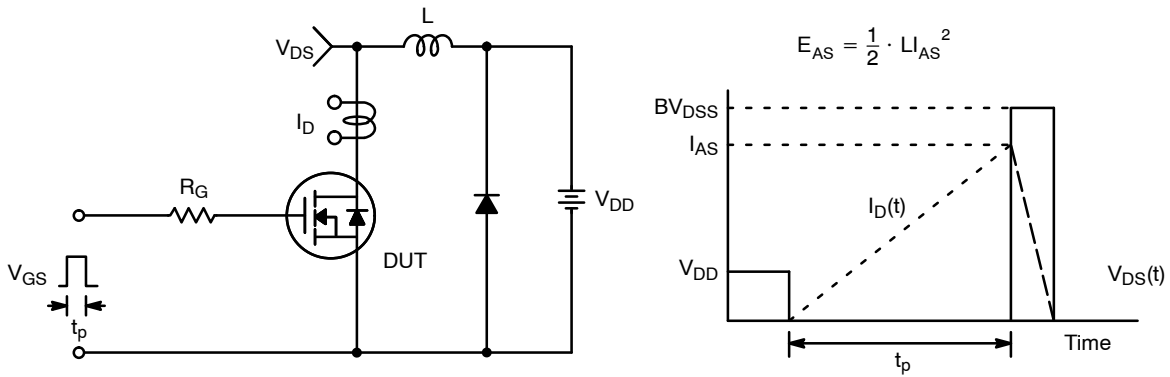
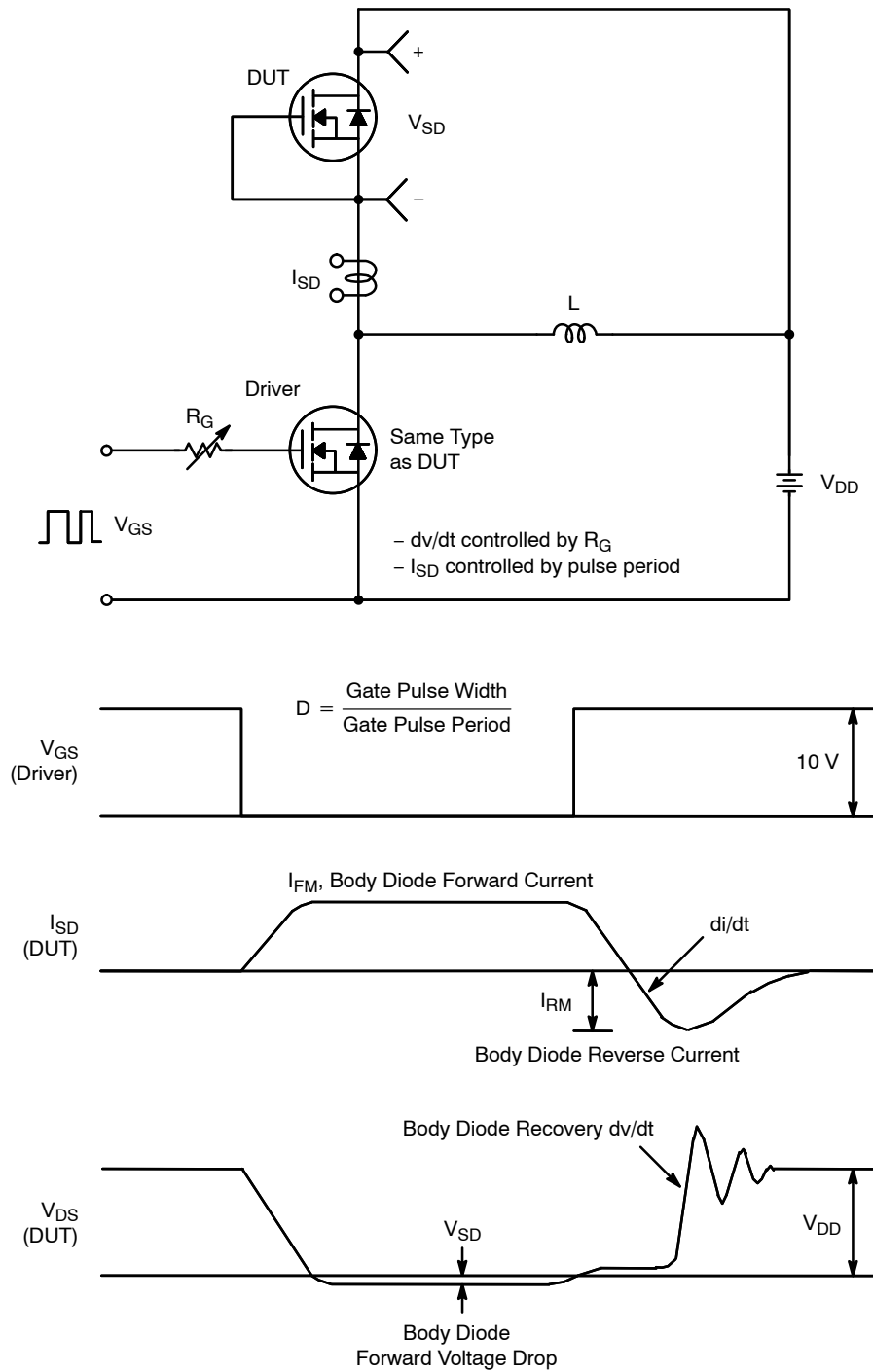


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

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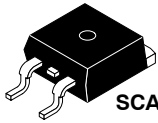


**Figure 16. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms**

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®



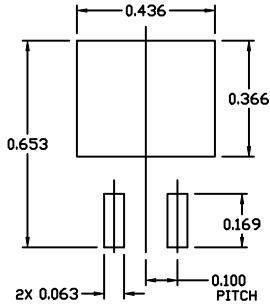
SCALE 1:1

### D<sup>2</sup>PAK-3 (TO-263, 3-LEAD)

#### CASE 418AJ

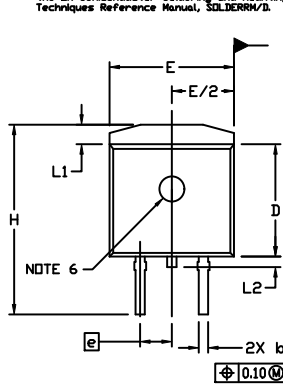
#### ISSUE F

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#### RECOMMENDED MOUNTING FOOTPRINT

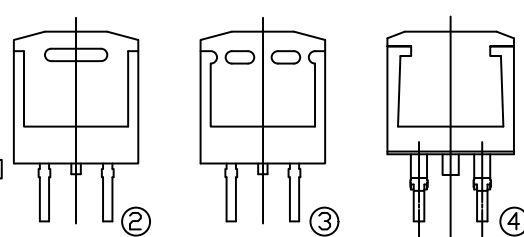
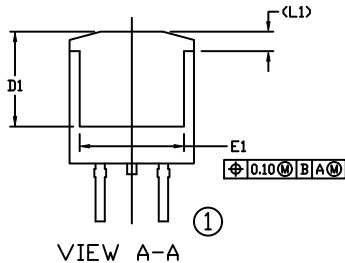
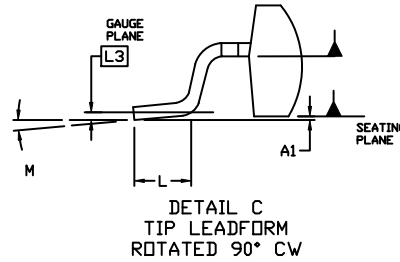
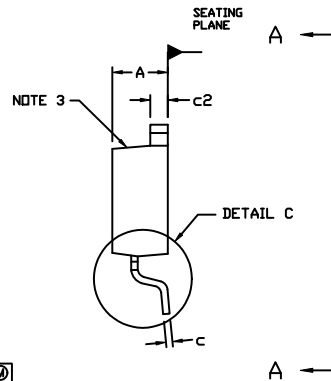
For additional information on our Pb-free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/T.



#### NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
- CONTROLLING DIMENSION: INCHES
- CHAMFER OPTIONAL.
- DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005 PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
- THERMAL PAD CONTOUR IS OPTIONAL WITHIN DIMENSIONS E, L1, D1, AND E1.
- OPTIONAL MOLD FEATURE.
- ①, ② ... OPTIONAL CONSTRUCTION FEATURE CALL OUTS.

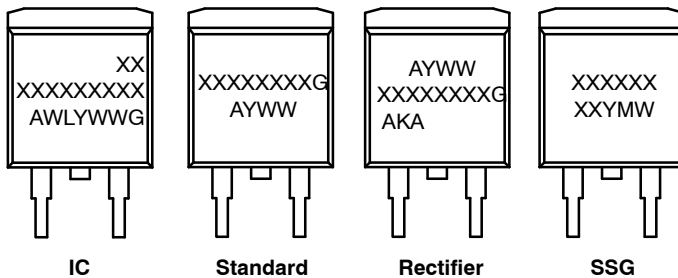
DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.160	0.190	4.06	4.83
A1	0.000	0.010	0.00	0.25
b	0.020	0.039	0.51	0.99
c	0.012	0.029	0.30	0.74
c2	0.045	0.065	1.14	1.65
D	0.330	0.380	8.38	9.65
D1	0.260	---	6.60	---
E	0.380	0.420	9.65	10.67
E1	0.245	---	6.22	---
e	0.100	BSC	2.54	BSC
H	0.575	0.625	14.60	15.88
L	0.070	0.110	1.78	2.79
L1	---	0.066	---	1.68
L2	---	0.070	---	1.78
L3	0.010	BSC	0.25	BSC
M	0*	8*	0*	8*



VIEW A-A

VIEW A-A  
OPTIONAL CONSTRUCTIONS

#### GENERIC MARKING DIAGRAMS\*



IC

Standard

Rectifier

SSG

- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- W = Week Code (SSG)
- M = Month Code (SSG)
- G = Pb-Free Package
- AKA = Polarity Indicator

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	D <sup>2</sup> PAK-3 (TO-263, 3-LEAD)	PAGE 1 OF 1

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