HARRIS SEMICONDUCTOR

HFA1245

Dual, 530MHz, Low Power, Video Operational Amplifier with Disable

November 1996

Features

- Low Supply Current . . . . . 5.8mA/Op Amp
- High Input Impedance 2MΩ
- Low Crosstalk (5MHz) . . . . . -73dB
- High Off Isolation (5MHz) . . . . . -61dB
- Wide -3dB Bandwidth (A_V = +2) 530MHz
- Very Fast Slew Rate 1050V/μs
- Gain Flatness (to 50MHz) . . . . . ±0.11dB
- Differential Gain 0.02%
- Differential Phase . . . . . 0.03 Degrees
- Individual Output Enable/Disable
- Output Enable/Disable Time 160ns/20ns
- Pin Compatible Upgrade to HA5022

Applications

- Flash A/D Drivers
- High Resolution Monitors
- Video Multiplexers
- Video Switching and Routing
- Professional Video Processing
- Video Digitizing Boards/Systems
- Multimedia Systems
- RGB Preamps
- Medical Imaging
- Hand Held and Miniaturized RF Equipment
- Battery Powered Communications
- High Speed Oscilloscopes and Analyzers

Description

The HFA1245 is a dual, high speed, low power current feedback amplifier built with Harris' proprietary complementary bipolar UHF-1 process.

The HFA1245 features individual TTL/CMOS compatible disable controls. When pulled low they disable the corresponding amplifier, which reduces the supply current and forces the output into a high impedance state. This feature allows easy implementation of simple, low power video switching and routing systems. Component and composite video systems also benefit from this op amp's excellent gain flatness, and good differential gain and phase specifications.

Multiplexed A/D applications will also find the HFA1245 useful as the A/D driver/multiplexer.

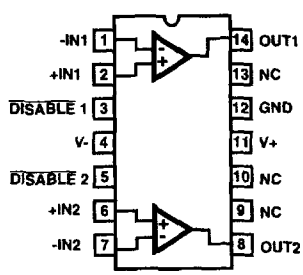
The HFA1245 is a low power, high performance upgrade for the popular Harris HA5022. For a dual amplifier without disable, in a standard 8 lead pinout, please see the HFA1205 data sheet.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HFA1245IP	-40 to 85	14 Ld PDIP	E14.3
HFA1245IB	-40 to 85	14 Ld SOIC	M14.15
HA5022EVAL	High Speed Op Amp DIP Evaluation Board		

Pinout

HFA1245
(PDIP, SOIC)
TOP VIEW



Absolute Maximum Ratings

Voltage Between V+ and V- 11V
DC Input Voltage . . . . . V_{SUPPLY}
Differential Input Voltage. 8V
Output Current (Note 2) . . . . . Short Circuit Protected
30mA Continuous
60mA ≤ 50% Duty Cycle
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7) . . . 600V

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
PDIP Package	100
SOIC Package	120

Maximum Junction Temperature (Die) . . . . . 175°C
Maximum Junction Temperature (Plastic Package) . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

Operating Conditions

Temperature Range . . . . . -40°C to 85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
2. Output is short circuit protected to ground. Brief short circuits to ground will not degrade reliability, however continuous (100% duty cycle) output current must not exceed 30mA for maximum reliability.

Electrical Specifications

V_{SUPPLY} = ±5V, A_V = +1, R_F = 560Ω, R_L = 100Ω, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	(NOTE 3) TEST LEVEL	TEMP. (°C)	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS							
Input Offset Voltage		A	25	-	2	5	mV
		A	Full	-	3	8	mV
Average Input Offset Voltage Drift		B	Full	-	1	10	µV/°C
Input Offset Voltage Common-Mode Rejection Ratio	ΔV_{CM} = ±1.8V	A	25	45	48	-	dB
	ΔV_{CM} = ±1.8V	A	85	43	46	-	dB
	ΔV_{CM} = ±1.2V	A	-40	43	46	-	dB
Input Offset Voltage Power Supply Rejection Ratio	ΔV_{PS} = ±1.8V	A	25	48	52	-	dB
	ΔV_{PS} = ±1.8V	A	85	46	50	-	dB
	ΔV_{PS} = ±1.2V	A	-40	46	50	-	dB
Non-Inverting Input Bias Current		A	25	-	6	15	µA
		A	Full	-	10	25	µA
Non-Inverting Input Bias Current Drift		B	Full	-	5	60	nA/°C
Non-Inverting Input Bias Current Power Supply Sensitivity	ΔV_{PS} = ±1.8V	A	25	-	0.5	1	µA/V
	ΔV_{PS} = ±1.8V	A	85	-	0.8	3	µA/V
	ΔV_{PS} = ±1.2V	A	-40	-	0.8	3	µA/V
Non-Inverting Input Resistance	ΔV_{CM} = ±1.8V	A	25	0.8	2	-	MΩ
	ΔV_{CM} = ±1.8V	A	85	0.5	1.3	-	MΩ
	ΔV_{CM} = ±1.2V	A	-40	0.5	1.3	-	MΩ
Inverting Input Bias Current		A	25	-	2	7.5	µA
		A	Full	-	5	15	µA
Inverting Input Bias Current Drift		B	Full	-	60	200	nA/°C
Inverting Input Bias Current Common-Mode Sensitivity	ΔV_{CM} = ±1.8V	A	25	-	3	6	µA/V
	ΔV_{CM} = ±1.8V	A	85	-	4	8	µA/V
	ΔV_{CM} = ±1.2V	A	-40	-	4	8	µA/V

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +1, R_F = 560Ω, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 3) TEST LEVEL	TEMP. (°C)	MIN	TYP	MAX	UNITS
Inverting Input Bias Current Power Supply Sensitivity	ΔV_{PS} = ±1.8V	A	25	-	2	5	µA/V
	ΔV_{PS} = ±1.8V	A	85	-	4	8	µA/V
	ΔV_{PS} = ±1.2V	A	-40	-	4	8	µA/V
Inverting Input Resistance		C	25	-	40	-	Ω
Input Capacitance		C	25	-	2.5	-	pF
Input Voltage Common Mode Range (Implied by V_{IO} CMRR, $+R_{IN}$, and $-I_{BIAS}$ CMS tests)		A	25, 85	±1.8	±2.4	-	V
		A	-40	±1.2	±1.7	-	V
Input Noise Voltage Density	f = 100kHz	B	25	-	3.5	-	nV/√Hz
Non-Inverting Input Noise Current Density	f = 100kHz	B	25	-	2.5	-	pA/√Hz
Inverting Input Noise Current Density	f = 100kHz	B	25	-	20	-	pA/√Hz
TRANSFER CHARACTERISTICS							
Open Loop Transimpedance Gain	A_V = -1	C	25	-	500	-	kΩ
AC CHARACTERISTICS A_V = +2, R_F = 560Ω, Unless Otherwise Specified							
-3dB Bandwidth (V_{OUT} = 0.2V_{P-P})	A_V = +1, $+R_S$ = 560Ω	B	25	-	290	-	MHz
	A_V = +2	B	25	-	530	-	MHz
	A_V = -1, R_F = 510Ω	B	25	-	230	-	MHz
Full Power Bandwidth (V_{OUT} = 5V_{P-P} at A_V = +2/-1, 4V_{P-P} at A_V = +1)	A_V = +1, $+R_S$ = 560Ω	B	25	-	150	-	MHz
	A_V = +2	B	25	-	130	-	MHz
	A_V = -1, R_F = 510Ω	B	25	-	120	-	MHz
Gain Flatness (A_V = +2, V_{OUT} = 0.2V_{P-P})	To 25MHz	B	25	-	±0.04	-	dB
	To 50MHz	B	25	-	±0.11	-	dB
Minimum Stable Gain		A	Full	-	1	-	V/V
Crosstalk (Note 4)	5MHz	B	25	-	-73	-	dB
	10MHz	B	25	-	-64	-	dB
OUTPUT CHARACTERISTICS R_F = 560Ω, Unless Otherwise Specified							
Output Voltage Swing	A_V = -1, R_L = 100Ω	A	25	±3	±3.4	-	V
		A	Full	±2.8	±3	-	V
Output Current	A_V = -1, R_L = 50Ω	A	25, 85	50	60	-	mA
		A	-40	28	42	-	mA
Output Short Circuit Current		B	25	-	90	-	mA
DC Closed Loop Output Impedance	A_V = +2, R_F = 560Ω	B	25	-	0.07	-	Ω
Second Harmonic Distortion (A_V = +2, R_F = 560Ω, V_{OUT} = 2V_{P-P})	10MHz	B	25	-	-50	-	dBc
	20MHz	B	25	-	-45	-	dBc
Third Harmonic Distortion (A_V = +2, R_F = 560Ω, V_{OUT} = 2V_{P-P})	10MHz	B	25	-	-55	-	dBc
	20MHz	B	25	-	-50	-	dBc
TRANSIENT CHARACTERISTICS A_V = +2, R_F = 560Ω, Unless Otherwise Specified							
Rise and Fall Times (V_{OUT} = 0.5V_{P-P})	Rise Time	B	25	-	0.65	-	ns
	Fall Time	B	25	-	1.20	-	ns
Overshoot	V_{OUT} = 0.5V_{P-P}, V_{IN} t_{RISE} = 1.0ns	B	25	-	7	-	%

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +1, R_F = 560Ω, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 3) TEST LEVEL	TEMP. (°C)	MIN	TYP	MAX	UNITS
Slew Rate (V_{OUT} = 4V_{P-P}, A_V = +1, +R_S = 560Ω)	+SR	B	25	-	1050	-	V/µs
	-SR	B	25	-	800	-	V/µs
Slew Rate (V_{OUT} = 5V_{P-P}, A_V = +2)	+SR	B	25	-	1400	-	V/µs
	-SR	B	25	-	900	-	V/µs
Slew Rate (V_{OUT} = 5V_{P-P}, A_V = -1, R_F = 510Ω)	+SR	B	25	-	1950	-	V/µs
	-SR	B	25	-	1050	-	V/µs
Settling Time (V_{OUT} = +2V to 0V step)	To 0.1%	B	25	-	15	-	ns
	To 0.05%	B	25	-	20	-	ns
	To 0.02%	B	25	-	30	-	ns
Overdrive Recovery Time	V_{IN} = ±2V	B	25	-	8.5	-	ns
VIDEO CHARACTERISTICS A_V = +2, R_F = 560Ω, Unless Otherwise Specified							
Differential Gain (f = 3.58MHz)	R_L = 150Ω	B	25	-	0.02	-	%
	R_L = 75Ω	B	25	-	0.03	-	%
Differential Phase (f = 3.58MHz)	R_L = 150Ω	B	25	-	0.03	-	Degrees
	R_L = 75Ω	B	25	-	0.05	-	Degrees
DISABLE CHARACTERISTICS							
Disabled Supply Current	$V_{\overline{DISABLE}}$ = 0V	A	Full	-	3	4	mA/Op Amp
$\overline{DISABLE}$ Input Logic Voltage	Low	A	Full	-	-	0.8	V
	High	A	25, 85	2.0	-	-	V
		A	-40°C	2.4	-	-	V
$\overline{DISABLE}$ Input Logic Low Current	$V_{\overline{DISABLE}}$ = 0V	A	Full	-	100	200	µA
$\overline{DISABLE}$ Input Logic High Current	$V_{\overline{DISABLE}}$ = 5V	A	Full	-	1	15	µA
Output Disable Time	V_{IN} = ±1V, $V_{\overline{DISABLE}}$ = 2.4V to 0V	B	25	-	20	-	ns
Output Enable Time	V_{IN} = ±1V, $V_{\overline{DISABLE}}$ = 0V to 2.4V	B	25	-	160	-	ns
Disabled Output Capacitance	$V_{\overline{DISABLE}}$ = 0V	B	25	-	3.8	-	pF
Disabled Output Leakage	$V_{\overline{DISABLE}}$ = 0V, V_{IN} = +2V, V_{OUT} = ±3V	A	Full	-	2	10	µA
Off Isolation ($V_{DISABLE}$ = 0V, V_{IN} = 1V_{P-P}, A_V = +2)	At 5MHz	B	25	-	-61	-	dB
	At 10MHz	B	25	-	-55	-	dB
POWER SUPPLY CHARACTERISTICS							
Power Supply Range		C	25	±4.5	-	±5.5	V
Power Supply Current		A	25	5.6	5.8	6.1	mA/Op Amp
		A	Full	5.4	5.9	6.3	mA/Op Amp

NOTES:

3. Test Level: A. Production Tested.; B. Typical or Guaranteed Limit Based on Characterization.; C. Design Typical for Information Only.
4. The typical use for these amplifiers is in multiplexed configurations, where one amplifier (hostile channel) is enabled, and the passive channel is disabled. The crosstalk data specified is tested in this manner, with the input signal applied to the hostile channel, while monitoring the output of the passive channel. Crosstalk performance with both the hostile and passive channels enabled is typically: -63dB at 5MHz, and -50dB at 10MHz.

Application Information

Optimum Feedback Resistor

Although a current feedback amplifier's bandwidth dependency on closed loop gain isn't as severe as that of a voltage feedback amplifier, there can be an appreciable decrease in bandwidth at higher gains. This decrease may be minimized by taking advantage of the current feedback amplifier's unique relationship between bandwidth and R_F. All current feedback amplifiers require a feedback resistor, even for unity gain applications, and R_F, in conjunction with the internal compensation capacitor, sets the dominant pole of the frequency response. Thus, the amplifier's bandwidth is inversely proportional to R_F. The HFA1245 design is optimized for a 560Ω R_F at a gain of +2. Decreasing R_F decreases stability, resulting in excessive peaking and overshoot (Note: Capacitive feedback will cause the same problems due to the feedback impedance decrease at higher frequencies). At higher gains the amplifier is more stable, so R_F can be decreased in a trade-off of stability for bandwidth.

The table below lists recommended R_F values for various gains, and the expected bandwidth. For good channel-to-channel gain matching, it is recommended that all resistors (termination as well as gain setting) be ±1% tolerance or better. Note that a series input resistor, on +IN, is required for a gain of +1, to reduce gain peaking and increase stability.

GAIN (A_{CL})	R_F (Ω)	BANDWIDTH (MHz)
-1	510	230
+1	560 (+R_S = 560Ω)	290
+2	560	530

Non-inverting Input Source Impedance

For best operation, the DC source impedance looking out of the non-inverting input should be ≥50Ω. This is especially important in inverting gain configurations where the non-inverting input would normally be connected directly to GND.

Optional GND Pin for TTL Compatibility

The HFA1245 derives an internal GND reference for the digital circuitry as long as the power supplies are symmetrical about GND. The GND reference is used to ensure the TTL compatibility of the $\overline{\text{DISABLE}}$ inputs. With symmetrical supplies the GND pin (Pin 12) may be floated, or connected directly to GND. If asymmetrical supplies (e.g., +10V, 0V) are utilized, and TTL compatibility is desired, the GND pin must be connected to GND.

PC Board Layout

The frequency response of this amplifier depends greatly on the amount of care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10μF) tantalum in parallel with a small value (0.1μF) chip capacitor works well in most cases.

Terminated microstrip signal lines are recommended at the input and output of the device. Capacitance directly on the output must be minimized, or isolated as discussed in the next section.

Care must also be taken to minimize the capacitance to ground seen by the amplifier's inverting input (-IN). The larger this capacitance, the worse the gain peaking, resulting in pulse overshoot and possible instability. To this end, it is recommended that the ground plane be removed under traces connected to -IN, and connections to -IN should be kept as short as possible.

Driving Capacitive Loads

Capacitive loads, such as an A/D input, or an improperly terminated transmission line will degrade the amplifier's phase margin resulting in frequency response peaking and possible oscillations. In most cases, the oscillation can be avoided by placing a resistor (R_S) in series with the output prior to the capacitance.

Figure 1 details starting points for the selection of this resistor. The points on the curve indicate the R_S and C_L combinations for the optimum bandwidth, stability, and settling time, but experimental fine tuning is recommended. Picking a point above or to the right of the curve yields an overdamped response, while points below or left of the curve indicate areas of underdamped performance.

R_S and C_L form a low pass network at the output, thus limiting system bandwidth well below the amplifier bandwidth of 290MHz (for A_V = +1). By decreasing R_S as C_L increases (as illustrated in the curves), the maximum bandwidth is obtained without sacrificing stability. Even so, bandwidth does decrease as you move to the right along the curve. For example, at A_V = +1, R_S = 62Ω, C_L = 40pF, the overall bandwidth is limited to 180MHz, and bandwidth drops to 70MHz at A_V = +1, R_S = 8Ω, C_L = 400pF.

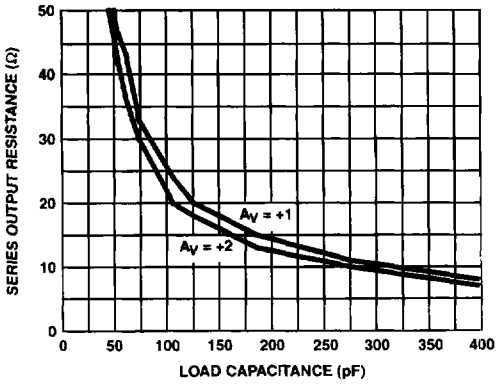


FIGURE 1. RECOMMENDED SERIES OUTPUT RESISTOR vs LOAD CAPACITANCE

Die Characteristics

DIE DIMENSIONS:

69 mils x 92 mils x 19 mils
1750µm x 2330µm x 483µm

METALLIZATION:

Type: Metal 1: AlCu(2%)/TiW
Thickness: Metal 1: 8kÅ ±0.4kÅ

Type: Metal 2: AlCu(2%)
Thickness: Metal 2: 16kÅ ±0.8kÅ

SUBSTRATE POTENTIAL (Powered Up):

Floating (Recommend Connection to V-)

PASSIVATION:

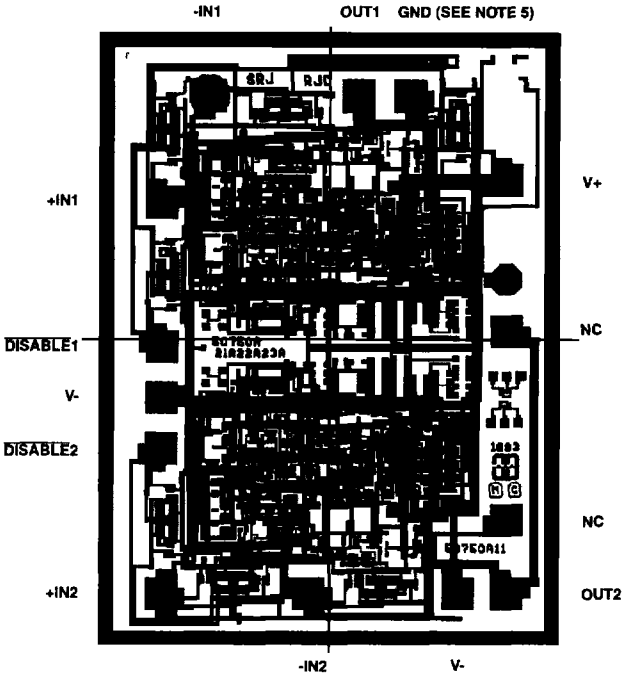
Type: Nitride
Thickness: 4kÅ ±0.5kÅ

TRANSISTOR COUNT:

180

Metallization Mask Layout

HFA1245



NOTE:

5. This is an optional GND pad. Users may set a GND reference, via this pad, to ensure the TTL compatibility of the $\overline{\text{DISABLE}}$ inputs when using asymmetrical supplies (e.g., V+ = 10V, V- = 0V). See the "Application Information" section for details.