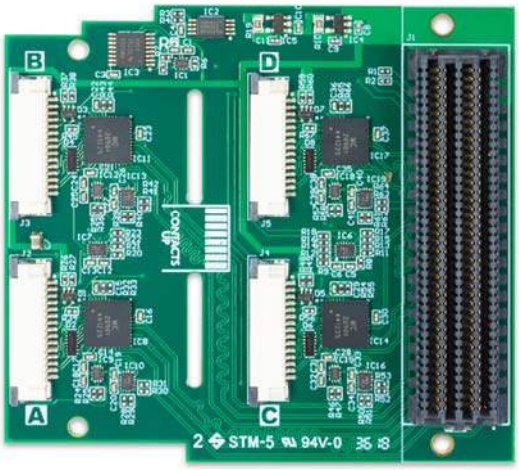
FMC Pcam Adapter Reference Manual

The FMC Pcam Adapter is an FMC mezzanine (peripheral) board allowing interfacing up to four Pcam camera modules to field-programmable gate array (FPGA) based systems. It extends the capabilities of development platforms to enable multi-camera video applications.



Features

- Two/Four Pcam system-side connectors
- Level translators from MIPI D-PHY to LVDS and LVCMOS
- Male FMC LPC connector for digital signals
- Compatible with a wide range of V_{ADJ} voltages (1.8V – 3.3V)

Purchasing Options

There are two variants available: Dual and Quad, based on the number of Pcam connectors and related circuitry. Dual makes connecting two Pcam 5C (or similar) possible, with Quad increasing that to four.

Revision History

Created April 9, 2019

This manual applies to REV C.0 of both variants (Dual and Quad) of the board.

Carrier Card Compatibility

As with any FMC mezzanine module, there are some compatibility requirements. These must be evaluated before connecting and powering the module.

- Supported V_{ADJ} voltage range is 1.8 V - 3.3 V. The voltage is controlled by the carrier card.
- The carrier card must be capable of providing enough current. See **Power Supplies**.
- Must use I/O standards compatible with the voltage levels of the digital outputs, and the chosen V_{ADJ}. For example, LVDS_25 and LVCMOS25 with a V_{ADJ} of 2.5V.
- Receiver signal termination for outputs is the responsibility of the carrier card. For example, DIFF_TERM can be used for LVDS_25 and a $V_{ADJ}$of 2.5V.
- The carrier card might have either the low-pin count or the high-pin count FMC female connector. However, not all pins are required to be wired. Compare the carrier card FMC pin-out against the pin-out from chapter 1.4 below.

FPGA I/O Architecture Compatibility

Receiving several independent source-synchronous high-speed interfaces in the FPGA is no easy feat due to I/O and clocking restrictions specific to the FPGA architecture. The VITA 57.1 specs are not granular enough for the requirements of today's high-speed I/O architectures. Therefore, not all carrier cards will be able to support all ports of the FMC Pcam Adapter simultaneously. Some of the requirements are:

- Clock inputs are mapped to LA00, LA01, LA17, and LA18. Verify that the carrier board maps these to clock-capable input pins.
- Each clock has two data lanes associated with it. Verify that the clock signal can be routed to I/O primitives sampling the data lanes. On some architectures the clock and its data lanes must be mapped to the same bank.
- Two ports are mapped to LA00-LA16, and the other two mapped to LA17-LA33. Usually, carrier cards split these groups into separate banks. Therefore, each bank must support two ports at once. This puts a considerable constraint on the resources available in each bank. Clock buffers, PLLs and high-speed de-serialization primitives must be capable of receiving two independent D-PHY interfaces. The UltraScale architecture in particular has a very restrictive clock/strobe propagation mechanism. The side-effect of propagation is that some pins are made unavailable for other purposes including other Pcam ports. This might include pins unrelated to FMC, but mapped to the FMC bank.

Digilent recommends implementing an RTL design with the desired number of D-PHY interfaces constrained to the pinout of the carrier card to be used for development before committing to the FMC Pcam Adapter.

Compatibility Matrix

The table below lists carrier cards confirmed compatible by Digilent. Boards not listed can still be compatible, if the requirements above are met. Check back for updates as the list will be extended.

Carrier Card	Manufacturer	FMC Port	V_{ADJ}	Simultaneous Pcam Port Usage			
				A	B	C	D
ZedBoard	Digilent	J1 (LPC)	2.5 V	✓	✓	✓	✓

Table 1. Confirmed compatibility matrix.

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1. Functional Description

The adapter board's main purpose is to translate the MIPI D-PHY input to LVDS/LVCMOS outputs that are supported on most FPGAs. It also translates the 3.3V control signals of the Pcam to the adjustable I/O voltage powering the FMC bank, V_{ADJ}. Therefore, compatibility is extended to boards with FPGAs that have only low-voltage I/O banks (<= 1.8V).

1.1. Pcam ports

The Pcam ports are system-side, 15-pin, bottom-load, top-contact FFC connectors. Pcam modules are connected using the flexible-foil cable provided with them. The correct cable orientation is with the contact pads facing away from the board. Please see Figure 2 below for details.

Ports are designated with letters from A to D in the Quad variant and A to B in the Dual variant. All signals have the letter designator in their name. It is also written on the silkscreen of the PCB.

Ports C and D were designed to channel the cable through cut-outs on the board so that four Pcam modules can be accommodated.

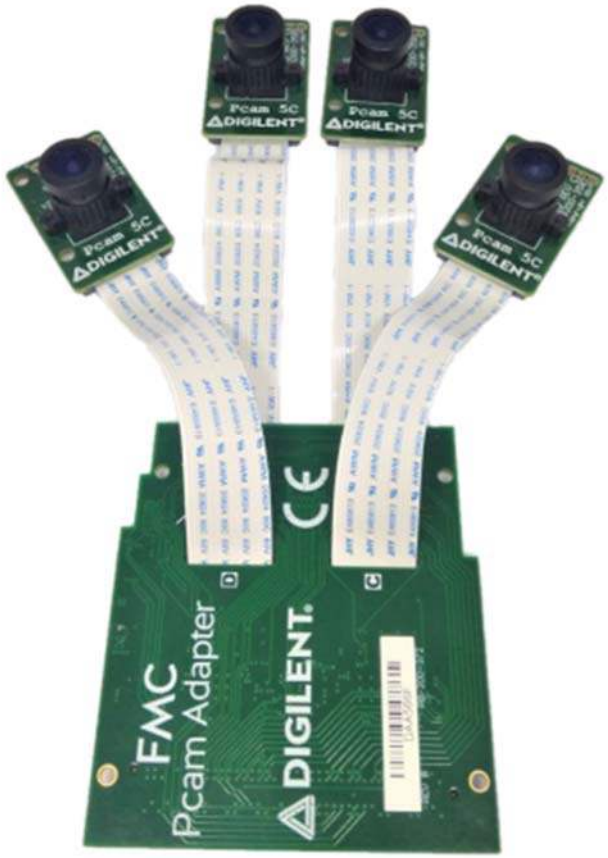

Figure 1. Four Camera Connection

Figure 2. Camera Connection Detail

1.2. Level translators

There are two types of level translators onboard: for control signals and for MIPI D-PHY inputs. Both translate between voltage levels of the FMC bank supplied by V_{ADJ} and a second power domain.

1.2.1. Control signals

Control signals are driven by SN74AVC4T245 or SN74AVC2T245, which are 4-bit or 2-bit dual-supply voltage level translation devices. The A-side pins are supported by VCCA, and the B-side are supported by VCCB. Starting from the logic diagram shown underneath, a high on DIR allows data transmission from side A to side B. Similarly, a low on DIR and OE# allows data transmission from side B to side A. When OE# is set to high, both sides are isolated, and all their pins are in the high-impedance state.

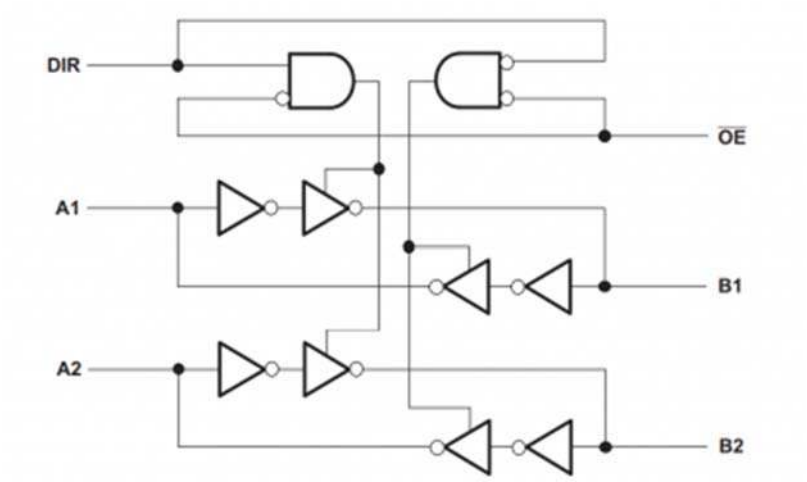

Figure 3. Logic Diagram for SN74AVC4T245

Some control signals are uni-directional, so the DIR and OE# of their level translators are hard-wired to always-on. These are: **CAM[A-D]_BTA**, **CAM_PWUP**, **LP[A-D]_LANE1_[PN]_LS**, and **LP[A-D]_CLK_[PN]_LS**.

Other control signals are bi-directional, so their DIR and OE# are available to the user. These are **CAM[A-D]_GPIO1** and **LP[A-D]_LANE0_[PN]_LS**.

GPIO1 signals from all four ports are controlled as a group using common **CAM_GPIO1_OEN** and **CAM_GPIO1_DIR**. The GPIO1 signals are connected to the camera ports (one per port). On Pcam 5C they are unused, but on other cameras they may have some extra functionality.

CONTROL INPUTS		OUTPUT CIRCUITS		
CAM_GPIO1_OEN#	**CAM_GPIO1_DIR**	**A Side**	**B Side**	**OPERATION**
L	L	Enabled	Hi-Z	From FMC to Pcam
L	H	Hi-Z	Enabled	From Pcam to FMC
H	-	Hi-Z	Hi-Z	N/A

Table 1. Summary of Communication Modes

LP[A-D]_LANE0_[PN]_LS signals support per-port direction reversal using CAM[A-D]_BTA. This functionality is described in chapter **1.6** below.

1.2.1. MIPI D-PHY inputs

The conversion of MIPI D-PHY input streams into LVDS high-speed and CMOS low-power is made with the MC20901 IC from Meticom. This requires an understanding of lane states and is done automatically by the level translator. It separates the superimposed low-power and high-speed voltage levels into dedicated signals easier to interpret by the FPGA input buffers.

MIPI D-PHY	**FPGA**
MIPI[A-D]_LANE0_[PN]	HS[A-D]_LANE0_[PN]
	LP[A-D]_LANE0_[PN]_LS
MIPI[A-D]_LANE1_[PN]	HS[A-D]_LANE1_[PN]
	LP[A-D]_LANE1_[PN]_LS
MIPI[A-D]_CLK_[PN]	HS[A-D]_CLK_[PN]

MIPI D-PHY	FPGA
	LP[A-D]_CLK_[PN]_LS

Table 2. MIPI D-PHY level translation

1.3. Voltage levels of output signals

The high-speed outputs are compliant with Xilinx LVDS_25 and LVDS standards. These standards have a typical input common-mode voltage of 1.2V for 100Ω transmission lines. It is important to mention that for LVDS high-speed lines, 100Ω differential termination is needed at the receiver, on the carrier board. The Xilinx LVDS_25 and LVDS standards offer the possibility of enabling differential termination internal to the FPGA (using DIFF_TERM = TRUE constraint); for this the constraint file has to be modified accordingly. If the carrier board has external differential termination on these lines, the DIFF_TERM constraint is not needed.

The low-power signals are compliant with the LVCMOS standard corresponding to the selected V_{ADJ} voltage level.

The DC characteristics for the high-speed outputs of the MC20901 IC are listed in the table below.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{CM-OUT}	Output common mode voltage	V_{DD}=1.2V	1.09	1.2	1.31	V
$V_{DO-Diff}$	Differential output voltage		250	300	350	mVp
Z_{OD}	Output impedance	Differential	80	100	120	Ω

Table 3. High-Speed Outputs (HS-X-P, HS-X-N)

1.4. Pin-out

FMC Pin	MIPI Function	FMC Pin	MIPI Function
LA01_P_CC	HSA_CLK_P	**LA19_P**	HSC_LANE1_P

LA10_P	HSA_LANE0_P	**LA22_P**	LPC_CLK_P_LS
LA06_P	HSA_LANE1_P	**LA25_P**	LPC_LANE0_P_LS
LA08_P	LPA_CLK_P_LS	**LA24_P**	LPC_LANE1_P_LS
LA03_P	LPA_LANE0_P_LS	**LA29_P**	CAMC_BTA
LA12_P	LPA_LANE1_P_LS	**LA11_N**	CAMC_GPIO1
LA16_P	CAMA_BTA	**LA18_P_CC**	HSD_CLK_P
LA07_N	CAMA_GPIO1	**LA23_P**	HSD_LANE0_P
LA00_P_CC	HSB_CLK_P	**LA27_P**	HSD_LANE1_P
LA02_P	HSB_LANE0_P	**LA21_P**	LPD_CLK_P_LS
LA04_P	HSB_LANE1_P	**LA26_P**	LPD_LANE0_P_LS
LA09_P	LPB_CLK_P_LS	**LA28_P**	LPD_LANE1_P_LS
LA13_P	LPB_LANE0_P_LS	**LA29_N**	CAMD_BTA
LA05_P	LPB_LANE1_P_LS	**LA15_P**	CAMD_GPIO1
LA16_N	CAMB_BTA	**LA14_P**	CAM_GPIO1_OEN
LA11_P	CAMB_GPIO1	**LA07_P**	CAM_PWUP

LA17_P_CC	HSC_CLK_P	**LA15_N**	CAM_GPIO1_DIR
LA20_P	HSC_LANE0_P		

Table 4. Pin Mapping

1.5. I2C Switch

All the cameras are configured using I²C. As all the cameras have identical I²C addresses, a 4-port I²C switch (TCA9546A) is used to connect the master SCL/SDA signal pair to all the cameras, one switch channel corresponding to one camera. It is important to mention that the master can select each individual switch channel as well as any combination of the four channels, SC0/SD0-SC3/SD3.

The power-on state of the switch is with the channels disabled. Therefore, before any communication with the Pcam ports can take place the corresponding channel must be enabled.

In order to configure the I²C switch, the master must send a start condition via I²C followed by the switch address. The switch address is selectable through GA0 and GA1 FMC connector pins. The switch address is 8 bits long and starts with “11100” followed by the logic values on the GA0 and GA1 pins, respectively. The last bit is reserved to define the operation to be performed. Logic 1 is the equivalent for read and 0 for write. After a successful acknowledgment of an address by the switch, the I²C master device sends a byte to the switch, which is then stored in its control register. This control register enables or disables each individual channel. Logic 1 on bits 0-3 in the control register enable channels SC0/SD0 - SC3/SD3. Conversely, logic 0 will disable the channel.

Once the switch is configured to enable the desired channel(s), a new start condition can be generated by the I²C master, after which it can output on his I²C bus the address of the camera with whom it is trying to communicate.

1.6. Low-Power Reverse Communication/Bus turn-around (BTA)

Normally MIPI CSI-2 lanes are unidirectional, input to the module. Support for bidirectional lanes and low-power reverse escape mode is provided on lane 0 of each Pcam port only. Control signals CAM[A-D]_BTA decide the direction of communication. Logic low is the normal use case, where the Pcam module is transmitting and the FMC Pcam Adapter forwards data to the FPGA. A logic high will reverse data flow and low-power signals from the FPGA will be forwarded to the Pcam module. A 4.7 Kohm pull-down on CAM[A-D]_BTA is provided on-board.

High-Speed Reverse Communication is not supported.

CAM[A-D]_BTA	Data flow	
	HS[A-D]_LANE0	LP[A-D]_LANE0_LS
Low	from Pcam to FMC	from Pcam to FMC
High	N/A	from FMC to Pcam

Table 5. Summary of Communication Modes

1.7. Power supplies

The adapter board is powered from three power rails available in the FMC connector.

Power rail	Powered circuits	Maximum current consumption [mA]	
		Quad	Dual
3P3VAUX	IPMI FRU EEPROM, I2C multiplexer	20	20
3P3V	LDOs, Pcam VCC3V3, level translators	1000	500
V_{ADJ}	Level translators	400	200

Table 6. Loads on FMC Power Rails

Two LDOs provide additional voltages for the level translators. Power rails VCC2V5 and VCC1V2 are used internally only and not provided to any external circuit.

Power rail	Powered circuits	Max current consumption [mA]	
		Quad	Dual

VCC2V5	Level translators	160	80
VCC1V2	Level translators	8	4

Table 7. Loads on Internal Power Rails

1.8. FMC Support

The FMC Pcam Adapter uses a Samtec ASP-134604-01 low pin-count male connector as the main connector for digital signals. The board fully conforms to the VITA 57.1 specs. The connector supports the full range of 1.8V-3.3V bank supply voltages (V_{ADJ}). Check compatibility requirements above.

I^2C serves as the IPMI EEPROM, providing hardware definition information. For more information, consult the VITA 57.1 specs.