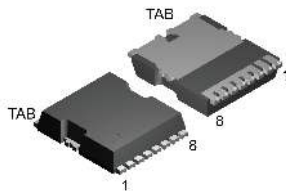
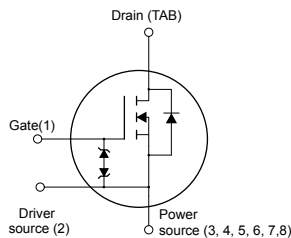


N-channel 600 V, 48 mΩ typ., 58 A MDmesh DM6 Power MOSFET in a TO-LL package


TO-LL type A2


N-chG1DS2PS345678DTABZ


Product status link
[STO67N60DM6](#)
Device summary

Order code	STO67N60DM6
Marking	67N60DM6
Package	TO-LL type A2
Packing	Tape and reel

Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
STO67N60DM6	600 V	59 mΩ	58 A

- Fast-recovery body diode
- Lower R_{DS(on)} per area vs previous generation
- Low gate charge, input capacitance and resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

Applications

- Switching applications

Description

This high-voltage N-channel Power MOSFET is part of the MDmesh DM6 fast-recovery diode series. Compared with the previous MDmesh fast generation, DM6 combines very low recovery charge (Q_{rr}), recovery time (t_{rr}) and excellent improvement in R_{DS(on)} per area with one of the most effective switching behaviors available in the market for the most demanding high-efficiency bridge topologies and ZVS phase-shift converters.

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	58	A
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	37	
$I_{DM}^{(2)}$	Drain current (pulsed)	190	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	240	W
$dv/dt^{(3)}$	Peak diode recovery voltage slope	100	V/ns
$di/dt^{(3)}$	Peak diode recovery current slope	1000	A/ μs
$dv/dt^{(4)}$	MOSFET dv/dt ruggedness	100	V/ns
T_{stg}	Storage temperature range	-55 to 150	$^\circ\text{C}$
T_J	Operating junction temperature range		$^\circ\text{C}$

1. Referred to TO-247 package.
2. Pulse width is limited by safe operating area.
3. $I_{SD} \leq 33\text{ A}$, $V_{DS}(\text{peak}) < V_{(BR)DSS}$, $V_{DD} = 400\text{ V}$.
4. $V_{DS} \leq 480\text{ V}$.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.52	$^\circ\text{C/W}$
R_{thJB}	Thermal resistance, junction-to-board ⁽¹⁾	43	$^\circ\text{C/W}$
	Thermal resistance, junction-to-board ⁽²⁾	22	

1. When mounted on 1 inch² FR-4 pcb, standard footprint 2 Oz copper board.
2. When mounted on 40x40mm FR-4 pcb, 6 cm² 2 Oz copper board.

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_J max.)	9	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	845	mJ

2 Electrical characteristics

$T_C = 25\text{ °C}$ unless otherwise specified.

Table 4. On /off-states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	600			V
I_{DSS}	Zero-gate voltage drain current	$V_{GS} = 0\text{ V}, V_{DS} = 600\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}, V_{DS} = 600\text{ V}, T_C = 125\text{ °C}^{(1)}$			100	
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}, V_{GS} = \pm 25\text{ V}$			± 5	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	3.25	4.00	4.75	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 29\text{ A}$		48	59	m Ω

1. Defined by design, not subject to production test.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 100\text{ V}, f = 1\text{ MHz}$	-	3400	-	pF
C_{oss}	Output capacitance		-	280	-	pF
C_{rSS}	Reverse transfer capacitance		-	2	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 0\text{ to }480\text{ V}$	-	520	-	pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	1.5	-	Ω
Q_g	Total gate charge	$V_{DD} = 480\text{ V}, I_D = 52\text{ A}, V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 14. Test circuit for gate charge behavior)	-	72.5	-	nC
Q_{gs}	Gate-source charge		-	24.5	-	nC
Q_{gd}	Gate-drain charge		-	28.5	-	nC

1. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}, I_D = 23.75\text{ A},$ $R_G = 4.7\text{ }\Omega, V_{GS} = 10\text{ V}$	-	24.5	-	ns
t_r	Rise time		-	32	-	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 13. Switching times test circuit for resistive load and Figure 18. Switching time waveform)	-	87.5	-	ns
t_f	Fall time		-	8.6	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		58	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		190	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 58\text{ A}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 47.5\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$,	-	125		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 60\text{ V}$	-	0.6		μC
I_{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	9.6		A
t_{rr}	Reverse recovery time	$I_{SD} = 47.5\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$,	-	228		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 60\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$	-	2.34		μC
I_{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	20.5		A

1. Pulse width is limited by safe operating area.
2. Pulse test: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

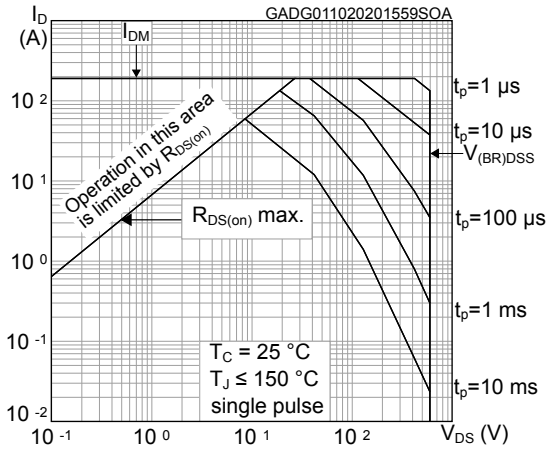


Figure 2. Maximum transient thermal impedance

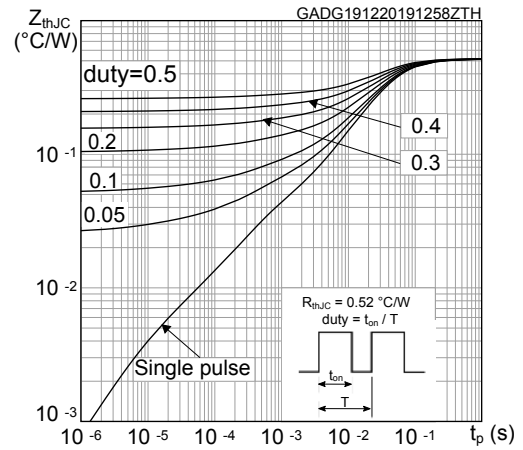


Figure 3. Typical output characteristics

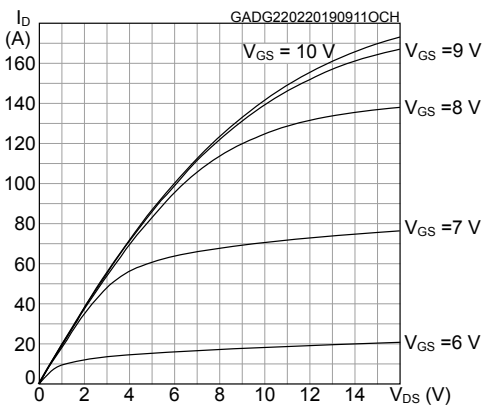


Figure 4. Typical transfer characteristics

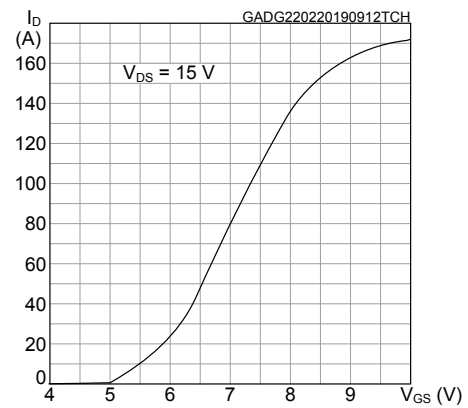


Figure 5. Typical gate charge characteristics

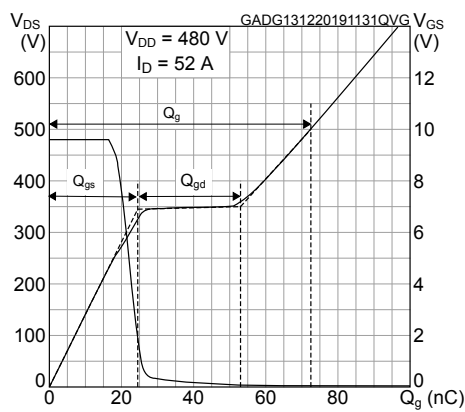


Figure 6. Typical drain-source on-resistance

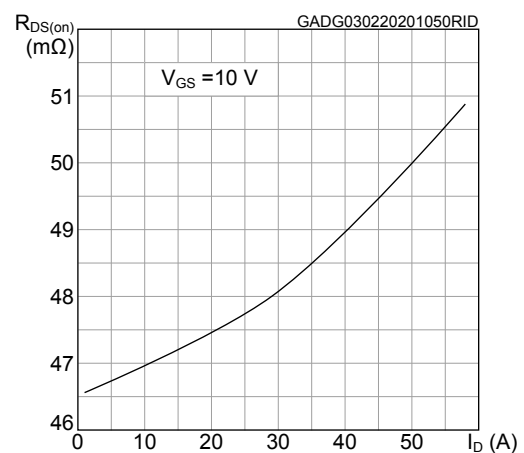


Figure 7. Typical capacitance characteristics

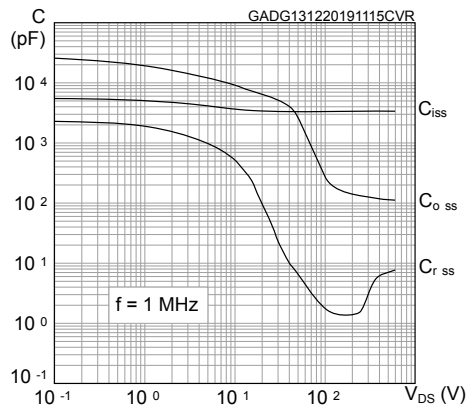


Figure 8. Normalized gate threshold vs. temperature

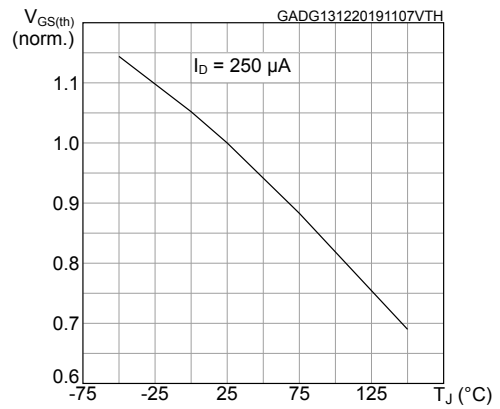


Figure 9. Normalized on-resistance vs. temperature

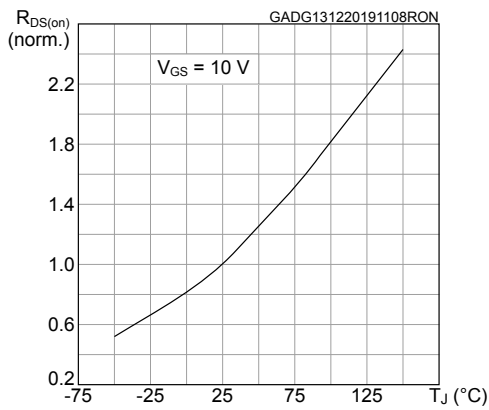


Figure 10. Normalized breakdown voltage vs temperature

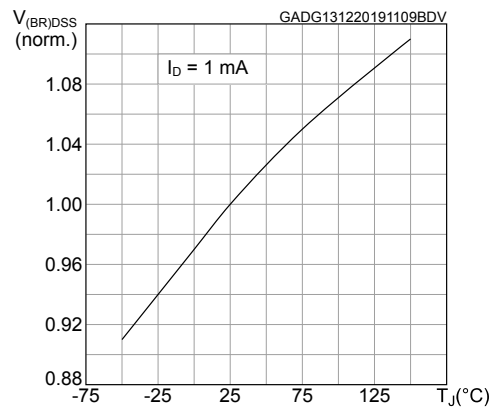


Figure 11. Output capacitance stored energy

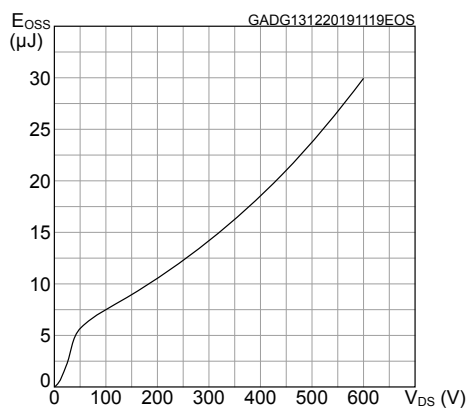
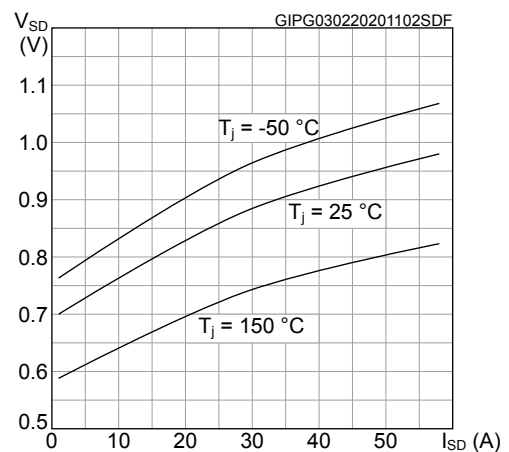
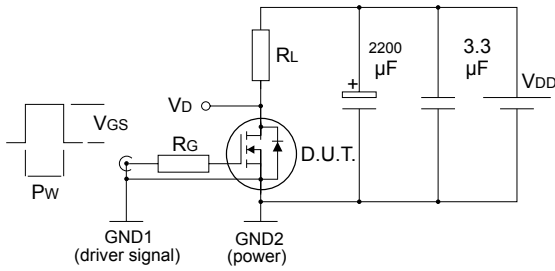


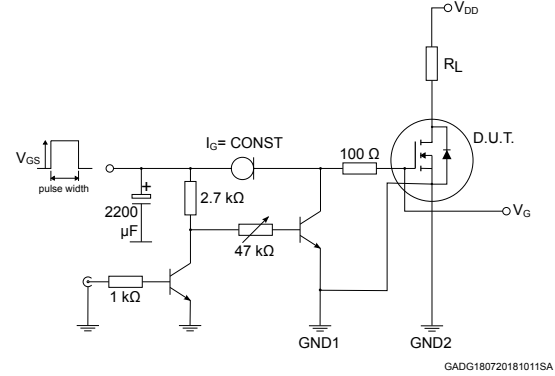
Figure 12. Typical reverse diode forward characteristics



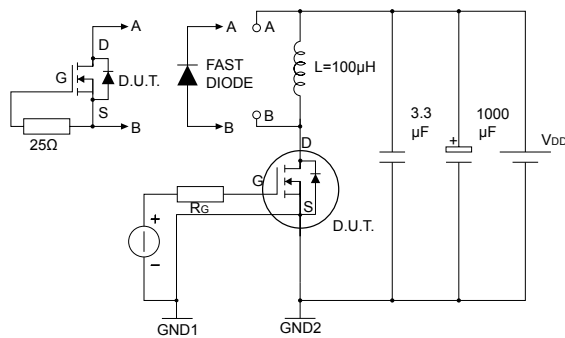
3 Test circuits

Figure 13. Switching times test circuit for resistive load


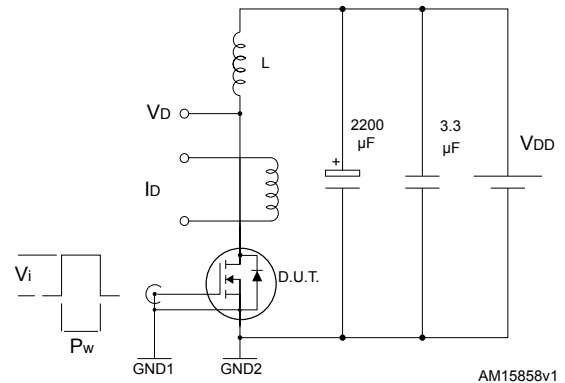
AM15855v1

Figure 14. Test circuit for gate charge behavior


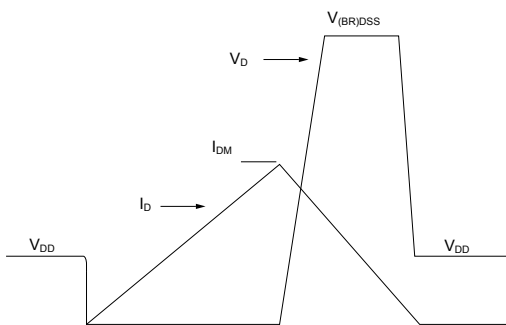
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Figure 15. Test circuit for inductive load switching and diode recovery times


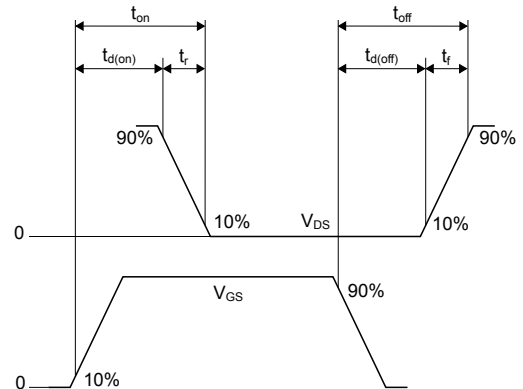
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Figure 16. Unclamped inductive load test circuit


AM15858v1

Figure 17. Unclamped inductive waveform


AM01472v1

Figure 18. Switching time waveform


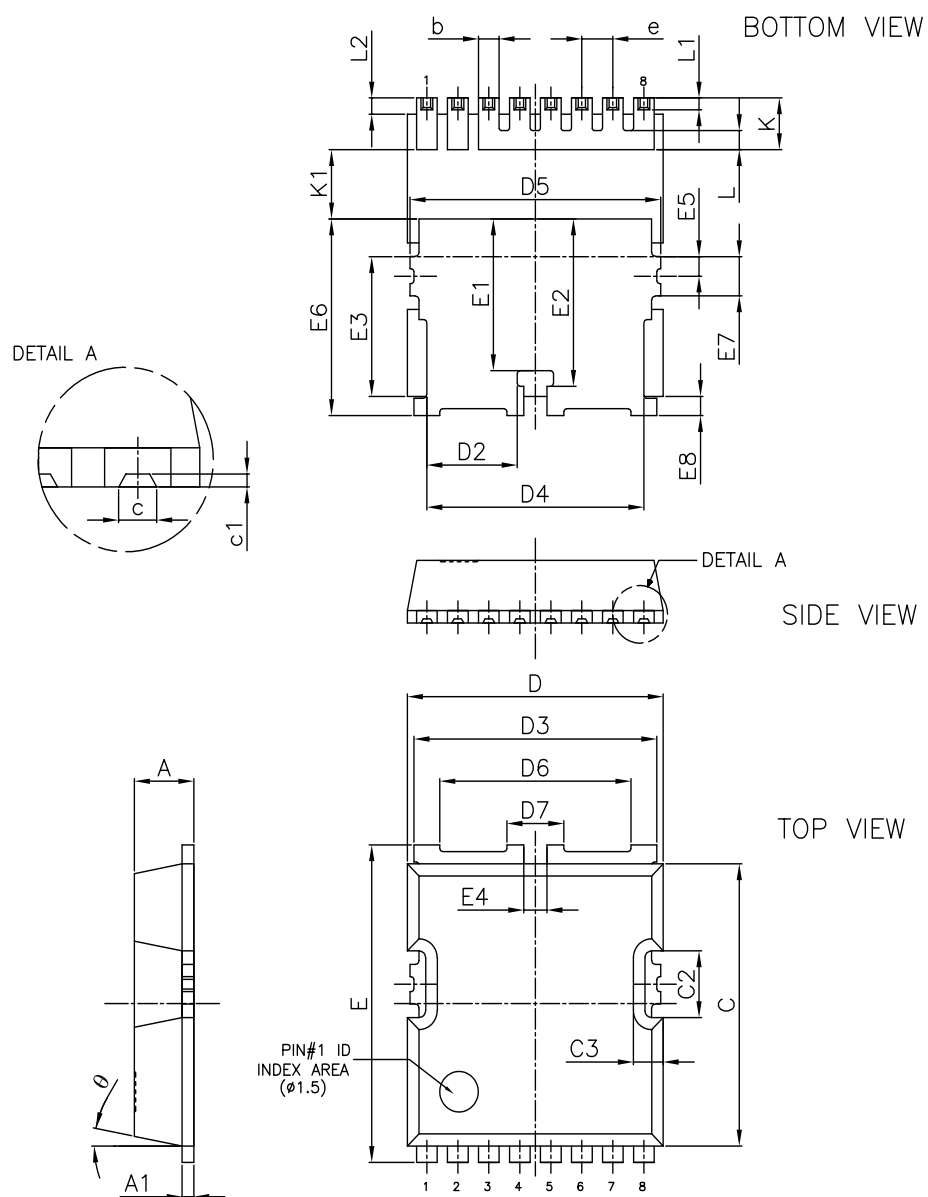
AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-LL type A2 package information

Figure 19. TO-LL type A2 package outline

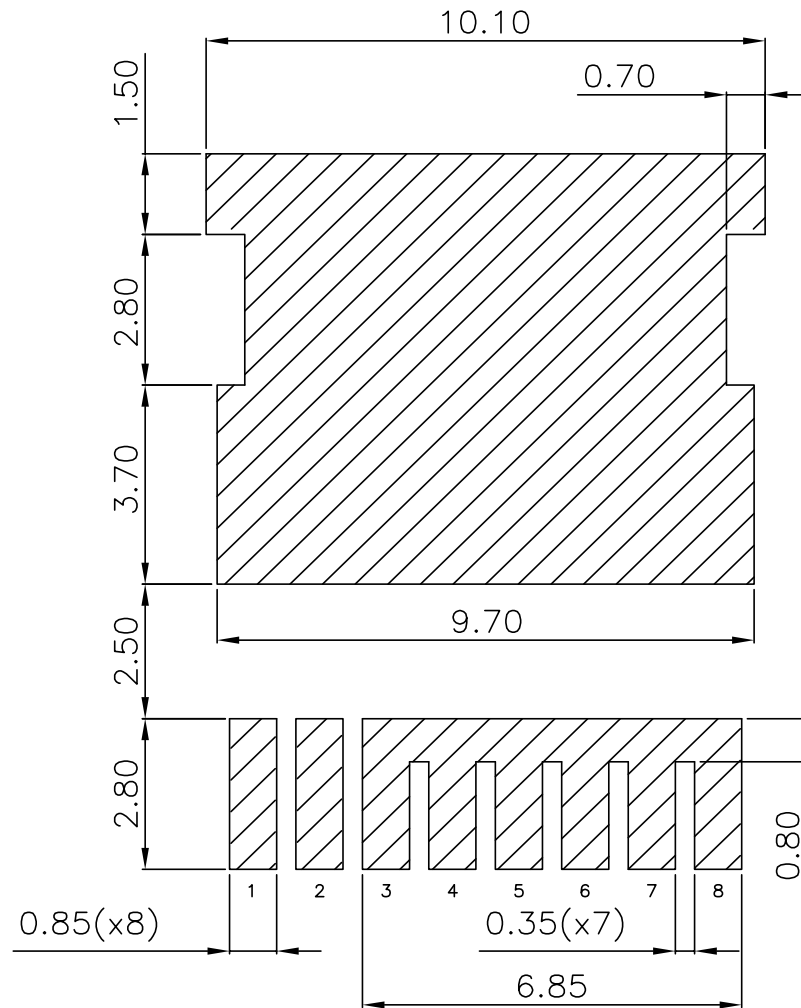


DM00276569_5_type_A2

Table 8. TO-LL type A2 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.40
A1	0.40	0.48	0.60
b	0.70	0.80	0.90
c		0.46	
c1		0.15	
C	10.28	10.38	10.48
C2	2.35	2.45	2.55
C3		1.16	
D	9.80	9.90	10.00
D2	3.30	3.50	3.70
D3	9.30	9.40	9.50
D4	8.20	8.40	8.60
D5	9.50	9.70	9.90
D6		7.40	
D7		2.20	
e		1.20	
E	11.48	11.68	11.88
E1		5.58	
E2		6.15	
E3		5.14	
E4		0.90	
E5		0.72	
E6	7.03	7.23	7.43
E7		1.44	
E8	0.50	0.70	0.90
K	1.70	1.90	2.10
K1	2.40		
L		0.70	
L1		0.44	
L2	0.40	0.60	0.80
θ		11°	

Figure 20. TO-LL type A2 recommended footprint (dimensions are in mm)



DM00276569_5_type_A2

4.2 TO-LL packing information

Figure 21. Carrier tape outline and dimensions

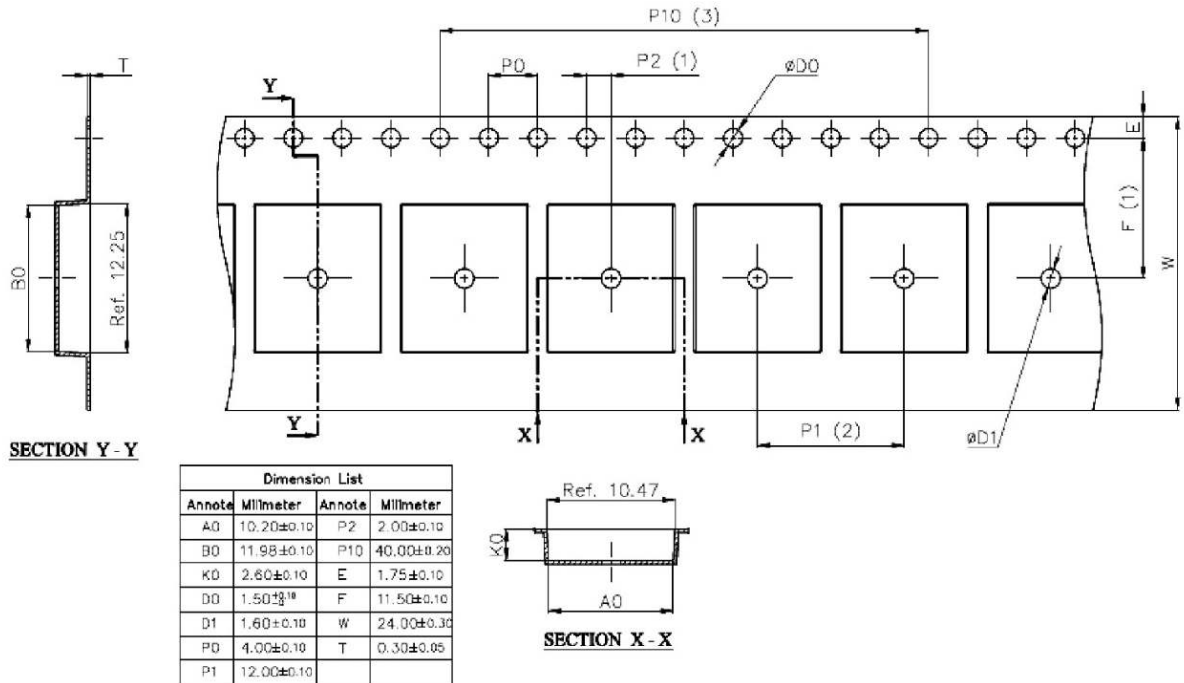


Figure 22. Reel outline and dimensions

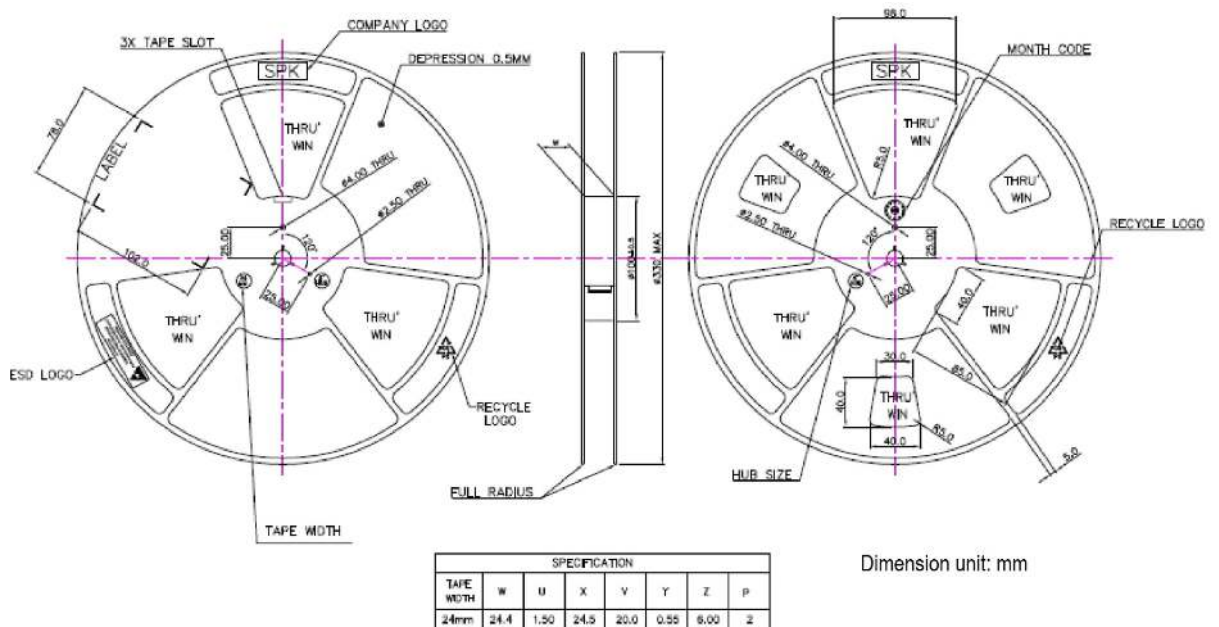
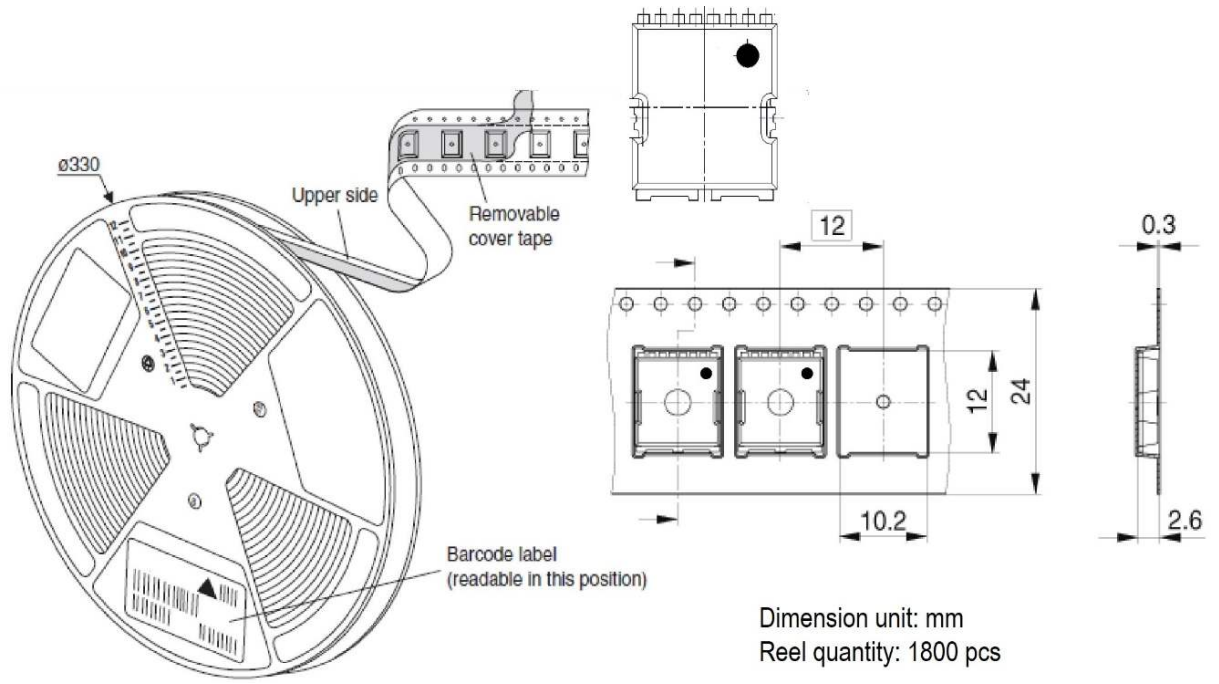


Figure 23. TO-LL orientation in tape pocket



Revision history

Table 9. Document revision history

Date	Revision	Changes
03-Feb-2020	1	First release.
20-Mar-2020	2	Updated title of the document, section <i>Features</i> , <i>Table 1. Absolute maximum ratings</i> , <i>Table 4. On /off-states</i> and <i>Table 7. Source-drain diode</i> .
28-Jul-2020	3	Updated <i>Table 1. Absolute maximum ratings</i> . Added <i>Section 4.2 TO-LL packing information</i> .
30-Apr-2021	4	Updated <i>title</i> and <i>Device summary</i> in cover page. Updated <i>Section 4 Package information</i> . Minor text changes.
08-Jun-2021	5	Modified features and I_D value on cover page. Modified <i>Table 1. Absolute maximum ratings</i> , <i>Table 2. Thermal data</i> , <i>Table 4. On /off-states</i> and <i>Table 7. Source-drain diode</i> . Modified <i>Figure 1. Safe operating area</i> , <i>Figure 2. Maximum transient thermal impedance</i> , <i>Figure 6. Typical drain-source on-resistance</i> and <i>Figure 12. Typical reverse diode forward characteristics</i> . Minor text changes.

Contents

1	Electrical ratings	2
2	Electrical characteristics	3
2.1	Electrical characteristics (curves)	5
3	Test circuits	7
4	Package information	8
4.1	TO-LL type A2 package information	8
4.2	TO-LL packing information	11
	Revision history	13

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