

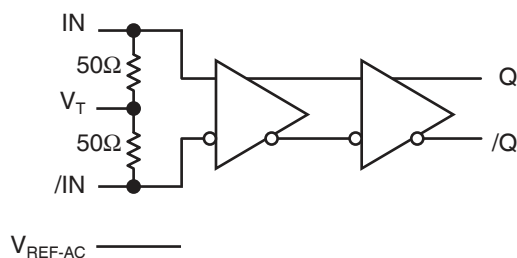
FEATURES

- **Guaranteed AC performance over temperature and voltage:**
 - DC-to >10.7Gbps data rate throughput
 - DC-to >7GHz clock f_{MAX}
 - <250ps In-to-Out t_{pd}
 - $t_r / t_f < 70ps$
- **Ultra low-jitter design:**
 - 75fs RMS phase jitter
- **Minimum input swing 200mV ($|IN-|IN|$)**
- **Unique, patent-pending input termination and VT pin accepts DC- and AC-coupled inputs (CML, PECL, LVDS)**
- **Typical 400mV LVPECL output swing**
- **Power supply 2.5V $\pm 5\%$ or 3.3V $\pm 10\%$**
- **-40°C to 85°C industrial temperature range**
- **Available in an ultra-small (2mm \times 2mm) 8-pin QFN package**

APPLICATIONS

- Backplane buffering
- OC-12 to OC-192 SONET/SDN clock/data distribution
- All Gigabit Ethernet distribution
- Fibre Channel distribution

FUNCTIONAL BLOCK DIAGRAM



DESCRIPTION

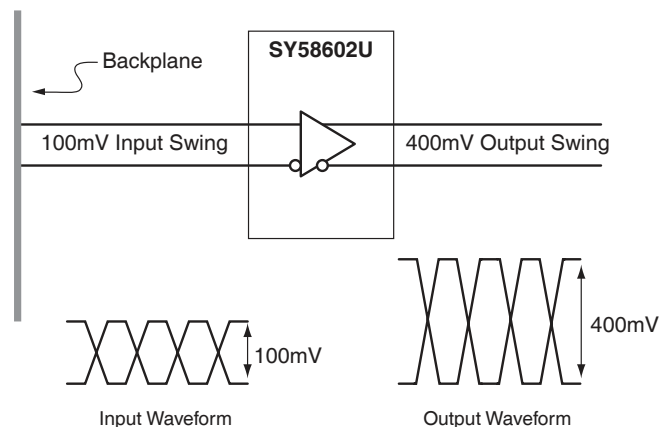
The SY58602U is a 2.5V/3.3V precision, high-speed, differential receiver capable of handling clocks up to 7GHz and data streams up to 10.7Gbps.

The differential input includes Micrel's unique, 3-pin input termination architecture that allows users to interface to any differential signal (AC- or DC-coupled) as small as 200mV_{pp} without any level shifting or termination resistor networks in the signal path. The outputs are 400mV LVPECL, with extremely fast rise/fall times guaranteed to be less than 70ps.

The SY58602U operates from a +2.5V $\pm 5\%$ supply or a +3.3V $\pm 10\%$ supply and is guaranteed over the full industrial temperature range of -40°C to +85°C. For applications that require CML outputs, consider the SY58600U or for 800mV LVPECL outputs the SY58601U. The SY58602U is part of Micrel's high-speed, Precision Edge® product line.

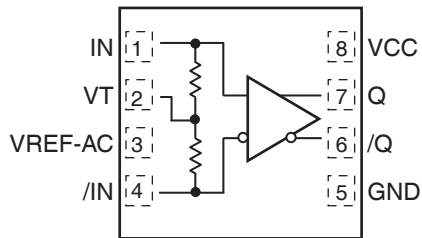
All support documentation can be found on Micrel's web site at: www.micrel.com.

TYPICAL APPLICATION



PACKAGE/ORDERING INFORMATION

Ordering Information⁽¹⁾



8-Pin QFN

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY58602UMGTR ⁽²⁾	MLF-8	Industrial	602 with Pb-Free bar-line indicator	Pb-Free NiPdAu

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC electricals only.
2. Tape and Reel.

PIN DESCRIPTION

Pin Number	Pin Name	Pin Function
1, 4	IN, /IN	Differential Input: This input pair is the signal to be buffered. These inputs accept AC or DC-coupled signals as small as 100mV. Each pin of this pair internally terminates to a VT pin through 50Ω. Note that this input will default to an indeterminate state if left open. Please refer to the “Input Interface Applications” section for more details.
2	VT	Input Termination Center-Tap: Each side of the differential input pair terminates to this pin. The VT pin provides a center-tap to a termination network for maximum interface flexibility. See “Input Interface Applications” section for more details.
3	VREF-AC	Reference Output Voltage: This output biases to V _{CC} –1.2V. Connect to VT pin when AC-coupling the input. Bypass with 0.01μF low ESR capacitor to V _{CC} . Maximum current source or sink is 0.5mA. See “Input Interface Applications” section.
8	VCC	Positive Power Supply. Bypass with 0.1μF 0.01μF low ESR capacitors as close to the VCC pin as possible.
7, 6	Q, /Q	Differential 100K LVPECL Output: This LVPECL output is the output of the device. Terminate through 50Ω to V _{CC} –2.0V. See “Output Interface Applications” section.
5	GND, Exposed	Ground. Ground pin and exposed pad must be connected to the same ground plane.

Absolute Maximum Ratings⁽¹⁾

Supply Voltage (V_{CC}) -0.5V to +4.0V
 Input Voltage (V_{IN}) -0.5V to V_{CC}
 LVPECL Output Current (I_{OUT})
 Continuous 50mA
 Surge 100mA
 Termination Current
 Source or Sink Current on V_T ± 100 mA
 Input Current
 Source or Sink Current on IN, /IN ± 50 mA
 Current (V_{REF})⁽³⁾
 Source or Sink Current on V_{REF-AC} ± 1.5 mA
 Lead Temperature (soldering, 20 sec.) +260°C
 Storage Temperature (T_S) -65°C to +150°C

Operating Ratings⁽²⁾

Supply Voltage (V_{CC}) +2.375V to +2.625V or
 +3.0V to +3.6V
 Ambient Temperature (T_A) -40°C to +85°C
 Package Thermal Resistance⁽⁴⁾
 QFN (θ_{JA})
 Still-Air 93°C/W
 QFN (ψ_{JB})
 Junction-to-Board 32°C/W

DC ELECTRICAL CHARACTERISTICS⁽⁵⁾

$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply	$V_{CC} = 2.5\text{V}$.	2.375	2.5	2.625	V
		$V_{CC} = 3.3\text{V}$.	3.0	3.3	3.6	V
I_{CC}	Power Supply Current	No Load, max. V_{CC} , Note 6		48	65	mA
R_{DIFF_IN}	Differential Input Resistance (IN-to-/IN)		80	100	120	Ω
R_{IN}	Input Resistance (IN-to- V_T , /IN-to- V_T)		40	50	60	Ω
V_{IH}	Input HIGH Voltage (IN, /IN)	Note 7	$V_{CC} - 1.6$		V_{CC}	V
V_{IL}	Input LOW Voltage (IN, /IN)		0		$V_{IH} - 0.1$	V
V_{IN}	Input Voltage Swing (IN, /IN)	See Figure 1a.	0.1		1.7	V
V_{DIFF_IN}	Differential Input Voltage Swing IN-, /IN	See Figure 1b.	0.2			V
V_{T_IN}	In-to- V_T (IN, /IN)				1.28	V
V_{REF-AC}	Output Reference Voltage		$V_{CC} - 1.3$	$V_{CC} - 1.2$	$V_{CC} - 1.1$	V

Notes:

1. Permanent device damage may occur if the ratings in "Absolute Maximum Ratings" section are exceeded. This is a stress rating only and functional operation is not implied for conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Due to the limited drive capability use for input of the same package only.
4. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB. ψ_{JB} uses 4-layer θ_{JA} in still-air, unless otherwise stated.
5. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
6. Includes current through internal 50 Ω pull-ups.
7. V_{IH} (min) not lower than 1.2V.

LVPECL OUTPUTS DC ELECTRICAL CHARACTERISTICS⁽⁸⁾

V_{CC} = 2.5V ±5% or 3.3V ±10%; T_A = -40°C to +85°C; R_L = 50Ω to V_{CC}-2V, unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V _{OH}	Output HIGH Voltage Q, /Q		V _{CC} -1.145		V _{CC} -0.895	V
V _{OL}	Output LOW Voltage Q, /Q		V _{CC} -1.545		V _{CC} -1.295	mV
V _{OUT}	Output Voltage Swing Q, /Q	See Figure 1a.	200	400		mV
V _{DIFF_OUT}	Differential Output Voltage Swing Q, /Q	See Figure 1b.	400	800		mV

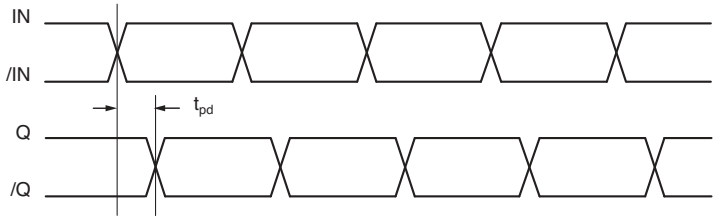
AC ELECTRICAL CHARACTERISTICS⁽⁹⁾

V_{CC} = 2.5V ±5% or 3.3V ±10%; T_A = -40°C to +85°C; R_L = 50Ω to V_{CC}-2V, unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f _{MAX}	Maximum Operating Frequency	V _{OUT} ≥ 400mV NRZ Data	10.7			Gbps
		Clock	7			GHz
t _{pd}	Propagation Delay IN-to-Q	V _{IN} ≥ 100mV	70	125	220	ps
t _{pd} Tempco	Differential Propagation Delay Temperature Coefficient			115		fs/°C
t _{JITTER}	RMS Phase Jitter	Output = 622MHz Integration range: 12kHz - 20MHz		75		fs
t _r , t _f	Output Rise/Fall Times Q, /Q	(20% to 80%) At full output swing.	20	40	70	ps

Notes:

- 8. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
- 9. High-frequency AC electricals are guaranteed by design and characterization.



DEFINITION OF SINGLE-ENDED AND DIFFERENTIAL SWINGS



Figure 1a. Single-Ended Swing

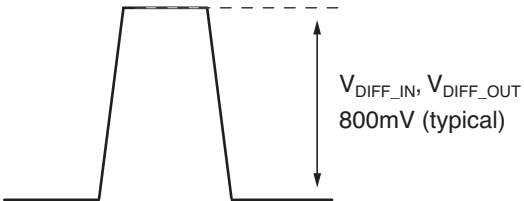
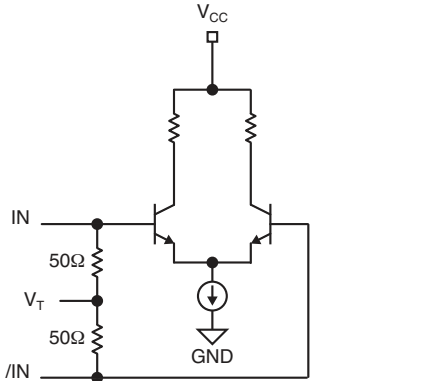


Figure 1b. Differential Swing

INPUT AND OUTPUT STAGE INTERNAL TERMINATION



Simplified Differential Input Stage

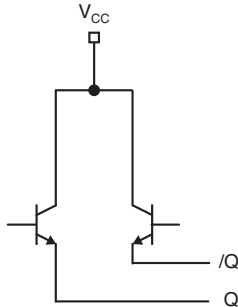
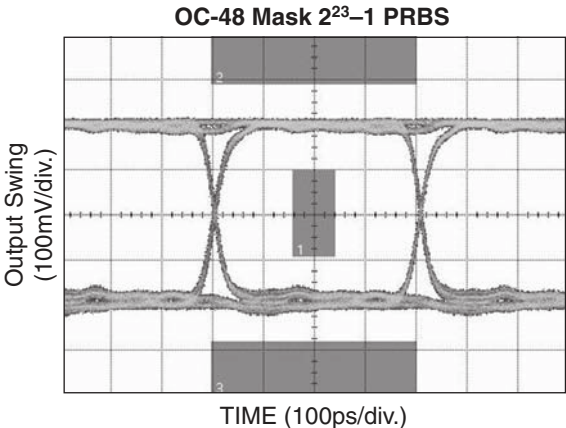
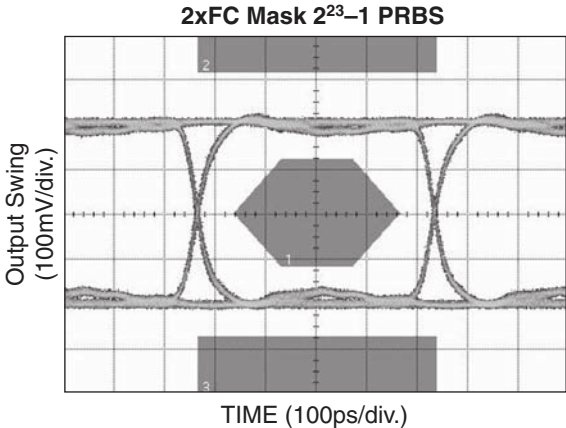
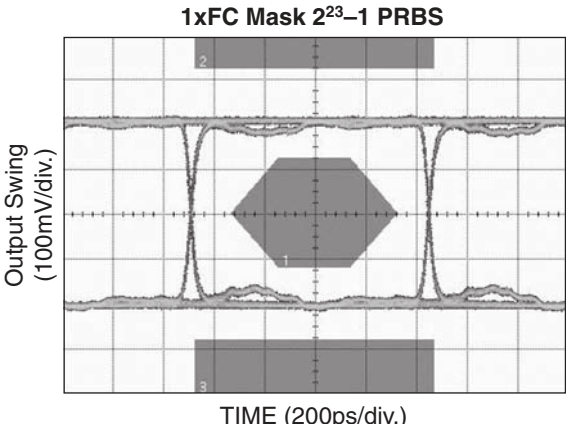
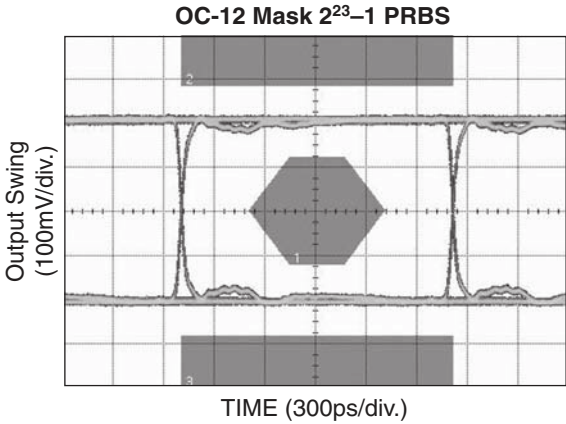
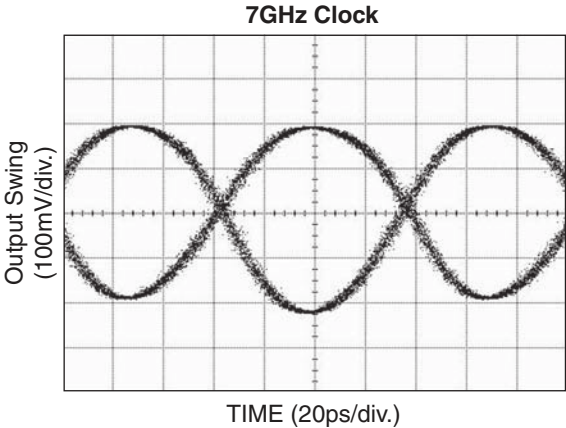
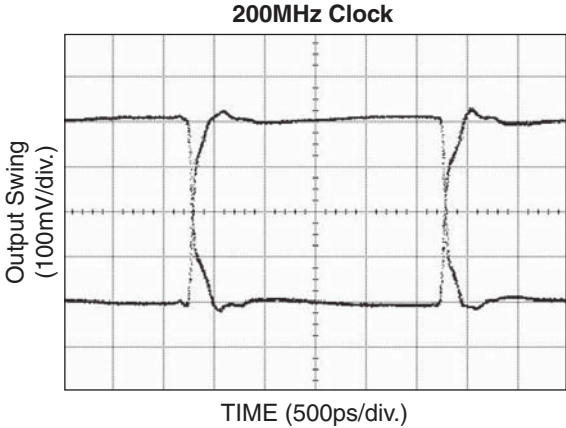


Figure 2b. Simplified Differential Output Stage

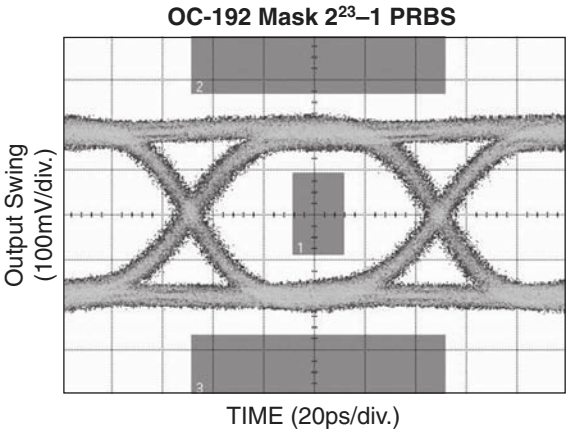
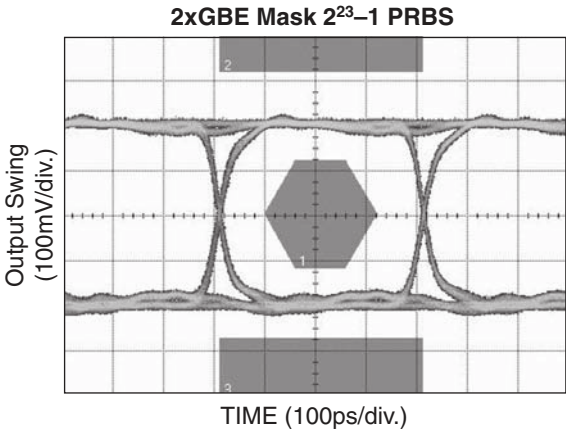
TYPICAL OPERATING CHARACTERISTICS

= 3.3V, GND = 0, $V_{IN} = 800mV$.

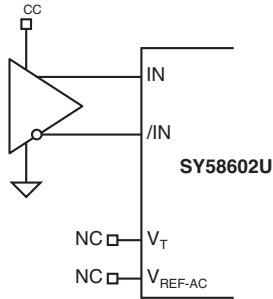


TYPICAL OPERATING CHARACTERISTICS CONT'D

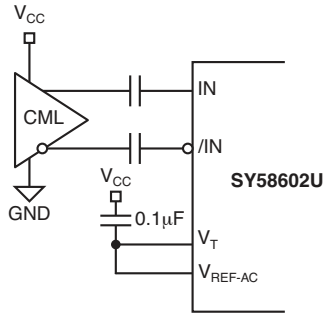
= 3.3V, GND = 0, $V_{IN} = 800mV$.



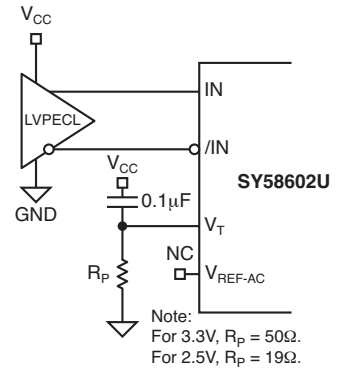
INPUT INTERFACE APPLICATIONS



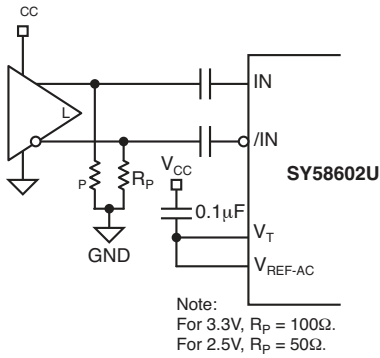
**CML Interface
(DC-Coupled)**
may be connected to V_{CC} .



**Figure 3b. CML Interface
(AC-Coupled)**



**Figure 3c. LVPECL Interface
(DC-Coupled)**



**VPECL Interface
(AC-Coupled)**

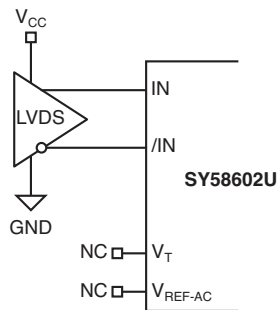


Figure 3e. LVDS Interface

OUTPUT INTERFACE APPLICATIONS

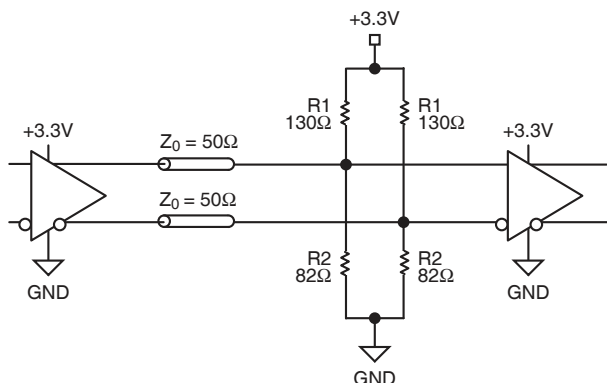


Figure 4a. Parallel Thevenin-Equivalent Termination

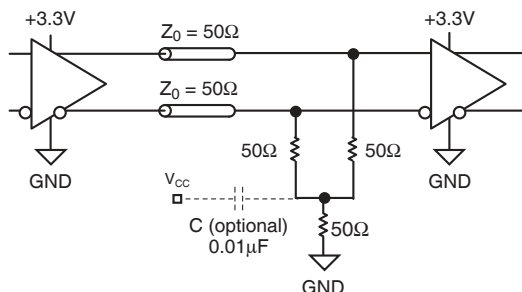
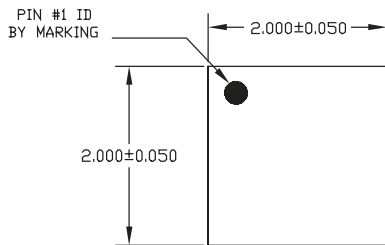


Figure 4b. Parallel Termination (3-Resistor)

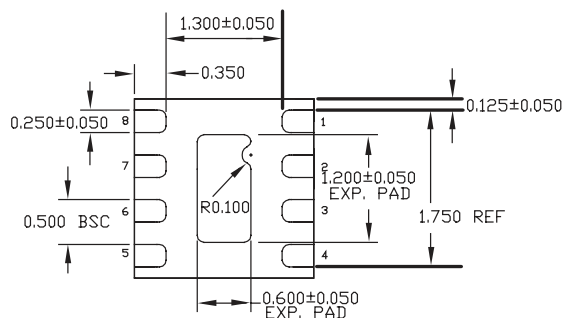
RELATED PRODUCT AND SUPPORT DOCUMENTATION

Part Number	Function	Data Sheet Link
SY58600U	Ultra-Precision Differential 400mV CML Line Driver/Receiver with Internal Termination	www.micrel.com/product-info/products/sy58600u.shtml
SY58601U	Ultra-Precision Differential 800mV LVPECL Line Driver/Receiver with Internal Termination	www.micrel.com/product-info/products/sy58601u.shtml
HBW Solutions	New Products and Applications	www.micrel.com/product-info/products/solutions.shtml

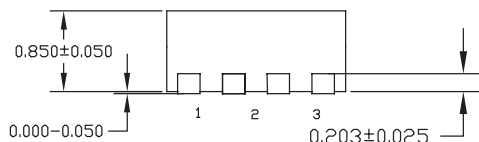
8-PIN ULTRA-SMALL EPAD QFN (QFN-8)



TOP VIEW

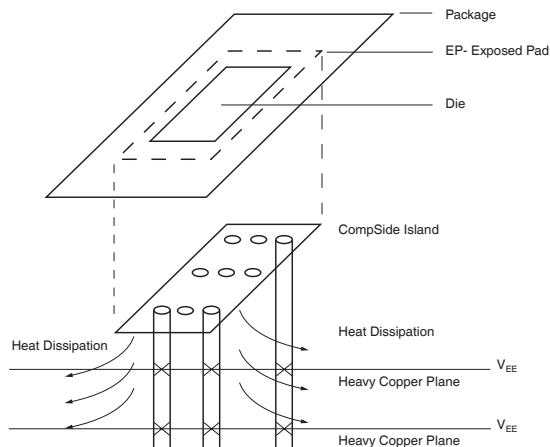


BOTTOM VIEW



SIDE VIEW

- NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
 2. MAX. PACKAGE WARPAGE IS 0.05 mm.
 3. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
 4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.



**PCB Thermal Consideration for 8-Pin QFN Package
(Always solder, or equivalent, the exposed pad to the PCB)**

Package Notes:

1. Package meets Level 2 qualification.
2. All parts dry-packaged before shipment.
3. Exposed pads must be soldered to a ground for proper thermal management.

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