STF20NK50Z, STP20NK50Z

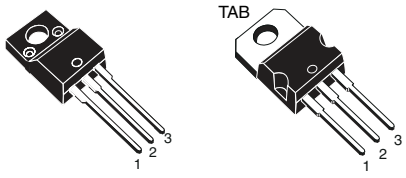
N-channel 500 V, 0.23 Ω, 17 A SuperMESH™ Power MOSFET Zener-protected in TO-220FP and TO-220 packages

Datasheet — production data

Features

Order codes	V_{DSS}	$R_{DS(on)}$ max	I_D	P_{TOT}
STF20NK50Z	500 V	< 0.27 Ω	17 A	40 W
STP20NK50Z	500 V	< 0.27 Ω	17 A	190 W

- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitance



TO-220FP **TO-220**

Applications

- Switching applications

Description

These devices are N-channel Zener-protected Power MOSFETs developed using STMicroelectronics' SuperMESH™ technology, achieved through optimization of ST's well established strip-based PowerMESH™ layout. In addition to a significant reduction in on-resistance, this device is designed to ensure a high level of dv/dt capability for the most demanding applications.

Figure 1. Internal schematic diagram

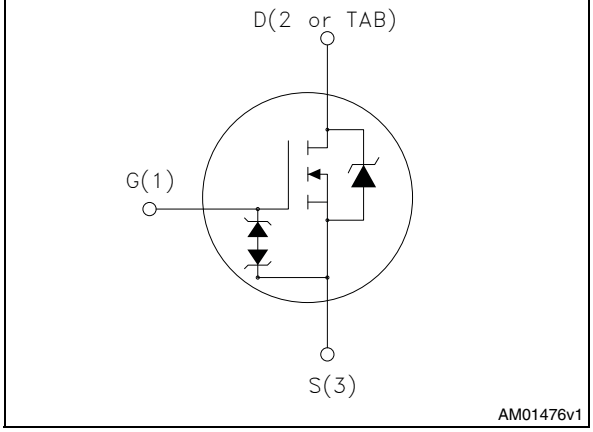


Table 1. Device summary

Order codes	Marking	Package	Packaging
STF20NK50Z	F20NK50Z	TO-220FP	Tube
STP20NK50Z	P20NK50Z	TO-220	

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220	TO-220FP	
V_{DS}	Drain-source voltage	500		V
V_{GS}	Gate-source voltage	± 30		V
I_D	Drain current (continuous) at T_C = 25 °C	17	17(1)	A
I_D	Drain current (continuous) at T_C = 100 °C	10.71	10.71 (1)	A
I_{DM} (2)	Drain current (pulsed)	68	68	A
P_{TOT}	Total dissipation at T_C = 25 °C	190	40	W
	Derating factor	1.52	0.32	W/°C
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T_C = 25 °C)		2500	V
ESD	Gate-source human body model (R=1.5 kΩ, C=100 pF)	6		kV
dv/dt (3)	Peak diode recovery voltage slope	4.5		V/ns
T_{stg}	Storage temperature	-55 to 150		°C
T_j	Max operating junction temperature	150		°C

1. Limited by maximum junction temperature.
2. Pulse width limited by safe operating area.
3. I_{SD} ≤ 17 A, di/dt ≤ 200 A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_j ≤ T_{JMAX}.

Table 3. Thermal data

Symbol	Parameter	Value		Unit
		TO-220	TO-220FP	
$R_{thj\text{-}case}$	Thermal resistance junction-case max	0.66	3.1	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max	62.5	62.5	°C/W

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by Tj max)	17	A
E_{AS}	Single pulse avalanche energy (starting T_J=25 °C, I_D=I_{AR}, V_{DD}=50 V)	850	mJ

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D =1 mA, V_{GS} = 0	500			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 500 V V_{DS} = 500 V, T_C = 125 °C			1 50	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			± 10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 8.5 A		0.23	0.27	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0	-	2600 328 72		pF pF pF
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{DS} =0, V_{DS} = 0 to 640 V	-	187		pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD} = 250 V, I_D = 8.5 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 16*)	-	28 20 70 15		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 400 V, I_D = 17 A, V_{GS} = 10 V (see *Figure 17*)	-	85 15.5 42	119	nC nC nC

1. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}(1)	Source-drain current Source-drain current (pulsed)		-		17 68	A A
V_{SD}(2)	Forward on voltage	I_{SD} = 17 A, V_{GS} = 0	-		1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 17 A, di/dt = 100 A/µs V_R = 100 V (see *Figure 18*)	-	355 3.90 22		ns µC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 17 A, di/dt = 100 A/µs V_R = 100 V, Tj = 150 °C (see *Figure 18*)	-	440 5.72 26		ns µC A

1. Pulsed: pulse duration=300µs, duty cycle 1.5%
2. Pulse width limited by safe operating area

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate-source breakdown voltage	Igs=± 1mA (open drain)	30	-		V

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220

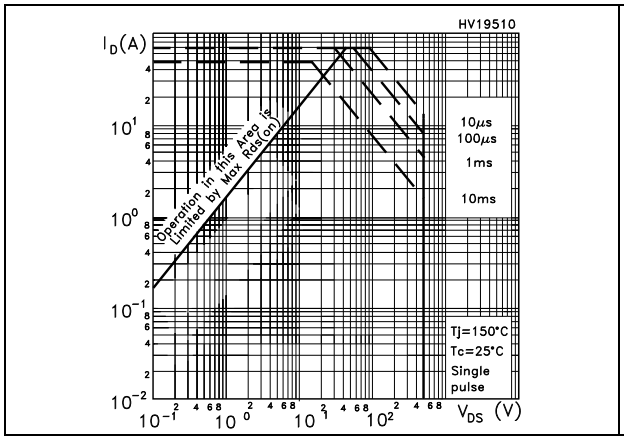


Figure 3. Thermal impedance for TO-220

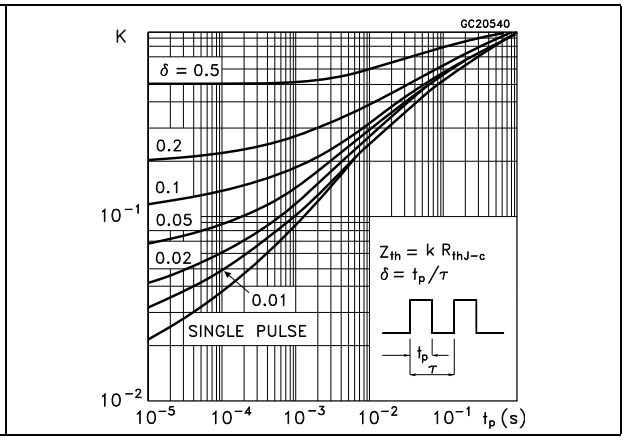


Figure 4. Safe operating area for TO-220FP

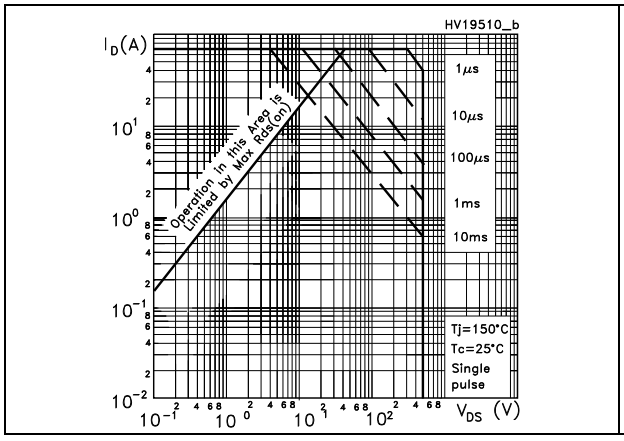


Figure 5. Thermal impedance for TO-220FP

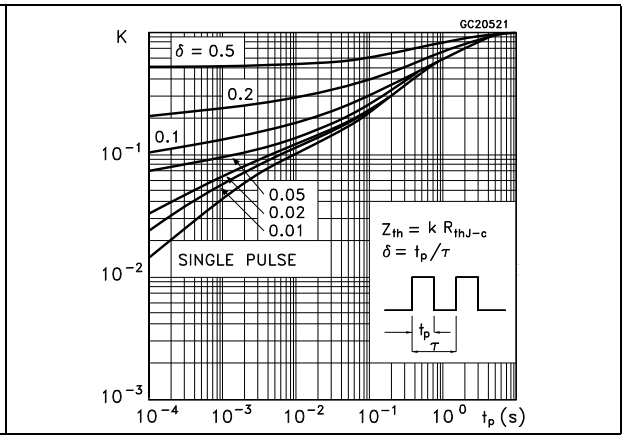


Figure 6. Output characteristics

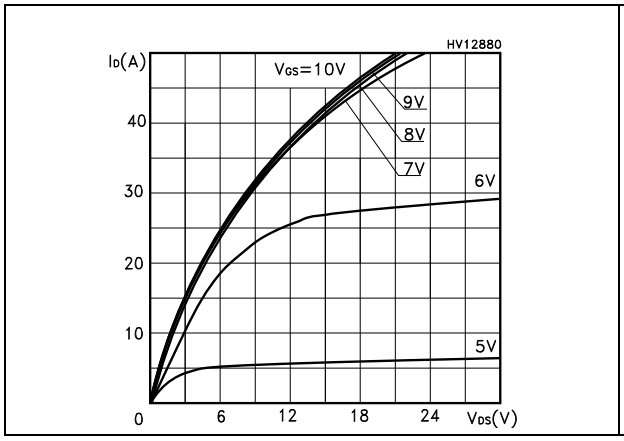


Figure 7. Transfer characteristics

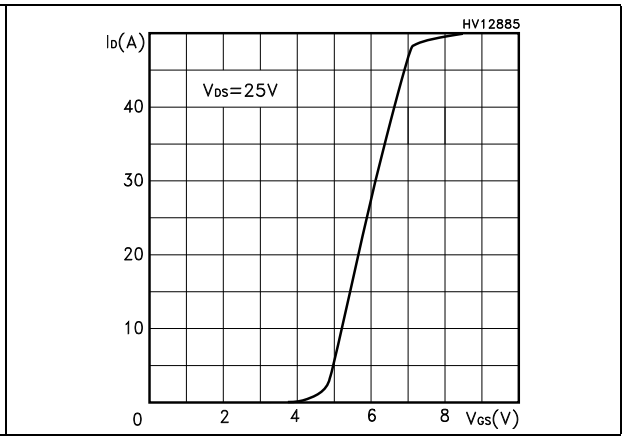


Figure 8. Normalized B_{VDSS} vs temperature

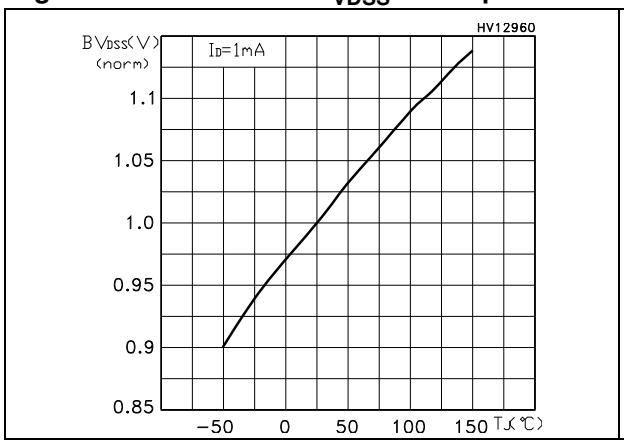


Figure 9. Static drain-source on-resistance

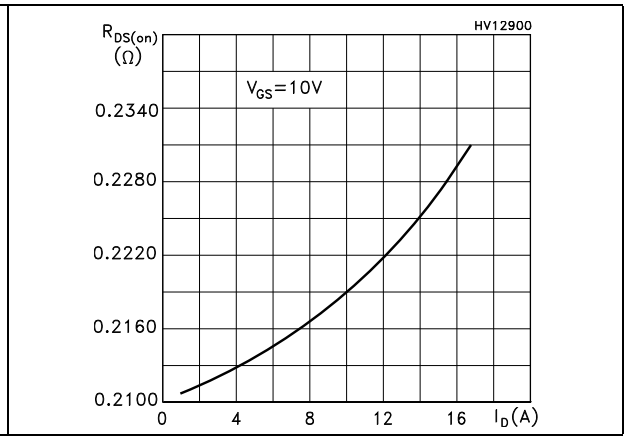


Figure 10. Gate charge vs gate-source voltage

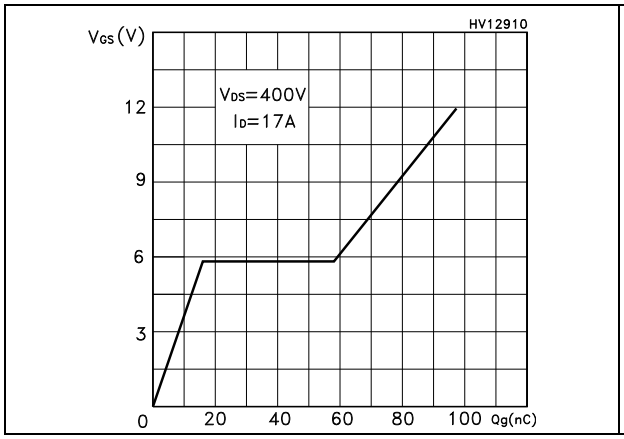


Figure 11. Capacitance variations

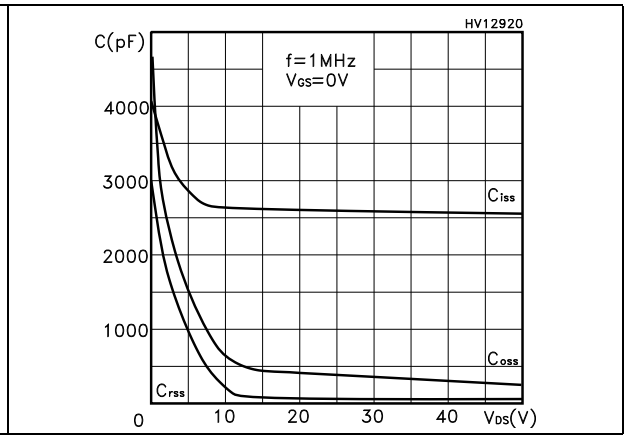


Figure 12. Normalized gate threshold voltage vs temperature

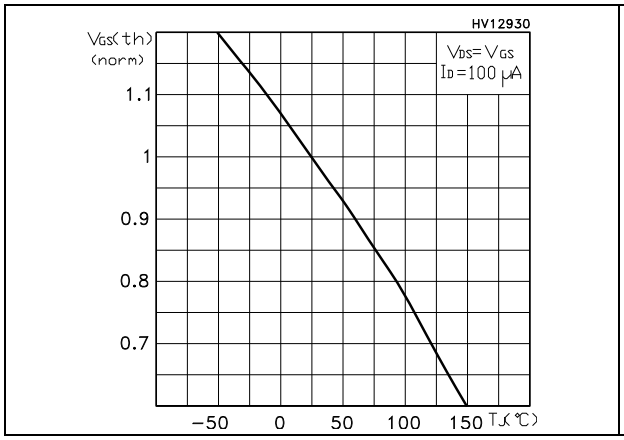


Figure 13. Normalized on-resistance vs temperature

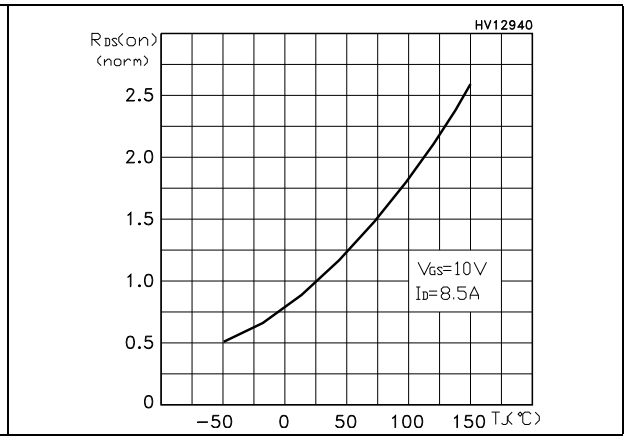


Figure 14. Maximum avalanche energy vs temperature

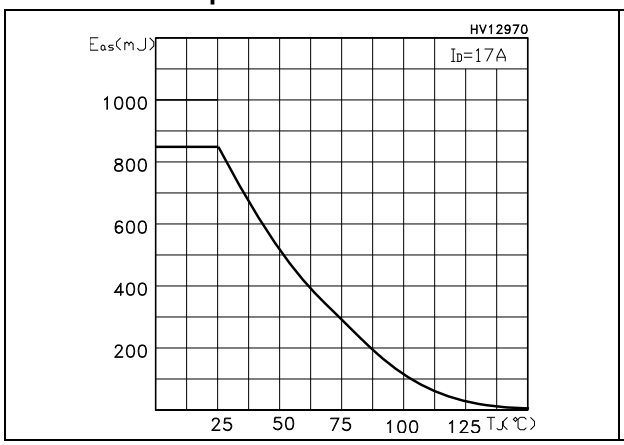
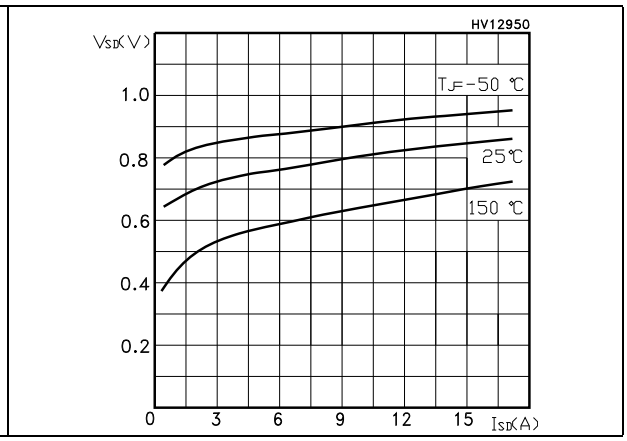


Figure 15. Source-drain diode forward characteristic



3 Test circuits

Figure 16. Switching times test circuit for resistive load

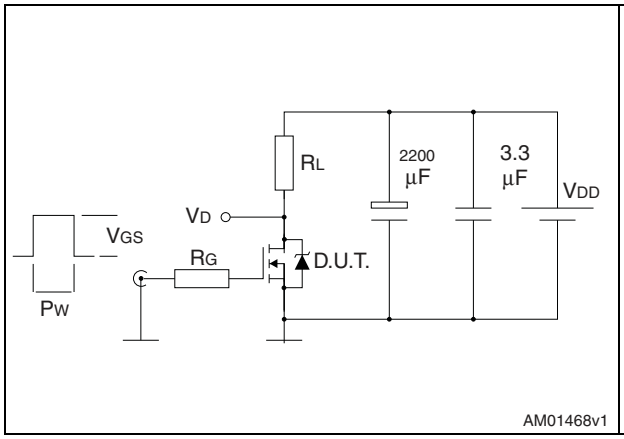


Figure 17. Gate charge test circuit

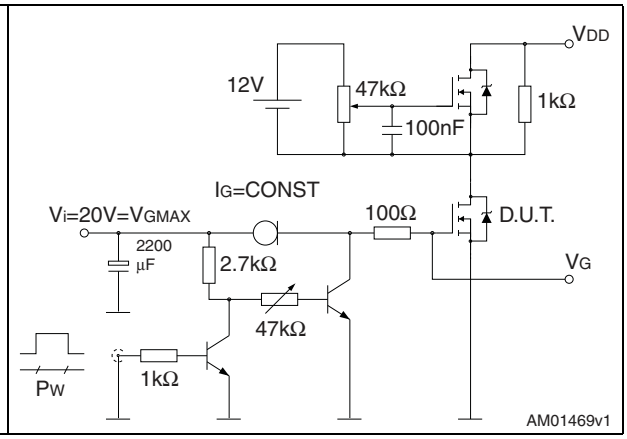


Figure 18. Test circuit for inductive load switching and diode recovery times

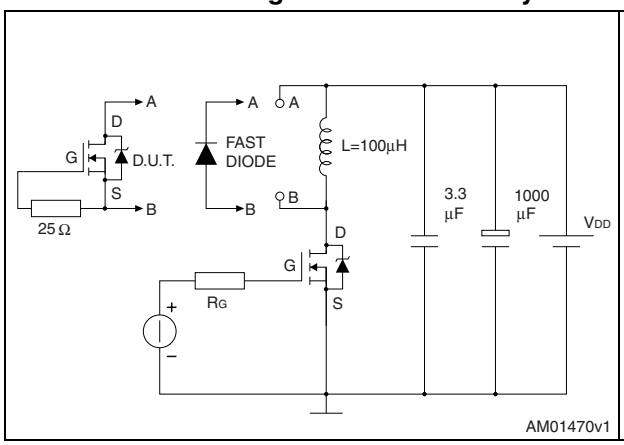


Figure 19. Unclamped inductive load test circuit

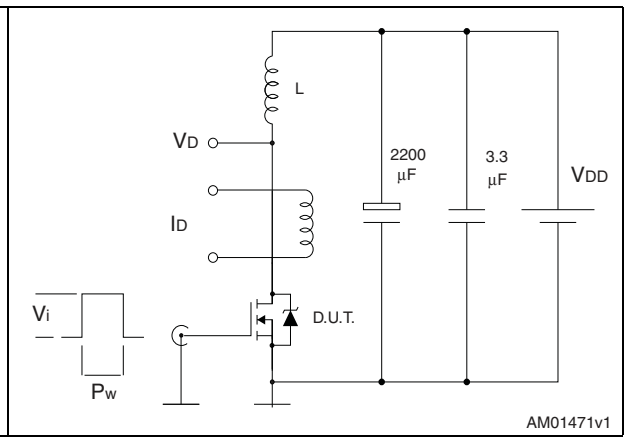


Figure 20. Unclamped inductive waveform

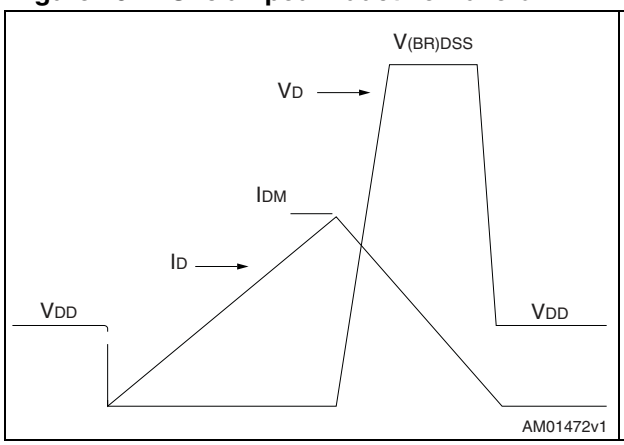
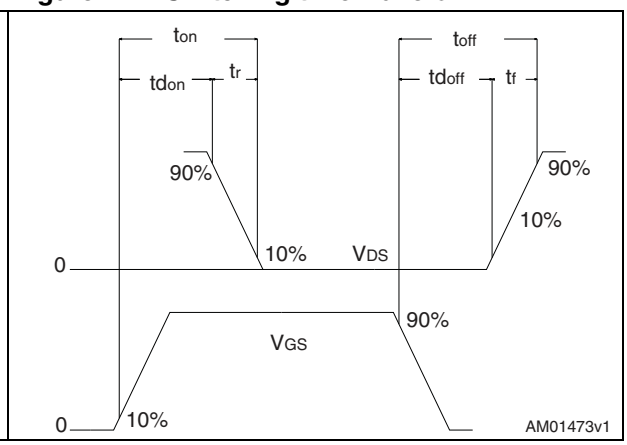


Figure 21. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 9. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Figure 22. TO-220FP drawing

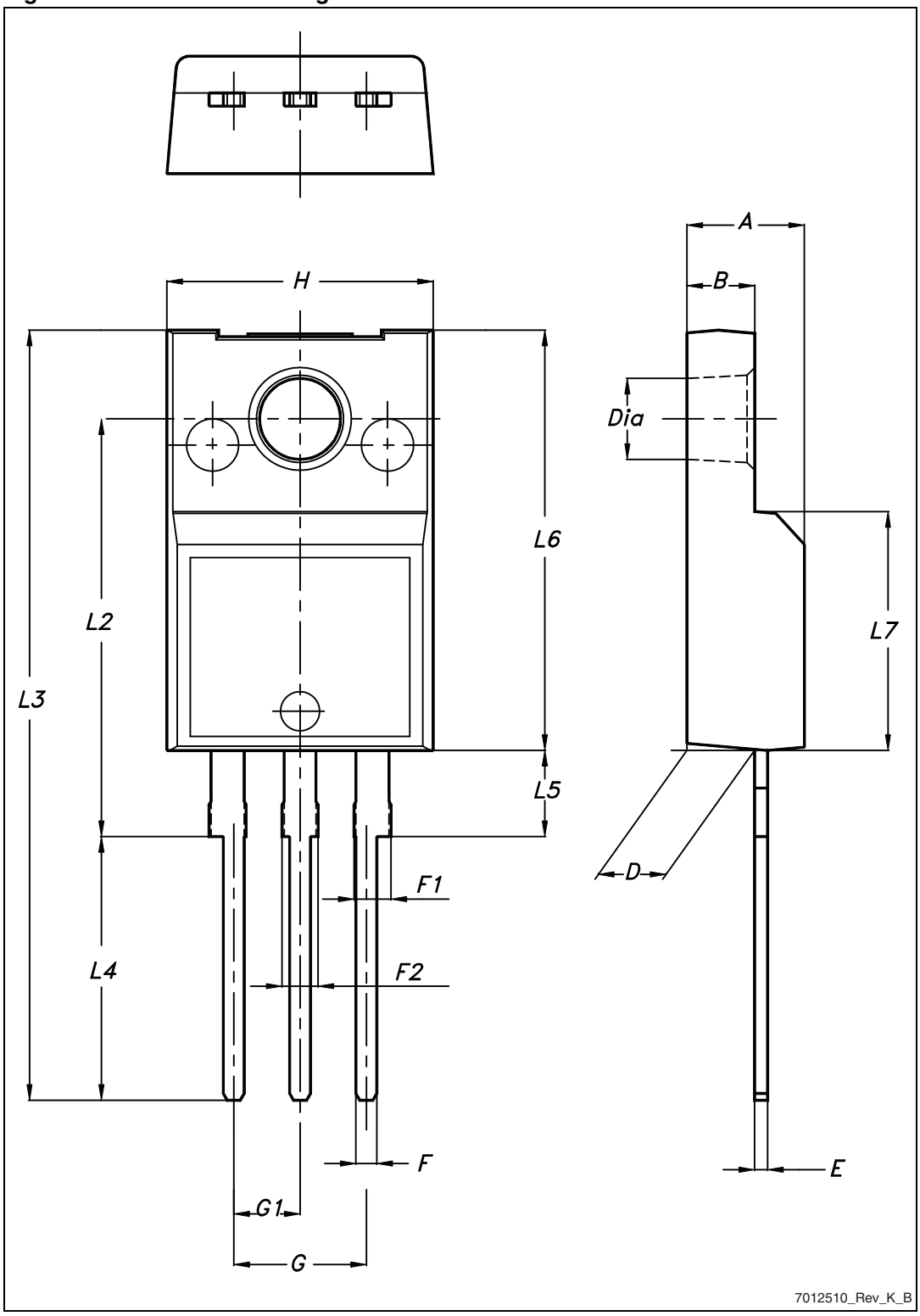
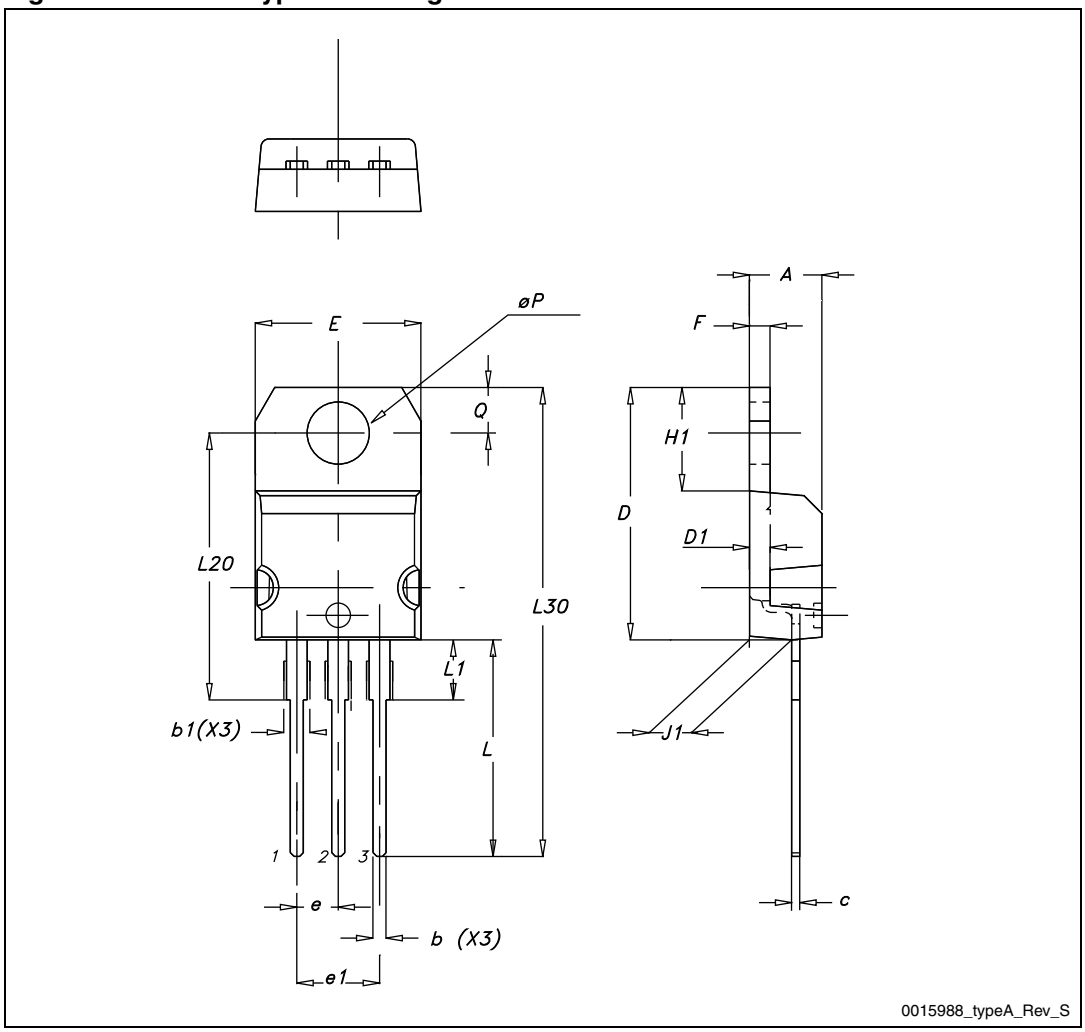


Table 10. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
∅P	3.75		3.85
Q	2.65		2.95

Figure 23. TO-220 type A drawing



5 Revision history

Table 11. Document revision history

Date	Revision	Changes
05-Apr-2012	1	First release.