HARRIS SEMICONDUCTOR

HM-6504

March 1997

4096 x 1 CMOS RAM

Features

- **Low Power Standby . . . . . 125µW Max**
- **Low Power Operation . . . . . 35mW/MHz Max**
- **Data Retention . . . . . at 2.0V Min**
- **TTL Compatible Input/Output**
- **Three-State Output**
- **Standard JEDEC Pinout**
- **Fast Access Time. . . . . 120/200ns Max**
- **18 Lead Package for High Density**
- **On-Chip Address Register**
- **Gated Inputs - No Pull Up or Pull Down Resistors Required**

Description

The HM-6504 is a 4096 x 1 static CMOS RAM fabricated using self-aligned silicon gate technology. The device utilizes synchronous circuitry to achieve high performance and low power operation.

On-chip latches are provided for addresses, data input and data output allowing efficient interfacing with microprocessor systems. The data output can be forced to a high impedance state for use in expanded memory arrays.

Gated inputs allow lower operating current and also eliminate the need for pull up or pull down resistors. The HM-6504 is a fully static RAM and may be maintained in any state for an indefinite period of time.

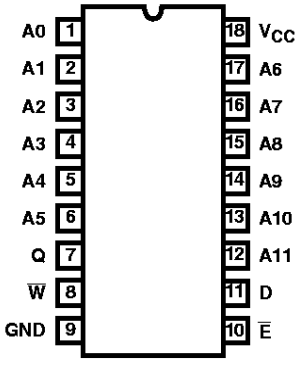
Data retention supply voltage and supply current are guaranteed over temperature.

Ordering Information

120ns	200ns	300ns	TEMP. RANGE	PACKAGE	PKG. NO.
-	HM3-6504B-9	HM3-6504-9	-40°C to +85°C	PDIP	E18.3
HM1-6504S-9	HM1-6504B-9	HM1-6504-9	-40°C to +85°C	CERDIP	F18.3
24501BVA	-	-	-	JAN #	F18.3
810240IVA	8102403VA	8102405VA	-	SMD #	F18.3
-	-	HM4-6504-9	-40°C to+85°C	CLCC	J18.B

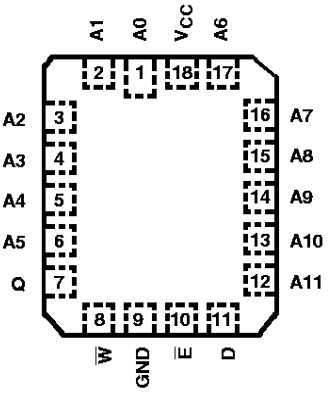
Pinouts

HM-6504 (PDIP, CERDIP)
TOP VIEW



PIN	DESCRIPTION
A	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
D	Data Input
Q	Data Output

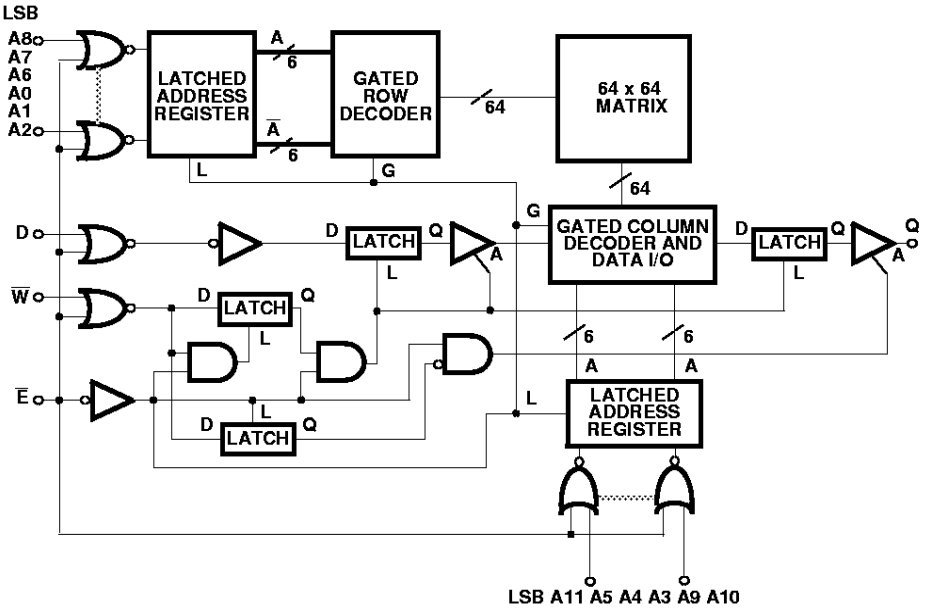
HM-6504 (CLCC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **2994.1**

Functional Diagram



NOTES:

1. All lines active high-positive logic.
2. Three-state Buffers: A high → output active.
3. Control and Data Latches: L low → Q = D and Q latches on rising edge of L.
4. Address Latches: Latch on falling edge of E.
5. Gated Decoders: Gate on rising edge of G.

Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input, Output or I/O Voltage . . . . . GND -0.3V to V_{CC} +0.3V
ESD Classification . . . . . Class 1

Thermal Information

Thermal Resistance (Typical)	θ_{JA}	θ_{JC}
CERDIP Package	75°C/W	15°C/W
PDIP Package	75°C/W	N/A
CLCC Package	90°C/W	33°C/W

Maximum Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature
Ceramic Package . . . . . +175°C
Plastic Package . . . . . +150°C
Maximum Lead Temperature (Soldering 10s) . . . . . +300°C

Die Characteristics

Gate Count . . . . . 6910 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V

Operating Temperature Range
HM-6504S-9, HM-6504B-9, HM-6504-9 . . . . . -40°C to +85°C
HM-6504B-8, HM-6504-8 . . . . . -55°C to +125°C

DC Electrical Specifications

V_{CC} = 5V ±10%; T_A = -40°C to +85°C (HM-6504B-9, HM-6504-9)
T_A = -55°C to +125°C (HM-6504B-8, HM-6504-8)

SYMBOL	PARAMETER		MIN	MAX	UNITS	TEST CONDITIONS
ICCSB	Standby Supply Current	HM-6504-9	-	25	µA	IO = 0mA, $\overline{E}$ = V_{CC} -0.3V, V_{CC} = 5.5V
		HM-6504-8	-	50	µA	
ICCOP	Operating Supply Current (Note 1)		-	7	mA	$\overline{E}$ = 1MHz, IO = 0mA, VI = GND, V_{CC} = 5.5V
ICCDR	Data Retention Supply Current	HM-6504-9	-	15	µA	IO = 0mA, V_{CC} = 2.0V, $\overline{E}$ = V_{CC}
		HM-6504-8	-	25	µA	
VCCDR	Data Retention Supply Voltage		2.0	-	V	
II	Input Leakage Current		-1.0	+1.0	µA	VI = V_{CC} or GND, V_{CC} = 5.5V
IOZ	Output Leakage Current		-1.0	+1.0	µA	VO = V_{CC} or GND, V_{CC} = 5.5V
VIL	Input Low Voltage		-0.3	0.8	V	V_{CC} = 4.5V
VIH	Input High Voltage		V_{CC} -2.0	V_{CC} +0.3	V	V_{CC} = 5.5V
VOL	Output Low Voltage		-	0.4	V	IO = 2.0mA, V_{CC} = 4.5V
VOH1	Output High Voltage		2.4	-	V	IO = -1.0mA, V_{CC} = 4.5V
VOH2	Output High Voltage (Note 2)		V_{CC} -0.4	-	V	IO = -100µA, V_{CC} = 4.5V

Capacitance

T_A = +25°C

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance (Note 2)	8	pF	f = 1MHz, All measurements are referenced to device GND
CO	Output Capacitance (Note 2)	10	pF	

NOTES:

1. Typical derating 5mA/MHz increase in ICCOP.
2. Tested at initial design and after major design changes.

AC Electrical Specifications V_{CC} = 5V ±10%; T_A = -40°C to +85°C (HM-6504S-9, HM-6504B-9, HM-6504-9)
T_A = -55°C to +125°C (HM-6504B-8, HM-6504-8)

SYMBOL	PARAMETER	HM-6504S		HM-6504B		HM-6504		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
(1) TELQV	Chip Enable Access Time	-	120	-	200	-	300	ns	(Notes 1, 3)
(2) TAVQV	Address Access Time	-	120	-	220	-	320	ns	(Notes 1, 3, 4)
(3) TELQX	Chip Enable Output Enable Time	5	-	5	-	5	-	ns	(Notes 2, 3)
(4) TEHQZ	Chip Enable Output Disable Time	-	50	-	80	-	100	ns	(Notes 2, 3)
(5) TELEH	Chip Enable Pulse Negative Width	120	-	200	-	300	-	ns	(Notes 1, 3)
(6) TEHEL	Chip Enable Pulse Positive Width	50	-	90	-	120	-	ns	(Notes 1, 3)
(7) TAVEL	Address Setup Time	0	-	20	-	20	-	ns	(Notes 1, 3)
(8) TELAX	Address Hold Time	40	-	50	-	50	-	ns	(Notes 1, 3)
(9) TWLWH	Write Enable Pulse Width	20	-	60	-	80	-	ns	(Notes 1, 3)
(10) TWLEH	Write Enable Pulse Setup Time	70	-	150	-	200	-	ns	(Notes 1, 3)
(11) TWLEL	Early Write Pulse Setup Time	0	-	0	-	0	-	ns	(Notes 1, 3)
(12) TWHEL	Write Enable Read Mode Setup Time	0	-	0	-	0	-	ns	(Notes 1, 3)
(13) TELWH	Early Write Pulse Hold Time	40	-	60	-	80	-	ns	(Notes 1, 3)
(14) TDVWL	Data Setup Time	0	-	0	-	0	-	ns	(Notes 1, 3)
(15) TDVEL	Early Write Data Setup Time	0	-	0	-	0	-	ns	(Notes 1, 3)
(16) TWLDX	Data Hold Time	25	-	60	-	80	-	ns	(Notes 1, 3)
(17) TELDX	Early Write Data Hold Time	25	-	60	-	80	-	ns	(Notes 1, 3)
(18) TELEL	Read or Write Cycle Time	170	-	290	-	420	-	ns	(Notes 1, 3)

NOTES:

1. Input pulse levels: 0.8V to V_{CC} - 2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent, C_L = 50pF (min) - for C_L greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. V_{CC} = 4.5V and 5.5V.
4. TAVQV = TELQV + TAVEL.

Timing Waveforms

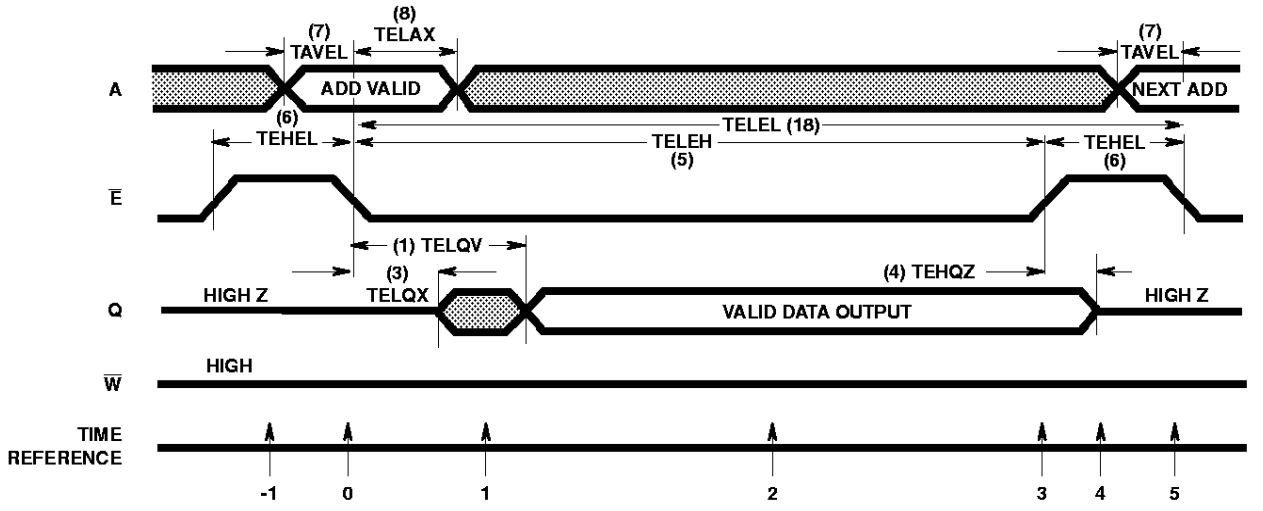


FIGURE 1. READ CYCLE

TRUTH TABLE

TIME REFERENCE	INPUTS			OUTPUT	FUNCTION
	$\overline{E}$	$\overline{W}$	A	Q	
-1	H	X	X	Z	Memory Disabled
0	↘	H	V	Z	Cycle Begins, Addresses are Latched
1	L	H	X	X	Output Enabled
2	L	H	X	V	Output Valid
3	↗	H	X	V	Read Accomplished
4	H	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↘	H	V	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The address information is latched in the on-chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address set-up and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1) the output becomes enabled but the data is not valid until during time (T = 2). $\overline{W}$ must remain high for the read cycle. After the output data has been read, $\overline{E}$ may return high (T = 3). This will disable the output buffer and all input and ready the RAM for the next memory cycle (T = 4).

Timing Waveforms (Continued)

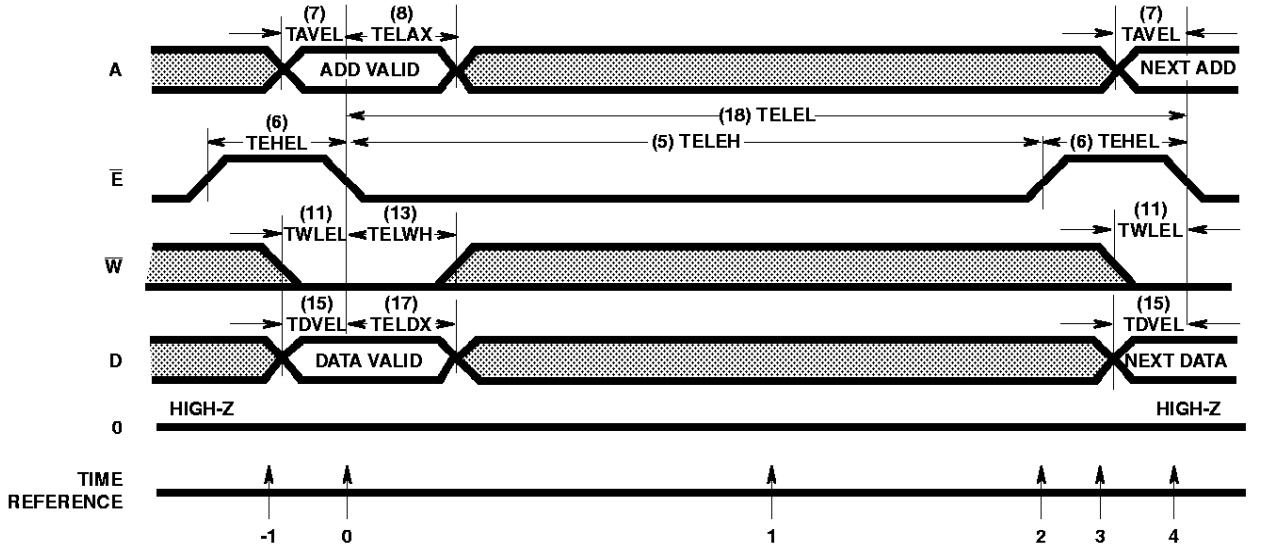


FIGURE 2. EARLY WRITE CYCLE

TRUTH TABLE

TIME REFERENCE	INPUTS				OUTPUT	FUNCTION
	$\overline{E}$	$\overline{W}$	A	D	Q	
-1	H	X	X	X	Z	Memory Disabled
0	↘	L	V	V	Z	Cycle Begins, Addresses are Latched
1	L	X	X	X	Z	Write in Progress Internally
2	↗	X	X	X	Z	Write Completed
3	H	X	X	X	Z	Prepare for Next Cycle (Same as - 1)
4	↘	L	V	V	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The early write cycle is the only cycle where the output is guaranteed not to become active. On the falling edge of $\overline{E}$ (T = 0), the addresses, the write signal, and the data input are latched in on-chip registers. The logic value of $\overline{W}$ at the time $\overline{E}$ falls, determines the state of the output buffer for that cycle. Since $\overline{W}$ is low when $\overline{E}$ falls, the output buffer is latched into the high impedance state and will remain in that state until $\overline{E}$ returns high (T = 2). For this cycle, the data input is latched by $\overline{E}$ going low; therefore, data set-up and hold times should be referenced to $\overline{E}$. When $\overline{E}$ (T = 2) returns to the high state, the output buffer and all inputs are disabled and all signals are unlatched. The device is now ready for the next cycle.

Timing Waveforms (Continued)

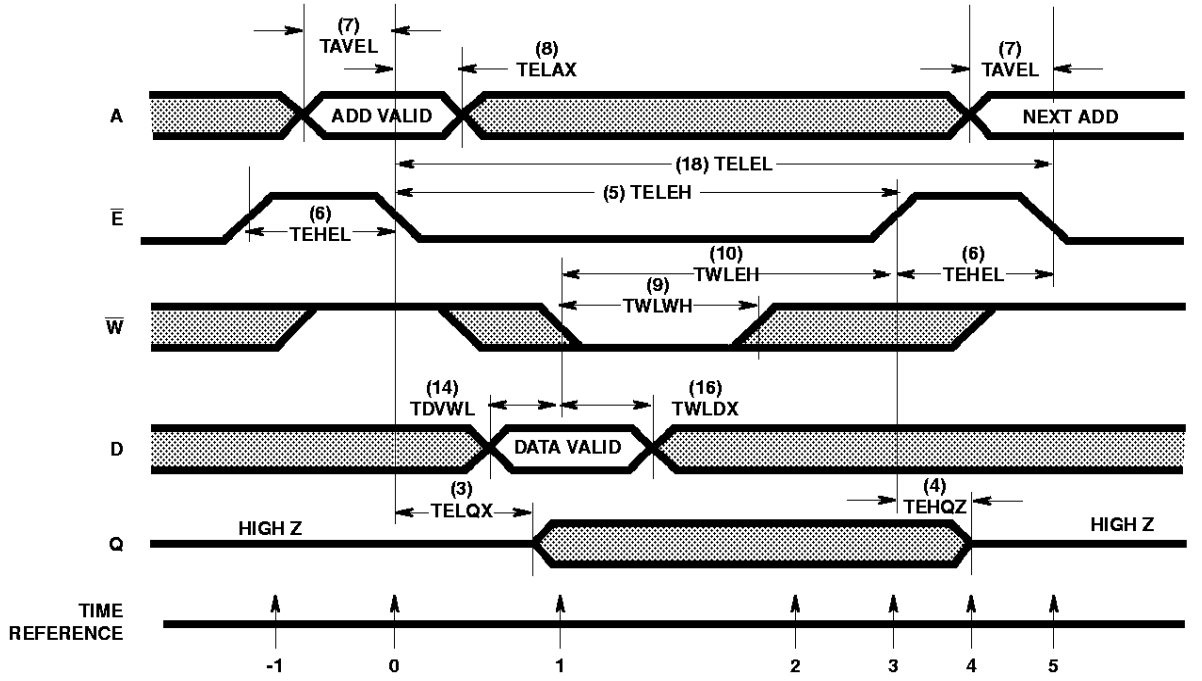


FIGURE 3. LATE WRITE CYCLE

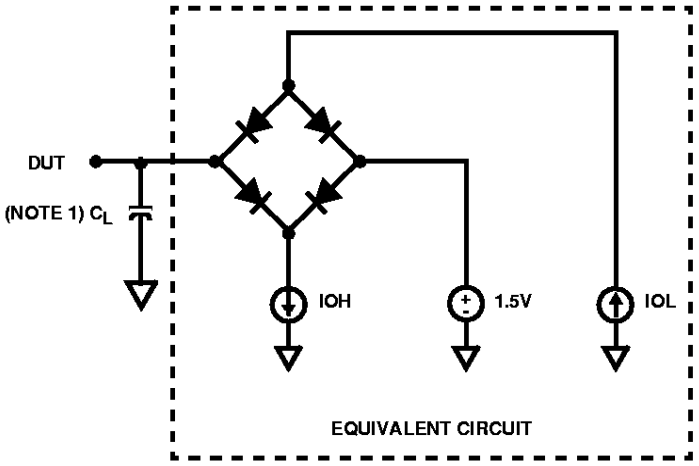
TRUTH TABLE

TIME REFERENCE	INPUTS				OUTPUTS	FUNCTION
	$\overline{E}$	$\overline{W}$	A	D	Q	
-1	H	X	X	X	Z	Memory Disabled
0	↘	H	V	X	Z	Cycle Begins, Addresses are Latched
1	L	↘	X	V	X	Write Begins, Data is Latched
2	L	H	X	X	X	Write In Progress Internally
3	↗	H	X	X	X	Write Completed
4	H	X	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↘	H	V	X	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The late write cycle is a cross between the early write cycle and the read-modify-write cycle.

Recall that in the early write, the output is guaranteed to remain high impedance, and in the read-modify-write the output is guaranteed valid at access time. The late write is between these two cases. With this cycle the output may become active, and may become valid data, or may remain active but undefined. Valid data is written into the RAM if data setup, data hold, write setup and write pulse widths are observed.

Test Load Circuit



NOTE:

1. Test head capacitance includes stray and jig capacitance.