Document Number: MC34SB0410
Rev. 3.0, 8/2016

Fully integrated quad valve controller system on chip

SB0410

INDUSTRIAL CONTROLLER CHIP

AE SUFFIX (PB-FREE)
98ASA00173D
48-PIN LQFP-EP

The SB0410 device is a SMARTMOS valve and motor controller system designed for use in harsh industrial environments.

It has four high-current low-side drivers for use with solenoid valves, and high-side gate pre-driver to control a DC motor through an inexpensive external N-channel MOSFETs. Alongside this, the SB0410 has three analog to digital converters, plus two low-side driver allowing to drive resistive charges. The digital I/O pins can be configured for both 5.0 V and 3.3 V levels for easy connection to any microprocessor. The SB0410 uses standard SPI protocol communication.

The SB0410 is a perfect solution for hydraulic and pneumatic applications.

Features

- Operating voltage 6.0 V to 36 V
- Four valves control
  - Four current regulated valves up to 2.25 A (5.0 kHz)
- Pump motor pre-driver up to 16 kHz PWM
- 16-bit SPI interface
- Three 10-bit ADC channels
- Two low-side driver for resistive charge ($R_{DS(on)}$ 14.0 Ω)
- Die temperature warning
- Supervision

Applications

Industrial Controller

- Spot Welding
- Temperature Control
- Brake Pressure
- Laser Cutting
- Bottle Moulding
- Filling Pressure
- 3D Printer
- Oxygen Concentrator
- Medical test equipment
- Dialysis machines
- Blood pressure
- Soda dispensers
- Heavy equipment and construction machinery
- Fork lifts
- Water control system for irrigation (connected to farm tractor)
- Food control in animal farm

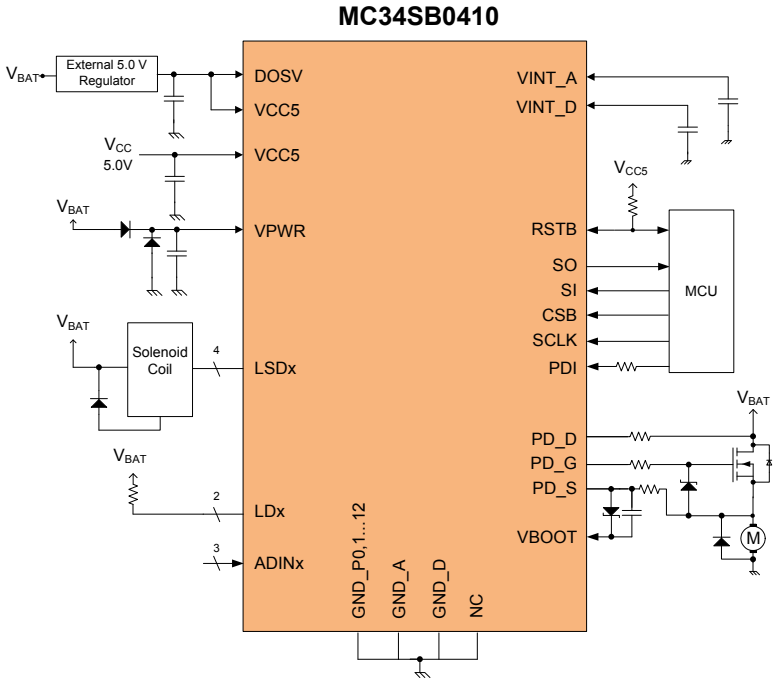


Figure 1. SB0410 simplified 5.0 V application diagram

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

Table of Contents

1 Orderable parts

This section describes the part numbers available to be purchased along with their differences. Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to http://www.nxp.com and perform a part number search for the following device numbers.

Table 1. Orderable part variations

Part number	Temperature (T_A)	Package	Notes
MC34SB0410AE	-40 °C to 125 °C	7.0 mm x 7.0 mm, 48 LQFP-EP	(1)

Notes
1. To order parts in Tape & Reel, add the R2 suffix to the part number.

2 Internal block diagram

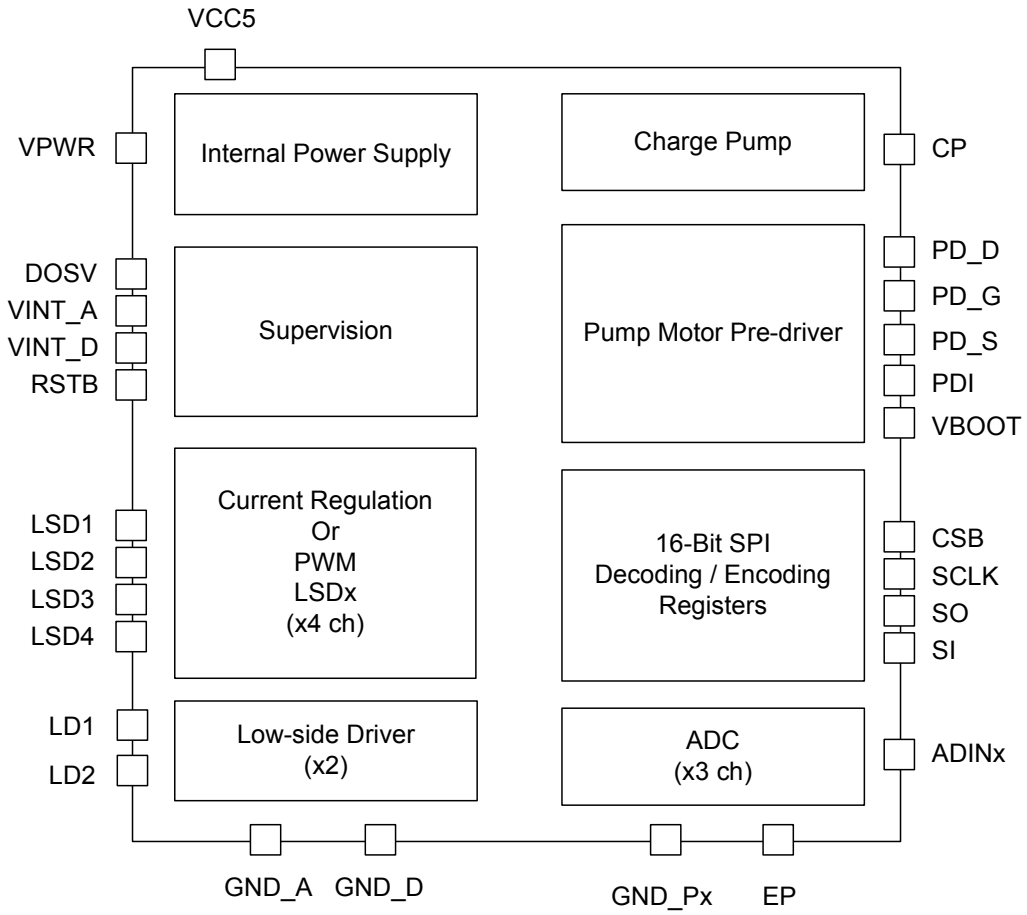


Figure 2. SB0410 simplified internal block diagram

3 Pin connections

3.1 Pinout diagram

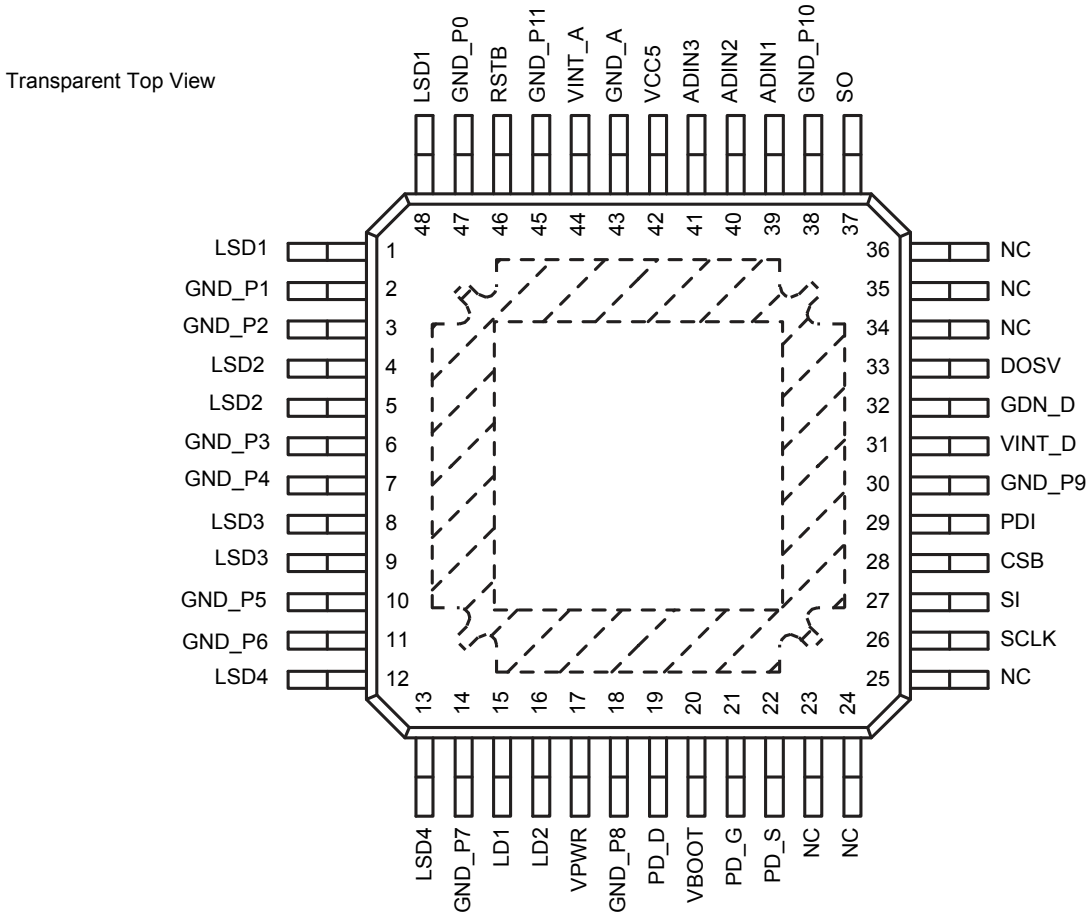


Figure 3. SB0410 48-pin LQFP-EP pinout diagram

3.2 Pin definitions

Table 2. SB0410 pin definitions

Pin number	Pin name	Pin function	Definition	DOSV = 5.0 V	DOSV = 3.3 V	Notes
1, 48	LSD1	Low-side driver for current regulated or PWMed valves	Open drain output for low-side driver 1	no	no	(2)
2	GND_P1	Supply	Power ground 1	no	no	(4)
3	GND_P2	Supply	power ground 2	no	no	(4)
4, 5	LSD2	Low-side driver for current regulated or PWMed valves	Open drain output for low-side driver 2	no	no	(2)
6	GND_P3	Supply	Power ground 3	no	no	(4)
7	GND_P4	Supply	Power ground 4	no	no	(4)
8, 9	LSD3	Low-side driver for current regulated or PWMed valves	Open drain output for low-side driver 3	no	no	(2)
10	GND_P5	Supply	Power ground 5	no	no	(4)
11	GND_P6	Supply	Power ground 6	no	no	(4)
12,13	LSD4	Low-side driver for current regulated or PWMed valves	Open drain output for low-side driver 4	no	no	(2)
14	GND_P7	Supply	Power ground 7	no	no	(4)
15	LD1	Low-side driver 1 for general purpose	Open drain output for low-side driver 1	no	no	
16	LD2	Low-side driver 2 for general purpose	Open drain output for low-side driver 2	no	no	
17	VPWR	Supply	Supply pin connect to battery through reverse diode	no	no	
18	GND_P8	Supply	Power ground 8	no	no	(4)
19	PD_D	Motor pump driver	Drain feedback pump motor FET. Connect to drain of external pump motor FET	no	no	
20	VBOOT	Motor pump driver	Bootstrap	no	no	
21	PD_G	Motor pump driver	Gate output to control pump motor FET. Connect to gate of external pump motor FET	no	no	
22	PD_S	Motor pump driver	Source feedback pump motor FET Connect to source of external pump motor FET	no	no	
26	SCLK	SPI	SPI interface clock input	no	no	
27	SI	SPI	SPI interface digital input	no	no	
28	CSB	SPI	SPI interface chip interface	no	no	
29	PDI	Motor pump driver	Pump driver input for MCU control	no	no	
30	GND_P9	Supply	Power Ground 9	no	no	(4)
31	VINT_D	Internal function	2.5 V internal supply for digital	no	no	(3)
32	GND_D	Supply	Digital ground	no	no	
33	DOSV	Supply	Digital output voltage supply, DOSV undervoltage reset	5.0 V	3.3 V	
37	SO	SPI	SPI interface digital output	DOSV bias		
38	GND_P10	Supply	Power Ground 10	no	no	(4)
39	ADIN1	ADC	Analog to digital input 1	no	no	
40	ADIN2	ADC	Analog to digital input 2	no	no	

Table 2. SB0410 pin definitions (continued)

Pin number	Pin name	Pin function	Definition	DOSV = 5.0 V	DOSV = 3.3 V	Notes
41	ADIN3	ADC	Analog to digital input 3	no	no	
42	VCC5	Supply	5.0 V supply pin	5V	5V	
43	GND_A	Supply	Analog ground	no	no	
44	VINT_A	Internal function	2.5 V internal supply for analog	no	no	(3)
45	GND_P11	Supply	Power ground 11	no	no	(4)
46	RSTB	Reset	Reset	no	no	
47	GND_P0	Supply	Power ground 0	no	no	(4)
23, 24, 25, 34, 35, 36	NC	Not connected	Pin used for production tests and must be grounded	no	no	
Exposed pad	GND_P12	Supply	Power ground 12	no	no	(4)

Notes

2. Pins with the same name must be shorted together
3. 220 nF/10 V capacitor needed
4. All GND_Px pins must be shorted together at the PCB level.

4 General product characteristics

4.1 Maximum ratings

Table 3. Maximum ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Description (rating)	Min.	Max.	Unit	Notes
Supply					
V_{VPWR}	Analog Power Supply Voltage	-0.3	40	V	
V_{DOSV}	Digital Output Supply Voltage	-0.3	7.0	V	
V_{VCC5}	Digital Power Supply Voltage	-0.3	7.0	V	
V_{GND_A}	Ground Analog	-0.3	0.3	V	
V_{GND_D}	Ground Digital	-0.3	0.3	V	
V_{GND_P}	Ground Exposed Pad	-0.3	0.3	V	
Internal function					
V_{VINT_A}	Internal Regulator Analog Power Supply	-0.3	3.0	V	
V_{VINT_D}	Internal Regulator Digital Power Supply	-0.3	3.0	V	
Charge pump					
V_{CP}	Internal Charge Pump	-0.3 or V_{PWR} -0.3	V_{PWR} +15	V	
High-side driver for general purpose					
V_{HS}	High-side Driver	-0.3	40 or V_{PWR} +0.3	V	
High-side driver for valve's fail-safe FET					
V_{HD_G}	Gate of the High-side Pre-driver	-20	55	V	
V_{HD_S}	Source of the High-side Pre-driver	-0.3	40	V	
V_{HD_D}	Drain of the High-side Pre-driver	-0.3	40	V	
Motor pump driver					
V_{PD_G}	Gate of the Motor Pump Pre-driver	-0.3 or PD_S-0.3	$V_{BOOT + 0.3}$	V	
V_{PD_S}	Source of the Motor Pump Pre-driver	-20	40	V	
V_{PD_D}	Drain of the Motor Pump Pre-driver	-20	40	V	
V_{BOOT}	Bootstrap Voltage	-10	V_{BOOT}+0.3	V	
V_{PDI}	Motor Control Input Voltage	-0.3	7.0	V	
Reset					
V_{RSTB}	Reset Pin	-0.3	7.0	V	
A to D converter					
V_{ADINx}	Input Analog to Digital	-0.3	7.0	V	

Table 3. Maximum ratings (continued)

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Description (rating)	Min.	Max.	Unit	Notes
SPI					
V_{SO}	Serial Peripheral Interface Slave Output	-0.3	DOSV +0.3	V	
V_{SI}	Serial Peripheral Interface Slave Input	-0.3	7.0	V	
V_{CSB}	Serial Peripheral Interface Chip Select	-0.3	7.0	V	
V_{SCLK}	Serial Peripheral Interface Clock	-0.3	7.0	V	
Low-side driver for valves (LSD1-4)					
V_{LSDx}	Low-side Driver for Valves	—	active clamp	V	
Low-side driver					
V_{LSD}	Low-side Driver	-100 mA	40	V	
Energy capability					
$E_{LSD1—4}$	Energy Capability (EAR) at 125 °C • LSD1—4, with 20 mH load	—	30	mJ	
Currents					
$I_{LSDX(POS)}$	Drain Continuous Current; during on state • LSDx	—	5.0	A	
$I_{LSDX(NEG)}$	Maximum Negative Current for 5.0 ms Without Being Destroyed • LSDx	-6.0	—	A	
I_{DIG}	Input Current • SI, CSB, SCLK, RSTB, PDI	-20	20	mA	

4.2 Operating conditions

This section describes the operating conditions and the current consumptions. Conditions apply to all the following data, unless otherwise noted.

Table 4. Operating conditions

Voltage parameters are absolute voltages referenced to GND. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
V_{PWR}	Functional Operating Supply Voltage. Device is fully functional. • All features are operating	6.0	—	36	V	
V_{CC5}	Functional Operating Supply Voltage. Device is fully functional. • All features are operating.	4.75	—	5.25	V	
V_{DOSV}	Functional Operating Supply Voltage. Device is fully functional. • All features are operating.	3.13	—	5.25	V	

4.3 Supply currents

This section describes the operating conditions and the current consumptions. Conditions apply to all the following data, unless otherwise noted.

Table 5. Supply currents

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 36 V, 4.75 V ≤ V_{CC5} ≤ 5.25 V, 3.13 V ≤ V_{DOSV} ≤ 5.25 V, -40 °C ≤ T_J ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
VPWR current consumptions						
I_{QVPWR}	Quiescent Current of VPWR Measured at 36 V, V_{CC5} = 0 V	—	—	30	µA	
I_{VPWR}	Current of VPWR in Operating Mode	—	—	20	mA	
VCC5 current consumptions						
I_{VCC5}	Current of VCC5 Pin in Operating Mode (SPI frequency at 10 MHz)	—	10	—	mA	
DOSV current consumptions						
I_{DOSV}	Current of DOSV Pin in Operating Mode (SPI frequency at 10 MHz)	—	10	—	mA	

4.4 Thermal ratings

Table 6. Thermal data

Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
T_J	Operational Junction Temperature	-40	—	150	°C	
T_{STG}	Storage Temperature	-65	—	150	°C	
$R_{\theta JC}$	RθJC, Thermal Resistance, Junction to Case (Package exposed pad) - Steady state	—	—	1.5	°C/W	(5)
T_{PPRT}	Peak Package Reflow Temperature During Reflow	—	—	Note 6	°C	(6)

Notes

5. Thermal resistance between the die and the solder pad on the bottom of the package based on simulation without any interface resistance.
6. NXP's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.nxp.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC34xxxD enter 34xxx), and review parametrics.

4.5 Logical inputs and outputs

Table 7. Logical inputs/outputs

VPWR = 6.0 V to 36 V, VCC5 = 4.75 V to 5.25 V, DOSV = 3.13 V to 5.25 V, T_J = -40 °C to 125 °C, unless otherwise specified.

Symbol	Description (rating)	Min.	Max.	Unit	Notes
Logical inputs					
V_{IH_X}	Input High-voltage • RSTB, SI, CSB, SCLK, PDI	—	2.0	V	
V_{IL_X}	Input Low-voltage • RSTB, SI, CSB, SCLK, PDI	0.8	—	V	
Logical outputs					
V_{OH_X}	Input High-voltage, with 1.0 mA • SO	0.8 x DOSV	—	V	
V_{OL_X}	Input Low-voltage, with 1.0 mA • SO	—	0.4	V	
$VOL_{\_RSTB}$	RSTB Low-voltage, with 1.0 mA • RSTB	—	0.4	V	

5 General description

5.1 Block diagram

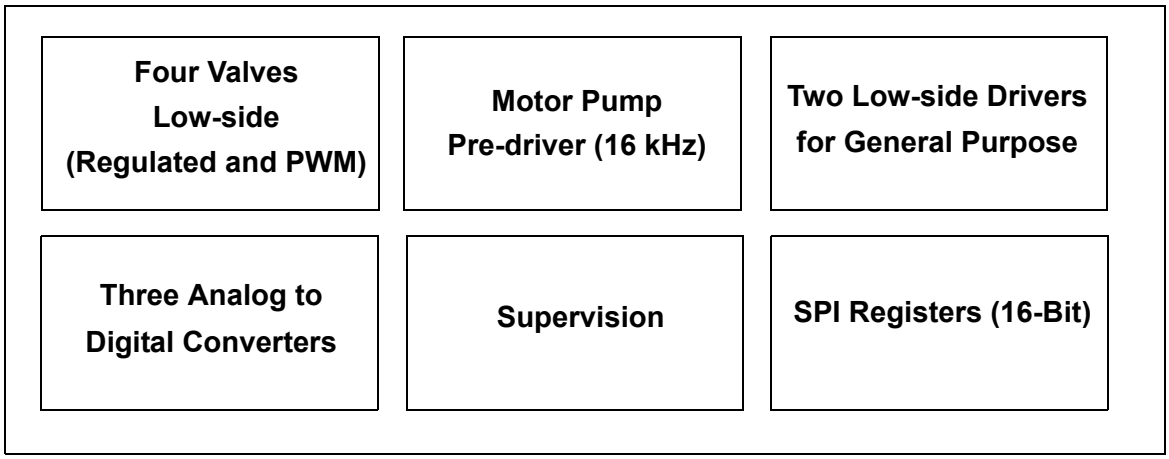


Figure 4. SB0410 functional block diagram

5.2 Functional description

The SB0410 device is a valves and DC motor controller, designed for use in harsh industrial environments, requiring few external components.

The SB0410 has four high-current low-side drivers to use with solenoid valves, and one high-side pre-drivers to controlling an external N-channel MOSFETs to use with a DC motor at high frequency thanks to the integrated bootstrap. In conjunction with this primary functionality, the SB0410 has two low-side drivers to control a resistive load. The digital I/O pins can be used for both 5.0 V and 3.3 V levels for easy connection to any microprocessor. The device includes three Analog to Digital converters. The SB0410 uses standard SPI protocol for communication.

5.3 Features

This section presents the detailed features of SB0410.

Table 8. Device features set

Function	Description
Low-side Solenoid Driver (x4)	• Solenoid driver (300 mΩ max. $R_{DS(on)}$ at 125 °C) works either as current regulator or as PWM • Current regulation deviation: ±2.0% • Configurable PWM frequency from 3.0 kHz to 5.0 kHz • 10-bit resolution on the current value targeted (Regulated mode). • 8-bit resolution on the duty cycle. (PWM mode) • Open load detection • V_{DS} state monitoring • Overcurrent shutdown • Overtemperature shutdown • Send current regulation error flag
Pump Pre-driver	• Motor pump pre-driver up to 16 kHz. PWM frequency controllable through SPI command or a digital signal (PDI pin). • Overcurrent shutdown between external FET drain and source • Overtemperature shutdown

Table 8. Device features set (continued)

Function	Description
Low-side Driver for Resistive Charge (x2)	• Low-side driver (20 mA max, $R_{DS(on)}$ 8.0 Ω) • Open load detection • V_{DS} state monitoring • Overcurrent shutdown • Overtemperature shutdown
Analog to Digital Converter	• 10-bit ADC • External ADINx pins (x3) • Internal voltages and temperature information • Duty cycle to current converter for low-side (LSDx).
Supervision	• VINT_x undervoltage (internal regulator) • VCC5 & DOSV undervoltage (supply voltage from external) • External reset fault • V_{PWR} undervoltage and overvoltage detections • Mismatch MAIN-AUX OSC CLK • Temperature warning • SPI failure • Bootstrap issue • GND supervision

6 Functional block description

6.1 Error handling

Table 9. Error handling

Type of error	Detection condition	Action	Clear SPI flag	Restart condition
Pump motor PWM driver				
Overcurrent between external FET Drain and Source	ON	PD_G Off+ SPI fault flag (PD_oc)	Write 1 to PD_clr_flt	Write 1 to PD_clr_flt and then turn on PDI
Overtemperature	ON	PD_G Off+ SPI fault flag (PD_ot)	Write 1 to PD_clr_flt	Write 1 to PD_clr_flt and then turn on PDI
LSDx				
Open load	OFF	SPI flag (LSDx_op)	Read diagnosis	No
V_{DS} state monitoring	ON/OFF	Read V_{DS} state by SPI (vds_LSDx)	Update with min filter time (T1) rise and fall edge	No
Overcurrent	ON	OFF fault FET only+ SPI fault flag (LSDx_oc)	Write 1 to LSD_clr_flt	Write 1 to LSD_clr_flt and turn on by SPI command (LSDx duty cycle or current set point)
Overtemperature	ON	OFF fault FET + SPI fault flag (LSDx_ot)	Write 1 to LSD_clr_flt	Write 1 to LSD_clr_flt and turn on by SPI command (LSDx duty cycle or current set point)
Current regulation error	ON	SPI flag (LSDx_crer)	Read diagnosis	No
LDx				
OpenLoad	OFF	SPI flag (LDx_op)	Read diagnosis	No
V_{DS} state monitoring	ON/OFF	V_{DS} state by SPI (V_{DS_LDx})	Update with min filter time (T1) rise and fall edge	No
Overcurrent	ON	OFF fault FET + SPI fault flag (LDx_oc)	Write 1 to LDx_clr_flt	Write 1 to LDx_clr_flt and turn on by SPI command (LDx_on)
Overtemperature	ON	OFF fault FET + SPI fault flag (LDx_ot)	Write 1 to LDx_clr_flt	Write 1 to LDx_clr_flt and turn on by SPI command (LDx_on)
Supervision				
VINT_x undervoltage	All except Sleep mode	SPI registers reset & Vint_uv go to High (See Table 19)	Read Vint_uv bit (See Table 19)	No
VCC5 & DOSV undervoltage	All except Sleep mode	SPI registers reset except some bit. (See Table 19)	Wait undervoltage reset filter time T1 (see Table 19)	See Table 19,
External reset fault	No internal RSTB pulldown	SPI registers reset except some bit. (See Table 19)	Read the corresponding message of the SPI register (see Table 19)	See Table 19,
VPWR undervoltage	RSTB is high state	All LSDx Off (Clear all LSDx duty cycle registers or current set point) + SPI fault flag (V_{PWR_UV})	1. Normal condition 2. Read diagnosis (V_{PWR_UV})	1. Normal condition 2. Turn on by SPI command (LSDx duty cycle or current set point)
VPWR overvoltage	RSTB is in high state	All LSDx Off (Clear all LSDx duty cycle registers or current set point) + SPI fault flag (V_{PWR_OV})	1. Normal condition 2. Read diagnosis (V_{PWR_OV})	1. Normal condition 2. Turn on by SPI command (LSDx duty cycle or current set point)
Mismatch SB0410 MAIN-AUX OSC CLK	RSTB is in high state	SPI registers goes to initial state low except (see Table 19,)	Read RST_clk bit	No
Temperature warning	RSTB is in high state	SPI flag	1. Normal condition 2. Read diagnosis	No

Table 9. Error handling (continued)

Type of error	Detection condition	Action	Clear SPI flag	Restart condition
Supervision (continued)				
SPI failure	RSTB is in high state	SPI flag (Fmsg)	Read diagnosis	No
V_{PRE} 1x monitoring [8]	RSTB is in high state	Send by SPI (ADC)	No	No
VINT_x monitoring [8]	RSTB is in high state	Send by SPI (ADC)	No	No
V_{GS_PD} monitoring	RSTB is in high state	Send by SPI (ADC)	No	No
Temperature monitoring [8]	RSTB is in high state	Send by SPI (ADC)	No	No
GND_D supervision	RSTB is in high state	SPI flag only (FGND)	No	No
GND_A supervision; indirect detection by VCC5 or DOSV	RSTB is in high state	SPI flag only (VCC5_UV or DOSV_UV)	No	No

Notes

7. To clear an error flag, SW engineer has to read the register concerned and then write a “1” on the xxx_clr_flt flag.
8. SW engineering can monitor internal supply voltage in real time with ADC SPI reading, and can use fail-safe function. If these ADC results are not in a certain range, uC can reset the SB0410 (see ADC section).

6.2 Low-side driver

6.2.1 Introduction

The SB0410 is designed to drive in current regulated or in digital mode inductive loads in low-side configuration. All four channels are managed by logic and faults are individually reported through the SPI. The device is self-protected against short-circuit, overtemperature, can detects an open-load and finally allows to monitor in real-time the V_{DS} state.

When Channels 1 to 4 work as a current regulator, a freewheeling diodes must be connected. Each channel comprises an output transistor, a pre-driver circuit, a diagnostic circuitry, and a current regulator. The SPI registers (10 to 13) defines the current output targeted. This output is controlled through the output PWM of the power stage. The LSD1-4 current slopes are controlled by a SPI command to reduce switching loss.

6.2.2 Digital mode

LSD1 to 4 can be used in digital mode (also called “PWM”). This function integrates a current recirculation thanks to the gate-drain clamp circuitry embedded. The output transistor is equipped with an active clamp limiting LSDx voltage to vcl_lsd. During turn-off, the inductive load forces the increasing output voltage until the active voltage clamps, such as when the power FET turns on again.

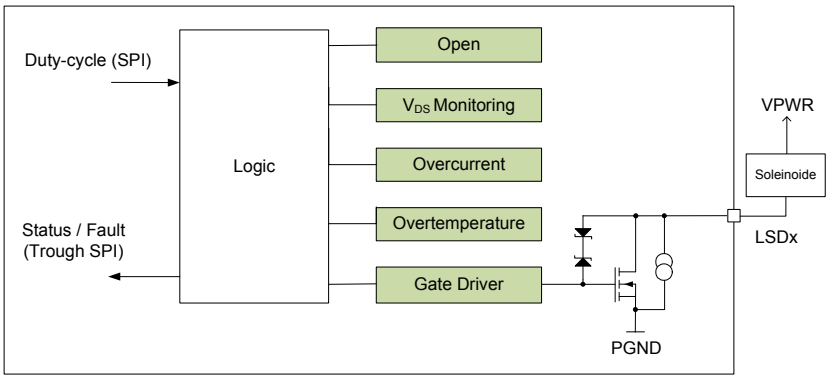


Figure 5. PWM low-side driver

The duty cycle of PWM low-side drivers is programmed via an 8-bit SPI message. The duty cycle between 0% and 100% can be selected and the LSB of the 8 bits is weighted with an 0.39% duty. Each channel has an 8-bit SPI register of PWM duty cycle.

The PWM low-side driver uses each channel as a digital low-side switch.

PWMx duty cycle = 0xFF - Digital low-side switch ON (conducting)

PWMx duty cycle = 0x00 - Digital low-side switch OFF

6.2.3 Interleave function

The SB0410 provides interleaved phase shift switching to minimize switching noise of the solenoid coil. Each LSDx is shift to 1/4 of the period from the previous one. this interleave function started with the LSD1.

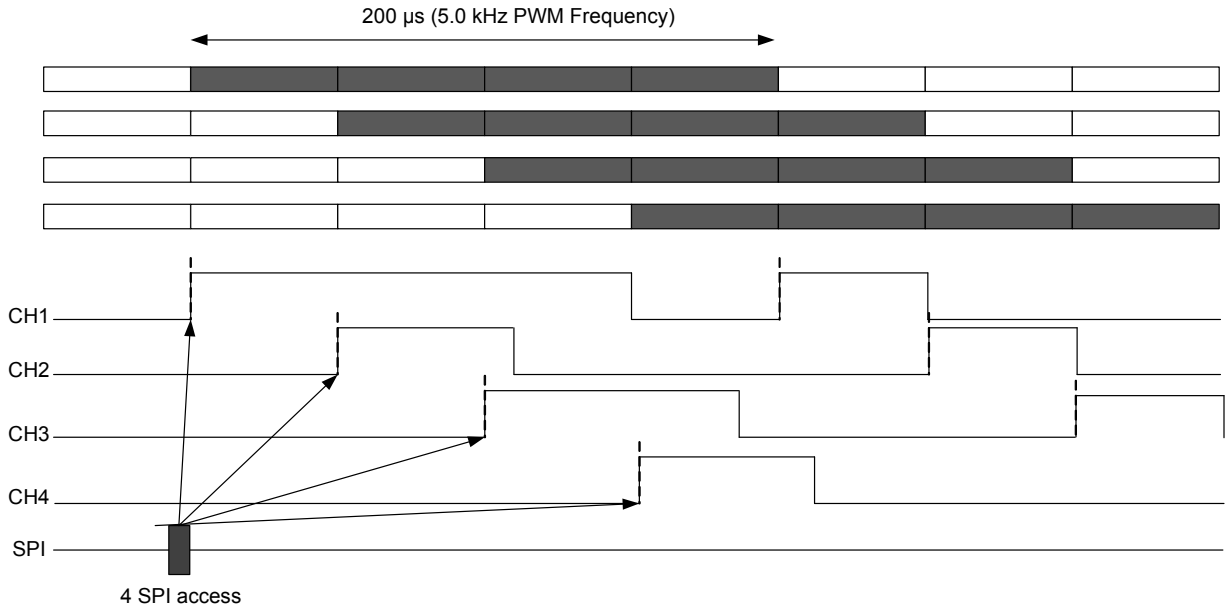


Figure 6. PWM valve control interleave

Table 10. Low-side driver electrical characteristics

VPWR = 6.0 V to 36 V, DOSV = 3.13 V to 5.25 V, T_J = -40 °C to 125 °C, unless otherwise specified.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Power output						
R_{ON_LSD14}	On Resistance Channel 1 to 4: CR • T_J = 125 °C; 9.0 V ≤ V_{PWR} ≤ 36 V; I_{LOAD} = 2.0 A	—	—	0.225	Ω	
$R_{ON\_LSD14\_E}$	On Resistance Channel 1 to 4: CR (extended mode) • T_J = 125 °C; 5.5 V ≤ V_{PWR} ≤ 9.0 V; I_{LOAD} = 2.0 A	—	—	0.330	Ω	
I_{LEAK_LSD}	Drain Leakage Current • LSD = 36 V	—	—	10	µA	
V_{CL_LSD}	Active Clamp Voltage	—	38	45	V	
Timings						
t_{R_CR1} t_{F_CR1}	Rise Time/Fall Time • 10% to 90%, I_{LOAD} = 1.0 A, V_{PWR} = 36 V; no capacitor didt = 0 (SPI bit)	1.0 0.1	1.7 1.35	3.0 3.0	µs	
t_{R_CR2} t_{F_CR2}	Rise Time/Fall Time • 10% to 90%, I_{LOAD} = 1.0 A, V_{PWR} = 36 V; no capacitor didt = 1 (SPI bit)	0.05 0.1	0.5 1.0	1.0 3.0	µs	
t_D on CR t_D off CR	Turn on/off Delay Time • Digital 1 to 10% or 90%, I_{LOAD} = 1.0 A, V_{PWR} = 36 V, no capacitor	0.0	—	3.0	µs	(9)
$Lf_{\_PWM}$	Output PWM frequency for LSD1-4 • LF_PWM xx = 111 • LF_PWM xx = 110 • LF_PWM xx = 101 • LF_PWM xx = 100 • LF_PWM xx = 000 (default) • LF_PWM xx = 011 • LF_PWM xx = 001 • LF_PWM xx = 010	-20%	3.0 3.2 3.4 3.6 3.9 4.2 4.5 5.0	20%	kHz	
0x00 0x01 … 0xFE 0xFF	PWM Duty Cycle Programming (8-bits)	— — — — —	OFF 0.39 — 99.61 ON	— — — — —	%	

Notes

9. Digital: internal digital signal delivered by interleave synchronization block. See Figure 6.

6.2.4 Current regulation mode

When the external fly-back diode is connected, the current re-circulation executes via the diode to the battery.When Channels 1 to 4 work as a current regulator, freewheeling diodes must be connected.

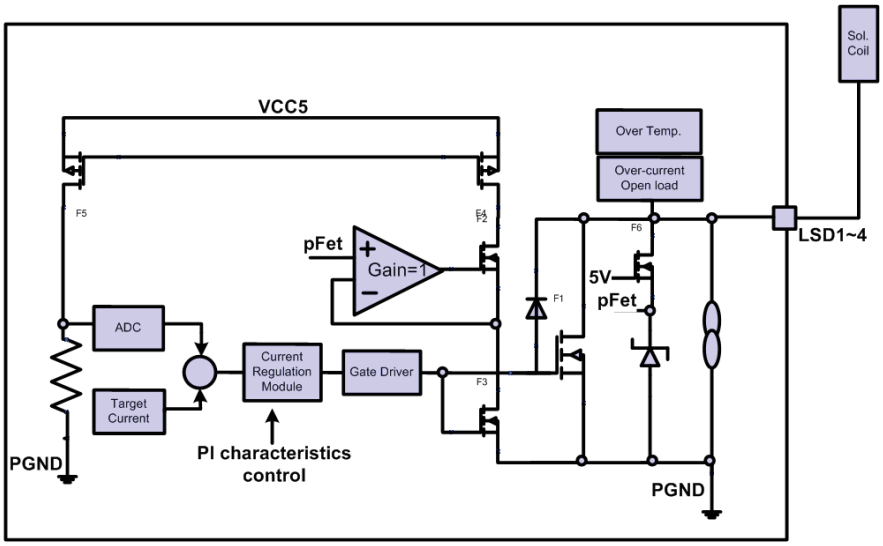


Figure 7. PWM low-side driver (current regulated)

The load current is sensed by an internal low-side sense FET and digitized by an internal A/D converter. The target value of the current is given SPI messages. A digital current regulation circuitry compares the actual load current with the target current value and steers the duty cycle of the low-side power switch. The PI regulator characteristic can be adjusted via the SPI.

6.2.4.1 Target current

Each current regulator channel has its own 10-bit target current register. The LSB of the 10 bits is weighted with 2.2 mA. A zero value disables the power stage of the respective channel. A new target current is instantaneously passed to the settling time, which is the settling of the new current value.

PWMx target current value = 00 0000 0000 → 0 mA

PWMx target current value = 00 0000 0001 → 2.2 mA

…

PWMx target current value = 11 1111 1110 → 2.248 A

PWMx target current value = 11 1111 1111 → 2.250 A

CR_DIS12/34	CR_fb	Mode	LSD1-4 duty cycle (8-bit) or current read (10-bit)
0	0	current regulation	Read current target (to check SPI write)
0	1	current regulation	Read output duty cycle value for gate driver.
1	0	PWM	Read programmed PWM duty cycle (to check SPI write)
1	1	PWM	Read hardware ADC current value

6.2.4.2 Current measurement

The output current is measured during the “ON’ phase of the low-side driver. A fraction of the output current is diverted and (using a “current mirror” circuit) generates across an internal resistance a voltage relative to ground, this being proportional to the output current.

6.2.4.3 PI characteristics

Digital PI-regulator with the Transfer function is programmed via the SPI register.

Transfer function: $\frac{KI}{z-1} + KP$

The integrator feedback register I charac bits define the regulation behavior of all channels. The default value is 1/8. Both current regulators remain idle until a non-zero value in I charac was programmed. A high proportional feedback value accelerates the regulator feedback and provides a faster settling of the regulated current after disturbances like battery voltage surge.

Table 11. Duty cycle descriptions

The duty cycle of the PWM output in clamped minimum by options and maximum 100% (see 6.7, “SPI and data register").

Option	LLC<1>	LLC<0>	Minimum Duty Cycle
0	0	0	10% • the measurement is done at $t_{ON}/2$ by consequence • the regulation current will be set at $t_{ON}/2$
1	0	1	3.12% • for a duty cycle > 10%, the measurement is done at $t_{ON}/2$ • for a duty cycle 3.2% < DC < 10%, the measurement is done at $t_{ON}/2$ for 10% of duty cycle up at t_{ON} for 3.2% of duty cycle
2	1	0	3.12% + forced min duty cycle to 1.56% every two cycles • for a duty cycle > 10%, the measurement is done at $t_{ON}/2$ • for a duty cycle 3.2% < DC < 10%, the measurement is done at $t_{ON}/2$ for 10% of duty cycle up at t_{ON} for 3.2% of duty cycle • for a duty cycle set at 1.56%, no measurement is done
3	1	1	3.12% + skip min duty cycle every two cycles • for a duty cycle > 10%, the measurement is done at $t_{ON}/2$ by consequence the regulation current will be set at $t_{ON}/2$ • for a duty cycle 3.2% < DC < 10%, the measurement is done at $t_{ON}/2$ for 10% of duty cycle up at t_{ON} for 3.2% of duty cycle • no measurement is done during the skipping mode

If the target current value is not reached within the regulation error delay time of t_{CR_ERR}, the flag of the SPI register “LSDx_crer” is set to high. The current regulation loop is still running and tries to regulate at the target. Because it is not at the target, the duty cycle is either 100%, or minimum duty cycle by option. LSDx_crer error detection has no effect on the driver, only SPI fault reporting. The microcontroller can detect the fault through the SPI (LSDx_crer bit + ADC current reading), and shutdown the driver by sending 0 target current. Set Current – ADC result > “error threshold” during t_{CR_ERR} then LSDx_crer is set to 1.

This flag is latched & can be reset by the SPI read (LSDx_crer). Each of the four current regulation low-side drivers can be used as a PWM low-side switch. CR_disxx flag is enabled HIGH. The 8 MSB bits of the target current message are the PWM duty cycle. The first duty is controlled by the SPI bit FDCL (See SPI and data register).

Table 12. LSD1 to LSD4 current regulation driver electrical characteristics

VPWR = 6.0 V to 36 V, VCC5 = 4.75 V to 5.25 V, DOSV = 3.13 V to 5.25 V, T_J = -40 °C to +125 °C, unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Current Regulation						
00 0000 0000 00 0000 0001 ... 11 1111 1111	Target current programming (10-bits)	— — — —	OFF 2.2 ... 2.25	— — — —	mA A	
I_{CR_DEV}	Maximum regulation deviation • 0 mA ≤ I_{TARGET} < 50 mA, includes ADC error • 50 mA ≤ I_{TARGET} < 100 mA, includes ADC error • 100 mA ≤ I_{TARGET} < 250 mA, includes ADC error • 250 mA ≤ I_{TARGET} < 400 mA, includes ADC error • 400 mA ≤ I_{TARGET} < 2.25 A, includes ADC error	 — — — — —	 — — — — —	 65 50 25 ±10 ±2.0	 mA mA mA % %	 (10) (11)

Notes

10. Maximum regulation deviation performances noted in the table depend on external conditions (V_{PWR}, load (R,L)).
11. The error can be decrease significantly by a calibration of the LSDx and using a current regulation loop done by software.

6.2.5 Fault detection (LSD1 to LSD4)

6.2.5.1 Open load

An open condition is detected when the LSDx output is below the threshold for the defined filter time; the fault bit is set (SPI error flag only). This function only operates during the off state.

6.2.5.2 V_{DS} state monitoring

The V_{DS} state monitoring gives real time state of LSD drain voltage vs OP_ISD voltage. This signal is filtered and sent through the SPI. If the LSDx voltage is higher than the OP_ISD with a filter time (T1), vds_lsd is set to “1”.

6.2.5.3 Overcurrent

When the current is above the overcurrent threshold for the defined filter time, the driver is switched off, a SPI fault bit is set, and the driver can be turned back to the “normal state” by a SPI write “1” to “LSDx_clr_flt “, followed by a send target current command.

6.2.5.4 Overtemperature

When the temperature is above the overtemperature threshold for the defined filter time, the driver is switched off, a SPI fault bit is set, and the turn-on SPI command is cleared. The driver can be turned back to the “normal state” when the temperature returns to a normal state, then SPI write “1” to “LSDx clr flt”, followed by a send target current command.

Table 13. Detection Electrical Characteristics

VPWR = 6.0 V to 36 V, VCC5 = 4.75 V to 5.25 V, DOSV = 3.13 V to 5.25 V, T_J = -40 °C to +125 °C, unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
PD_G						
OC_{LSD}	Overcurrent Detection Threshold Current	—	8.5	—	A	
Open load detection						
OP_{LSDSRC}	Open Load Detection Threshold (also used for V_{DS} monitoring)	—	2.0	—	V	
V_{DS} Monitoring						
t_{VDS_LSDX}	V_{DS} State Filter Time	—	T1	—	µs	
Overtemperature Shutdown						
V_{PD_OC}	Overcurrent detection threshold - VPD_D - VPD_src	-15%	1.0	+15%	V	
Overtemperature Shutdown						
OT_{LSD}	Overtemperature Detection Threshold	180	195	210	°C	
Current Regulation Error (Regulation mode only)						
ICR_{DELTA}	Current Regulation Error - ADC Result (measurement data) - (target programming current) • 1LSB = 2.25 A/1024 = 2.197 mA	—	25	—	LSB	

6.3 Pump motor pre-driver

6.3.1 Function description

This module is designed for DC motor pump, a maximum of 16 kHz PWM is possible. The pre-driver is made with a bootstrap as well as small charge pump structure to operate to 100% duty cycle.

.

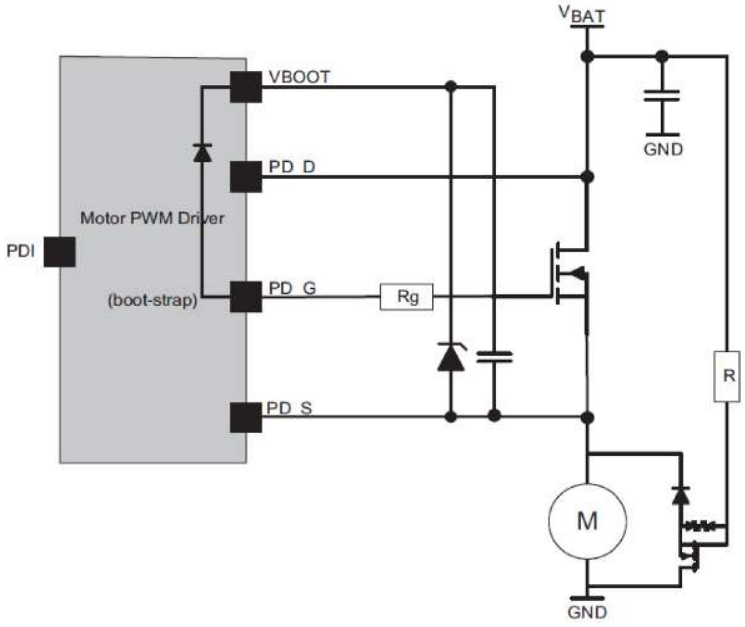


Figure 8. Pump motor pre-driver

A duty cycle comprised between 0% to 10% and between 90% to 100% is not possible due to the structure.

6.3.2 Fault detection

6.3.2.1 Overcurrent

The pump driver protects the external N-channel power FET on the PD_G pin in overcurrent conditions. The drain-source voltage of the FET on PD_G is checked if the pump driver is switched on. If the measured drain-source voltage exceeds the overcurrent voltage threshold, the output PD_G is switched off. Overcurrent detection logic has a masking time from PDI turn-on against malfunction on transient time. After switching off the power FET by an overcurrent condition, the power FET can be turned back to “normal state” by only SPI write 1 to “PD_clr_flt” register, and then turn on with PDI.

After pump driver is switched on and it stays on during minimum time period T1/2 (masking period), a cumulate/decumulate process of overcurrent fault detection logic is enabled. After the masking period is over, if both events are present (PDI = 1 and overcurrent condition), there is a cumulate (increment) process taking place measuring the maximum time period T1 to qualify an overcurrent fault event. If both events are present longer than T1, this activates an overcurrent fault (and consequently sets corresponding flag). If PDI = 0, the cumulate process is halted but not reset. If during PDI = 1 the event of the overcurrent condition is not present, this resets a previously cumulated value.

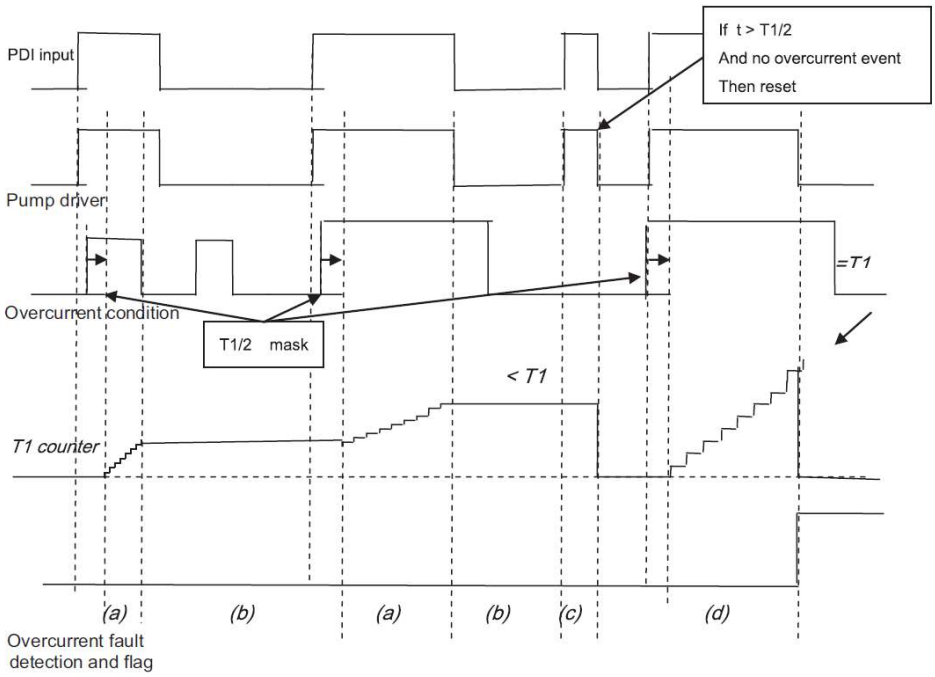


Figure 9. Block diagram of cumulate/de-cumulate process of overcurrent fault detection logic

Function of T1 counter:

a) Increment
b) Hold
c) Reset
d) Overcurrent fault detected

6.3.2.2 Overtemperature

When the temperature is above the overtemperature threshold for the defined filter time, the driver is switched off and a SPI fault bit is set. The driver can be turned back to the “normal state” by writing a 1 to PD_clr_flt, then turn PDI on.

6.3.2.3 External components of pump pre-driver

An external 15 V Zener clamping (1 direction) is necessary between VBOOT and PD_S to protect the gate of the external Power MOSFET. An internal diode between VBOOT and PD_G ensures that PD_G cannot go higher than VBOOT (1 V_{BE} higher). Optional 15 V Zener clamping can be added between PD_G & PD_S (not necessary). The zener chains are used for avalanche clamping and protection against transients.

A typical external MOSFET is IPB80N04S2, which is 4.0 mΩ (for indication only). An external resistor of 500 kΩ is connected between PD_G & PD_S to turn the MOSFET OFF, in case of an open soldering contact. An external resistor (R_G) in series with PD_G is added to decrease the slew rate and optimize EMC. The value of the C_{BOOT} capacitor between VBOOT & PD_S can be 330 nF (for 5.0 kHz & 20 kHz).

Table 14. Pump motor pre-driver electrical characteristics

VPWR = 6.0 V to 36 V, VCC5 = 4.75 V to 5.25 V, DOSV = 3.13 V to 5.25 V, T_J = -40 °C to +125 °C, unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
PD_G						
$V_{PD\_ON\_5K}$	• 5.5 V ≤ V_{PWR} < 6.0 V • 6.0 V ≤ V_{PWR} < 7.0V • 7.0 V ≤ V_{PWR} < 10 V • 10 V ≤ V_{PWR} < 36 V	V_{PWR}+ 4 V_{PWR}+5 V_{PWR}+7 V_{PWR}+10	— — — —	V_{PWR}+ 15 V_{PWR}+15 V_{PWR}+15 V_{PWR}+15	V	(12)
$V_{PD\_ON\_20K}$	• 5.5 V ≤ V_{PWR} < 7.0 V • 7.0 V ≤ V_{PWR} < 12.0V • 12.V ≤ V_{PWR} < 36 V	V_{PWR}+ 4.5 2xV_{PWR}-2.0 V_{PWR}+10	— — —	V_{PWR}+ 15 V_{PWR}+15 V_{PWR}+15	V	(13)
V_{GS_OFF}	PD_G switch-off voltage	—	—	0.1	V	
I_{PDG_OFF}	Turn-off current	—	300	—	µA	
PD_S						
$I_{LEAK\_PD\_SRC}$	Leakage Current - VCC5 = DOSV = 0.0 V, VPWR = 36 V, PD_S = 36 V	—	—	1.0	mA	
PD_D						
$I_{LEAK\_PD\_DRN}$	Leakage current - VCC5 = DOSV = 0.0 V, PD_D = VPWR = 36 V	—	—	15	µA	
Overcurrent detection						
V_{PD_OC}	Overcurrent detection threshold - VPD_D - VPD_src	-15%	1.0	+15%	V	
t_{PD_OC}	Overcurrent Detection Filter Time - Cumulate counter during on phase after masking time, reset counter if no OC event during 1 cycle	—	T1	—	µs	
$Duty_{Alo}$	10% to 90% duty cycle is allowed (also 0% and 100% is allowed)	10	—	90	%	
Overtemperature shutdown						
OT_{PMD}	Overtemperature Detection Threshold	180	195	210	°C	
tOT_{PMD}	Overtemperature Detection Filter Time	—	T1	—	µs	
VBOOT charge						
t_{BOOT_DELAY}	Bootstrap Start Time - Time to charge C_{BOOT} after wake-up of part (V_{CC5} = 5.0 V). Allow Pump driver to turn on after this timing. (This timing is smaller than reset recovery time (45 ms), so has no effect on the application)	—	30	—	ms	

Notes:
12. Frequency = 5.0 kHz , duty cycle = 10~90% and 100%, voltage measured 20 µs after turn on.
13. Frequency = 20.0 kHz , duty cycle = 10~90% and 100%, voltage measured 5.0 µs after turn on.

6.4 Low-side driver for resistive load

6.4.1 Power output stages

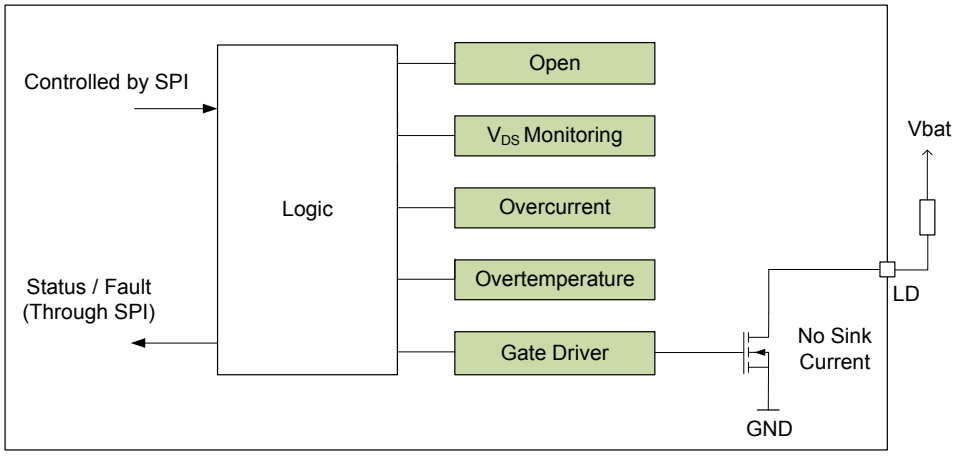


Figure 10. Low-side driver for resistive load diagram block

The low-side driver consists of DMOS power transistors with open drain output. The low-side driver can be driven by SPI commands. The low-side driver is composed of an output transistor, a pre-driver circuit, and diagnostic circuitry. The pre-driver applies the necessary voltage on the output transistor gate to minimize the On resistance of the output switch. To avoid leakage current path, LD has no sink current.

Table 15. Low-side driver electrical characteristics

VPWR = 6.0 V to 36 V, VCC5 = 4.75 V to 5.25 V, DOSV = 3.13 V to 5.25 V, T_J = -40 °C to 125 °C, unless otherwise specified.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Power output LD						
R_{ON_LD}	On Resistance for LD • T_J = 125 °C, 6.0 V ≤ V_{PWR} ≤ 36 V	—	8.0	14	Ω	
	DC Current Capability	—	—	20	mA	
I_{LEAK_LD}	Drain Leakage Current • V_{PWR} = 0, V_{CC5} = 0, LD = 36 V, no sink current	—	—	10	µA	
V_{BVDSS_LD}	BVDSS Voltage	40	—	—	V	
I_{NEG_LD}	Maximum Negative Current for 5.0 ms Without Destroying the device	100	—	—	mA	
Timings						
$t_{D\_ON\_LD}$	Turn On Delay Time for LD	—	—	2.0	µs	(14)
$t_{D\_OFF\_LD}$	Turn Off Delay Time for LD	—	—	2.0	µs	(14)

Notes

14. From Digital Signal to 50% (turn ON) or 50% (turn OFF). R_L = 1.0 kΩ, V_{PWR} = 36 V, no capacitor

6.4.2 Fault detection

6.4.2.1 Open load

An open condition is detected when the LD output is below the threshold OP_{LD} for the defined filter time t_{OP_LD}, the fault bit is set ld_OP (SPI error flag only). This function only operates during the Off state.

6.4.2.2 V_{DS} state monitoring

The V_{DS} state monitoring gives real time state of LD drain voltage vs OP_{LD} voltage. This signal is filtered and sent through the SPI vds_ld bit. If the V_{DS} voltage is higher than OP_{LD} with a filter time (T1), vds_ld is set to “1”.

6.4.2.3 Overcurrent

When the current is above the overcurrent threshold OC_{LD} for the defined filter time t_{OC_LD}, the driver is switched off, a SPI fault bit ld_OC is set, and the turn-on SPI command is cleared. The driver can be returned to the “normal state” by a SPI write “1” to “LD_clr_flt”, then turned on by a SPI command (LD_on).

6.4.2.4 Overtemperature

When the temperature is above the overtemperature threshold OT_{LD} for the defined filter time t_{OT_LD}, the driver is switched off, a SPI fault bit ld_OT is set, and the turn-on SPI command is cleared. The driver can be returned to the “normal state” when the temperature returns to the normal state, a SPI write “1” to “LD_clr_flt”, then turning on a SPI command (LD_on).

Table 16. Low-side driver electrical characteristics

VPWR = 6.0 V to 36 V, VCC5 = 4.75 V to 5.25 V, DOSV = 3.13 V to 5.25 V, T_J = -40 °C to 125 °C, unless otherwise specified.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Overcurrent shutdown						
I_{OCLD}	Overcurrent Shutdown Threshold Current for LD	—	100	—	mA	
t_{OC_LD}	Overcurrent Shutdown Filter Time	—	T1	—	µs	
Open load detection						
V_{OPLD}	OpenLoad Detection Threshold (also used for V_{DS} monitoring)	—	2.0	—	V	
t_{OP_LD}	OpenLoad Detection Filter Time	—	T2	—	µs	
V_{DS} monitoring						
t_{VDS_LD}	V_{DS} State Filter Time (rise & fall edge filter time)	—	T1	—	µs	
Overtemperature shutdown						
T_{OTLD}	Overtemperature Detection Threshold	180	195	210	°C	
t_{OT_LD}	Overtemperature Detection Filter Time	—	T1	—	µs	

6.5 Analog to digital converter (x3ch)

ADC is referenced to VCC5 voltage and converts the voltage on 10 bits. It is used to read the following voltages:

- Three analog input pins: ADINx
- Internal voltage supplies (VINT_A, VINT_D, V_{PRE10}, V_{PRE12}, V_{GS_PD})
- Average temperature of die, which is used by the temperature warning detection circuit (TEMP). Refer to the SPI Message Structure, Message #9.
- Current to voltage converter for current regulation of LSD1-4

Table 17. ADC electrical characteristics

VPWR = 6.0 V to 36 V, VCC5 = 4.75 V to 5.25 V, DOSV = 3.13 V to 5.25 V, T_J = -40 °C to 125 °C, unless otherwise specified.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
ADC						
ADC_ERR	Total Error - 0 < ADINx < VCC5	-6.0	—	6.0	LSB	(15)
t_{CONV}	Conversion Time	—	—	10	µs	
t_{RFT}	Refresh Time - min ADC update time; shorter than 1.0 ms	—	100	—	µs	
ADINx						
I_{ADI_LK}	Input Leakage Current - 0 < ADINx < VCC5	-2.0	—	2.0	µA	
Internal voltage						
$A_{D\_VINT\_A}$	V_{INT_A}	440	512	590	LSB	
$A_{D\_VINT\_D}$	V_{INT_D}	440	512	590	LSB	
A_{D_VPRE10}	V_{PRE10} - ADC ratio =V_{PRE10}/3.3, 9.0 < V_{PWR} < 16 V	400	600	800	LSB	
A_{D_VPRE12}	V_{PRE12} - ADC ratio = V_{PRE12}/3.0, 9.0 < V_{PWR} < 16 V	590	790	980	LSB	
A_{D_VCP}	V_{CP}-V_{PRWR} - ADC ratio = V_{CP} - V_{PWR}/4.0, 9.0 < V_{PWR} < 16 V	330	—	810	LSB	
Temperature reading						
A_{D_TEMP25}	Voltage at 25 °C	—	717	—	LSB	
$A_{D\_DEV\_TEMP}$	Deviation with 1.0 °C increments	—	-2.0	—	LSB/°C	

Notes

15. If ADINx voltage is between VCC5 to max_rating, the ADC value does not change. Also between VCC5 min and GND, the ADC value does not change.
16. SW engineer can monitor internal supply voltage in real time with ADC, SPI reading, and can use fail-safe function.

6.6 Supervision

Event	RSTB	LSDx	PDI	LD	SPI	Notes
Normal mode: After RSTB rising edge, No fault	High	Normal	Normal	Normal	Normal	
VINT_x undervoltage	Low (output)	OFF	OFF	OFF	SPI register go to initial state Low except for Vint_uv which is reset to 1. After first read of Vint_uv, it is set back to 0.	(17)
Clock fail reset	Low (output)	OFF	OFF	OFF	SPI registers go to initial state Low except for Vint_uv unchanged & RST_clk which is set to 1. After first read of RST_clk, it is set back to 0.	(17)
DOSV undervoltage	Low (output)	OFF	OFF	OFF	SPI register go to initial state except reset flag (Vint_uv, VCC5_uv, DOSV_uv, RST_ext, RST_CLK).	(17)
VCC5 undervoltage	Low (output)	OFF	OFF	OFF	SPI register go to initial state except reset flag (Vint_uv, VCC5_uv, DOSV_uv, RST_ext, RST_CLK).	(17)
External Reset	Low (input)	OFF	OFF	OFF	SPI register go to initial state except reset flag (Vint_uv, VCC5_uv, DOSV_uv, RST_ext, RST_CLK).	

Event	RSTB	LSDx	PDI	LD	SPI	Notes
VPWR overvoltage	No effect	OFF	ON	No effect	Following SPI registers go to initial state Low: A. LSDx Duty cycle or current set point. B. PDI is ON.	
VPWR undervoltage	No effect	OFF	ON	No effect	Following SPI registers go to initial state Low: A. LSDx Duty cycle or current set point. B. PDI is ON.	

Notes

17. State defines for the duration of the fault and the following reset recovery time period.

Restart conditions:
SPI write message #0 has first to be executed to clear any reset or fault flags. Then new SPI command can be sent.

Table 18. Start point of reset recovery time

Fault mode	Start point of t_{RST_REC}
VINT_A or VINT_D_uv or VCC_uv or DOSV_uv	Come back normal voltage of all voltages

6.6.1 Additional safety functions

6.6.1.1 VINT_A or VINT_D undervoltage supervision

The 900718 uses an internal supply for analog functions (V_{INT_A}) and digital functions (VINT_D). The supply voltage V_{INT_A} and V_{INT_D} are supervised for undervoltage. When the voltage becomes lower than each threshold, $V_{INT\_A\_UV}$ and $V_{INT\_D\_UV}$, the RSTB pin is asserted low, after the detection filter time (t_{VINT}). This reset state continues until the voltage at the VINT pin rises again. If VINT becomes higher than each threshold, $V_{INT\_A\_UV}$ and $V_{INT\_D\_UV}$, for same filter time (t_{VINT}), the RSTB pin goes high after reset recovery time (t_{RST_REC}) and the related flag of the SPI register is set to a high.

For stabilization, the VINT_A & VINT_D internal supply requires external capacitors. Two bandgaps are included in the 900718. One is for the voltage reference and the other is for the diagnostic. The ADC data for VINT_A and VINT_D are sent through the SPI.

6.6.1.2 VCC5 supervision

See Table 19 Reset condition and reaction.

6.6.1.3 DOSV supervision

The supply voltage DOSV is supervised for undervoltage. When the voltage at pin DOSV becomes lower than DOSV_uv, the RSTB pin is asserted low after detection filter time (t_{VDUV}). This reset state continues until the voltage at pin DOSV raises again. If DOSV becomes higher than (DOSV_uv) for same filter time (t_{VDUV}), the RSTB Pin goes high after reset recovery time (t_{RST_REC}) and the related flag of the SPI register is set high.

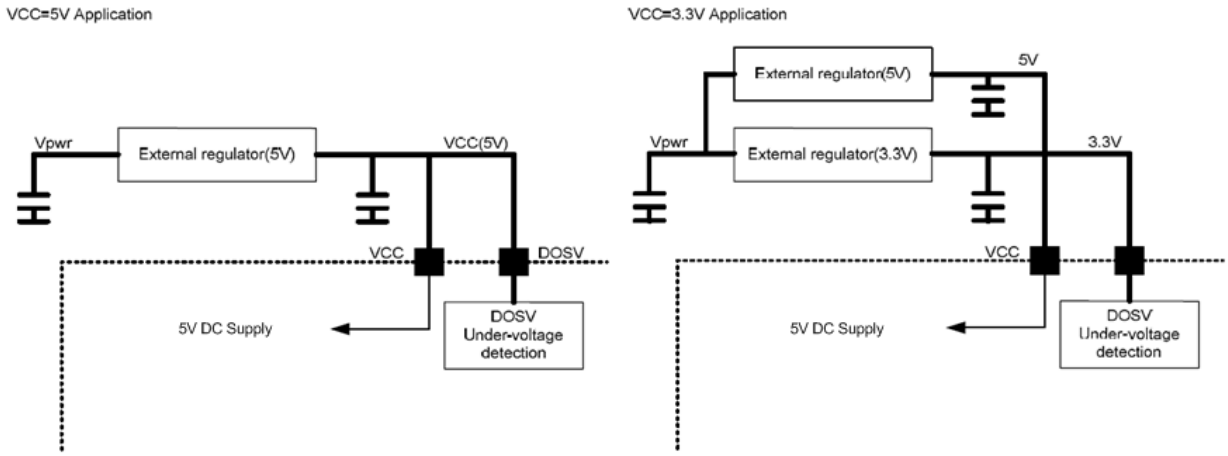


Figure 11. DOSV supervision application

6.6.1.4 Internal clock supervision (mismatch MAIN-AUX CLK)

The SB0410 has two independent clock modules, one is the main supply clock to all SB0410 systems. The other monitors the main clock fault and if a fault is detected, the SB0410 resets with the RST_CLK function (Table 19). This function starts when RSTB is in a high state.

Mutual Supervision of Both Main and Auxiliary Clock:

Clock monitoring continues to perform comparisons between the two clocks sources, CLK1 and CLK2. When everything is working correctly, both clocks are present and both have the same frequency of 14 MHz. If one of the clocks stops or if clocks are misaligned in frequency more than ±25% of 14 MHz (Table 19), an RSTB reset is generated (Table 19) and a SPI flag is reported (RST_CLK). The reset flag RST_CLK (same as other reset flags) is cleared in “clear on read” fashion, or in other words, the flag is cleared by a SPI Read command which reads the flag. In the case of a clock monitoring fault, the clock monitoring process restarts only after the clock monitoring flag (RST_CLK) is cleared on the first SPI message.

If either CLK1or CLK2 disappears indefinitely, the clock monitoring fault shows anywhere from T1 to 2*T2. If clock frequencies are misaligned more than ±25% of 14 MHz, the clock monitoring fault shows after a time delay of T2, as measured by the reference clock CLK1. The misaligned frequency detection error is measured in the time window of T2 and the measurement is based on CLK1 clock as reference, therefore if the CLK1 frequency changes, the time window T2 cannot be guaranteed.

The SB0410 internal clock monitoring function can be disabled by the SPI command (StopCLK2), with no effect of functionality except the clock monitoring function, because CLK1 is activated, but CLK2 is deactivated. Frequency modulation can be controlled by the FM_amp and FM_EM bits (See SPI and data register). The SPI command (FM_EN) enables the frequency modulated oscillator by two deviation frequency to spread the oscillator’s energy over a wide frequency band. There are two kinds of deviation frequencies (350 kHz and 700 kHz), which are decided by the SPI command (FM_amp). This spreading decreases the peak electromagnetic radiation level and improves electromagnetic compatibility (EMC) performance.

If preferred, the sequence following by SPI command (StopCLK2), and later on if decided to reactivate the CLK2 (clock monitoring re-activated), a reset clk can be generated due to the fact the clk2 re-start, and can have a settling time > 2*T2, 1.0 ms max. In this case, reset is detected during reset recovery time and the CLK_RST (reading message #0) flag should read in a normal condition.

6.6.1.5 Die temperature warning

The SB0410 has one temperature warning sensor in the cool place of the die. The threshold of temperature warning is 20 °C below overtemperature. In case of a temperature warning, outputs are not shutdown and the SPI-Bit shows the actual status at accessing time.

6.6.1.6 V_{PRE10}, V_{PRE12} undervoltage supervision

V_{PRE10} and V_{pre12} are internal regulator supplying power FET. These two voltage can be monitored through the SPI (Message 6 and 7). This voltage monitoring can be used as a additional fail safe function.

6.6.1.7 Ground supervision

GND-loss monitors the voltage between PGND (global reference GND) and GND_D. In case of a disconnection of GND_D vs. all other grounds (pin 2, 3, 6, 7, 10, 11, 14, 18, 30, 38, 43, 45, 47), and back side ground are soldered to ground), a detection GND_D disconnect as soon as the GND_D is higher than the threshold (V_GL) vs. others grounds, is reported through the flag FGND via the SPI register and set high after a filter time (t_{GL}).

1. Connection degraded (resistive path)
   A. GND_D vs other grounds > V_GL but by having Vint_D –GND_D > min voltage required
   B. SPI communication still possible, and the flag FGND will be at 1
2. Disconnection (open physically) during a sequence (in Normal mode), the logic embedded is frozen, because the voltage Vint_D – GND_D < min voltage required
   A. No SPI communication is possible
   B. If GND_D is reconnected normally, SPI communication recovers and the flag FGND is at 1

Table 19. Electrical characteristics

VPWR = 6.0 V to 36 V, VCC5 = 4.75 V to 5.25 V, DOSV = 3.13 V to 5.25 V, T_J = -40 °C to +125 °C, unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Reset output SB0410 to MCU						
t_{RSTB_REC}	Reset Recovery Time	-20%	45	20%	ms	
Reset input MCU to SB0410						
t_{RSTB_EXT}	External Reset Detection Filter time - Filter on falling of RSTB pin. Mask shorter glitch.	—	2.0	—	µs	
t_{RST_MIN}	Minimum External Reset Time (only for application)	—	10	—	ms	
DOSV undervoltage						
$DOSV_{UV\_3P3}$	Undervoltage Reset Threshold at Shutdown (falling edge of DOSV)	—	2.9	—	V	
t_{DVUV}	Undervoltage Reset Filter Time	—	T1	—	µs	
VCC5 undervoltage						
$VCC5_{UV}$	Undervoltage Threshold	—	4.5	—	V	
t_{VCUV}	Undervoltage Filter Time	—	T1	—	µs	
VCC5 supply						
I_{VCC5} I_{DOSV}	Consumption Current • VCC5 = 5.0 V; HD,PD = on; RSTB = high • During SPI communication	— —	20 10	— —	mA	
Internal logic supply						
Vint_A	Internal Analog Voltage - I_{LOAD} = -10 mA	2.30	2.5	2.8	V	
Vint_D	Internal Digital Voltage - I_{LOAD} = -10 mA	2.30	2.5	2.8	V	
C_Vint	Stabilization Capacitor at V_INT - Low-voltage capacitor (<4.0 V)	—	220	—	nF	
Internal logic supply undervoltage						
$Vint\_A_{UV}$ $Vint\_D_{UV}$	Undervoltage Reset threshold	—	2.1	—	V	
t_{VINT}	Undervoltage Reset Filter time	—	1.0	—	ms	
VPWR supply						
I_{VPWR}	Consumption current - VPWR = 36 V, HD, PD = on, RSTB = high	—	5.0	—	mA	
I_{STBY_VPWR}	Consumption current at sleep mode - VCC5 = DOSV = 0 V, HD_D = PD_D = VPWR = 36 V	—	2.0	20	µA	

Table 19. Electrical characteristics (continued)

VPWR = 6.0 V to 36 V, VCC5 = 4.75 V to 5.25 V, DOSV = 3.13 V to 5.25 V, T_J = -40 °C to +125 °C, unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VPWR & HD overvoltage						
$VPWR_{\_OV}$	VPWR Overvoltage Threshold (rising edge)	—	38	—	V	
$VPWR_{\_OV\_HYS}$	Overvoltage Detection Hysteresis - $VPWR_{\_OV(ON)} = VPWR_{\_OV(SHUTDOWN)} - VPWR_{\_OV\_HYS}$	—	0.6	1.0	V	
t_{VPWR_OV}	Overvoltage Detection Filter Time - Both directions	—	T2	—	µs	
VPWR undervoltage						
$VPWR_{\_UV}$	Undervoltage Shutdown Threshold (falling edge)	—	5.1	—	V	
$VPWR_{\_UV\_HYS}$	Undervoltage Detection Hysteresis - $VPWR_{\_OV(ON)} = VPWR_{\_OV(SHUTDOWN)} - VPWR_{\_OV\_HYS}$	30	100	200	mV	
t_{VPUV}	Undervoltage Detection Filter Time	—	T2	—	µs	
Ground-loss detection						
$V_{\_GL}$	GND_d-loss detection threshold - Reference GND_Px	—	0.5	—	V	
t_{GL}	GND_d-loss detection filter time - Reference GND_Px	—	T2	—	µs	
Oscillator						
$f_{\_OSC}$	Main Oscillator Frequency	-7.0%	14	7.0%	MHz	
e_{CLK}	Mismatch MAIN-AUX OSC CLK - enable V_{INT_X} is normal voltage digital comparison between the two clocks.	-35	±25	35	%	
t_{CLK}	Mismatch OSC Filter Time	T1	T2	2*T2	µs	(18)
	Frequency Modulation Band 1 - FM_amp = 0	-30%	350	30%	kHz	
	Frequency Modulation Band 2 - FM_amp = 1	-30%	700	30%	kHz	
	Frequency Modulation Speed	-30%	110	30%	kHz	
Overtemperature/temperature warning						
T_W	Temperature Warning Detection Threshold	150	165	180	°C	
t_{TW}	Temperature Warning Detection Filter Time	—	T2	—	µs	
Timing						
T1	Logic time base T1	14.4	18.2	22	µs	
T2	Logic time base T2	232	293	360	µs	

Notes

18. The t_{CLK} parameter is decided by a frequency checker and comparing two clocks. If either main clock or AUX clock frequency disappears longer than T1, the SB0410 goes to reset by the clock frequency checker and the CLK_RST flag will be detected. Meanwhile, comparing the main clock and AUX clock is done during T2 and the SB0410 is possible to go to reset every T2. Because measurement and reset activation are asynchronous, t_{CLK} can reach 2*T2 in the worst case by comparing two clocks.

Write 1 to any xxx_clr_flt register will create a reset of the fault flag during 1 clock period after the SPI message. xxx_clr_flt automatically goes to “0” after 1 clock from fault flag reset.

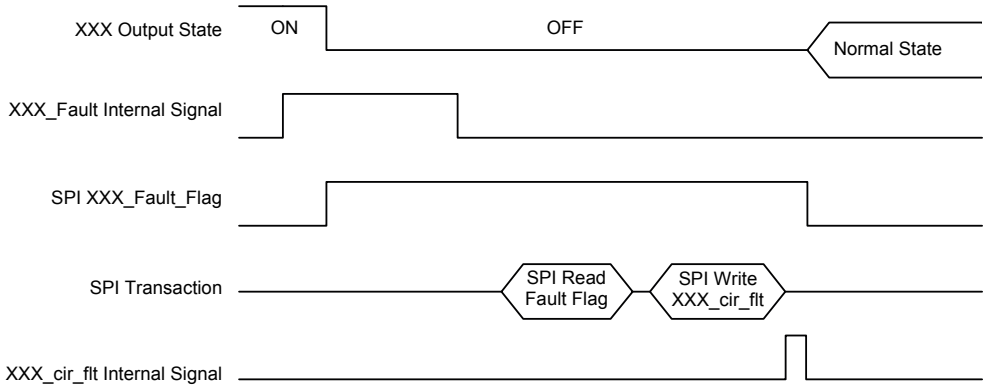


Figure 12. Timing diagram of xxx_clr_flt

6.7 SPI and data register

6.7.1 Function description

The SPI serial interface has the following features:

- Full duplex, four-wire synchronous communication
- Slave mode operation only
- Fixed SCLK polarity and phase requirements
- Fixed 16-bit command word
- SCLK operation up to 10.0 MHz

The Serial Peripheral Interface (SPI) is used to transmit and receive data synchronously with the MCU. Communication occurs over a full-duplex, four-wire SPI bus. The SB0410 device operates only as a slave device to the master, and requires four external pins; SI, SO, SCLK, and CSB. All words are 16 bits long and MSB is sent first.

The SPI simultaneously turns on the serial output SO and returns the MISO return bits. When receiving, valid data is latched on the rising edge of each SCLK pulse. The serial output data is available on the rising edge of SCLK, and transitions on the falling edge of SCLK. The number of clock cycles occurring on the pin SCLK while the CSB pin is asserted low must be 16. If the number of clock pulses is not 16 or a parity fault, the SPI MOSI data is ignored. The SB0410 takes even parity. On next data read SO message, “Fmsg” bit sets to 1, and other data bits sets to 0. The parity bit sets to 1. On the first SPI communication after reset, the read SO message sets to 1010101010101010.

The fault registers are double buffered. The first buffer layer latches a fault at the time the fault is detected. This inner layer buffer clears when the fault condition is no longer present and the fault bit communicates to the MCU by a MISO response. The second layer buffer latches the output of the inner layer buffer whenever the CSB pin transitions from low to high. The output of the second layer buffer is transferred to the shift register after the corresponding MOSI command is received from the MCU.

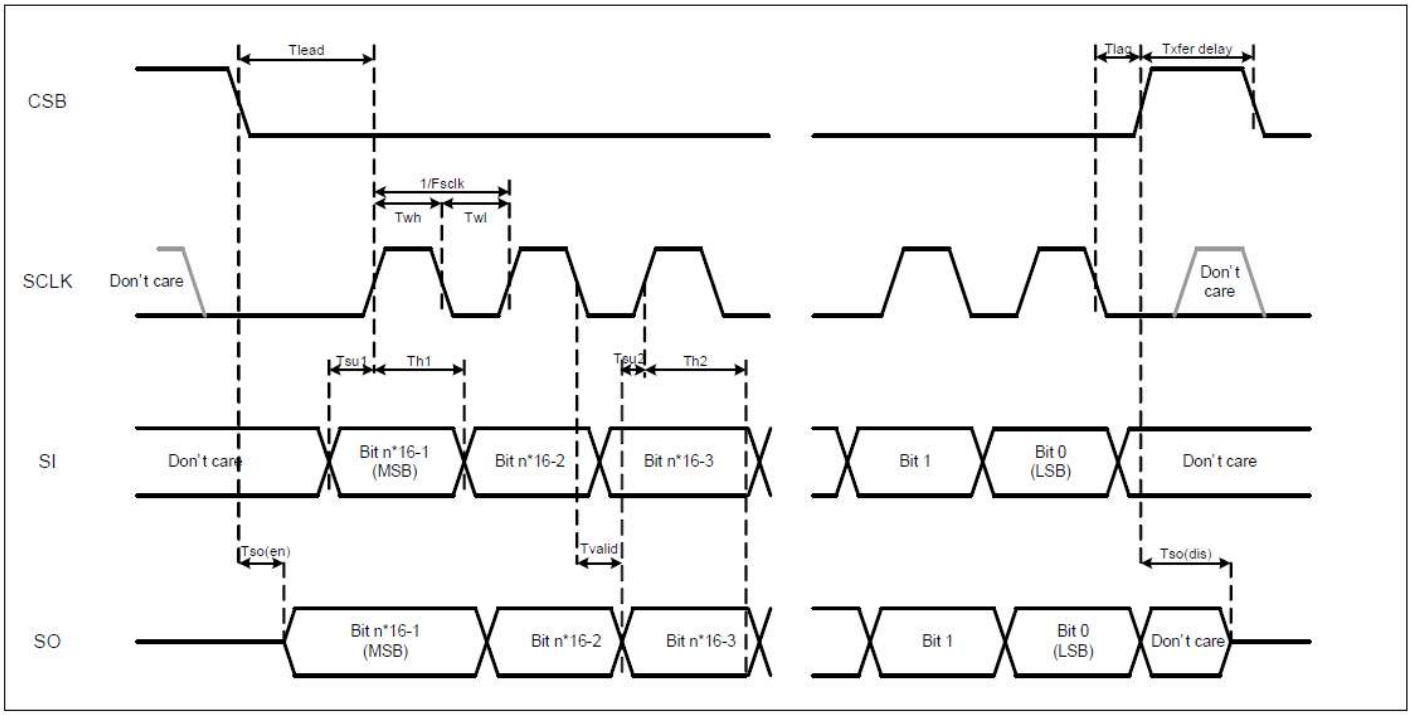


Figure 13. SPI timing diagram

Table 20. SPI timing electrical characteristics

VPWR = 6.0 V to 36 V, VCC5 = 4.75 V to 5.25 V, DOSV = 3.13 V to 5.25 V, T_J = -40 °C to 125 °C, unless otherwise specified.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
SPI interface timing [19]						
f_{SPI}	Recommended Frequency of SPI Operation - $t_{SPI} = 1/f_{SPI}$	—	—	10	MHz	
t_{LEAD}	Falling Edge of CSB to the Rising Edge of SCLK (required setup time)	30	$t_{SPI}/2$	50	ns	
t_{LAG}	Falling Edge of SCLK to the Rising Edge of CSB (required setup time)	30	$t_{SPI}/2$	50	ns	
t_{XFER_DELAY}	No Data Time Between SPI Commands	300	—	—	ns	
t_{WH}	High Time of SCLK	45	$t_{SPI}/2$	—	ns	
t_{WL}	Low Time of SCLK	45	$t_{SPI}/2$	—	ns	
t_{SU1}	SI to Rising Edge of SCLK (required setup time)	15	—	—	ns	
$t_{SO(EN)}$	Time from Falling Edge of CSB to SO Low-impedance	—	—	30	ns	
$t_{SO(DIS)}$	Time from Rising Edge of CSB to SO High-impedance	—	—	30	ns	
t_{VALID}	Time from Falling Edge of SCLK to SO Data_valid - 0.2xDOSV ≤ 0.8xDOSV, CL = 50 pF	0.0	—	30	ns	

Notes

19. The inputs of the SPI module (SCLK, CSB, SI) are driven between 0 V and DOSV voltage.

6.7.2 SPI message structure

Table 21. SPI message structure

addr #		Write										Read													
DEC	BIN	9	8	7	6	5	4	3	2	1	0	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	00000	0	0	0	0	0	0	0	OCM_pd	0	0	Version				dosv_uv	Vcc_uv	Vint_uv	RST_clk	RST_ext	X	X	X	X	X
1	00001	P charac				I charac			lsd_sink_dis	1	0	Manufacturing data				P charac				I charac			lsd_sink_dis	X	X
2	00010	Reserved																							
3	00011	0	0	0	0	FM_amp	FM_EN	StopCLK2	0	0	0	SB0410_CLK_CNT<7:0>								Vpwr_ov	X	Vpwr_uv	FGND	OTW	PD_ot
4	00100	0	0	Iclamp	didt	FDCL	LLC<1>	LLC<0>	CR_fb	CR_dis12	CR_dis34	PD_oc	CR_fb	CR_dis|12	CR_dis34	VINT_A<9:0>									
5	00101	0	0	0	0	0	0	0	0	LD2_on	LD_on	lsd1_crer	lsd2_crer	lsd3_crer	lsd4_crer	VINT_D<9:0>									
6	00110	0	0	0	0	0	0	LD2_clr_flt	LD_clr_flt	PD_clr_flt	LSD_clr_flt	ld_oc	ld_op	ld_ot	vds_ld	vpre10<9:0>									
7	00111	0	0	0	0	0	0	0	0	0	0	ld2_oc	ld2_op	ld2_ot	vds_ld2	vpre12<9:0>									
8	01000	0	0	0	0	0	0	0	0	0	0	X	X	X	X	Vgs_pd<9:0>									
9	01001	0	0	0	0	LF_PWM_14			0	0	0	X	X	X	X	TEMP<9:0>									
10	01010	LSD1 duty cycle (8-bit) or current set point (10-bit)										lsd1_oc	lsd1_op	lsd1_ot	vds_LSD1	LSD1 duty cycle (8bit) or current read (10 bit)									
11	01011	LSD2 duty cycle (8-bit) or current set point (10-bit)										lsd2_oc	lsd2_op	lsd2_ot	vds_LSD2	LSD2 duty cycle (8bit) or current read (10 bit)									
12	01100	LSD3 duty cycle (8-bit) or current set point (10-bit)										lsd3_oc	lsd3_op	lsd3_ot	vds_LSD3	LSD3 duty cycle (8bit) or current read (10 bit)									
13	01101	LSD4 duty cycle (8-bit) or current set point (10-bit)										lsd4_oc	lsd4_op	lsd4_ot	vds_LSD4	LSD4 duty cycle (8bit) or current read (10 bit)									
14	01110	0	0	0	0	0	0	0	0	0	0	X	X	X	X	AD_RST1<9:0>									
15	01111	0	0	0	0	0	0	0	0	0	0	X	X	X	X	AD_RST2<9:0>									
16	10000	0	0	0	0	0	0	0	0	0	0	X	X	X	X	AD_RST3<9:0>									

MSB(B15) of both write and read messages is parity bit, whereas only B14 of read message is Fmsg, which show previous write message fault.
The 'X' bit is used for tests manufacturing.

6.7.3 SPI message description

6.7.3.1 Message #0

Table 22. Write message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	MSG_ID					0	0	0	0	0	0	0	OCM_pd	0	0

Field	Bits	Description
P	15	Parity bit
MSG_ID	14: 10	Message Identifier: 00000
OCM_pd	02	Over current Masking time of Pump pre-driver selection

Table 23. Read message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	Fmsg	Version #				dosv_uv	Vcc_uv	Vint_uv	RST_clk	RST_ext	X	X	X	X	X

Field	Bits		Description
P	15	Parity bit	
Fmsg	14	Bit = 0	Previous transfer was valid
		Bit = 1	Parity bit is not correct. Error detected during previous transfer
Version #	13: 10	Version number is xxxx pass	
dosv_uv	09	Bit = 0	DOSV continues normal voltage
		Bit = 1	DOSV was less than DOSV undervoltage threshold longer than tDVUV
Vcc5 uv	08	Bit = 0	VCC5 continues normal voltage
		Bit = 1	VCC5 was less than VCC5_uv longer tVCUV
Vint uv	07	Bit = 0	Vint_D and Vint_A continues normal voltage
		Bit = 1	Vint_D or Vint_A voltage was low
RST_clk	06	Bit = 0	SB0410 internal clock is okay
		Bit = 1	SB0410 internal clock fault was detected.
RST_ext	05	Bit = 0	Normal
		Bit = 1	Reset from external (RSTB pin)

6.7.3.2 Message #1

Table 24. Write message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	MSG_ID					P charac				I charac			lsd_sink_dis	1	X

Field	Bits	Description	
P	15	Parity bit	
MSG_ID	14: 10	Message Identifier: 00001	
P charac	09: 06	BIT	P character
		0111	Factor of P-characteristic = 1.2188
		0110	Factor of P-characteristic = 1.1875
		0101	Factor of P-characteristic = 1.1562
		0100	Factor of P-characteristic = 1.125
		0011	Factor of P-characteristic = 1.0938
		0010	Factor of P-characteristic = 1.0625
		0001	Factor of P-characteristic = 1.0312
		1000	Factor of P-characteristic = 1
		0000	Factor of P-characteristic = 1
		1001	Factor of P-characteristic = 0.9688
		1010	Factor of P-characteristic = 0.9375
		1011	Factor of P-characteristic = 0.9062
		1100	Factor of P-characteristic = 0.875
		1101	Factor of P-characteristic = 0.8438
		1110	Factor of P-characteristic = 0.8125
		1111	Factor of P-characteristic = 0.7812
I charac	05: 03	001	Factor of I-characteristic = 0.25
		010	Factor of I-characteristic = 0.1875
		011	Factor of I-characteristic = 0.1562
		100	Factor of I-characteristic = 0.3125 (Imax)
		000	Factor of I-characteristic = 0.125 (default)
		101	Factor of I-characteristic = 0.0938
		110	Factor of I-characteristic = 0.0625
		111	Factor of I-characteristic = 0.0312
lsd_sink_dis	02	Bit = 0	LSD sink current for open detection is enabled (default mode)
		Bit = 1	LSD sink current for open detection is disabled

Table 25. Read message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	Fmsg	Manufacturing data				P charac				I charac			lsd_sink_dis	X	X

Field	Bits	Description	
P	15	Parity bit	
Fmsg	14	Bit = 0	Previous transfer was valid.
		Bit = 1	Parity bit is not correct. Error detected during previous transfer.
Manufacturing data	13: 10	Could be used for traceability (same as version #)	
P charac	09: 06	Feedback of P charac	
I charac	05: 03	Feedback of I charac	
lsd_sink_dis	02	Feedback of lsd_sink_dis	

6.7.3.3 Message #2

Reserved

6.7.3.4 Message #3

Table 26. Write message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	MSG_ID					0	0	0	0	FM_amp	FM_EN	Stop CLK 2	0	0	0

Field	Bits	Description	
P	15	Parity bit	
MSG_ID	14:10	Message Identifier: 00011	
FM_amp	05	Bit = 0	Frequency modulation band 1
		Bit = 1	Frequency modulation band 2
FM_EN	04	Bit = 0	Frequency of Main/Aux oscillator clocks is fixed
		Bit = 1	Frequency of Main/Aux oscillator clocks is modulated by the frequency defined by FM_amp
StopCLK2	03	Bit = 0	SB0410 internal clock monitoring function is enabled
		Bit = 1	SB0410 internal clock monitoring function is disabled

Table 27. Read message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	Fmsg	SB0410_CLK_CNT<7:0>								Vpwr ov	X	Vpwr uv	FGND	OTW	PD_ot

Field	Bits	Description	
P	15	Parity bit	
Fmsg	14	Bit = 0	Parity bit is correct. Previous transfer was valid.
		Bit = 1	Parity bit is not correct. Error detected during previous transfer.
SB0410_CLK_CNT<7:0>	13: 06	Monitoring result from SB0410 internal clock(?)	
Vpwr_ov	05	Bit = 0	Normal
		Bit = 1	VPWR overvoltage
Vpwr_uv	03	Bit = 0	Normal
		Bit = 1	VPWR undervoltage
FGND	02	Bit = 0	Normal
		Bit = 1	GND _D loss detection
OTW	01	Bit = 0	Normal
		Bit = 1	Overtemperature warning
PD_ot	00	Bit = 0	Normal
		Bit = 1	Overtemperature warning on the motor pump pre-driver

6.7.3.5 Message #4

Table 28. Write message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	MSG_ID					0	0	Iclamp	didt	FDCL	LLC <1>	LLC <0>	CR_fb	CR_dis 12	CR_dis 34

Field	Bits	Description
P	15	Parity bit
MSG_ID	14: 10	Message Identifier: 00100
Iclamp	07	Bit = 0 Integrator limit is 0x03FF
		Bit = 1 Integrator limit is 0x07FF
didt	06	Bit = 0 Rise / Fall time of LSD is long (tr/tf_CR1)
		Bit = 1 Rise / Fall time of LSD is short (tr/tf_CR2)
FDCL	05	Bit = 0 The first duty cycle is controlled by current
		Bit = 1 First duty cycle from off state to a target value is limited to a fixed duty cycle. (Fixed value is the duty cycle which a target current is transformed in duty cycle, lowest value is 10%)

LLC	04:03	Bit = 00	Minimum duty cycle (DC) is 10% The measurement is done at Ton/2	
		Bit = 01	Minimum duty cycle (DC) is 3.12% For DC > 10%, the measurement is done at Ton/2. For 3.12% < DC < 10%, the measurement is done at the maximum value between Ton/2 and 3.12%	
		Bit = 10	Bit = 10 Minimum duty cycle (DC) is: 3.12% + 1.56% every two cycles For DC > 10%, the measurement is done at Ton/2. For 3.12% < DC < 10% the regulation current approach up to 3.12% of DC and the measurement is done at the maximum value between Ton/2 and 3.12% For 1.56% < DC < 3.12%, 3.12% of DC and 1.56%. DC are forced every two cycles and no measurement is done during 1.56% of DC.	
		Bit = 11	Minimum duty cycle (DC) is: 3.12% + skipping DC every two cycles For DC > 10%, the measurement is done at Ton/2. For 3.12% < DC < 10% the regulation current approach up to 3.12% of DC and the measurement is done at the maximum value between Ton/2 of DC and 3.12% For DC < 3.12%, the regulation current forces 3.12% and skipping every two cycles and no measurement is done during the skipping mode.	
CR_fb	02	Bit = 0	LSDx Feedback = SPI written value	
		Bit = 1	LSDx Feedback = output	
			CR_fb = 0	CR_fb = 1
CR_dis12	01	CR_dis12 = 0	LSD1,2 Current regulation	LSD1,2 Current regulation
		CR_dis12 = 1	LSD1,2 PWM	LSD1,2 PWM
CR_dis34	00	CR_dis34 = 0	LSD3,4 Current regulation	LSD3,4 Current regulation
		CR_dis34 = 1	LSD3,4 PWM	LSD3,4 PWM

Table 29. Read message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	Fmsg	PD_oc	CR_fb	CR_dis 12	CR_dis 34	VINT_A<9:0>									

Field	Bits	Description	
P	15	Parity bit	
Fmsg	14	Bit = 0	Parity bit is correct. Previous transfer was valid.
		Bit = 1	Parity bit is not correct. Error detected during previous transfer.
PD_oc	13	Bit = 0	Normal
		Bit = 1	Over current detected on the motor pump pre-driver
CR_fb	12	Feedback of CR_fb	
CR_dis12	11	Feedback of CR_dis12	
CR_dis34	10	Feedback of CR_dis34	
VINT_A<9:0>	09:00	10-bit ADC of Analog internal supply	

6.7.3.6 Message #5

Table 30. Write message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	MSG_ID					0	0	0	0	0	0	0	0	LD2_on	LD_on

Field	Bits	Description	
P	15	Parity bit	
MSG_ID	14: 10	Message Identifier: 00101	
LD2_on	01	Bits = 0	Low-side is off
		Bits = 1	Low-side turn on
LD_on	00	Bits = 0	Low-side is off
		Bits = 1	Low-side turn on

Table 31. Read message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	Fmsg	lsd1_ crer	lsd2_ crer	lsd3_ crer	lsd4_ crer	VINT_D<9:0>									

Field	Bits	Description	
P	15	Parity bit	
Fmsg	14	Bit = 0	Parity bit is correct. Previous transfer was valid.
		Bit = 1	Parity bit is not correct. Error detected during previous transfer.
lsd1_crer	13	Bit = 0	Normal
		Bit = 1	Current regulation error detection of LSD1
lsd2_crer	12	Bit = 0	Normal
		Bit = 1	Current regulation error detection of LSD2
lsd3_crer	11	Bit = 0	Normal
		Bit = 1	Current regulation error detection of LSD3
lsd4_crer	10	Bit = 0	Normal
		Bit = 1	Current regulation error detection of LSD4
VINT_D<9:0>	09:00	10-bit ADC internal supply	

6.7.3.7 Message #6

Table 32. Write message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	MSG_ID					0	0	0	0	0	0	0	LD_ clr_flt	PD_ clr_flt	LSD_ clr_flt

Field	Bits	Description	
P	15	Parity bit	
MSG_ID	14: 10	Message Identifier: 00110	
LD2_clr_flt	03	Bit = 0	LD_oc and LD_ot are conserved (default mode)
		Bit = 1	Clear LD_oc and LD_ot
LD_clr_flt	02	Bit = 0	LD_oc and LD_ot are conserved (default mode)
		Bit = 1	Clear LD_oc and LD_ot
PD_clr_flt	01	Bit = 0	PD_oc is conserved (default mode)
		Bit = 1	Clear PD_oc
LSD_clr_flt	00	Bit = 0	All LSDx_oc and LSDx_ot are conserved (default mode)
		Bit = 1	Clear All LSDx_oc and LSDx_ot

Table 33. Read message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	Fmsg	ld_oc	ld_op	ld_ot	vds_ld	vpre10<9:0>									

Field	Bits	Description	
P	15	Parity bit	
Fmsg	14	Bit = 0	Parity bit is correct. Previous transfer was valid.
		Bit = 1	Parity bit is not correct. Error detected during previous transfer.
ld_oc	13	Bit = 0	Normal
		Bit = 1	Overcurrent shut down of low-side
ld_op	12	Bit = 0	Normal
		Bit = 1	Open load detection of low-side
ld_ot	11	Bit = 0	Normal
		Bit = 1	Overtemperature shut down of low-side
vds_ld	10	Bit = 0	Normal
		Bit = 1	Vds detection of low-side (information only)
vpre10<9:0>	09:00	10-bit ADC of vpre10	

6.7.3.8 Message #7

Table 34. Write message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	MSG_ID					0	0	0	0	0	0	0	0	0	0

Field	Bits	Description
P	15	Parity bit
MSG_ID	14: 10	Message Identifier: 00111

Table 35. Read message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	Fmsg	ld2_oc	ld2_op	ld2_ot	vds_ld2	vpre12<9:0>									

Field	Bits	Description	
P	15	Parity bit	
Fmsg	14	Bit = 0	Parity bit is correct. Previous transfer was valid.
		Bit = 1	Parity bit is not correct. Error detected during previous transfer.
ld2_oc	13	Bit = 0	Normal
		Bit = 1	Overcurrent shut down of low-side
ld2_op	12	Bit = 0	Normal
		Bit = 1	Open load detection of low-side
ld2_ot	11	Bit = 0	Normal
		Bit = 1	Overtemperature shut down of low-side
vds_ld	10	Bit = 0	Normal
		Bit = 1	Vds detection of low-side (information only)
vpre12<9:0>	09:00	10-bit ADC of vpre12	

6.7.3.9 Message #8

Table 36. Write message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	MSG_ID					0	0	0	0	0	0	0	0	0	0

Field	Bits	Description
P	15	Parity bit
MSG_ID	14: 10	Message Identifier: 01000

Table 37. Read message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	Fmsg	X	X	X	X	vgs_pd<9:0>									

Field	Bits	Description	
P	15	Parity bit	
Fmsg	14	Bit = 0	Parity bit is correct. Previous transfer was valid.
		Bit = 1	Parity bit is not correct. Error detected during previous transfer.
vgs_pd<9:0>	09:00	10-bit ADC of vgs_pd	

6.7.3.10 Message #9

Table 38. Write message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	MSG_ID					0	0	0	0	LF_PWM_14			0	0	0

Field	Bits	Description	
P	15	Parity bit	
MSG_ID	14: 10	Message Identifier: 01001	
LF_PWM_14	05:03	Bit = 000	Output PWM frequency of LSD(1~4)= 3.9 kHz
		Bit = 001	Output PWM frequency of LSD(1~4)= 4.5 kHz
		Bit = 010	Output PWM frequency of LSD(1~4)= 5.0 kHz
		Bit = 011	Output PWM frequency of LSD(1~4)= 4.2 kHz
		Bit = 100	Output PWM frequency of LSD(1~4)= 3.6 kHz
		Bit = 101	Output PWM frequency of LSD(1~4)= 3.4 kHz
		Bit = 110	Output PWM frequency of LSD(1~4)= 3.2 kHz
		Bit = 111	Output PWM frequency of LSD(1~4)= 3.0 kHz

Table 39. Read message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	Fmsg	X	X	X	X	TEMP<9:0>									

Field	Bits	Description	
P	15	Parity bit	
Fmsg	14	Bit = 0	Parity bit is correct. Previous transfer was valid.
		Bit = 1	Parity bit is not correct. Error detected during previous transfer.
TEMP<9:0>	09:00	10-bit ADC of average die temperature	

6.7.3.11 Message #10

Table 40. Write message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	MSG_ID					LSD1 duty cycle (8-bit) or current set point (10-bit)									

Field	Bits	Description		
P	15	Parity bit		
MSG_ID	14: 10	Message Identifier: 01010		
LSD1 duty cycle (8-bit) or current set point(10-bit)	09:00		CR_fb=0	CR_fb=1
		CR_dis12= 0	LSD1, 2 current regulation Write current target (10 bits, 0 to 2.25 A)	LSD1,2 current regulation Write current target (10 bits, 0 to 2.25 A)
		CR_dis12= 1	LSD1, 2 PWM Write programmed duty cycle (8 bits at 0%, 100% and 10% to 90%) LSD1[1:0]=XX	LSD1,2 PWM Write programmed duty cycle (8 bits at 0%, 100% and 10% to 90%) LSD1[1:0]=XX

Table 41. Read message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	Fmsg	lsd1_ oc	lsd1_op	lsd1_ot	vds_ LSD1	LSD1 duty cycle (8-bit) or current read (10-bit)									

Field	Bits	Description		
P	15	Parity bit		
Fmsg	14	Bit = 0	Parity bit is correct. Previous transfer was valid.	
		Bit = 1	Parity bit is not correct. Error detected during previous transfer.	
lsd1_ oc	13	Bit = 0	Normal	
		Bit = 1	Overcurrent shutdown of LSD1	
lsd1_op	12	Bit = 0	Normal	
		Bit = 1	Open Load detection of LSD1	
lsd1_ot	11	Bit = 0	Normal	
		Bit = 1	Overtemperature shutdown of LSD1	
vds_LSD1	10	Bit = 0	Normal	
		Bit = 1	V_{DS} detection of LSD1 (information only)	
LSD1 duty cycle (8-bit) or current read (10-bit)	09:00		CR_fb=0	CR_fb=1
		CR_dis12= 0	LSD1,2 current regulation Read current target (to check SPI write) (10 bits, 0 to 2.25 A)	LSD1,2 current regulation Output duty cycle value for gate driver (8 bits, for the range to 100%)
		CR_dis12= 1	LSD1,2 PWM Read programmed PWM duty cycle (to check SPI write) (8 bits at 0%, 100% and 10% to 90%) LSD(1~2)[1:0]=00	LSD1,2 PWM Read hardware ADC current value (10 bits for the range to 4.5A)

6.7.3.12 Message #11

Table 42. Write message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	MSG_ID					LSD2 duty cycle (8bit) or current set point (10-bit)									

Field	Bits	Description		
P	15	Parity bit		
MSG_ID	14: 10	Message Identifier: 01011		
LSD2 duty cycle (8-bit) or current set point(10-bit)	09:00		CR_fb=0	CR_fb=1
		CR_dis12= 0	LSD1,2 current regulation Write current target (10 bits, 0 to 2.25 A)	LSD1,2 current regulation Write current target (10 bits, 0 to 2.25 A)
		CR_dis12= 1	LSD1,2 PWM Write programmed duty cycle (8 bits at 0%, 100% and 10% to 90%) LSD2[1:0]=XX	LSD1,2 PWM Write programmed duty cycle (8 bits at 0%, 100% and 10% to 90%) LSD2[1:0]=XX

Table 43. Read message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	Fmsg	lsd2_ oc	lsd2_op	lsd2_ot	vds_LSD2	LSD2 duty cycle (8-bit) or current read (10-bit)									

Field	Bits	Description		
P	15	Parity bit		
Fmsg	14	Bit = 0	Parity bit is correct. Previous transfer was valid.	
		Bit = 1	Parity bit is not correct. Error detected during previous transfer.	
lsd2_ oc	13	Bit = 0	Normal	
		Bit = 1	Overcurrent shutdown of LSD2	
lsd2_op	12	Bit = 0	Normal	
		Bit = 1	OpenLoad detection of LSD2	
lsd2_ot	11	Bit = 0	Normal	
		Bit = 1	Overtemperature shutdown of LSD2	
vds_LSD2	10	Bit = 0	Normal	
		Bit = 1	V_{DS} detection of LSD2 (information only)	
LSD2 duty cycle (8-bit) or current read (10-bit)	09:00		CR_fb = 0	CR_fb=1
		CR_dis12= 0	LSD1,2 current regulation Read current target (to check SPI write) (10 bits, 0 to 2.25 A)	LSD1,2 current regulation Output duty cycle value for gate driver (8 bits, for the range to 100%)
		CR_dis12= 1	LSD1,2 PWM Read programmed PWM duty cycle (to check SPI write) (8 bits at 0%, 100% and 10% to 90%) LSD(1~2)[1:0]=00	LSD1,2 PWM Read hardware ADC current value (10 bits for the range to 4.5 A)

6.7.3.13 Message #12

Table 44. Write message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	MSG_ID					LSD3 duty cycle (8-bit) or current set point (10-bit)									

Field	Bits	Description		
P	15	Parity bit		
MSG_ID	14: 10	Message Identifier: 01100		
LSD3 duty cycle (8-bit) or current set point(10-bit)	09:00		CR_fb=0	CR_fb=1
		CR_dis34= 0	LSD3,4 current regulation Write current target (10 bits, 0 to 2.25 A)	LSD3,4 current regulation Write current target (10 bits, 0 to 2.25 A)
		CR_dis34= 1	LSD3,4 PWM Write programmed duty cycle (8 bits at 0%, 100% and 10% to 90%) LSD3[1:0]=XX	LSD3,4 PWM Write programmed duty cycle (8 bits at 0%, 100% and 10% to 90%) LSD3[1:0]=XX

Table 45. Read message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	Fmsg	lsd3_ oc	lsd3_ op	lsd3_ot	vds_ LSD3	LSD3 duty cycle (8-bit) or current read (10-bit)									

6.7.3.14 Message #13

Table 46. Write message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	MSG_ID					LSD4 duty cycle (8-bit) or current set point (10-bit)									

Field	Bits	Description		
P	15	Parity bit		
MSG_ID	14: 10	Message Identifier: 01101		
LSD4 duty cycle (8-bit) or current set point (10-bit)	09:00		CR_fb=0	CR_fb=1
		CR_dis34= 0	LSD3, 4 current regulation Write current target (10 bits for the range to 2.25 A)	LSD3, 4 current regulation Write current target (10 bits for the range to 2.25 A)
		CR_dis34= 1	LSD3,4 PWM Write programmed duty cycle (8 bits for the range to 100%) LSD4[1:0]=XX	LSD3, 4 PWM Write programmed duty cycle (8 bits for the range to 100%) LSD4[1:0]=XX

Read message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	Fmsg	lsd4_ oc	lsd4_op	lsd4_ot	vds_LSD4	LSD4 duty cycle (8-bit) or current read (10-bit)									

Field	Bits	Description		
P	15	Parity bit		
Fmsg	14	Bit = 0	Parity bit is correct. Previous transfer was valid.	
		Bit = 1	Parity bit is not correct. Error detected during previous transfer.	
lsd4_ oc	13	Bit = 0	Normal	
		Bit = 1	Overcurrent shutdown of LSD4	
lsd4_op	12	Bit = 0	Normal	
		Bit = 1	OpenLoad detection of LSD4	
lsd4_ot	11	Bit = 0	Normal	
		Bit = 1	Overtemperature shutdown of LSD4	
vds_LSD4	10	Bit = 0	Normal	
		Bit = 1	V_{DS} detection of LSD4 (information only)	
LSD4 duty cycle (8-bit) or current read (10-bit)	09:00		CR_fb=0	CR_fb=1
		CR_dis34= 0	LSD3,4 current regulation Read current target (to check SPI write) (10 bits, 0 to 2.25 A)	LSD3,4 current regulation Output duty cycle value for gate driver (8 bits, for the range to 100%)
		CR_dis34= 1	LSD3,4 PWM Read programmed PWM duty cycle (to check SPI write) (8 bits at 0%, 100% and 10% to 90%) LSD(3~4)[1:0]=00	LSD3,4 PWM Read hardware ADC current value (10 bits for the range to 4.5 A)

6.7.3.15 Message #14

Table 47. Write message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	MSG_ID					0	0	0	0	0	0	0	0	0	0

Field	Bits	Description
P	15	Parity bit
MSG_ID	14: 10	Message Identifier: 01110

Read message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	Fmsg	x	x	x	x	AD_RST1<9:0>									

Field	Bits	Description	
P	15	Parity bit	
Fmsg	14	Bit = 0	Parity bit is correct. Previous transfer was valid.
		Bit = 1	Parity bit is not correct. Error detected during previous transfer.
AD_RST1<9:0>	09:00	10-bit ADC of ADIN1	AD_RST1<9:0>

6.7.3.16 Message #15

Table 48. Write message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	MSG_ID					0	0	0	0	0	0	0	0	0	0

Field	Bits	Description
P	15	Parity bit
MSG_ID	14: 10	Message Identifier: 01111

Read message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	Fmsg	x	x	x	x	AD_RST2<9:0>									

Field	Bits	Description	
P	15	Parity bit	
Fmsg	14	Bit = 0	Parity bit is correct. Previous transfer was valid.
		Bit = 1	Parity bit is not correct. Error detected during previous transfer.
AD_RST2<9:0>	09:00	10-bit ADC of ADIN2	AD_RST2<9:0>

6.7.3.17 Message #16

Table 49. Write message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	MSG_ID					0	0	0	0	0	0	0	0	0	0

Field	Bits	Description
P	15	Parity bit
MSG_ID	14: 10	Message Identifier: 10000

Read message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	Fmsg	x	x	x	x	AD_RST3<9:0>									

Field	Bits	Description	
P	15	Parity bit	
Fmsg	14	Bit = 0	Parity bit is correct. Previous transfer was valid.
		Bit = 1	Parity bit is not correct. Error detected during previous transfer.
AD_RST3<9:0>	09:00	10-bit ADC of ADIN3	AD_RST3<9:0>

7 Typical applications

7.1 Application diagrams

This section presents a typical Industrial applications schematic using SB0410, as shown in Figure 14.

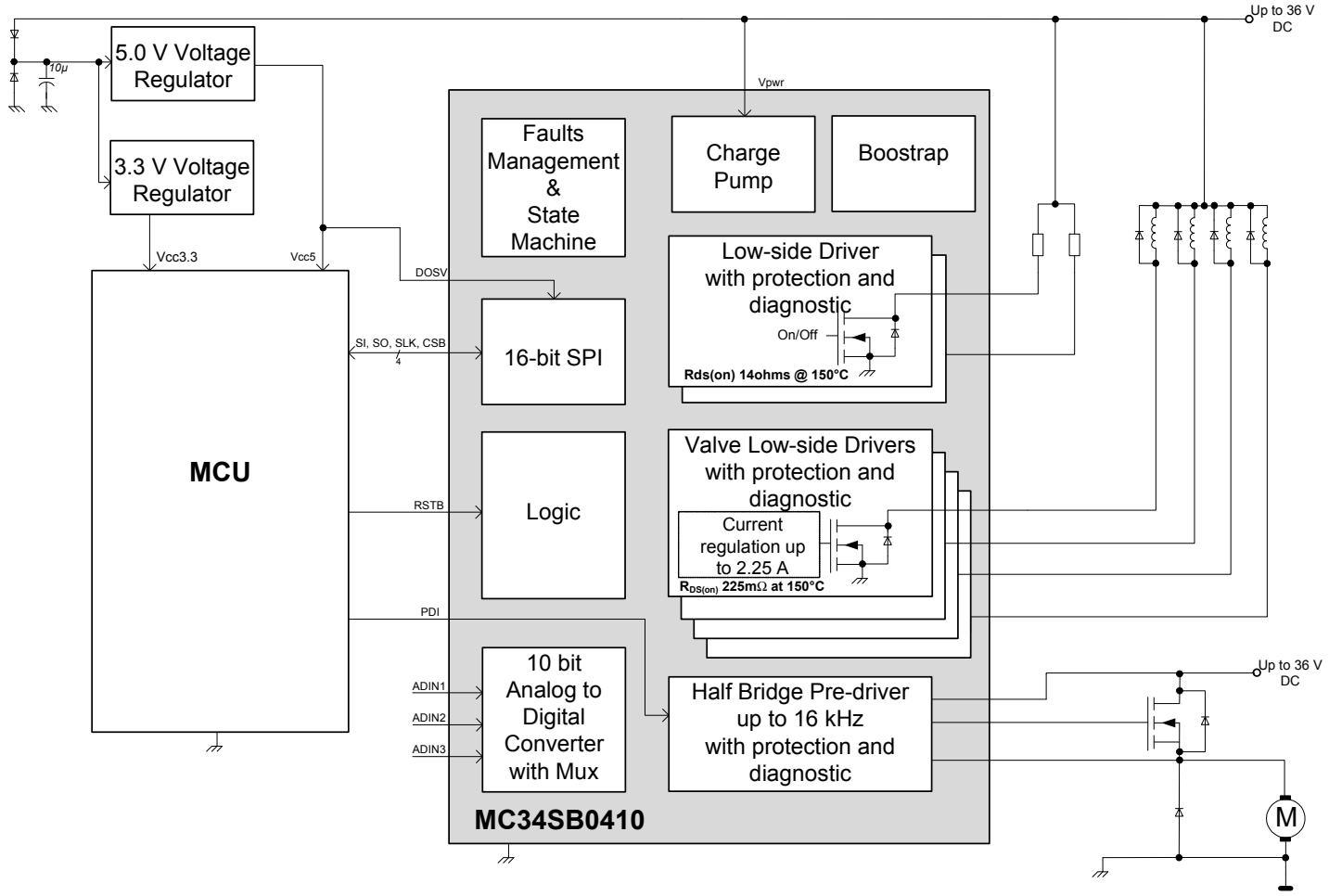


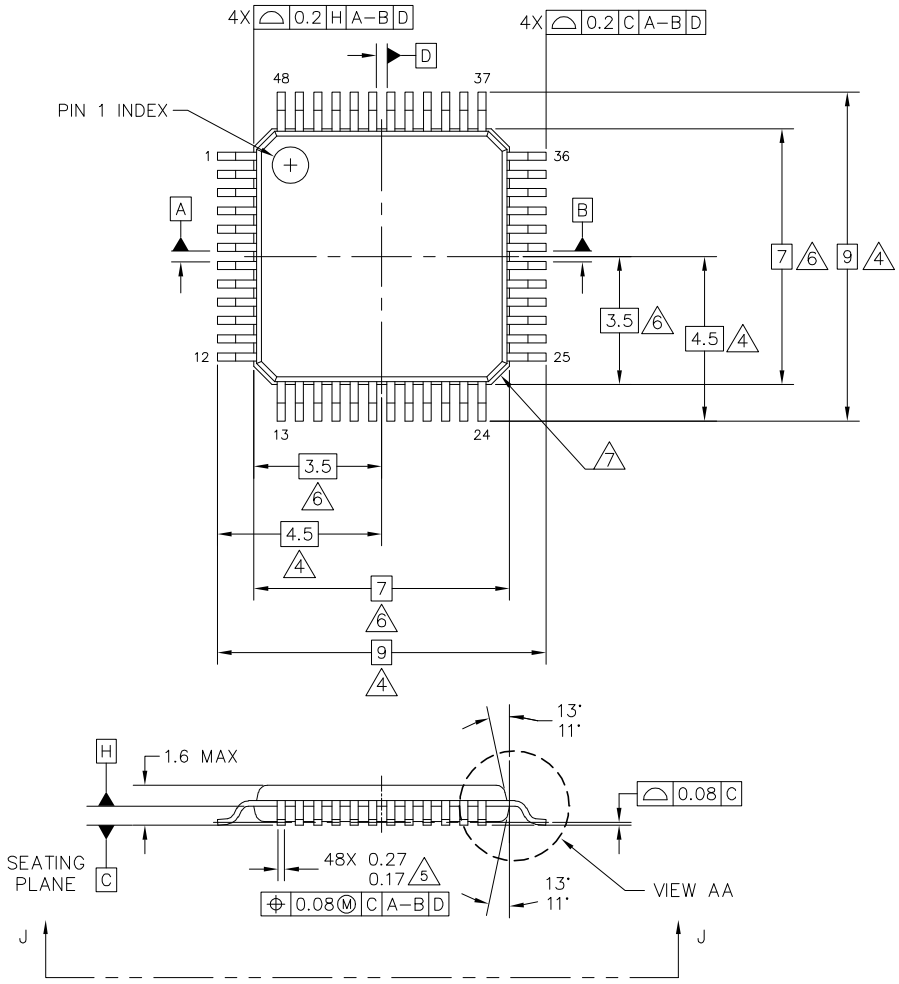
Figure 14. Industrial valves and pump control unit simplified diagram

8 Packaging

8.1 Package mechanical dimensions

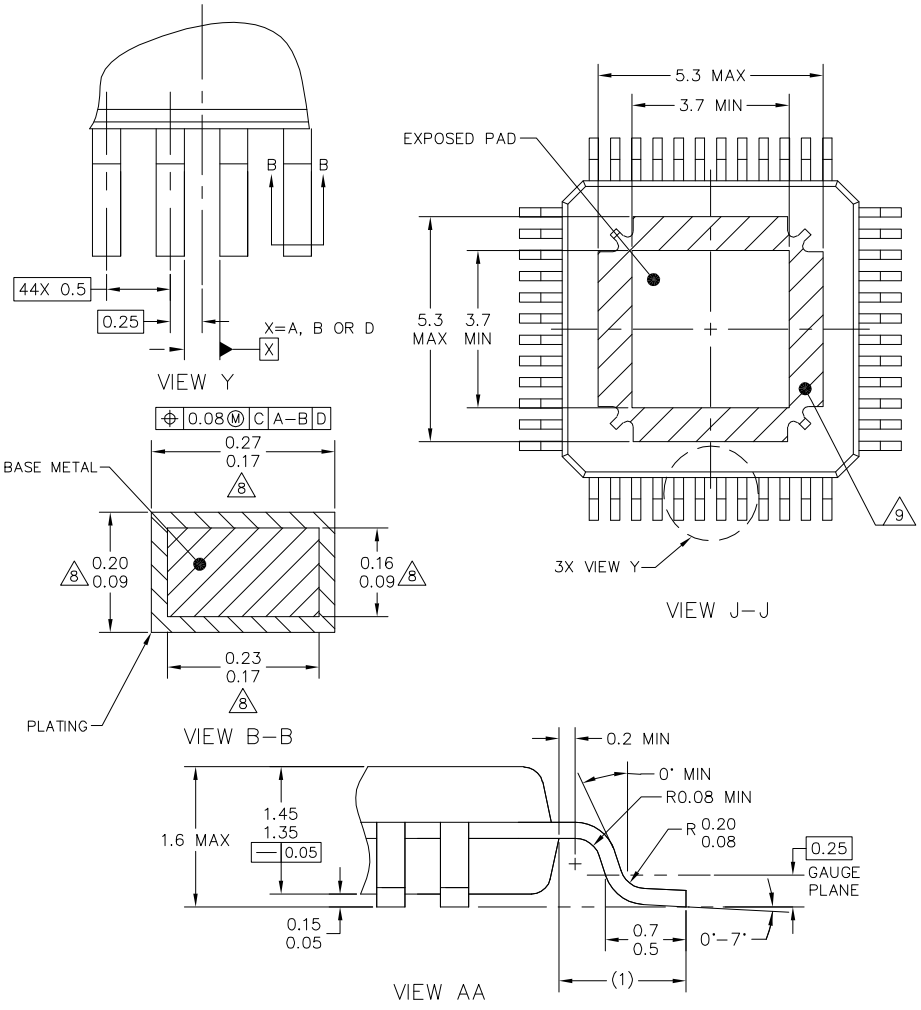
Package dimensions are provided in package drawings. To find the most current package outline drawing, go to www.nxp.com and perform a keyword search for the drawing's document number.

Package	Suffix	Package outline drawing number
7 x 7, 48-Pin LQFP Exposed Pad, with 0.5 mm pitch, and a 4.5 x 4.5 exposed pad	AE	98ASA00173D



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 48 LEAD LQFP, 7X7X1.4 PKG, 0.5 PITCH, 4.5X4.5 EXPOSED PAD	DOCUMENT NO: 98ASA00173D	REV: A
	CASE NUMBER: 2003–02	30 JUN 2011
	STANDARD: JEDEC MS–026 BBC	

SB0410



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 48 LEAD LQFP, 7X7X1.4 PKG, 0.5 PITCH, 4.5X4.5 EXPOSED PAD	DOCUMENT NO: 98ASA00173D	REV: A
	CASE NUMBER: 2003-02	30 JUN 2011
	STANDARD: JEDEC MS-026 BBC	

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSION TO BE DETERMINED AT SEATING PLANE C.
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08MM AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07MM.
6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25MM PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1MM AND 0.25MM FROM THE LEAD TIP.
9. HATCHED AREA TO BE KEEP OUT ZONE FOR PCB ROUTING.

	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: 48 LEAD LQFP, 7X7X1.4 PKG, 0.5 PITCH, 4.5X4.5 EXPOSED PAD	DOCUMENT NO: 98ASA00173D		REV: A
	CASE NUMBER: 2003–02		30 JUN 2011
	STANDARD: JEDEC MS–026 BBC		

9 Revision history

Revision	Date	Description of changes
1.0	11/2014	• Initial release
2.0	4/2015	• Changed document status to Advance Information. • Changed MC to PC in Orderable part variations
	5/2015	• Updated document title
3.0	5/2015	• Updated Table 21, Table 30, Table 32, and Table 33
	8/2016	• Updated to NXP document form and style

How to Reach Us:

Home Page:
NXP.com

Web Support:
http://www.nxp.com/support

Document Number: MC34SB0410
Rev. 3.0
8/2016