New Product



SiA920DJ

RoHS

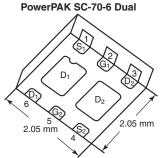
COMPLIANT

HALOGEN FREE

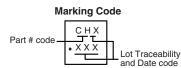
Vishay Siliconix

Dual N-Channel 8 V (D-S) MOSFET

PRODUCT SUMMARY					
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^a	Q _g (Typ.)		
8	0.027 at V _{GS} = 4.5 V	4.5			
	0.031 at V _{GS} = 2.5 V	4.5			
	0.036 at Vgs = 1.8 V	4.5	4.8 nC		
	0.047 at Vgs = 1.5 V	4.5			
	0.110 at Vgs = 1.2 V	1.5			



Ordering Information: SiA920DJ-T1-GE3 (Lead (Pb)-free and Halogen-free)

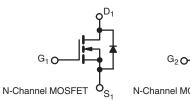


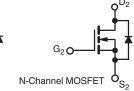
FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET[®] Power MOSFET
- Thermally Enhanced PowerPAK® SC-70 Package
 - Small Footprint Area
 - Low On-Resistance
- 100 % Rg Tested
- Compliant to RoHS Directive 2002/95/EC

APPLICATIONS

- Load Switch with Low Voltage Drop
- Load Switch for 1.2 V/1.5 V/1.8 V Power Lines
- Smart Phones, Tablet PCs, Portable Media Players





ABSOLUTE MAXIMUM RATIN	IGS (T _A = 25 °C	, unless othe	erwise noted)	
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V _{DS}	8	V
Gate-Source Voltage		V _{GS}	± 5	v
	T _C = 25 °C		4.5 ^a	
Continuous Drain Current ($T_1 = 150 \ ^{\circ}C$)	T _C = 70 °C	L	4.5 ^a	
Continuous Drain Current (1) = 150°C)	T _A = 25 °C		4.5 ^{a, b, c}	
	T _A = 70 °C		4.5 ^{a, b, c}	A
Pulsed Drain Current (t = 300 µs)		I _{DM}	20	
Continuous Source-Drain Diode Current	T _C = 25 °C		4.5 ^a	
	T _A = 25 °C	۱ _S	1.6 ^{b, c}	
	T _C = 25 °C	P _D	7.8	
Maximum Power Dissipation	T _C = 70 °C		5	w
Maximum Power Dissipation	T _A = 25 °C	U'U	1.9 ^{b, c}	VV
	T _A = 70 °C		1.2 ^{b, c}	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150	℃
Soldering Recommendations (Peak Temperature) ^{d, e}		Ĭ	260	U

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit		
Maximum Junction-to-Ambient ^{b, f}	t ≤ 5 s	R _{thJA}	52	65	°C/W		
Maximum Junction-to-Case (Drain)	Steady State	R _{thJC}	12.5	16	7 0/10		
Notoo:							

a. Package limited

b. Surface mounted on 1" x 1" FR4 board.

C. t = 5 s.

d. See solder profile (<u>www.vishay.com/doc?73257</u>). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

Rework conditions: manual soldering with a soldering iron is not recommended for leadless components. e.

Maximum under steady state conditions is 110 °C/W. f.

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SPECIFICATIONS ($T_J = 25 \text{ °C}$, Parameter	Symbol	Test Conditions	Min.	Turn	Max.	Unit
Static	Symbol	Test conditions	IVIII.	Тур.	wax.	Unit
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	8			V
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$		0	11		mV/°C
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	l _D = 250 μA		- 2.3		
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_{D} = 250 \ \mu A$	0.35	2.0	0.7	V
Gate-Source Leakage		$V_{DS} = 0 V, V_{GS} = \pm 5 V$	0.00		± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = 8 V, V_{GS} = 0 V$			1 1	
		$V_{DS} = 8 V, V_{GS} = 0 V, T_J = 55 °C$			10	μA
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 V, V_{GS} = 4.5 V$	10			А
	'D(on)	$V_{GS} = 4.5 \text{ V}, \text{ I}_{D} = 5.3 \text{ A}$		0.022	0.027	Ω
		$V_{GS} = 2.5 \text{ V}, \text{ I}_{D} = 4.9 \text{ A}$		0.025	0.031	
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = 1.8 \text{ V}, \text{ I}_{D} = 4.6 \text{ A}$		0.029	0.036	
	20(01)	$V_{GS} = 1.5 \text{ V}, \text{ I}_{D} = 1.5 \text{ A}$		0.035	0.047	
		$V_{GS} = 1.2 \text{ V}, \text{ I}_{D} = 0.5 \text{ A}$		0.050	0.110	
Forward Transconductance ^a	9 _{fs}	$V_{DS} = 10 \text{ V}, \text{ I}_{D} = 5.3 \text{ A}$		28		S
Dynamic ^b						
Input Capacitance	C _{iss}			470		pF
Output Capacitance	C _{oss}	V _{DS} = 4 V, V _{GS} = 0 V, f = 1 MHz		175		
Reverse Transfer Capacitance	C _{rss}			85		
Total Gate Charge	Qg			4.8	7.5	nC
Gate-Source Charge	Q _{gs}	$V_{DS} = 4 V, V_{GS} = 4.5 V, I_{D} = 6.9 A$		0.63		
Gate-Drain Charge	Q _{gd}			0.6		
Gate Resistance	R _g	f = 1 MHz	0.8	4	8	Ω
Turn-On Delay Time	t _{d(on)}			5	10	
Rise Time	t _r			12	25	- ns
Turn-Off Delay Time	t _{d(off)}	$V_{DD} = 10 \text{ V}, \text{ R}_{L} = 1.9 \Omega$		20	40	
Fall Time	t _f	$I_{D} \cong 5.5 \text{ A}, \text{ V}_{\text{GEN}} = 4.5 \text{ V}, \text{ R}_{\text{g}} = 1 \Omega$		7	15	
Drain-Source Body Diode Characteristic	s			<u> </u>		
Continuous Source-Drain Diode Current	۱ _S	T _C = 25 °C			4.5	•
Pulse Diode Forward Current	I _{SM}				20	A
Body Diode Voltage	V _{SD}	$I_{\rm S} = 5.5 \text{ A}, V_{\rm GS} = 0 \text{ V}$		0.8	1.2	V
Body Diode Reverse Recovery Time	t _{rr}			15	30	ns
Body Diode Reverse Recovery Charge	Q _{rr}	$\frac{Q_{rr}}{t_a}$ I _F = 5.5 A, dI/dt = 100 A/µs, T _J = 25 °C		5	10	nC
Reverse Recovery Fall Time	t _a			7.8		ns
Reverse Recovery Rise Time	t _b			7.2		

Notes:

a. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %

b. Guaranteed by design, not subject to production testing.

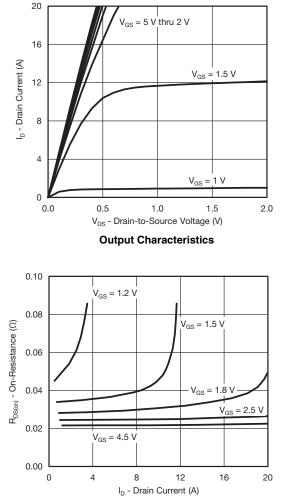
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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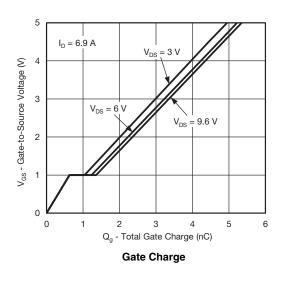


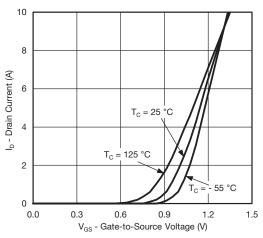
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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

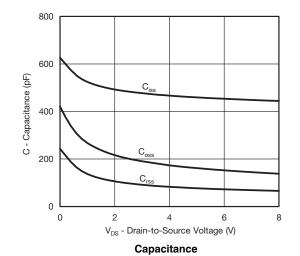


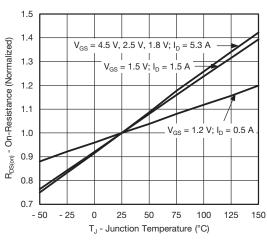
On-Resistance vs. Drain Current and Gate Voltage





Transfer Characteristics





On-Resistance vs. Junction Temperature

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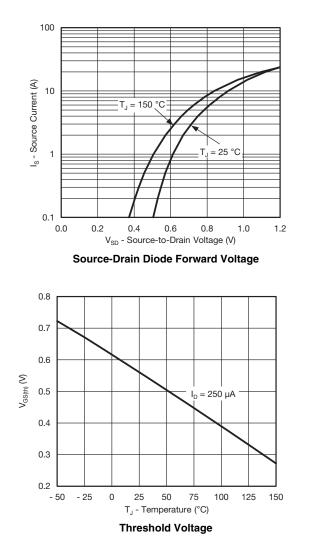
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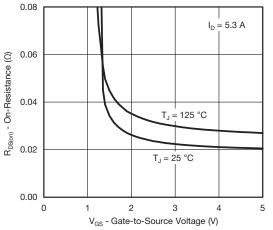
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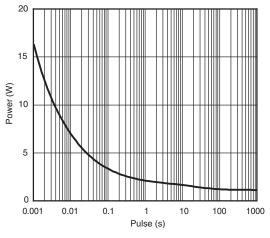


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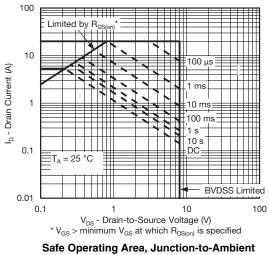




On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power (Junction-to-Ambient)



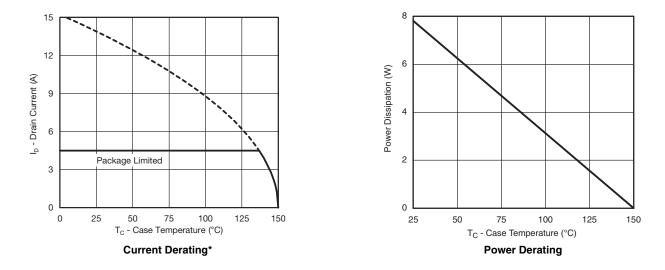
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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



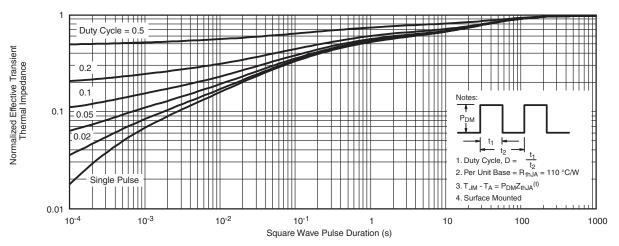
* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

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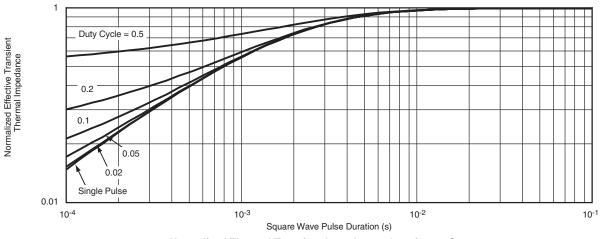
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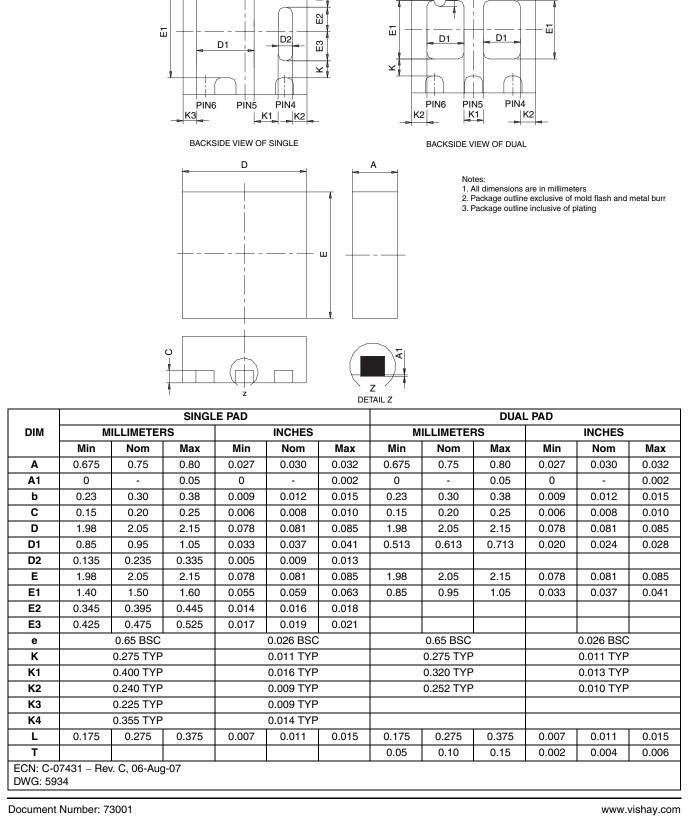


Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?63299.

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PowerPAK[®] SC70-6L

b PIN2 PIN1 PIN3 _ ₹

Package Information Vishay Siliconix

__ ₿

b

PIN3

PIN2

PIN1

¥

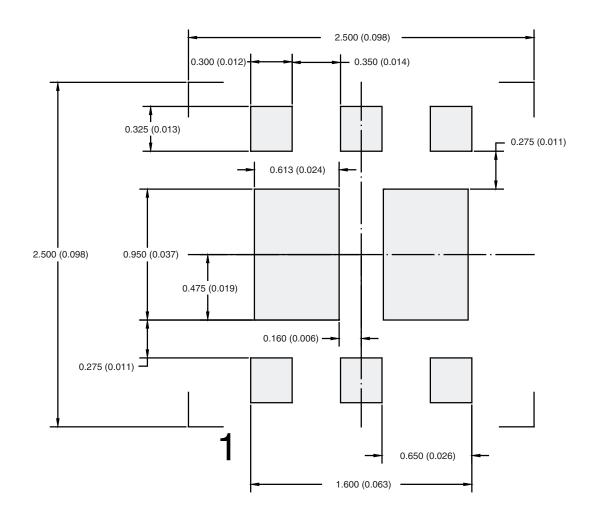
VISHA

Application Note 826

Vishay Siliconix



RECOMMENDED PAD LAYOUT FOR PowerPAK® SC70-6L Dual



Dimensions in mm (inches)

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